Perspective on high density technology and supply chain for rad-hard ASIC and ASSP

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Semiconductor Foundry Landscape
Companies with Wafer Fab facilities

Source: IBS, 2017
Advanced CMOS Foundry Landscape

GF – SEC – UMC – STM partnered through the former IBM SemiConductor Development Alliance

- Common set of technology IP portfolio
- Manufacturing flexibility
- Differentiated technologies
Semiconductor Manufacturing new paradigm
Cost of Developing New-Generation Process

Revenue Payback Requirement for IDM Process Development

IBS, May’16
Complexity is at the interconnect

The PPA of an advanced technology is no longer dominated by the effective length of the transistor gate (FEOL) but by the Metal Interconnect (BEOL), in particular the « contact to gate » length.

28nm FD-SOI Cross Section – STMicroelectronics 2012
Introducing High Density CMOS Technology

• Demonstrating a new FEOL technology is one thing but…
• ….BEOL industrialization is another one
  • very much dominating the cost of introducing a new technology
  • Learning curve
    • 50K R&D wafers estimated to mature a 28nm technology
    • 100K R&D wafers to mature a 14nm technology
    • Meaning 1 to several B$ to bring a new technology on the market

• A new technology exists when it has found its volume lead market!

• SPACE Market cannot be such a lead market!
RadHard Design Paradigm
Cost of Design in CMOS nodes

Cost of Advanced Designs, IBS Jul’17

Cost of Followers Designs, IBS, Jul’17
Technology Downscaling Forcing Design Mitigation

- Aggregate fail rate for all hard reliability mechanisms: 5-100 FIT
  - 1 FIT = 1 Failure-In-Time = 1 fail/1B hours or 114,155 years
  - electromigration, oxide breakdown, hot carrier injection, bias T° instabilities

- Without mitigation, Soft Error Rate (SER) may exceed 100kFIT/chip
  - with downscaling ~constant SER/cell but growing SER/chip
  - <10 FIT/SoC achievable with strong design hardening

- Logic & SRAM transition to FDSOI & FinFET improves SER by 100-10x
  - 100x better intrinsic SER with FDSOI

- Design mitigation additionally required for safety-critical missions
  - Intrinsic techno robustness not sufficient for space (failures on commercial IPs)
20+ years of experience building strong RadHard Design methodology......and

- **End-User Inputs**
  - Layout
  - Netlist with electrical state
  - Irradiation configuration

- **Proprietary Monte Carlo core**
  - 3D structure creation
  - Layout-Versus-Schematic linking
  - Monte Carlo ion generation
  - Ion transport in 3D structure
  - Charge collection:
    - Analytical diffusion
    - Random-walk drift diffusion
    - Bipolar amplification
  - Circuit response
  - Simulation post-processing

- **Physical Inputs**
  - Technological process data
  - Nuclear database
  - Ion stopping power
  - TCAD for physical insight, parameters extraction...

- **Output Display**
  - 2D & 3D plots
  - Upset map
  - Error rate
  - Many technologies covered, including 28/22nm FDSOI

- **Key Points**
  - Started in 2007, 7 PhDs
  - 53,000 lines of C++ code
  - 30% when calibrated
  - 10 min for full-spectrum

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P. Roche, SEU code TNS'13, V. Malherbe, NSREC'16
....the way is still long to harden SoC’s, even with FDSOI technology!

- Commercial FDSOI is not robust enough to fly in space without critical errors
- Strong modeling/design/testing actions for months to achieve quasi-immunity in space
Moving ahead with the ASIC/ASSP SPACE roadmap
SatCom Digital Payload driving and looking for the most efficient signal processing & computing platform
Continuing the Space Roadmap

- Several opportunities ahead in FDSOI, potentially also with **enhanced Body Biasing**
  - Capitalizing on 100 ST space-IPs already qualified for both LEO/GEO
  - Leveraging on ST pioneered FBB usage, industrially deployed for automotive market in 28nm but not qualified for Space usage yet

- **FinFET** is also a good candidate to continue the space roadmap but **will not come for free**
  - NASA, ESA, Sandia already reported critical SEL events in FinFET
  - Rad-tolerant circuit already introduced, e.g. by XILINX with SEL mitigation on Ultrascale+
  - Deploying FinFET for space ASIC will require space skills, tools and strong industrial experience

![Illustration of FinFET transistor](source:GLOBALFOUNDRIES)
FD-SEI technology has not been fully harnessed yet …and still represents a very attractive alternative for SPACE

- Planar technology
- Best trade off performance vs implementation & production cost
- Strong RF/analog integration capability
- Promising Body Biasing technics already used in consumer/automotive areas
- Strong leadership in Europe for such technology with …and a growing ecosystem
High Performance Package roadmap will come with its share of opportunities & constraints

Performance:
- FlipChip Thermal
- Enhanced Organic Packaging

Supply chain:
- leadfree only
- High volume REX required
  - Packaging
  - Bumping
5G: the main growth driver for SemiConductor market

No doubt SPACE INDUSTRY will get its « share of the pie » but !....
Does « New Space » follow the 5G trend?

Are we getting close to the peak of expectation for constellations?

Which technology to safely reach « slope of enlightenment »?