STM – Teledyne e2v Cooperation

- STMicroelectronics and Te2v Semiconductors have signed a contract agreement in Oct 2018, setting up the frame for a long term cooperation.

- Goal for Te2v is to leverage our assembly capabilities and flight model heritage and provide STMicroelectronics with space-grade assembly services.

- STMicroelectronics and Te2v Semiconductors, being both key actors of the Grenoble “Silicon Valley”, we have decided to combine our strengths as, it flows from sources...

- Point is to create together a unique space-grade flip chip center of expertise for large dies, using ST C65Space wafers and moving forward 28 FDSOI wafers on both ceramic and organic substrates.
Flip Chip for space: state of the art & future developments

Jean-Philippe PELTIER | Integrated Microelectronics Solutions
Flip Chip, from one ESCCON to another...

- **2011**: Virtex 5 QV introduction
- **2013**: Mil Prf 38535K class Y issued in December for ceramic-based non-hermetic microcircuits. Packaging aspects include flip chip, underfills,..
- **2016**: Several ongoing developments in Europe & USA
- **2019**: Space level Flip Chip is considered as the norm

Everyone is convinced that Flip Chip is a must

...even if some people are still very “careful” about flip chip

ESCC9000 & 2269000 introducing flip chip (hermetic & non hermetic) issued a few days before ESCCON

Need for “organic for space” standards

Flip Chip already widely used for Hi Rel, non space
Flip Chip, from one ESCCON to another...

at Teledyne e2v

- **2011**: 100 mm² die, 90 nm, Hi Rel, non Space, unlidded
  - 2012: 100 ku cumulated shipment

- **2013**: 100 mm² die, High lead bumps (10/90)

- **2016**: 300 mm² die, 65 nm, Eutectic bumps (63/37)
  - Space level, ceramic, non hermetic, lidded (with TIM)
  - 2017: 200 ku cumulated shipment

- **2019**: 450 mm² in production (3 lots)
  - 2018: DLA certification for Hermetic (QML V) & Non-hermetic (QML Y) flip chip

- **2012**: 100 ku cumulated shipment
Current Flip Chip assembly at Teledyne e2v

Hermetic

Non Hermetic

Ceramic (Al2O3, AlN, HiTCE)

- without lid
- lidded
Enabling Technology for Teledyne e2v Standard Offering

High pin count and Highly integrated digital products.

Integration of NXP Quad Cortex A72 ARM cores, + 4GB of DDR4 memory.

Assessment for ECSS-Q-ST-60-13C to start in 2019

QLS1046 Qormino™ Module

PC8548

PowerPC single core microprocessor.

Built to QML-Y grade at Teledyne e2v Grenoble

PC7448

PowerPC single core microprocessor.

Built to QML-Y grade at Teledyne e2v Grenoble

Data conversion technology with increasing frequency capabilities.

Future Gen Ka-Band ADCs & DACs

Ka-Band capable 12+GSPS DAC and ADC.

Built by Teledyne e2v Grenole in suitable grade.

EV12DS480

K-Band capable 12bit 8GSPS DAC.

Made as per ECSS-Q-ST-60-13C by Teledyne e2v Grenole

EV12AQ600

C-Band capable Quad 1.5GSPS ADC

Built to QML-Y grade at Teledyne e2v Grenoble
TELEDYNE e2v Flip Chip roadmap
At the beginning of the 2010’s, **65 nm** was supposed to be the techno of choice for the 10 coming years

But, it quickly appeared that transition to deeper nodes would occur much faster than expected

**28 nm** is now the standard for current advanced product developments
There is a huge trend in microelectronics towards **System in Package**, heterogeneous integration. HiRel / Space is concerned as well.

But SiP is a concept, not a package type or a technology. It includes:

- Side by side (2D) / Interposer (2.5D) / Stacked die (3D) / + variants / combinations!

With the addition of old space/new space, hermetic/non-hermetic, ceramic/organic, etc., we are facing **infinite potential configurations**!
For years, SnPb (including high lead alloys) has been the material of choice for flip chip bumping.

But, the landscape has now changed for several reasons
1. Flip Chip assembly houses have to face EOL of leaded bumping sources
2. SnPb alloys exhibit poorer performance wrt electromigration

RoHS bumping (eg. SnAg) must be included in capabilities portfolio
For years, ceramic packages have been the material of choice for high reliability packages/substrates.
But organic substrates bring advantages over ceramic solutions for
• Complexity, Pitch
• Speed

eg. Te2v is designing a MCM, where bandwidth would be 1.5 X higher with an organic substrate than with a ceramic one

→ In many cases (not all), organic substrates need to be considered
On Going Projects
On going Packaging Projects (1)

hermetic flip chip with very large die

ST – NanoXplore  NG Large

Die: 560 mm²  ST-C65SPACE

Package: ceramic (Al2O3 )CLGA1752 45 x 45 mm

Start: june 2019

reliability assessment Q4 2019
29 x 29 mm Organic Package, 1.27 mm thickness / 0.80mm core Build up 4/2/4.

(12 x) 0201 SMD passives

Customer design, Teledyne e2v assembly

First delivery to customer Q2 2019 (industrial grade)

Multi flip chip on organic substrate

Ni/Au plated copper lid
1.5 mm thickness

5 flip chip dies
- (4 x) 65nm die, 635 SnAg bumps, 200µm pitch
- 130 nm die, 478 SnAg bumps, 250µm pitch

478 solder balls

(4 x) 65nm die, 635 SnAg bumps, 200µm pitch

130 nm die, 478 SnAg bumps, 250µm pitch
On going Packaging Projects (3)

**multi flip chip on organic substrate**

- 3 dies
- RF (Ka band)
- Prototypes Q4 2019

Die & Substrate designs, assembly: Teledyne e2v

Space grade
Teledyne e2v has launched a project aiming at development of ST FDSOI28, large die, flip chip on organic substrate.

**Die Test Vehicle**
- 388 mm² (21.1 x 18.4 mm)
- Bump pitch: 150 microns
- 17,000 bumps SnAg (1.8% Ag)

**Substrate Test Vehicle**
- FCBGA 50x50mm (16 layers 6/4/6)
- Core thickness 400 µm
- Substrate Thickness 1.370 mm

**Reliability assessment Q1 2020**

Space grade
Summary: flip chip for Space

- **2000’s**: ceramic, wire bond, hermetic
- **2010’s**: hermetic flip chip (SnPb), non-hermetic flip chip (SnPb)
- **2020’s**: SiP, organic, leadfree flip chip

**Note:** The diagram illustrates the progression of flip chip technologies over the decades, highlighting hermetic and non-hermetic types, along with organic and leadfree options.
Thank you !