Introduction
FPGA antifuse
FPGA SRAM based
FPGA Flash based
SOC
Conclusion
Why FPGA in Space Application

- **Integration**
  - New technologies permit to integrate all the digital unit functions in one FPGA except memories and some interfaces.

- **Performances**
  - The last technologies integrate DSP able to propose more than 1 Tflops.

- **Efficiency**
  - Processing per Watt is an order of magnitude better for FPGA than CPU or even GPU.

- **Cost**
  - Even if more efficient, ASICs are costly mainly due to low quantity used in space and high non recurring costs.

FPGAs are mandatory for space digital designs.
FPGA main characteristics for Space

- **Radiations Sensitivity**
  - SEU : can be managed by design
  - Latch-up : depending on sensitivity

- **Packaging**
  - Mainly ceramic but trend to use plastic package. The 10 Gbits/s or more high speed link data rates impose the use of plastic package.

- **Reprogramming**
  - In flight : for SRAM based only
  - On ground during test and manufacturing
FPGA families

- **Anti-fuse**
  - Configuration non sensitive to radiations
  - Old technology

- **Flash**
  - Re programmable
  - Configuration non sensitive to radiations

- **SRAM**
  - Re programmable even in flight
  - Configuration sensitive to radiations

- **System On Chip**
  - Integration of Powerful processors
Introduction

**FPGA antifuse**
FPGA SRAM based
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Conclusion
RT AX (Microsemi)

- Rad Hardened
- Antifuse (150 nm)
- Up to 36 K lut4 = 500 K Asic Gates
- Up to 120 DSP

- Trend not to use this technology for new designs
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ProASIC 3 (Microsemi)

- Flash based technology
- Latch up immune (130 nm)
- Rad tolerant for configuration
- TMR needed

- 75 K versatile (=> lut/FF équivalent with triplication to RTAX2000S = 21K LUT4 / 10 K FF)
- no DSP
- No HSSL
- Speed limit with TMR : 50 Mhz

- Trend to use this technology to replace antifuse FPGA.
RTG4 (Microsemi)

- Flash based technology
- Latch up immune (65 nm)
- Rad Hardened

- Up to 151 K LUT4 / 151K FF
- Up to 462 DSP
- HSSL: 24 @ 3,125 Gbps

- Difficulties with the design tools.
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VIRTEX 5 QV (XILINX)

- Radiation Hardened Technology (65 nm)
- SEU sensitive
- Non Hermetic packaging
- Up to 130K LUT6
- 320 DSP
- HSSL: 18 @ 4,25 Gbps

Difficult to use for packaging reasons and dissipation (high consumption).
Kintex ultrascale (XILINX)

- Radiation Tolerant Technology (20 nm)
- Latch up free
- TMR mitigation needed including configuration

- Up to 633 K DFF/331 K LUT6
- Up to 2760 DSP slices
- HSSL: up to 32 @ 12,5 Gbps

Promoted for space processing by Xilinx
Spartan 6 (XILINX)

- COTS
  - Available up to CQ1

- Latch up immune (45 nm)
- TMR needed including for configuration

- 92 K LUT6 / 184 K FF
- 180 DSP
- HSSL: 8 @ 2.7 Gbps (-2)

Good candidate for low cost; low dissipation processing FPGA.
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ZYNQ 7000

- SRAM based (28 nm TSMC)
- TMR needed including configuration
- 2 x ARM9 core
- 277K LUT6 / 554K FF (ZYNQ 7100)
- 2020 DSP slices (ZYNQ 7100)
- HSSL: 16 @ 12.5 Gbps
BRAVE ULTRA (NanoXplore)

- SRAM FDSOI 28 nm
- Rad-Hard Technology
- 4 x ARM Cortex R52
- Up to 550K LUT4 (TBC)
- Up to 1500 DSP (TBC)
- HSSL: 32 @ 12.5 Gbps (TBC)

- European challenging product
- Promising FPGA SOC for Space Applications
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Conclusion

- Trend to replace antifuse technology by ProAsic 3, Brave Medium or RTG4.

- Use of COTS for high performance FPGA or SOC

- Design of mitigation architecture to cope with radiations to achieve availability target.
Thank you

Questions