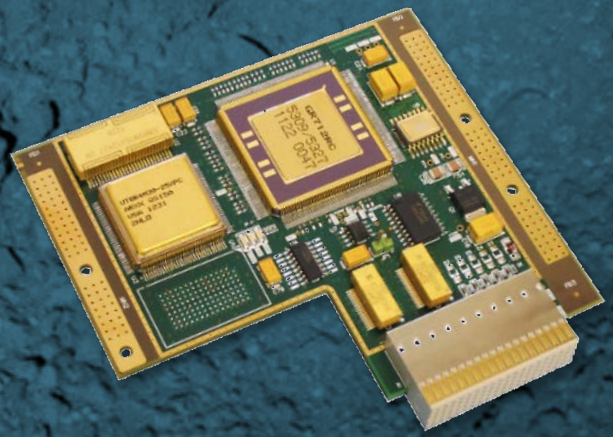
Advances in European Processor Technology

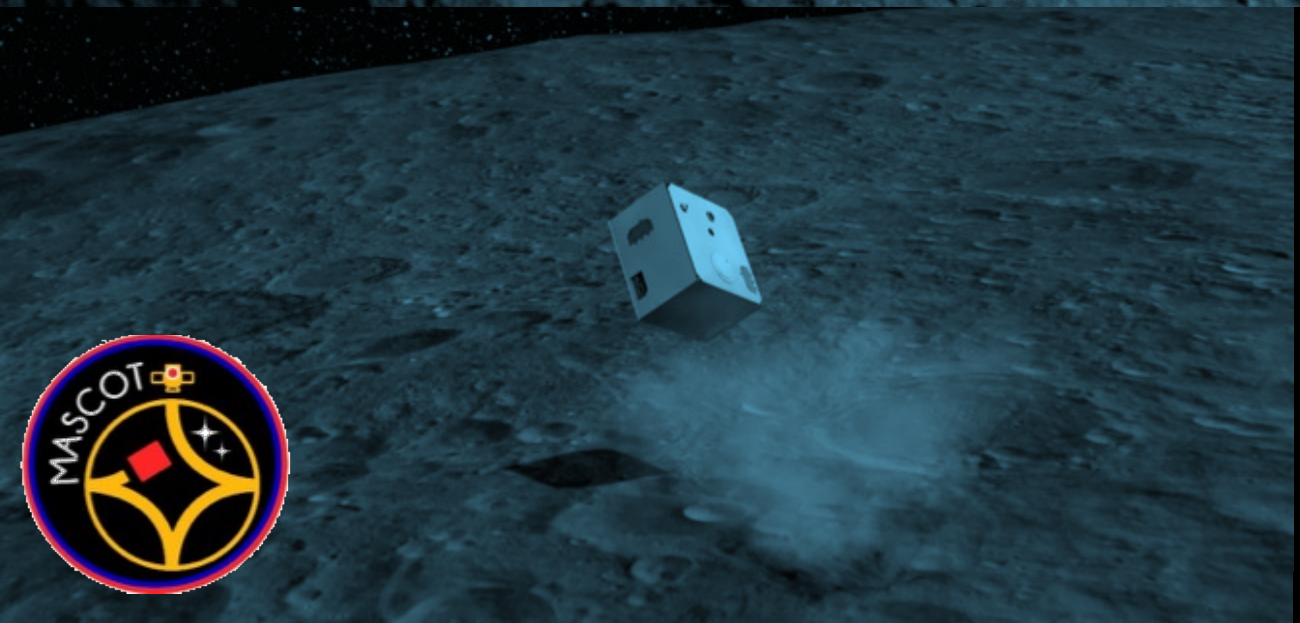
Cobham Gaisler AB
ESCCON 12 March 2019
ESTEC/ESA, Noordwijk, The Netherlands

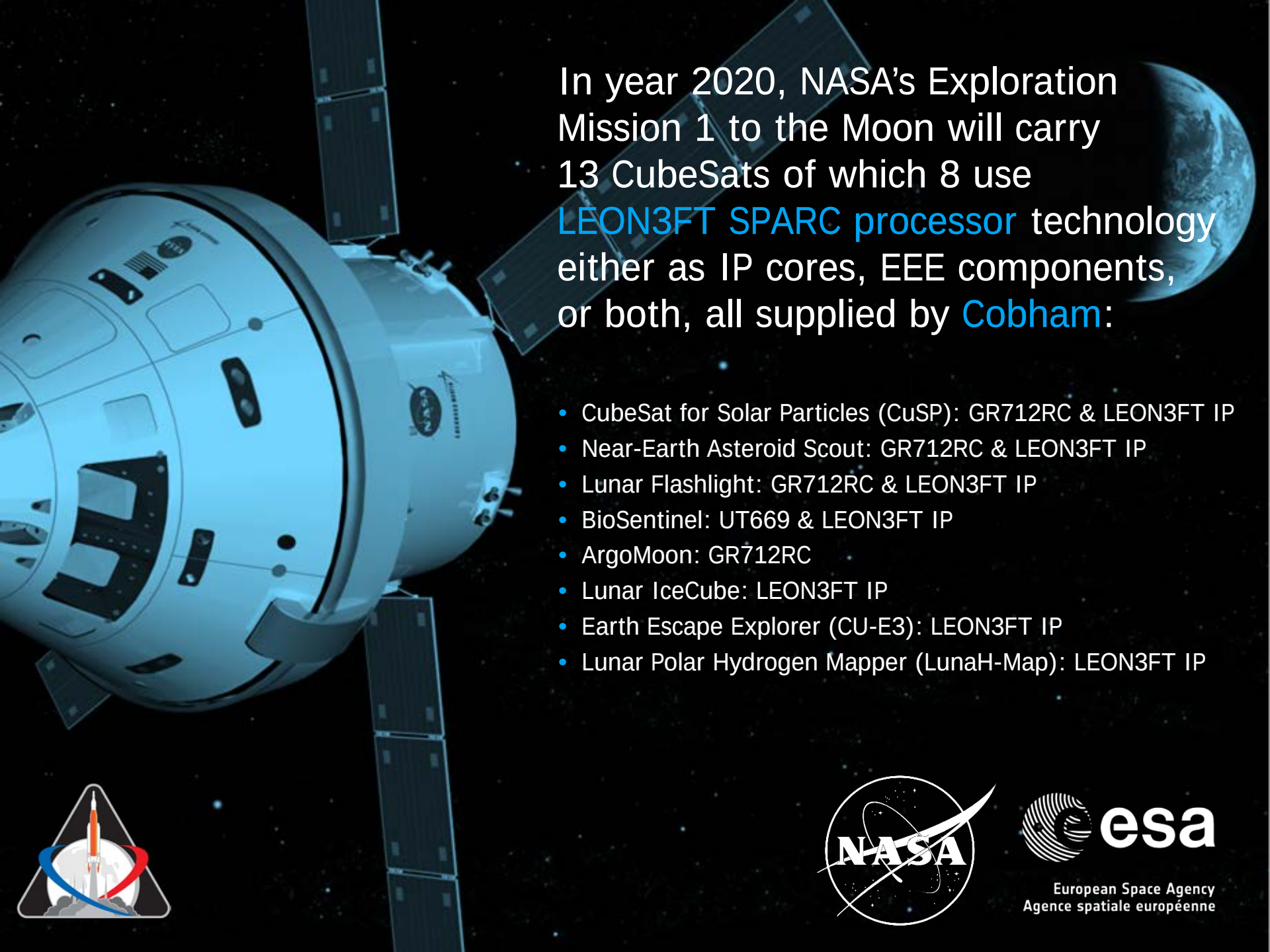
In October 2018, the MASCOT lander touched down on the Ryugu asteroid after hitching a ride with the Japanese Hayabusa 2 probe.

MASCOT successfully completed its mission 325 million kilometers away from Earth!

Cobham developed the MASCOT onboard computer based on their GR712RC processor.







In year 2020, NASA's Exploration Mission 1 to the Moon will carry 13 CubeSats of which 8 use LEON3FT SPARC processor technology either as IP cores, EEE components, or both, all supplied by Cobham:

- CubeSat for Solar Particles (CuSP): GR712RC & LEON3FT IP
- Near-Earth Asteroid Scout: GR712RC & LEON3FT IP
- Lunar Flashlight: GR712RC & LEON3FT IP
- BioSentinel: UT669 & LEON3FT IP
- ArgoMoon: GR712RC
- Lunar IceCube: LEON3FT IP
- Earth Escape Explorer (CU-E3): LEON3FT IP
- Lunar Polar Hydrogen Mapper (LunaH-Map): LEON3FT IP

NASA

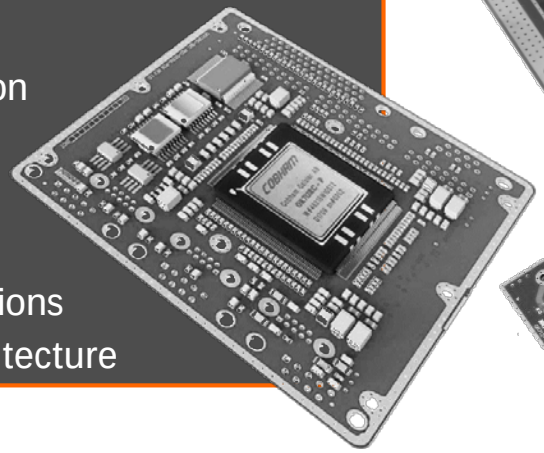
esa

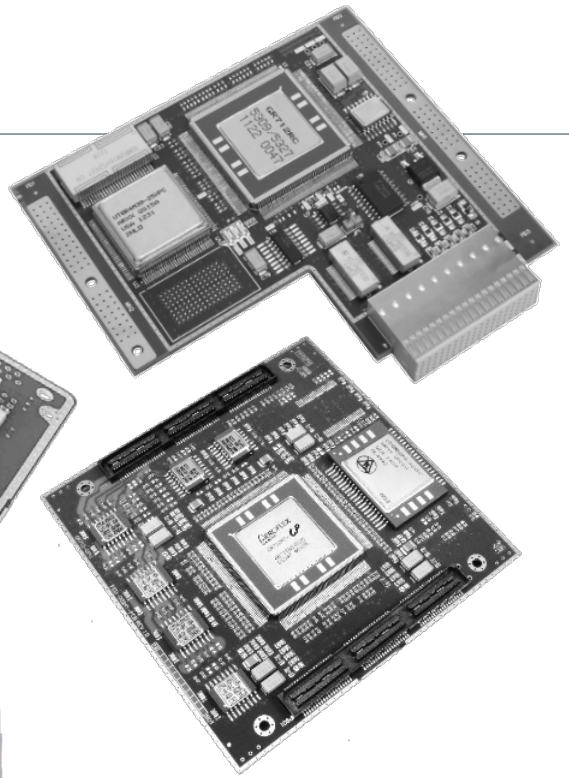
European Space Agency
Agence spatiale européenne

GR712RC - Dual-Core LEON3FT Processor

An ongoing success story

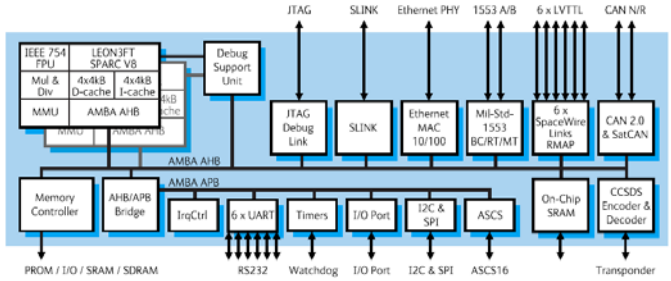
- Why choose GR712RC?
  - Flight proven technology
  - Highly integrated system on-chip solution
  - Low power solution
  - Simple package for assembly
  - Several single board computer designs
  - Selected by several ESA and NASA missions
  - Forward and backward compatible architecture





- GR712RC value add
  - Radiation-hardened by design
  - A multi-core solution developed for space
  - Multiple SpaceWire interfaces with RMAP
  - Mil-Std-1553, SPI, CAN, I2C, Ethernet
  - CCSDS Telemetry and Telecommand on-chip
  - Outstanding floating-point performance - times two
  - Engage second processor core at only 30% power increase
  - Supports SRAM, SDRAM, Flash PROM, EEPROM, MRAM etc.
  - Flight certified boot software available

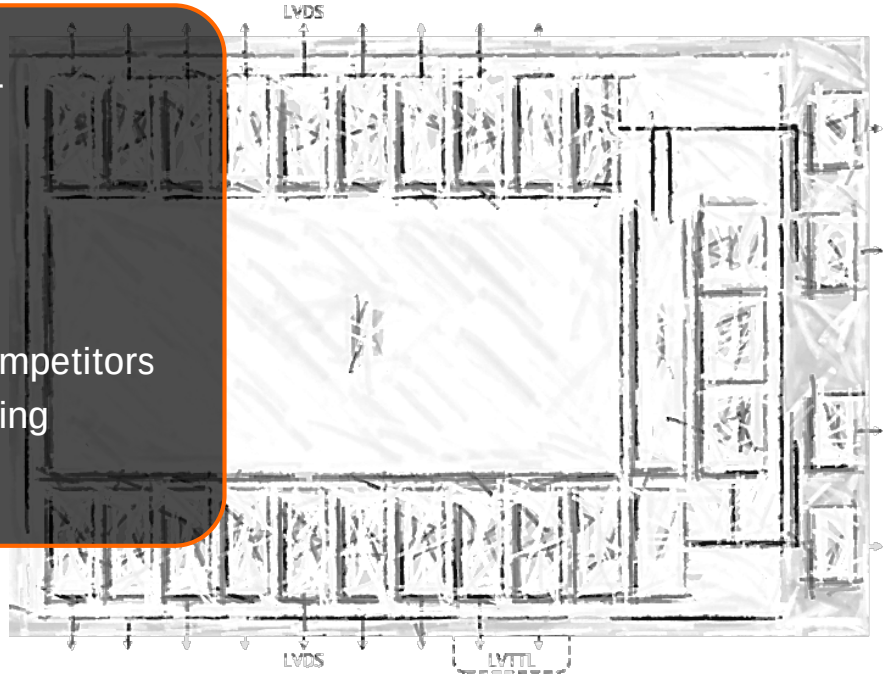
SPARC



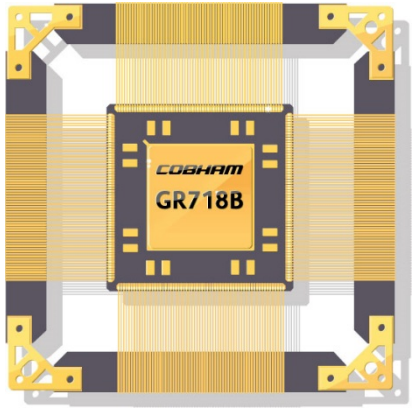
GR718B – 18-port SpaceWire Router

Already a success story

- Why choose GR718B?
  - We offer a stand-alone 18-port SpaceWire Router
  - Includes new features like packet distribution
  - Quality control with ESCC9000 Lot Validation
  - Baselined on ESA JUICE mission
  - Flight parts available since 2017
  - More port and better power performance than competitors
  - Supports external SPI based ADCs for housekeeping
  - EPPL Part 2 listed since December 2018



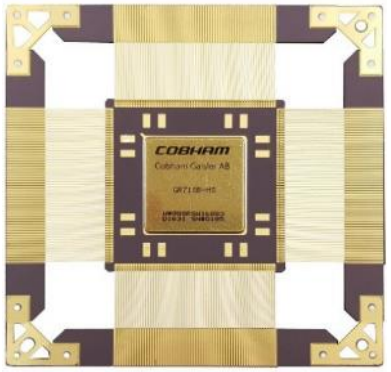
- GR718 value add
  - Supports ECSS-E-ST-50-12C Rev 1 features:
    - Distributed Interrupt support
    - System-Time distribution via all ports
  - Support functions for SpaceWire-D, Deterministic
  - Support for SpaceWire Plug-n-Play
  - UART and JTAG interfaces for local configuration
  - GPIO and SPI access directly from RMAP
  - On-chip SpaceWire In-System Test functionality
  - Outperforms Microchip/Atmel 10-port router on power



GR718B evolution and improvements

Dare to evolve – not static because set in silicon

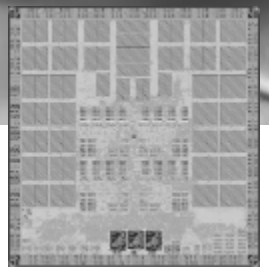
- Planned revision for 2020:
  - LVDS with fail safe and cold-spare
  - Improved packet distribution to support mass memory functionality, take advantage of lessons learned from JUICE
  - Investigate improved functionality required to support standards such as SpW-R and SpW-D
  - SPI4SPACE protocol support
  - Drop in compatible
  - New smaller package option
  - Organic or plastic package alternative

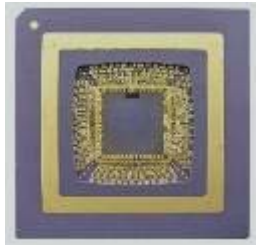


GR740 Success Story

Multiple flight part wins

- Multiple GR740 flight parts wins!
  - Early adopters of new multi-core technologies
  - Ordered evaluation boards, prototypes, protoflight parts
  - Perfect timing – customers about to change technology
  - Building in our technology in their platforms
  - Baselined to be used in several platforms and programmes
  - Undisclosed customers and programmes
  - First protoflight parts delivered!
- New flight silicon revision has been validated.



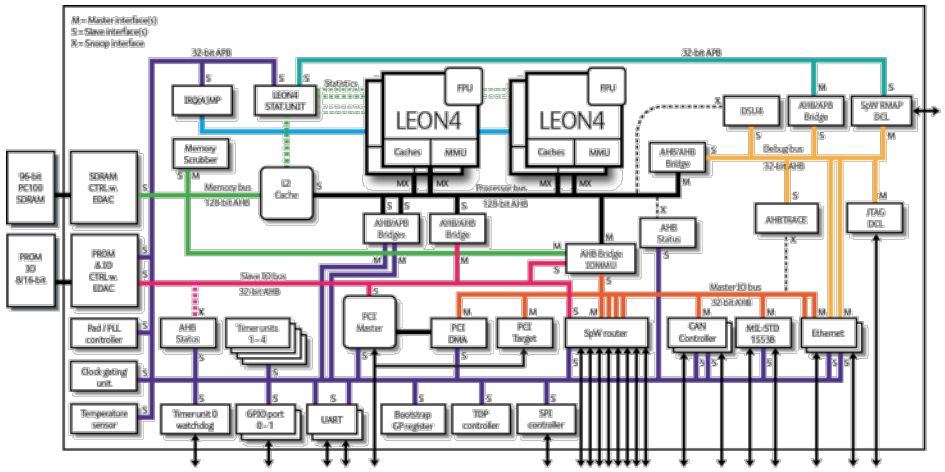


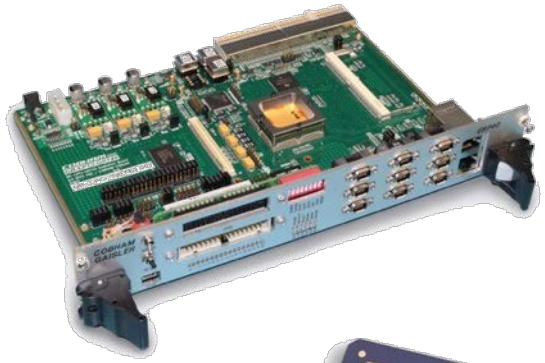
- Why did we win? Cobham Gaisler Value Add
  - Best performance both versus price and versus power
  - Multi-core system with L2 cache gives performance
  - Outperforms RAD750 and other LEON solutions
  - On-chip interfaces for Spacecraft communication
  - Flexibility in meeting programme schedule requirements
  - Path to QML-V

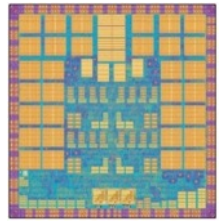
GR740 – Quad-Core LEON4FT

European Next Generation Microprocessor development

- Quad-core LEON4FT rad-tolerant SoC device
  - 4x LEON4FT with dedicated FPU and MMU
  - 128 KiB L1 caches connected to 128-bit bus
  - 2 MiB L2 cache, 256-bit cache line, 4-ways
  - 64-bit SDRAM memory I/F (+32 checkbits)
  - 8-port SpaceWire router with +4 internal ports
  - 32-bit 33 MHz PCI interface
  - 2x 10/100/1000 Mbit Ethernet
  - Debug links: Ethernet, JTAG, SpaceWire
  - MIL-STD-1553B, CAN 2.0B, 2 x UART
  - SPI master/slave, GPIO, Timers & Watchdog
- LGA625 / CGA625 package
- ST C65SPACE - Rad hard 65nm CMOS technology platform for space applications
- ESA's Next Generation Microprocessor (NGMP) activity
- System frequency of 250 MHz over full temperature and supply range.
- Power consumption (including I/O) at 40°C:
  - 4x CPU: 1.85 W (1700 DMIPS)
- First parts for flight delivered H1 2018
- Part of ESA roadmap for standard microprocessor components







COBHAM
Cobham Gaisler AB

life.augmented

SPARC

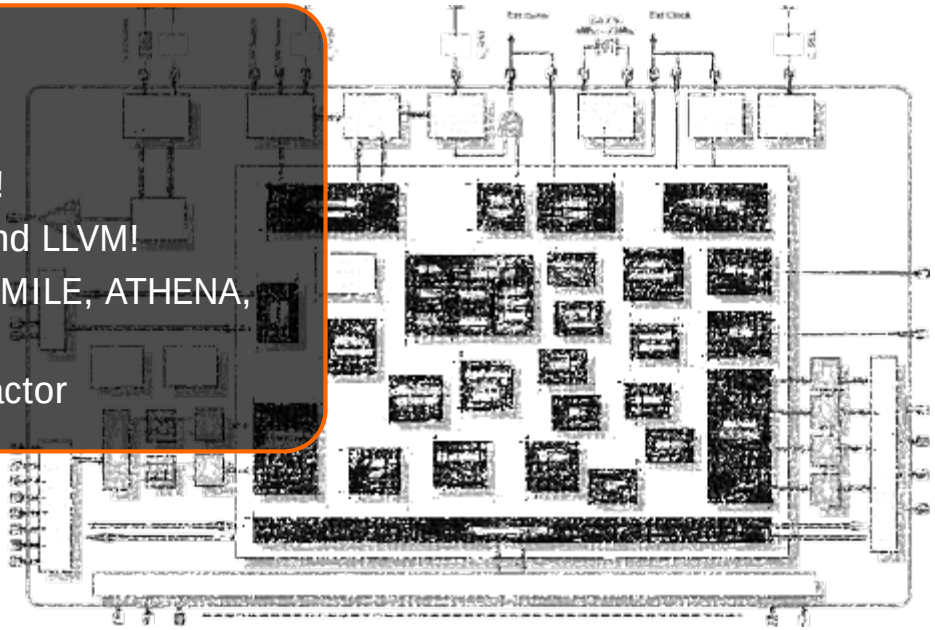
GR740 – Customer Feedback

- The good: Mission enabling technology
- Most frequent requests:
  - Pin sharing limits designs:
    - Either PCI or second Ethernet (not both) can be enabled only when SDRAM is in 48-bit mode
    - CAN,1553,UART,SpwDebug are shared with PROM top address bits and part of 16-bit PROM data bus unused in 8-bit mode
  - SDRAM interface limitations:
    - DDR2 or DDR3 SDRAM support required
    - Available IOs and capacitive load of space-grade SDRAMs are a bad combination
  - Requests for interfaces:
    - HSSL: SpaceFibre and Serial RapidIO
    - NAND Flash controller interface
    - Additional MIL-STD-1553B interface
    - Support for CAN-FD
  - Requests for improved operating frequency / performance
  - Requests for new functionality:
    - TM/TC functions on-chip
    - Separation between software instances

GR716 – Single-Core LEON3FT Microcontroller

Success story in the making

- Why chose GR716?
  - We offer free loaner evaluation boards!
  - We offer free loaner GRMON3 GUI licenses!
  - We offer free compiler tool chains – GCC and LLVM!
  - Already considered in ESA studies: CoRA, SMILE, ATHENA, Sensor & Actuator Nodes, etc.
  - Prototypes already ordered by prime contractor

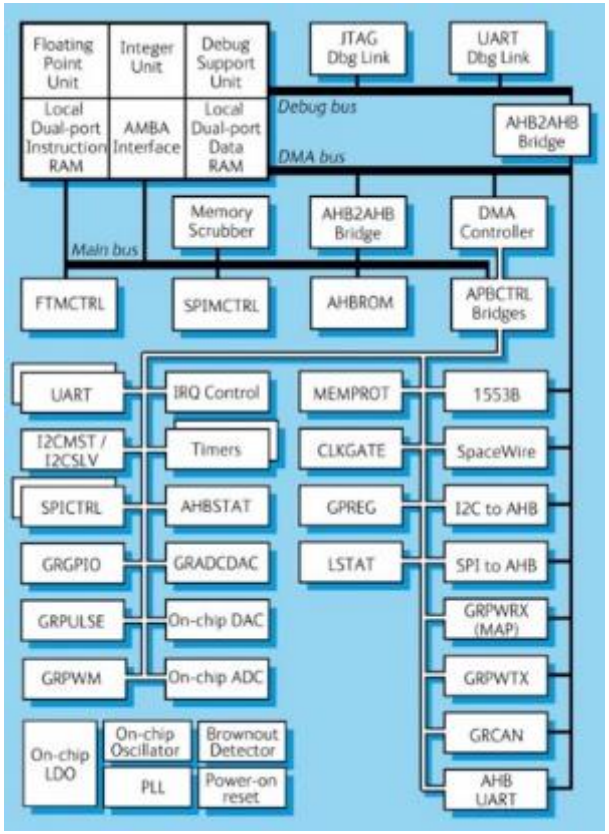


- GR716 value add
  - Mixed signal – integrated ADC/DAC
  - LEON / SPARC compatible – large installed user base, 25+ years
  - 32-bit and 16-bit operation, backward compatible
  - Deterministic timing – can replace FPGAs
  - Most integrated part on the market – with all interfaces
  - SpaceWire, Mil-Std-1553, SPI, CAN, I2C, PacketWire
  - Up to 64 Mixed-Signal General Purpose I/O
  - TID 100krad(Si), SEL 118 MeV-cm^{2}mg, SEU 10^{-12}

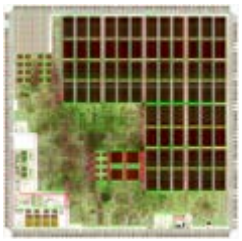
GR716 – Single-Core LEON3FT Microcontroller

European Microcontroller development – prototypes in Q1 2019

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, 50 MHz
  - LEON-REX – extension with 16-bit instructions: improved code density
  - Floating Point Unit
  - 192KiB on-chip instruction and data memory
  - Non-intrusive advanced on-chip debug support unit
  - Determinism: Multi-bus, fixed interrupt latency, cache-less architecture
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- SpaceWire interface with time distribution support, 100 Mbps
- MIL-STD-1553B interface
- 2x CAN 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Interrupt controller, Status registers, JTAG debug, etc.
- Dual ADC 11bits @ 200Ksps, 4 differential or 8 single ended
- Mixed General purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- DAC 12bits @ 3Msps, 4 channels
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm



SPARC Compliant SCD V8



GR716 path to flight models

- Cobham will during 2019 respin the GR716 design to add functionality:
  - Additional DAC
  - Additional MIL-STD-1553B interface
  - Inclusion of new LVDS I/O with cold-spare and fail-safe
  - Dedicated logic for FPGA programming / control
  - .. And more!

- GR716 has proven to be the Swiss Army knife of microcontrollers
  - Ideal for bridge applications between different buses
  - Supervisor circuit
  - Simple control, replace FPGAs with short development cycle

GR7x5 – Quad-Core LEON4FT

COBHAM

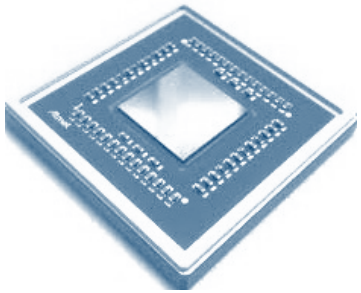
Baseline specification – to be influenced by launch customers – no fixed schedule

Baseline specification

- Quad-core LEON4FT rad-tolerant SoC device
  - 4x – 8x LEON4FT with dedicated FPU and MMU
  - 128 KiB L1 caches connected to 128-bit bus
  - 2 MiB L2 cache, 256-bit cache line, 4-ways
  - **DDR2/3 SDRAM memory I/F (+32 checkbits)**
  - 8-port SpaceWire router with +4 internal ports
  - 32-bit 33 MHz PCI interface
  - 2x 10/100/1000 Mbit Ethernet
  - Debug links: Ethernet, JTAG, SpaceWire
  - **2x** MIL-STD-1553B, 2x **CAN-FD**, 2 x UART
  - SPI master/slave, GPIO, Timers & Watchdog
  - **I²C interface**
  - **NAND Flash controller interface**
  - **SpaceFibre (SRIO TBD) 4+ lanes 6.25 Gbit/s**
- **No pin sharing**
- Worst-case frequency **of 300 MHz, 4'000 DMIPS**
- Power consumption (including I/O) at 40°C < 3 W

Under consideration

- Architectural changes: Multi-layer connection to L2C with processors and IO on separate ports
- LEON5FT IP core inclusion
- TM/TC functions on-chip
- Target technology change
- Extended support for HW-in-the-loop simulation
- Multi-core separation



SPARC Compliant SCD V8

Cobham is now a Multi-Architectural Company

Cobham continues to be committed to and invested in the SPARC architecture and its LEON implementations.

SPARC/LEON will be maintained and further developed going forward. The company has customers expecting it to provide components and support for decades to come. This is also ensured via long term supply agreements.

The RISC-V architecture is expected to grow in the future with a larger number of developers compared to SPARC V8.

Going forward, Cobham will add RISC-V to its product portfolio as a complement to SPARC and ARM, not as a replacement.

LEON5 Processor Core

Primary goals:

- SPARC V8 32-bit compliant processor core
- Improved performance over LEON4
- Superscalar – baseline is dual issue
- Goal is to have modes with deterministic, or bounded timing performance
- Reduction of configuration options
- Hardware support for virtualization
- SEU tolerance
- Leverage existing software support, maintain binary compatibility with LEON3 and LEON4

Primary feature set:

- SPARC V8e
- AHB and AXI4 bus support
- HW support for virtualization
- Local RAM (TCM)
- Copy-back cache (subject to performance evaluation in combination with multi-ported memory controllers with striped ports)
- Little endian support

Target technologies:

- ASIC implementations for space applications
- High-end space FPGAs: Kintex Ultrascale

Target applications:

- General purpose payload processing
- Mixed platform and payload applications

Complemented by:

- New DDR2 and DDR3 SDRAM controller (FTADDR23), specifically targeted for space applications
- Multi-port L2 cache extensions allowing bandwidth extensions from L1 to off-chip memory devices

RISC-V Processor Core

Primary goals:

- RISC-V 64-bit compliant processor core
- Superscalar – baseline is dual issue
- Fault Tolerance - Error Correction Codes (ECC)
- Cybersecurity (proprietary solutions)
- RTCA/DO-254 certification (Design Assurance Guidance for Airborne Electronic Hardware)
- ISO 26262/FUSA certification (Road vehicles – Functional safety)
- Leverage foreseen uptake of RISC-V software and tool support in the commercial domain
- Compatible with GRLIB IP Core library

Primary feature set:

- RISC-V RV64GC
- AHB and AXI4 bus support

Supportive activities

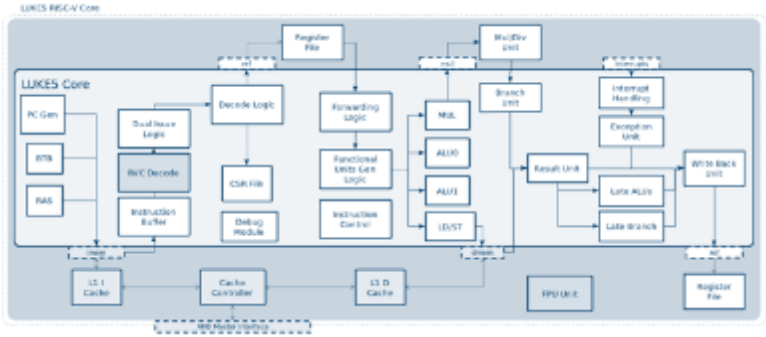
- RISC-V Foundation Membership in 2019
- RISC-V PhD position at University of Delft with ESA

Target technologies:

- ASIC implementations for space applications
- High-end space FPGAs: Kintex Ultrascale

Target applications:

- General purpose payload processing
- Mixed platform and payload applications
- With future DDR4 SDRAM controller, specifically targeted for space applications

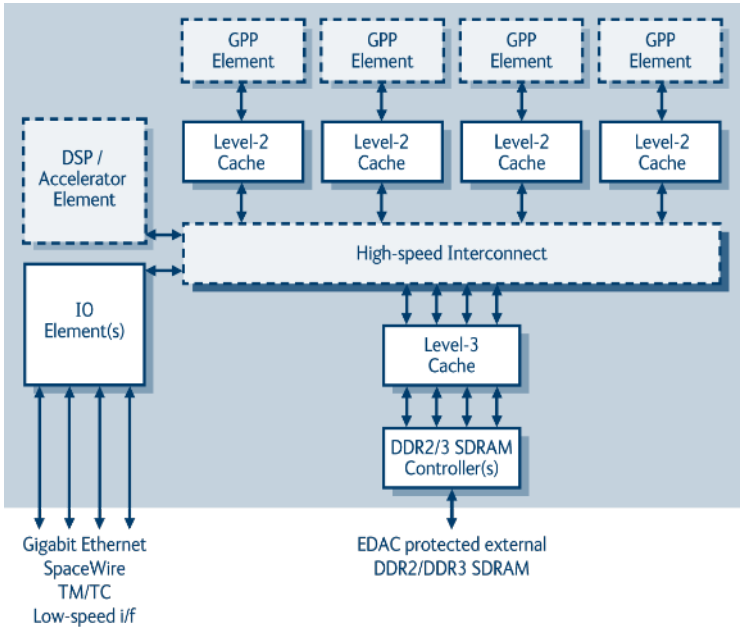


Cobham Gaisler GRLIB IP Library©

GR7xx – Deep-Submicron Multi-Core

Closer to COTS – make do with what technology exists now, optimize later

- Baseline SoC specification
  - Octo-core with islands of 2 – 4 processors each with dedicated L2C
  - DDR2/3/4 SDRAM memory I/F (+32 checkbits)
  - SpaceFibre, PCIe, (SRIO TBD) eight lanes 6.25 Gbit/s
  - JESD204B/C support
  - 8-port SpaceWire router with +4 internal ports
  - 2x 10/100/1000 Mbit Ethernet (GMII, SGMII TBD)
  - 32-bit 33 MHz PCI interface (TBD)
  - MIL-STD-1553B, CAN-FD, 8 x UART with DMA
  - SPI master/slave, I^2C master/slave
  - GPIO, Timers & Watchdog
  - CCSDS TM/TC functions on-chip
  - Debug links: Ethernet, JTAG, SpaceWire
  - NAND Flash controller interface
  - Interfaces for connecting COTS accelerators (MIPI?)



- High-pin count package
- **Need to identify additional interfaces for leveraging COTS accelerators**
- **Increased focus on cyber-security and isolation (processor and SoC design features)**
- **Input on accelerators is welcome**
- **Input processing performance is welcome (int, fp, ..)**

Thank you for listening!