What do we all dream about?

High performance processing solution
With high flexibility for future applications
Allowing multitasks for integration
Suitable for Space
Developed with a European team spirit
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- Allowing multitasks for integration
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High performance processing solution
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And of course at reasonable price
Introduction
Key Features
ARM Technology
Software
Use Cases
Conclusion
Context & Objectives

**DAHLIA** is an answer to the H2020 topic ‘**COMPET-1-2016: Critical Space Technologies for European Strategic Non-Dependence**’

**DAHLIA** is an **ARM-based SoC** implemented in **28nm FDSOI** technology with **eFPGA** designed to boost competitiveness and ensure **strategic non-dependence** of future European Space equipment.

**DAHLIA** is associated to the **NG-Ultra** development and vice-versa.
DAHLIA development has been initiated by **CNES, Airbus DS** and **TAS** targeting 3 main objectives:

- a large improvement of **performances** to cope with evolutions of needs in the mid/long term
- a dynamic **ecosystem** closer to Ground applications in order to enhance possible synergies
- a competitive **computing solution** allowing much more integration/miniaturation
H2020 Organization

7 partners from 4 countries

ESA and CNES are also part of an Advisory Group
Development Plan

- Kick-Off in 2017
- Development in 2017-2018-2019
- SoC FPGA first prototyping Q1 2019
- DAHLIA prototypes available Q1/Q2 2020
Clarification on DAHLIA & NanoXplore FPGA Roadmap

- **Low-End FPGA**:
  - Just FPGA fabric
  - 35kLUT

- **Mid-End FPGA**:
  - with SERDES & single-core ARM Cortex-R5
  - 140kLUT

- **High-End SoC FPGA**
  - based on quad-core ARM Cortex-R52
  - 500kLUT

Frequency:
- 500 MHz
- 200 MHz

Logic Density:
- Low-End FPGA
- Mid-End FPGA
- High-End SoC FPGA

Complexity:
- Low-End FPGA
- Mid-End FPGA
- High-End SoC FPGA
Introduction

**Key Features**

ARM Technology

Software

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Conclusion
Features

ARM-based quad-core CPU
- Cortex-R52
- Cortex-R52
- Cortex-R52
- Cortex-R52

Debug & Trace

External Memory
- DDR
- FLASH

On chip Memory
- eRAM
- eROM

Enhanced AXI Interconnect Cross-Bar

Embedded FPGA

SoC Services
- Clock & Reset
- V&T Monitor
- Error Mgmt
- Boot SpW
- Security

Connectivity
- Embedded FPGA
- DMA

Security
- DMA

GPIO
- UART, SPI
- CAN
- GNSS

SpW RMAP
- HSSL (SpFi)
- 1553 BC & RT
- CCSDS TM & TC

Enhanced AXI Interconnect Cross-Bar

ESCCON 2019

DAHLIA
Features

On chip Memory
- eRAM
- eROM

ARM-based quad-core CPU
- Cortex-R52
- Cortex-R52
- Cortex-R52
- Cortex-R52

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- Security

16 channels

ultra NG ultra NG ultra ultra NG ultra NG ultra NG ultra NG ultra NG ultra NG ultra NG ultra

ESCCON 2019 DAHLIA
STM 28nm FDSOI Technology

- Intrinsically **immune to Latch-up**
- Reduced pitch size providing **good dose tolerance**
- Very good immunity to SEU

- 28nm FDSOI is combined with **RHBD solutions** such as Hardened DFF, ECC on memories or Embedded Configuration Memory Integrity Check (CMIC) for the embedded FPGA
28 nm → Moore’s Law is (as usual) still on our side
Memories & Sizes

Some sizes to be consolidated during detailed design step
Features

ARM-based quad-core CPU
- Debug & Trace
- Cortex-R52
- Cortex-R52
- Cortex-R52
- Cortex-R52

On chip Memory
- eRAM
- eROM

External Memory
- DDR
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Enhanced AXI Interconnect Cross-Bar

Embedded FPGA

SoC Services
- Clock & Reset
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- Security

16 channels DMA
Why looking at ARM?

100 BILLION arm-BASED CHIPS

A VAST ECOSYSTEM OF 1,000+ PARTNERS

arm POWERS 95% OF ALL MOBILE DEVICES

arm TOUCHES 70% OF THE WORLD’S POPULATION
ARM technology selection

Cortex-A
Highest performance
Optimized for rich operating systems

Cortex-R
Fast response
Optimized for high-performance, hard real-time applications

Cortex-M
Smallest/lowest power
Optimized for discrete processing and microcontroller
ARM Cortex-R family

- **Cortex-R7**: High performance 4G modem and storage
- **Cortex-R8**: Highest performance 5G modem and storage
- **Cortex-R4**: Real-time performance
- **Cortex-R5**: Real-time performance with functional safety
- **Cortex-R52**: Most advanced processor for functional safety

**ARMv7-R**

**ARMv8-R**

**Storage & Modem**

**Functional Safety**
Cortex-R52

High performance processing
• 2.2 DMIPS/MHz @ 600 MHz
• FPU Single and Double Precision
• Advanced SIMD co-processing NEON

Improved MPU
• 14x faster context switch than Cortex-R5
• Hard real-time determinism

Safety features dedicated to random errors
• ECC protected memory
• Software BIST libraries
• Level 2 MPU with new privilege level

Fully integrated Generic Interrupt Controller supporting complex priority-based interrupt handling
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Cortex-R52

- ARM’s most advanced processor for safety
- Simplifies integration of software in complex safety systems
- Optimized for Time and Space Partitioning
NG-Ultra Ecosystem

Around the Processing
- ARM ecosystem
- SW Development tools
- Hypervisor
- Simulator
- …

Around the FPGA
- NanoXmap tools cover from RTL synthesis, P&R up to bitstream generation
- …

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Example of Use Cases

• Platform OBC & Integrated Avionics

• Payload OBC
Example of Use Cases

- Platform OBC & Integrated Avionics

DAHLIA / NG-Ultra will make possible several levels of avionics integration.

At spacecraft level, four HW+SW functional groups can be identified:
- Platform core avionics
- Mission data storage and payload interconnection
- Instrument management and data processing (ICU)
- Spacecraft housekeeping and commanding discrete I/O acquisitions (RTUs)
Integration levels vs SAVOIR

GNSS Integration

- GNSS (AGGA5)
- Safe-Guard Memory
- Reconfiguration
- Platform Telemetry
- Security
- Platform Data Storage
- Processing
- Telecommand
- Time
- CLCW
- TC CLTUs
- Encryption
- TM packets
- On-Board Time
- Status
- Time & Tick
- Time reference
- Essential TM
- PIO

Processing Cores

- Essential TC
- Mission Data Links
- Payload Data Routing
- Payload Data Storage
- Payload Telemetry
- Security
- Payload direct monitoring
- TM packets, files
- Time & Tick
- Payload control
- Payload sync

Platform

- Platform commanding
- Platform Payload
- TC Segments
- TM packets
- Status
- Time reference
- Essential TM
- Time & Tick
- Time reference
- TC CLTUs

Payload

- Payload sync
- Payload direct monitoring
- CADUs
- TM packets
- Time & Tick
- Time reference
- Essential TM
- Time & Tick

NG

High speed bus

Cold redundant operation

Hot redundant operation

Warm or cold redundant operation

Multiple bus support (MIL, CAN)

Integrated RTU

High speed payload processing

ESCON 2019

DAHLIA
Example of Use Cases

• **Payload OBC**

Payload OBC typically requires:

• High performance computation capability for execution of mission/instrument control and/or specific algorithms
• High data rate communication link for acquisition of specific sensor data and/or payload data
• Low data rate for command and control function
• Efficient HW implementation of very customized specific functions and interfaces

DAHLIA covers all of these requirements
Conclusion

DAHLIA H2020 & NG-Ultra will offer to European Space Community a unique **rad-hard** high performance quad-core **ARM** SoC in 28nm FDSOI technology, with **huge eFPGA** for flexibility.

It will enable development of products for multiple platform and payload Space applications, enabling the convergence with terrestrial applications benefiting from the strong **ARM ecosystem**.

**Success/adoption** of the **DAHLIA / NG-Ultra** will predominantly depend on the quality of the **tools** that will be available for any development with such component. Indeed **HW/SW** is the keypoint for such new component.

**DAHLIA / NG-Ultra** is a key for future **European Strategic Non-Dependence** & for **all of us**.
More details on DAHLIA are available on the project website
Thank you

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