

# Class Y Status and Update on JEDEC JC-13 and SAE SSTC CE-12 Related Tasks

***Shri G. Agarwal***

*NASA – Jet Propulsion Laboratory,  
California Institute of Technology*

*Shri.G.Agarwal@nasa.gov  
818-354-5598*

***Michael J. Sampson***

*NASA – Goddard Space Flight Center*

*Michael.J.Sampson@nasa.gov  
301-614-6233*

<http://nepp.nasa.gov>

This is NASA InSight's first selfie on Mars. It displays the lander's solar panels and deck. On top of the deck are its science instruments, weather sensor booms, and UHF antenna.



- Thank you Mikko, Ralf, Anastasia, and Fernando for your invitation. It's always a great pleasure to visit Noordwijk.
- Congratulations on this year's ESCCON!
- ESA is a valued partner in NASA Electronic Parts Assurance Group (NEPAG) activities.

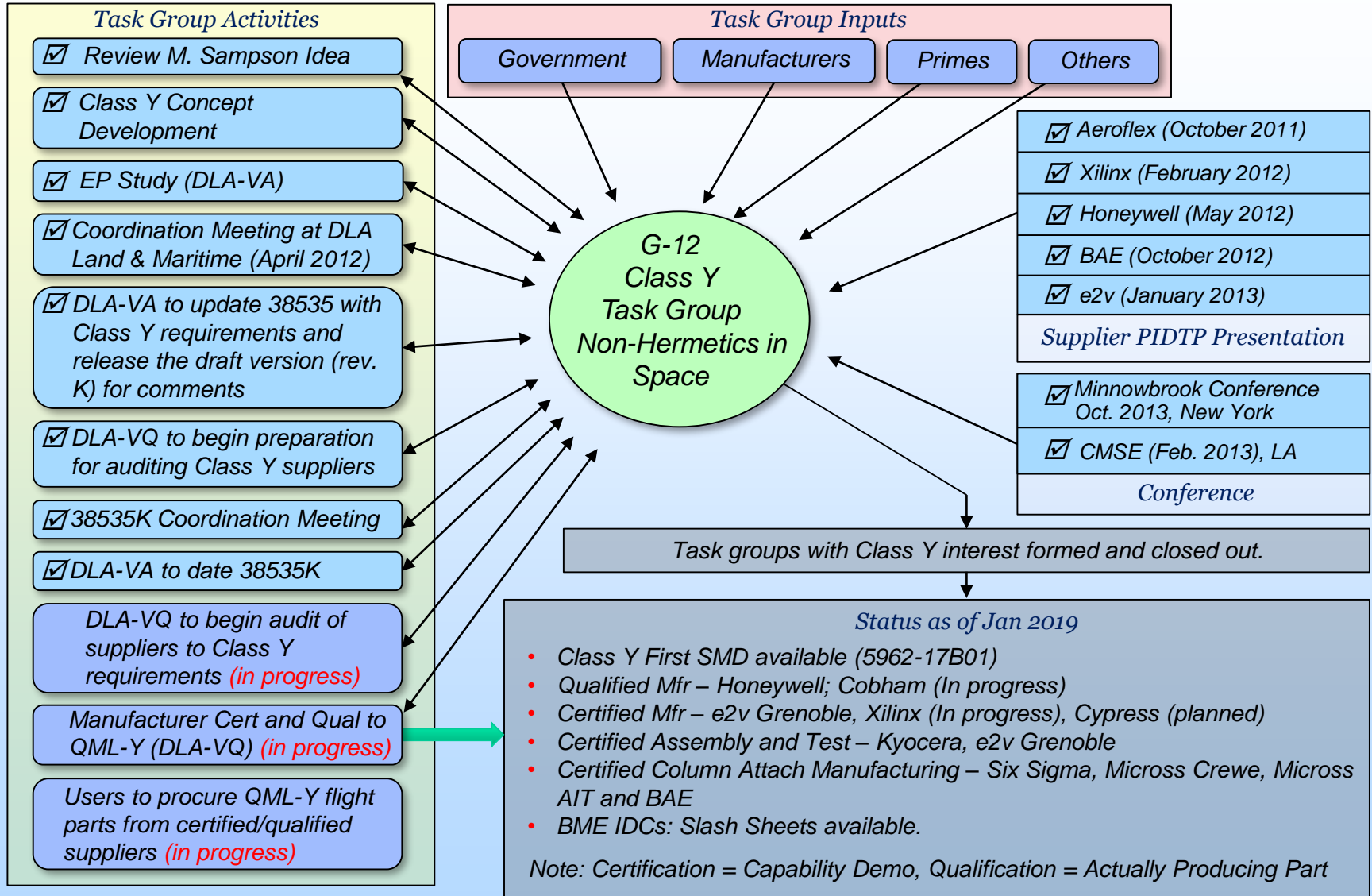


# The “Class Y” Initiatives



- In order to enable space flight projects to benefit from the newly developed devices, e.g., Xilinx Virtex-4 and -5 FPGAs (which are ceramic-based flip-chip nonhermetic parts), a new class was needed.
- NASA worked on a CE-12 initiative, called Class Y, for infusing Xilinx FPGAs and other similar devices into military/space standards.
  - Such an effort must be coordinated with the suppliers and users.
  - Need to address all aspects of packaging configuration.
  - New test methods must be created and the existing standards updated as necessary.
- **A Follow-on to Ceramic Substrate Class Y**
  - Interest in organic Class Y, and molded plastic parts is growing.
  - **The JC-13.7 task group created a new task group on organic substrate Class Y at the September 2018 meeting.**
- Class Y is ***Classy***.

# Infusion of the New Class (Y) Technology into the QML System for Space (Status Jan 2019)



BGA / CGA = Ball-Grid Array / Column-Grid Array  
 BME = Base Metal Electrode  
 IDC = Inter Digitized Capacitor

PIDTP = Package Integrity Demonstration Test Plan  
 SMD = Standard Microcircuit Drawing

# Infusion of New Technology into MIL/Space Standards PIDTP and Its Applicability



- **Issue**
  - How to address the manufacturability, test, quality, and reliability issues unique to new non-traditional assembly/package technologies intended for space applications.
  
- **Solution implemented**
  - A new concept: package integrity demonstration test plan (PIDTP).
  - Each manufacturer shall develop a PIDTP to be approved by the qualifying activity after consultation with the space community.
  
- **The PIDTP requirement applies to:**
  - Non-hermetic packages
  - Flip-chip assembly
  - Solder terminations
  - (Refer to 38535, Appendix H)
  
- **The PIDTP approach seems to be working well so far.**



# First Released SMD for Class Y Part

REVISIONS													
LTR	DESCRIPTION							DATE (YR-MO-DA)			APPROVED		
<p><i>Preliminary Last updated 5/9/17</i></p> <p><b>Class Y SMD</b></p> <p>(Class Y Ceramic non hermetic flip chip LGA devices)</p>													
REV													
SHEET													
REV													
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27
REV STATUS													
OF SHEETS								1	2	3	4	5	6
PMIC N/A	PREPARED BY Phu H. Nguyen			<b>DLA LAND AND MARITIME</b> COLUMBUS, OHIO 43218-3990 <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a>									
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Muhammad A. Akbar			<b>MICROCIRCUIT, CERAMIC NON HERMETIC FLIP            CHIP, DIGITAL, CMOS SOI, GATE ARRAY            HX5000, RADIATION HARDENED,            MONOLITHIC SILICON</b>									
	APPROVED BY												
	DRAWING APPROVAL DATE												
AMSC N/A	REVISION LEVEL			SIZE A	CAGE CODE 67268	5962-17B01							
				SHEET			1 OF XX						

DSCC FORM 2233  
APR 97

5962-EXXX

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

## STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: XX-XX-XX

Approved sources of supply for SMD 5962-17B01 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx>

Standard microcircuit drawing PIN 1/ 2/	Vendor CAGE number	Vendor similar PIN
5962H17B0106YXC	34168	HX518X
5962H17B0106YYC	34168	HX518Y

- 1/ Microcircuits devices supplied to this drawing are land grid array (LGA) packages with lead finish mark letter C (gold). However, for future AID drawing column grid array (CGA) or ball grid array (BGA) packages terminal lead finish mark shall be provided with "F".
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

Vendor name and address

34168

Honeywell Aerospace - Plymouth  
12001 Highway 55  
Plymouth, MN 55441-4744

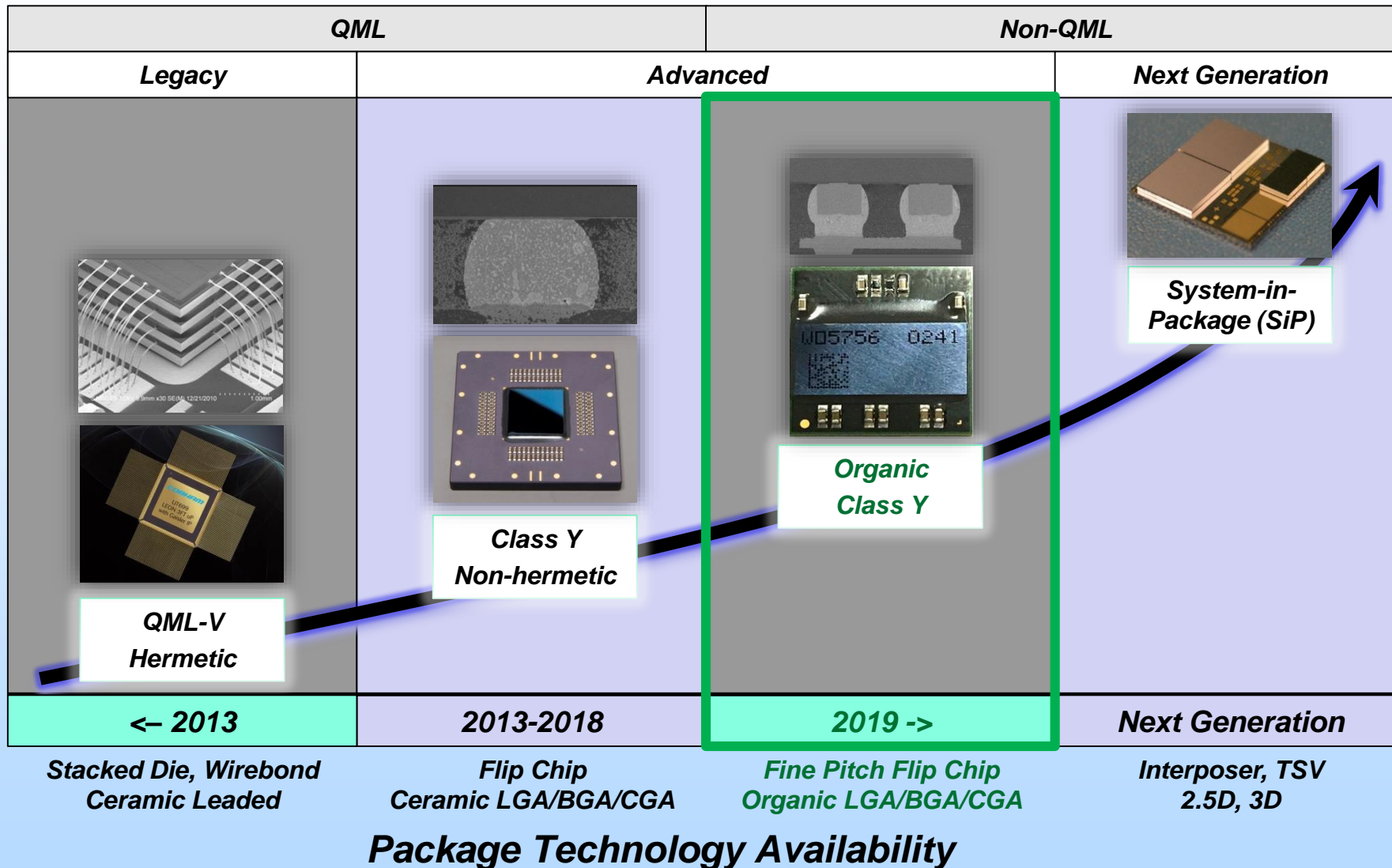
The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

# Next Generation Package Technology for Space

## Development Roadmap for Space Applications



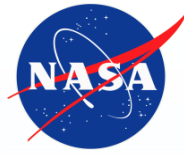
Performance Requirements



Credit: Scott Popelar, Cobham, 2019 MRQW, February 7, 2019

# JC-13.7/CE-12 Task Group 2018-02

## Class Y Expansion to Organic Substrates



- **Notional Milestones/Schedule for 2019 and 2020**
  - **What do we want to accomplish by the end of 2019?**
    - ❖ Organic Class Y definitions and technology classes
    - ❖ **DLA Engineering Practice Study**
    - ❖ **NASA NEPP Special Bulletin article**
    - ❖ Define PIDTP risk areas
    - ❖ Preliminary PIDTP demonstrations
    - ❖ Organic Class Y poster child identification
    - ❖ Determine if new QML designation is needed, or use Class Y or Class N?
  - **What do we want to accomplish by the end of 2020?**
    - ❖ **Poster child characterization and qualification demonstration**
    - ❖ Recommendations for technology insertion into MIL-PRF-38535 and MIL-STD-883
- **Bi-Weekly Conference Calls Starting on January 30**





# Partnering

## JEDEC JC-13 (Manufacturers)

JC-13	Solid State Devices for Government Products
JC-13.1	Discrete Semiconductors for Government Products
JC-13.2	Microelectronics for Government Products
JC-13.4	Radiation Hardness
JC-13.5	Hybrids and Multi-chip Modules for Government Products
JC-13.7	New Electronic Device Insertion for Government Products

## SAE CE-11/CE-12 (Industry Users, Primes, Subs)

SAE SSTC CE-11	Users of Passive Components
SAE SSTC CE-12	Users of Solid State Devices
<b>CE-12 Management:</b>	
<b>Chair – A. Touw</b>	
<b>Vice Chair – (JPL) S. Agarwal</b>	
SAE SSTC CE-11 & CE-12	Space Subcommittee Chair – S. Agarwal



### NASA Centers:

ARC            JSC  
GRC            KSC  
GSFC          LaRC  
JPL             MSFC

### Partners from Outside NASA:

Domestic  
JHU/APL, Others  
The Aerospace Corp,  
U.S. Air Force, U.S. Navy,  
U.S. Army, DLA,

International  
ESA, JAXA, CSA



## NASA and JC-13

- NASA is an active participant in many JC-13 activities.
- Some of the JC-13 Task Groups were started at NASA's request.
  - Example: Electronic Parameters and Burn-in Standardization.
- The newly started New Technology initiative (JC-13.7) provides a look ahead
  - Identify new technologies, develop path for their infusion into military & space
  - A task group (TG) on Organic Substrate Class Y was started in September '18.

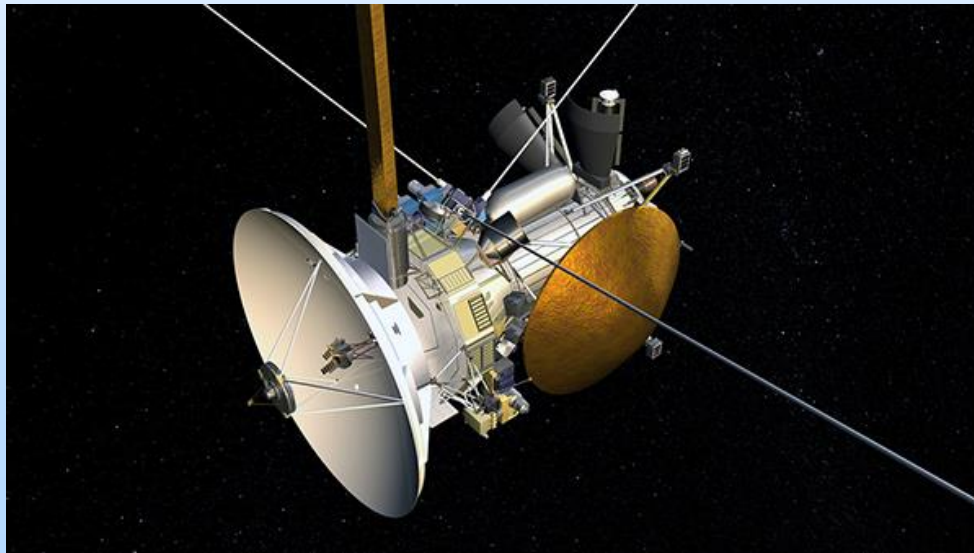
## NASA and SAE SSTC CE-12\*

- NASA is an active participant in many CE-12 activities.
- When requested, NASA has led the CE-12 Task Groups.
  - Example: Infusion of new technology into DoD standards, the Class Y initiative.
- With the appointment of Shri Agarwal as the Vice-Chair of CE-12, NASA is helping to run the organization.
- **NASA chairs the CE-12 Space subcommittee.**
- \* SAE = Society of Automotive Engineers  
SSTC = Systems, Standards and Technology Council  
CE-12 = Solid State Devices

# NASA's Involvement in Developing New Space Products



- With the Defense Logistics Agency (DLA) and the Aerospace Corporation, NASA participates in the review and approval of new space products:
  - **Standard Microcircuit Drawings (SMDs)**
  - **Characterization and qualification data per Appendix H of MIL-PRF-38535 (for the monolithics)**
- **During fiscal year 2018, 16 microcircuit SMDs were approved for release.**
- Per manufacturers, there is a **continuing strong demand for space products**



*Launched in 1997 with the European Space Agency's (ESA) Huygens probe, Cassini was the first spacecraft to orbit Saturn. Among Cassini's objectives was the study of Saturn's rings, Titan's atmosphere, and the behavior of Saturn's magnetosphere. Cassini ended its mission with an intentional dive into Saturn's atmosphere on September 15, 2017.*



# Example of Updated Requirements, Microcircuits Burn-in (BI)

- **Status**
  - Task Group (TG) chaired by N. Shindler
  - Published Guideline document JEP163.
  - Task Group is still open to address new concerns.
  - **The last TG meeting decided to produce a white paper on the on-going concerns (see below)**
- **On-going Concerns**
  - Ambient vs. case vs. junction temperature
  - BI of high-speed devices (frequencies approaching gigahertz range)
    - ❖ What about hot spots on the die? For example, a serializer/deserializer (SERDES) in an FPGA may run much hotter than the rest of the die.
      - Practically no data on hot spots (no verification of models)

## JEDEC PUBLICATION

---

**Selection of Burn-In/Life Test  
Conditions and Critical Parameters  
for QML Microcircuits**

---

**JEP163**

SEPTEMBER 2015

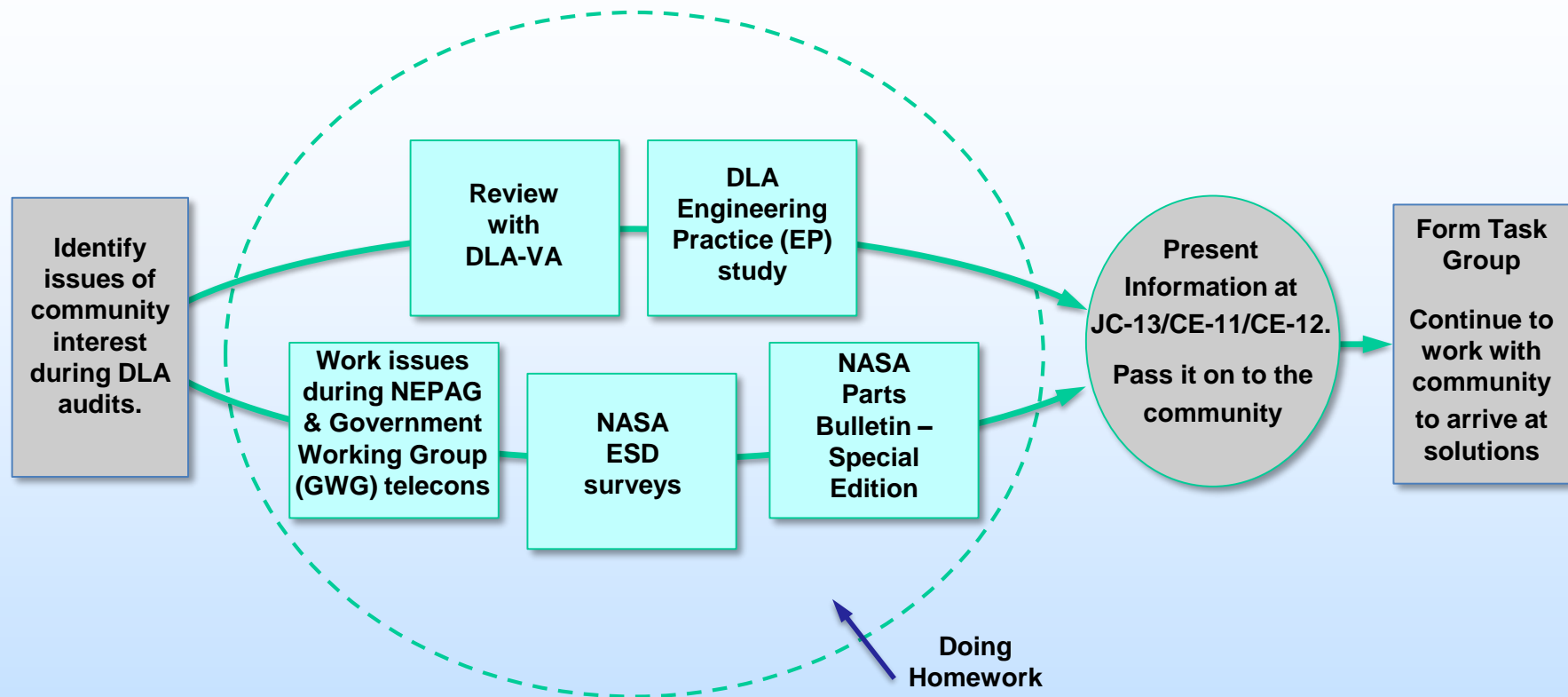
---

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

**JEDEC**<sup>®</sup>



# Taking Audit Findings a Step Further! NASA Timesaving Approach



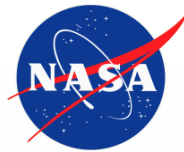
- Bring general awareness (Via NASA Bulletins, Surveys)
- Work with DLA to help them conduct an engineering practice (EP) study
- Generate a basic proposal and related information so the potential task group (TG) has a strong starting point.
- This path has saved time in resolving major issues found during audits.

# Electronic Parts and Electrostatic Discharge (ESD) – Gaps and Mitigation Strategies



- Gaps have evolved because of new technology and inconsistencies of standards development (e.g., three zaps vs. one zap per pin for testing). **Parts have continued shrinking to smaller sizes and growing in complexity. Consequently, they are more susceptible to ESD and require more testing effort.**
- **Costs cannot be ignored—per unit price for advanced devices is approaching \$200K. ESD mitigation costs are minute compared to the device unit costs.**
- **Mitigation strategies include NASA ESD surveys, observations during audits, standards updates (including harmonization of standards), and outreach to the military and space communities.**

# NASA ESD Surveys of Microcircuit Supply Chain



- **NASA ESD Surveys for Domestic and International Suppliers**
  - **Benefits not only NASA but the whole community**
    - ❖ **Especially vendors processing very expensive new technology parts (per unit price could approach \$200k)**
  - **Candidate companies are identified during DLA audits—but not a DLA activity**
  - **Conducted by NASA ESD experts**
    - ❖ **The survey findings and corrective actions have been merely suggestions for improvements**
  - **Very well received**
    - ❖ **Vendors have implemented most suggestions**
    - ❖ **Some vendors have requested re-surveys every two years**
  - **Working with Suppliers and DLA to incorporate NASA ESD Surveys into DLA audit agendas**
    - ❖ **Make efficient use of resources**
  - **Seeking to coordinate with international partners regarding incorporation of ESD into specs**

# A Changing Landscape (Shipping/Handling/ESD Challenge)



## A New Trend – Supply Chain Management

Ensuring gap-free alignment for each qualified product

(All entities in the supply chain must be certified/approved)

Manufacturer A	Die design
Manufacturer B	Fabrication
Manufacturer C	Wafer bumping
Manufacturer D	Package design and package manufacturing
Manufacturer E	Assembly
Manufacturer F	Column attach and solderability
Manufacturer G	Screening, electrical and package tests
Manufacturer H	Radiation testing

***More Stops — More Places with ESD Risk***

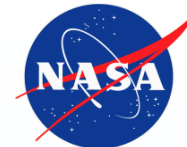


# Electronic Parts and ESD – NASA Concerns



- **MIL-STD-883, Test Method 3015**
  - Too old
  - Does not include the charge device model (CDM), only the human body model (HBM)
  - The Test Method needs to be revisited for new technology
    - ❖ Smaller feature sizes (down to 30 nm)
    - ❖ Large number of contacts/pins (e.g., ~1750 for Xilinx FPGA)
    - ❖ Vastly increased time to test
    - ❖ Advancements in packaging (2.5D, 3D)
  
- **MIL-PRF-38535 - Performance specification for microcircuits**
  - DLA audits of microcircuit manufacturers and their supply chains
    - ❖ Are done to the requirements stated in 38535
  - Poor coverage for ESD
    - ❖ No CDM testing required
    - ❖ Confusing requirements
      - 883 vs. JEDEC (3 zaps/pin vs. 1 zap/pin, for HBM test)
    - ❖ No requirements for wafer foundries
  - Needs to be updated
    - ❖ For new technology
    - ❖ For shipping and handling of products in multi-supply chain production of parts (which is becoming the norm)
  - 38535 Revision L covers a number of these issues.

# Electrostatic Discharge



## • NASA EEE Parts Bulletin (August 2017 – May 2018)

National Aeronautics and Space Administration

### EEE Parts Bulletin

A periodic newsletter of the NASA Electronic Parts Program / NASA EEE Parts Assurance Group and the Jet Propulsion Laboratory

August 2017 – May 2018 • Volume 10, Issue 1 (Published since 2009), July 17, 2018

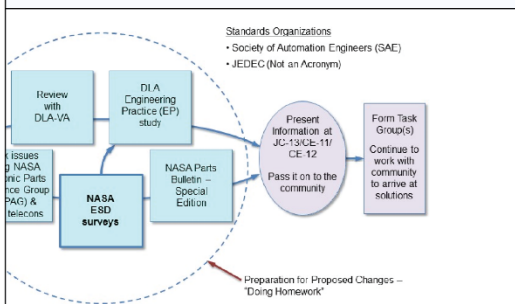
Third Special Edition on Electrostatic Discharge (ESD)

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. This is the third issue on the subject. The first issue dealt with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. The second ESD special issue focused on a parts failure investigation that ultimately concluded that ESD was the most likely cause of the failure. The second issue also included an important reminder about regular ESD testing. This third issue provides an example demonstrating the importance of maintaining ESD discipline and a high-level risk analysis related to electrostatic discharge. Figure 1 shows a major failure caused by ESD.

Figure 1. An ESD event of roughly 2.3 kV struck an RF transistor. The current caused a hole penetrating the underlying diffusions and an accumulation of material that re-solidified and shorted between the emitter and the collector (image courtesy of Hi-Rel Laboratories).

**ESD Issues and Specification Updates in Progress**

Figure 2 summarizes the flow process developed to address major issues such as multiple conflicting ESD standards. In the figure, two paths lead from DLA audits and NASA ESD surveys to eventual changes in standards related to updates in ESD practices. The organizations involved are the Defense Logistics Agency (DLA with its engineering practice studies) in the upper path. The lower path includes the NASA Electronic Parts Assurance Group (NEPAG, with its Government Working Group, GWG), the NASA ESD surveys, and the NASA *EEE Parts Bulletins*. The two paths converge with the findings



standards as a sample of how observations from DLA audits and NASA ESD surveys raise developed for those issues.

before the parts community primary document MIL-PRF-

(e.g., 883 vs. JEDEC of respectively, for human

at the ESD requirements

Method 3015 items that own to 45 nm)

contacts/pins (previous pins, now many more, in a FPGA). This greatly

(e.g., 2.5D, 3D) have not

ends when revising test more important because devices are very high (and inclination is added), on a scale of dollars per unit. Each product creates the damage to them, either of Costs for implementing a minuscule compared to

the overall cost incurred in dealing with ESD damage.

NASA is working with the community on electronic parts and ESD. DLA has issued a marked-up version of MIL-

PRF-38535 to Revision L. It includes many updates on ESD requirements. NASA is continuing to perform ESD surveys of the supply chain. There is also an effort to harmonize JEDEC JESD 625 and the Electrostatic Discharge Association (ESDA) 20.20 documents.

#### Reference

- MIL-STD-883K, *Test Method Standard, Microcircuits*, Defense Logistics Agency, Columbus Ohio, April 26, 2016.
- MIL-PRF-38535K, *Integrated Circuits (Microcircuits) Manufacturing, General Specification for*, Defense Logistics Agency, Columbus Ohio, Dec. 20, 2013.

#### For more information, contact

Shri Agarwal 818-354-5598

#### Lessons Learned on the Importance of ESD Training and Hardware Access Limitations for CubeSat-Level Projects

In order to minimize the chance of an electrostatic discharge (ESD) event occurring and damaging hardware, it is extremely important to keep hardware access limited to those experienced with ESD precautions and/or trained to ESD control standards such as ANSI S20.20.

An example of this manifested on a small project using a comparably small supplier. The project was a six-unit CubeSat, a 20 X 30 X 10 cm spacecraft, that was deployed from the International Space Station (ISS) with a short mission duration of 90 days.

with a cost of less than \$10 number of sophisticated came from suppliers to the small projects, many people this extends to CubeSat of these systems do not have ent system (QMS); rather they ed experience.

bar QMS level and can be without additional support. The lites may need ESD guidance

of the small suppliers was a up providing a subsystem for development group needed software. However, software as experienced with handling p are more intimately involved king of said hardware. Under ple pressure, the software e task needing regular access efficiently instructed as to the or the ESD controls required.

electronics board to the testing, and during this testing ing. The root cause was not low-up investigations strongly s were not properly exercised during testing. One individual y wrist strap while powering lining and experience of these f ESD controls was clearly controls probably resulted in using significant schedule and t. Possibly, the damage could subsystem had processes for teams and monitoring their

ere learned. First, a project check the ESD practices of all ond, that surveying actively level teams or individuals who he hardware in addition to all mbly and test personnel. nstruct their supplier to upgrade y and possibly even provide

tection of Electrical and bilities and Equipment (Ex- tled Explosive Devices), Association, 2014.

#### A Risk Analysis Related to Electrostatic Discharge and Other Failure Mechanisms

##### A. Failure Reports Analyses and Results

The data analyzed for this study originated in failure reports spanning a period from January 2001 through September 2013. These reports were created when a system development project requests the failure analysis lab to perform a detailed analysis of a failed electrical component.

Background information for each is included describing the situation that led to the failure (e.g., failed a visual inspection or electrical testing). Occasionally, detailed information regarding the assembly history is included, for example, an incident occurring at initial power up or following environmental of electrical testing, or a unique situation such as testing following a component repair/replacement.

A total of 283 reports were reviewed. Data from 232 of these reports were described for this analysis. The remaining 51 reports described instances where the initial failures during system testing were not confirmed at the failure analysis lab. Situations where this could have occurred include undetected defects in the component mounting (e.g., an improper solder joint that was no longer present after the component was removed) or an intermittent fault. Figure 3 shows the number of failures that occurred per year, with a mean of 18 failures per year.

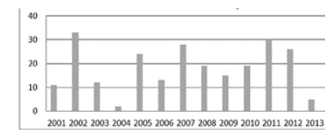


Figure 3. Number of failures per year.

All of the failure reports were carefully examined to diagnose the root cause of the failure. In order to ascertain trends and causes, the failures were sorted into the following categories: electrostatic discharge, electrical overstress, thermal overstress, mechanical overstress, foreign material, and chemical reaction.

Electrostatic discharge (ESD) is the failure mechanism that occurs when there is evidence on the semiconductor die of severe, localized damage. The indication is typically in the form of a crater or eruption through the insulating oxide layer seen only using extremely high magnification such as a scanning electron microscope.

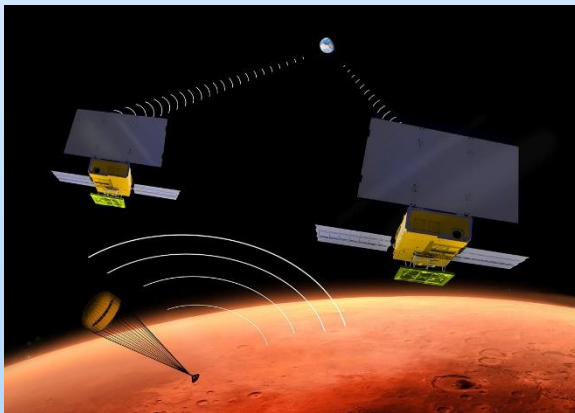
Incidence of ESD damage involves almost instantaneous transfer of electrical energy coupled with a very high static potential. Thermal damage is minimal as compared to electrical overstress. Some reports mentioned instances in which device or circuit board handling was suspect with

For more information, contact  
Amanda Donner 818-393-8636

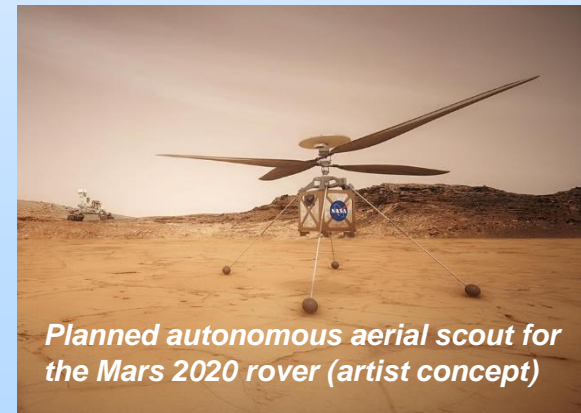
# CubeSats for Deep Space Exploration!



- Excerpt from November 27, 2018 email: Office of Director to the JPL community:
- “We are celebrating a “second Thanksgiving” of sorts for November 26, 2018 successful landing of **InSight on Mars**. The lander will help us understand the common origins of rocky planets and the divergent paths they have taken. InSight’s seismometer promises to add a new word – marsquake – to the vocabulary of planetary exploration.
- **We knew almost immediately that InSight had landed safely thanks to our twin Mars Cube One spacecraft (MarCO 1 and 2), the first CubeSats to fly into deep space. By successfully relaying data from another planet, this technology experiment has opened new possibilities for space exploration.”**



*Mars Cube One, MarCO for short, is a CubeSat mission of NASA’s Jet Propulsion Laboratory comprising two functionally identical six-unit CubeSats accompanying the InSight Mars Lander to provide communications relay during the Entry, Descent and Landing phase when the lander will not be able to directly communicate with Earth.*



*Planned autonomous aerial scout for the Mars 2020 rover (artist concept)*

# Growing Use of NASA CubeSats and SmallSats



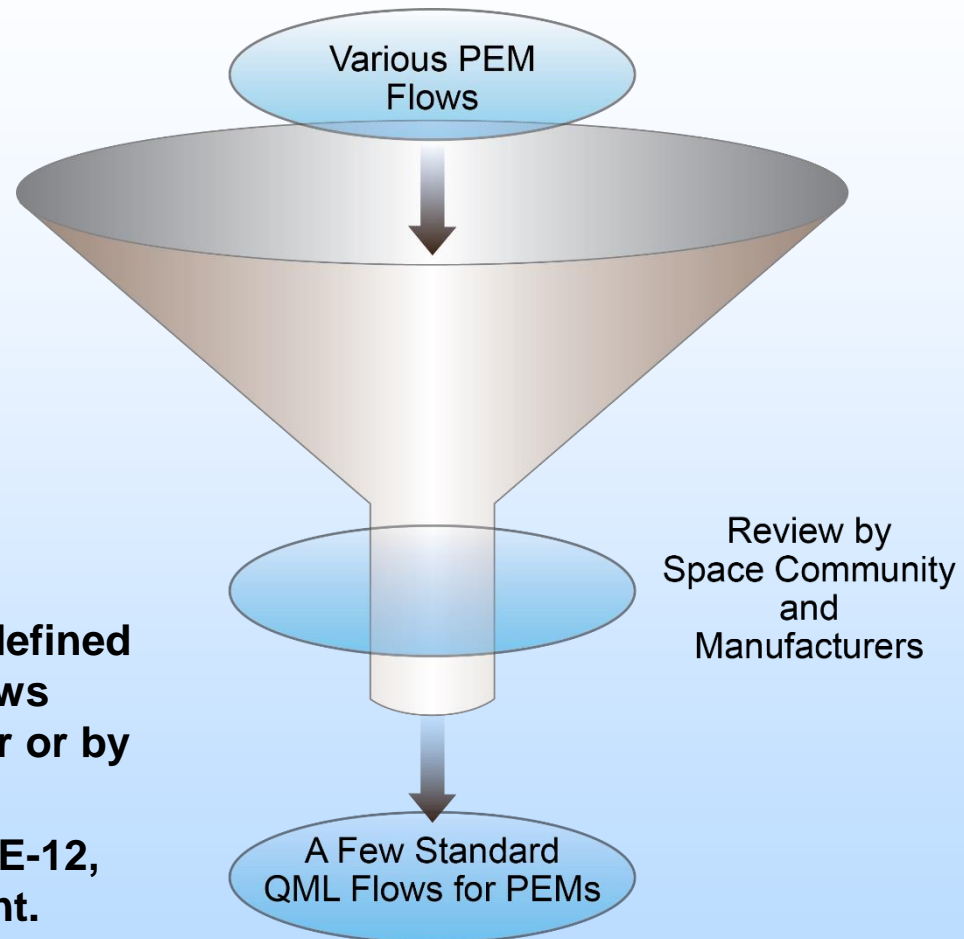
- Many new NASA flight missions are CubeSats and SmallSats.
- The parts manufacturers are offering customized parts, e.g.,
  - Cobham Aeroflex has several flows assigned based on extent of testing to assist users in picking the best parts.
  - Texas Instruments offers parts in five different versions, including their QML offerings.
  - Linear Technology (now a part of Analog Devices, Inc., ADI) plans to offer PEM products with guaranteed total dose radiation (rad tolerant, RT) ratings.
- Possible methods to get standardized flows
  - The ideal situation would be for the space community and manufacturers to agree on a limited number of standard QML PEM flows to offer solutions for small missions (CubeSats, NanoSats, SmallSats, etc.).
  - There is an existing QML N flow for standard non-space PEM devices.
  - **CE-12 developed a document SAE AS6294. That would be a good starting point.**
  - In addition, DLA has the Vendor Item Drawing (VID) program and parts built for automotive applications.

- **Newer Applications**

- **CubeSats**
- **SmallSats**

**Standardizing on a few well-defined flows rather than multiple flows defined by each manufacturer or by each standards group.**

**SAE AS6294, developed by CE-12, would be a good starting point.**



# NASA's Electronics Technology Workshop (ETW)



- The ETW is held in June every year
- Venue: Goddard Space Flight Center, Greenbelt, MD
- Past papers posted on NEPP Website:  
[nepp.nasa.gov](http://nepp.nasa.gov)
- See above website for other details
- **ETW 2019 will be held June 17–20, 2019**



Apollo 11



Space Shuttle



Voyager 1



# NASA 61 YEARS and COUNTING!!

QuikScat



Hubble Space Telescope

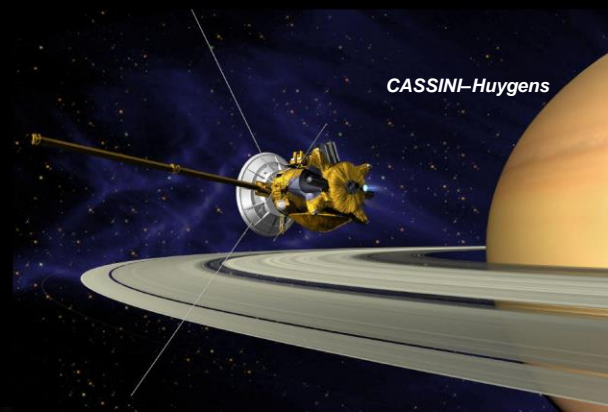


MER



Image Credit: NASA

CASSINI-Huygens



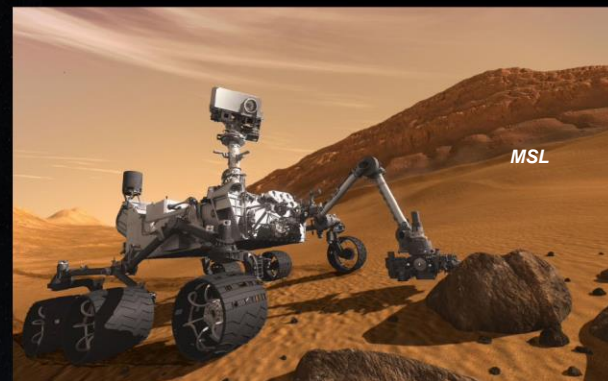
InSight



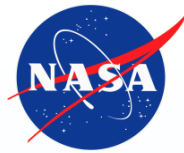
JUNO



MSL



# Goodbye, Opportunity!

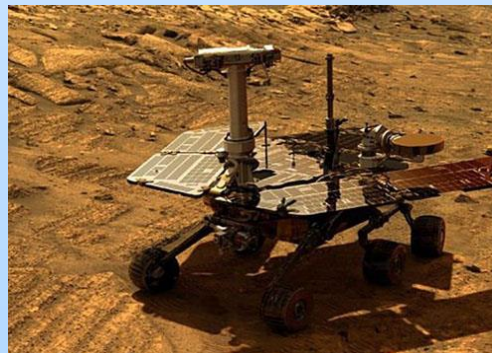


- Excerpt from Feb 13, 2019 email: NASA Administrator to the NASA community:
- “It was my privilege to join the staff of the Jet Propulsion Laboratory as we said goodbye to the Mars Rover Opportunity, which has remained quiet after a storm last June. For **15 years**, Opportunity has engaged billions of people worldwide in Martian science. Not bad for a mission originally slated for **90 days** on the surface! Holding the off-planet driving distance record, and lasting 60 times longer than its design predictions, Opportunity and its twin Spirit gave us a great run of science on the Red Planet and helped engage many future engineers and explorers who want to go to Mars themselves.

## [HIS VISION]

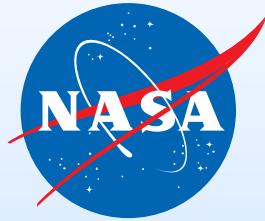
- **Because of trailblazers such as Opportunity, there will come a day when our brave astronauts walk on the surface of Mars. And when that day arrives, some portion of that first footprint will be owned by the men and women of our Mars Exploration Rovers mission, and the robotic explorers that defied the odds and did so much on the surface of Mars.”**
- **Before I conclude, I would like to take this opportunity to thank everyone who help us make the missions such as Mars Rover Opportunity successful!**

**Thank you!**





# <http://nepp.nasa.gov>



## **ACKNOWLEDGMENTS**

The research described in this publication was carried out, in part, at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. Help is gratefully acknowledged from Melissa Klose, Nazia Ovee, Mohammad Mojjaradi, Joon Park, and Michael Sampson.

Government sponsorship acknowledged.