# Recent EEE Components R&D and Evaluation for space applications

**Wenyan Wang  (wangwy09@gmail.com) , Ying Zhang**
**China Aerospace Components Engineering Center (CACEC),**
**China Academy of Space Technology (CAST)**

**Mar. 11-15, 2019, ESCCON 2019**

# Contents

# Contents

**✓ Introduction**

■ **New technology or parts**

➤ **Anti-fuse parts based on MTM**

➤ **65nm RH design platforms**

➤ **100V Input DC/DCs**

➤ **High voltage CMOS technology**

➤ **CMOS visible light image sensor**

■ **Quality assurance**

■ **Summary & about CACEC**

# Strategy of CAST EEE Parts

**Goal:**

- ➢ Achieve autonomous control of aerospace components

- ➢ Support the independent development of aerospace missions

**Action:**

- ➢ Miniaturize equipments into parts such as SiP, SoC or ASIC

- ➢ Develop new type parts according to application requirements of space equipments

- ➢ Take sufficient verification and validation for new developed parts to ensure the success of aerospace missions

# Research & Development Flow of New Parts

**Demand proposal**

- Aerospace costumer, e.g. CAST, puts forward parts development needs.

**R&D program approval**

- Management agency reviews the needs and make approvals for feasible needs.

**R&D implement**

- R&D company develops the parts according to costumer's requirements.

**Verification and validation**

- The developed parts are examined and verified by the third party organization.
- The costumers carry out the validation to judge whether the parts are to meet the requirements .

**Selection and application**

- The qualified parts enter CAST's PPL.
- The costumers select and apply the adaptable parts according to the PPL.

# Contents

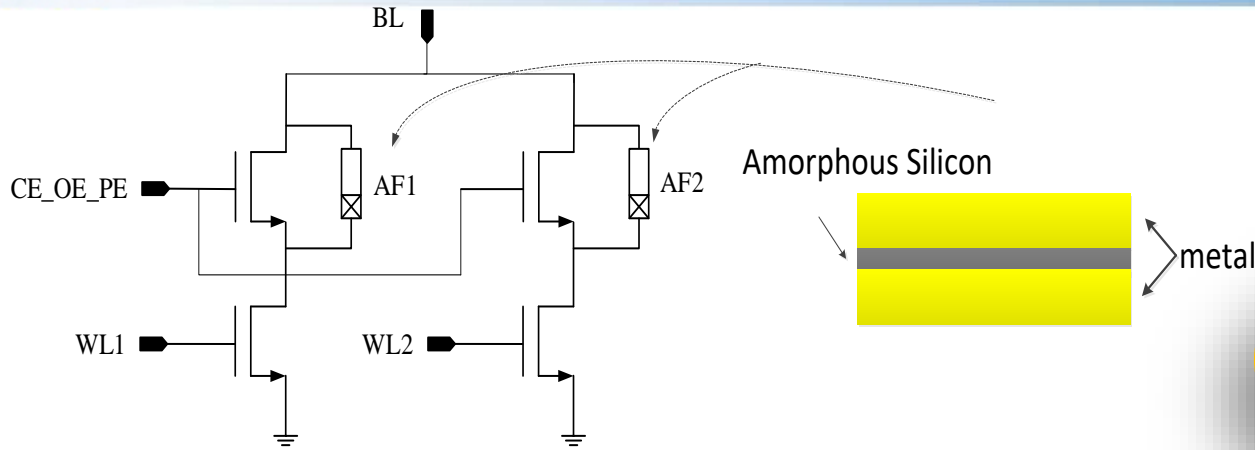**Introduction**

✓ **New technology or parts**

➢ **Anti-fuse parts based on MTM**

➢ **65nm RH design platforms**

➢ **100V Input DC/DCs**

➢ **High voltage CMOS technology**

➢ **CMOS visible light image sensor**

**Quality assurance**

**Summary & about CACEC**

# Anti-fuse parts based on MTM

BL

CE_OE_PE  AF1  AF2

Amorphous Silicon

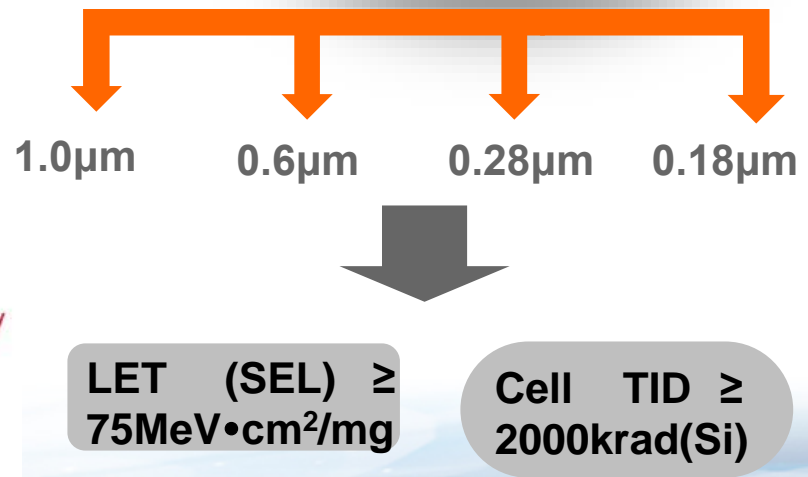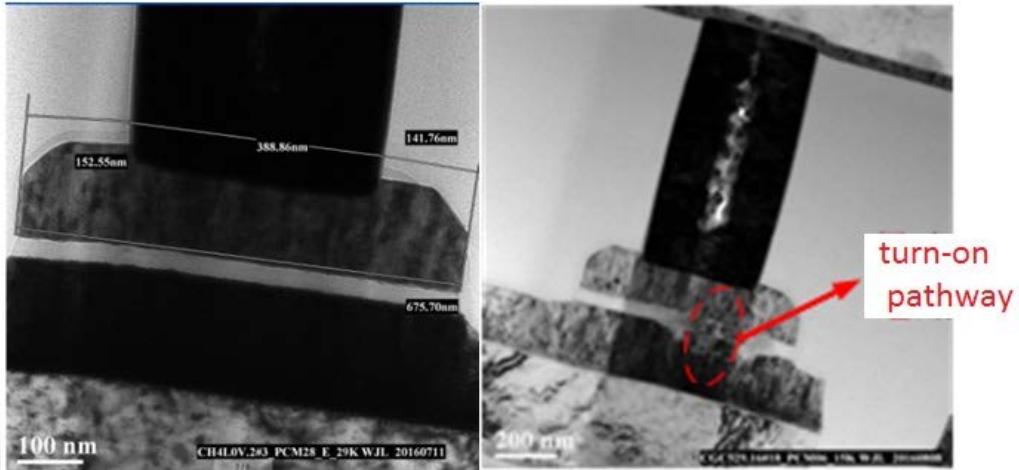metal

WL1  WL2

**Radiation harden anti-fuse CMOS plateform**

The schematic of memory cell with a MTM anti-fuse structure

152.55nm  388.86nm  141.76nm

675.70nm

100 nm  CH4L0V.2#3_PCM28_E_29K WJL 20160711

200 nm

turn-on pathway

1.0μm    0.6μm    0.28μm    0.18μm

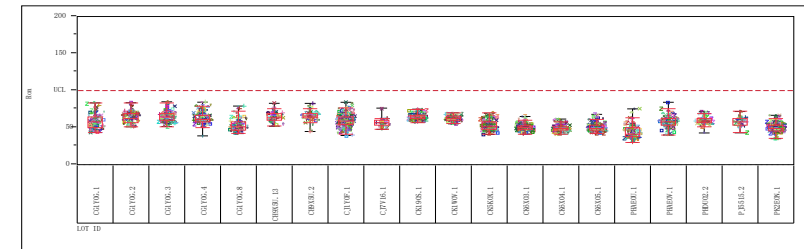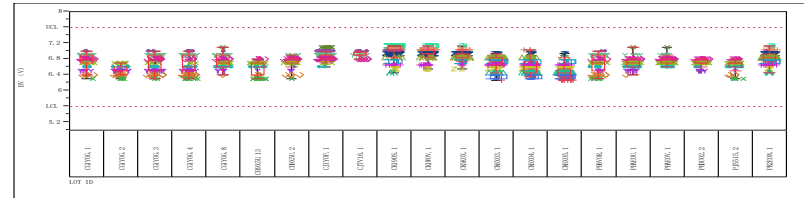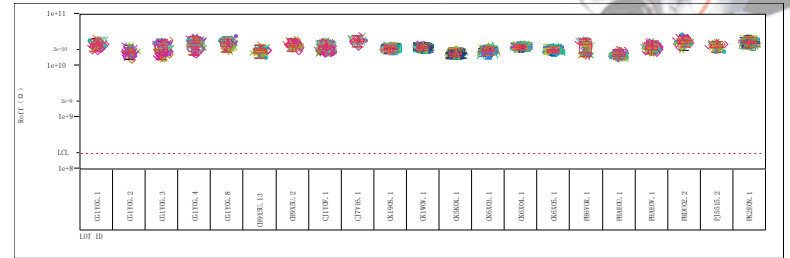LET (SEL) ≥ 75MeV•cm$^2$/mg
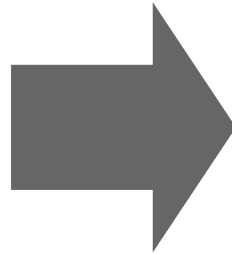
Cell TID ≥ 2000krad(Si)

The SEM images of the cross-sections of the MTM anti-fuse structure before and after being programmed
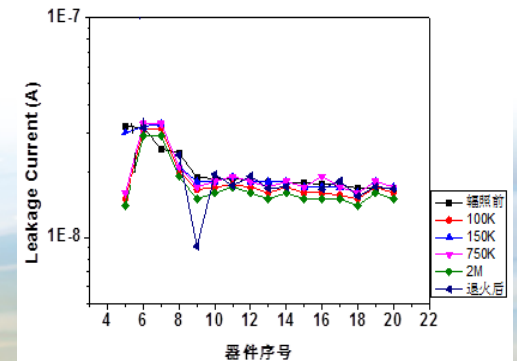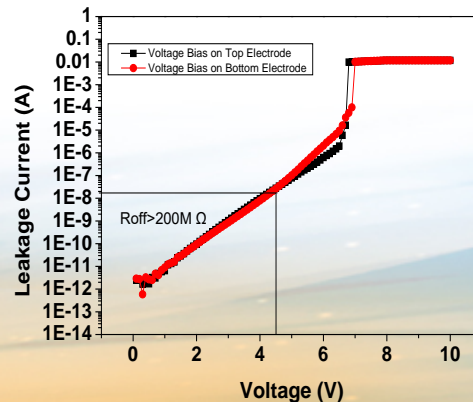
# Anti-fuse parts based on MTM

Reliability Test for MTM anti-fuse cell

- ✓ Leakage current
- ✓ Breakdown voltage
- ✓ Programming resistor
- ✓ Co60 r-ray test
- ✓ Programming characteristics
- ✓ IV characteristics

Life expectancy is greater than 20 years

# Anti-fuse parts based on MTM

✓ Series PROM parts have entered CAST's PPL.

✓ The anti-fuse 30K gates FPGA based on MTM will be released in winter, 2019.

✓ The 0.13um process development is on going and it can support 2M~4M gates FPGA.

| | Part No.1 | Part No.2 | Part No.3 |
|---|---|---|---|
| Supply Voltage | 5V±0.5V | | 3.3V±0.3V |
| Volume | 64Kbit | 256Kbit | 256Kbit |
| Package | CFP28/CDIP28 | | |
| Read rate | ≤65ns | ≤45ns | ≤65ns |
| Static current | ≤1mA | | |
| ESD | ≥2000V | | |
| TID | ≥100k rad(Si) | | |
| LET（SEL） | ≥99.8MeV•cm$^2$/mg | | |
| LET（SEU） | ≥37MeV•cm$^2$/mg | | |
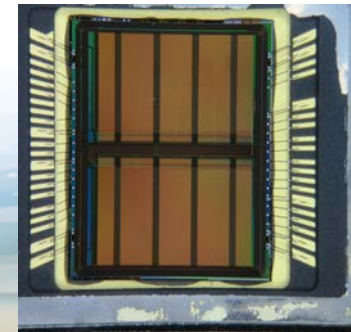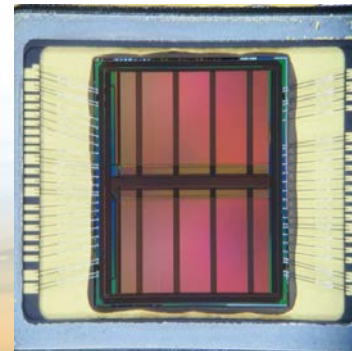
# Radiation-Hardened 65nm Platforms

➢ **China has developed 0.5μm, 0.18μm and 65nm ASIC design platforms, supporting RH ASIC with a scale up to 50 Million gates**

➢ **3 mature platforms, including 65nm: 50Mgate, 0.18μm: 5Mgate and 0.5μm: 500kgate, are thoroughly verified by ground tests and flight experiences**
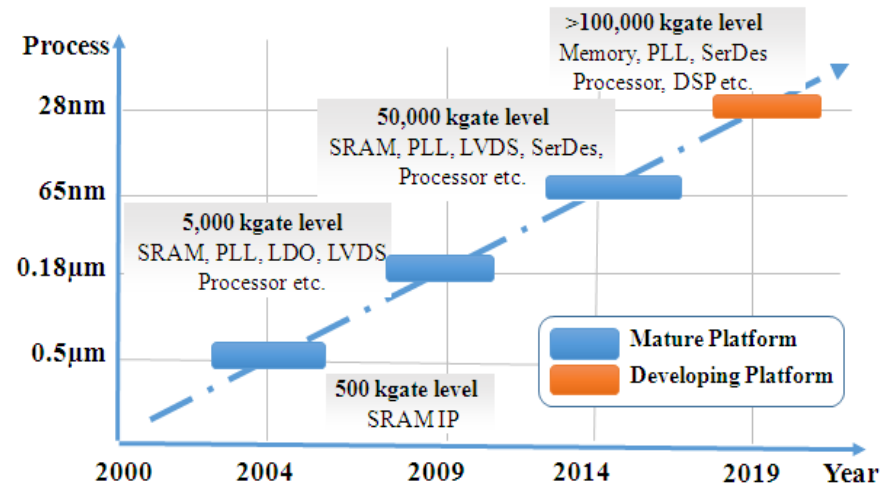


**Roadmap of RH ASIC**

➢ **Plentiful IP resources, complete sets of design kits and fluent design flow make ASIC design easy, fast and reliable**

➢ **The next-generation (28nm) platform is under development and to be released in Winter, 2019**

# Radiation-Hardened 65nm Platforms

## Main Features

☐ **Library**

- ✓ **11-track height**
- ✓ **3 $V_{TH}$ (RVT/HVT/LVT) for all core cells**
- ✓ **Includes SEU hardness options (high/medium/low)**
- ✓ **Supports both wire bonding and flip-chip**

☐ **Hard Macros**

- ✓ **Process: 65nm 1P10M CMOS, Voltage: 1.2/3.3, $F_{TYP}$(MHz): 300**
- ✓ **SRAM: SP/DP, up to 160 kbit/module, access time < 3ns**
- ✓ **PLL: 100MHz-1.5GHz, jitter$_{RMS}$ <100ps, SEFI hardened**
- ✓ **LVDS: 600Mbps, compliant to ANSI/TIA/EIA-544-A-2001**
- ✓ **DDR2/3: PHY + IO + Controller**

☐ **Design Kit**

- ✓ **Deliverable: verilog (.v), liberty (.lib/dB),  PR (.lef)**
- ✓ **Self owned: layout (.gds), netlist (.cdl)**

☐ **Radiation-Harden Feature**

- ✓ **TID: 300 krad(Si)**
- ✓ **SEL LETTH >99 MeV/mg/cm$^2$, SEU Rate:  <$10^{-10}$err/bit·day**
- ✓ **ESD (HBM): >2000V**

# Radiation-Hardened 65nm Platforms

## Main Features

☐ **SRAM IP (Fully hardened)**
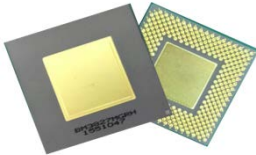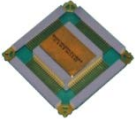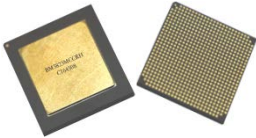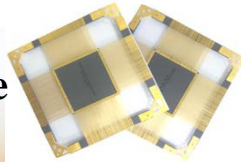
| SRAM Type | Address Depth | Bit Width |
|---|---|---|
| Single/Dual Port | 256 ~ 4096, increment 128 | 2 ～ 40 |

| Size | | Access Time (ns) | Power (uA/MHz) | Area (um$^2$) |
|---|---|---|---|---|
| Single Port | 256x2 | 1.70 | 5.15 | 7565.481 |
| | 2048x2 | 2.20 | 21.43 | 24857.78 |
| | 4096x40 | 2.70 | 97.70 | 541639.1 |
| Dual Port | 256x2 | 1.82 | 4.12 | 17637.1 |
| | 2048x2 | 2.25 | 17.56 | 52900.16 |
| | 4096x40 | 2.81 | 78.16 | 854977.5 |

- ✓ **Volume/module: 512 bits to 160k bits**
- ✓ **Access Time: <3ns**
- ✓ **Bit-interleaved array to mitigate MBUs, special for EDAC**

# Radiation-Hardened 65nm Platforms

## Product Types

| Product type | Main Features | Radiation Hardness |
|---|---|---|
| ASIC Or SoC | ✧System Gates: More than 12M Gates<br>✧72 SRAM modules, 1.26M bits in total<br>✧Package: CPGA391 | ✧TID>300 krad (Si)<br>✧SEL>99 MeV·cm²/mg<br>✧SER<1×10⁻⁵ error/day·device (GEO) |
| SRAM | ✧Capacity: 64M/39M/32M/19.5M bits<br>✧Package: CQFP84 | ✧TID>300 krad (Si)<br>✧SEL≥99 MeV·cm²/mg<br>✧SER<1×10⁻¹² error/bit·day (GEO) |
| CPU | ✧Max Frequency: 300MHz<br>✧with SRAM, PLL and DDR2/3<br>✧Package: CCGA717 | ✧TID>500K Rad (Si)<br>✧SEL>99 MeV·cm²/mg<br>✧SER<1×10⁻⁵ error/day·device (GEO) |
| Spacewire | ✧Data rate: 400Mbps<br>✧with PLL and LVDS interface<br>✧Package: CQFP240 | ✧TID>300K Rad (Si)<br>✧SEL>99MeV·cm²/mg<br>✧SER<1×10⁻⁵ error/day·device (GEO) |

*Some (about 20 ) other 65nm ASICs are now under development*

# Radiation-Hardened 65nm Platforms

## Description (LCDSP1601ARH：A RH Heterogeneous Multi-core Digital Signal Processor)

- •65 nm CMOS Technology
- •1 PowerPC Processor with ISA 2.05
  - −Out-of-order, superscalar with 4 launches
  - −32K Byte L1 P-Cache/32K Byte L1 D-Cache/256K Byte L2 Cache
- •16 Autonomous Digital Signal Processors with Revealer-ISA, Each With
  - −Revealer-ISA: 32bit Instruction Set facing to digital signal processing
  - −64K Byte D-Memory/64K Byte P-Memory
- •Network on Chip（NoC）Interconnection and Communication Architecture
  - −4×4 2D Mesh NoC based on GALS Architecture
  - −Fault Tolerant Routing, 102.4Gbps Communication Bandwidth per Direction
- •4 Channels of RapidIO 2.2
  - −2.5Gbps per Lane, 4 Lanes per Channel, supports 1x/4x mode
- •2 DDR SDRAM Controllers
  - −Supports DDR3-800, DDR2-400, DDR2-533, DDR2-667, DDR2-800
- •1 QDR SDRAM Controller
  - −Compliant with CYPRESS QDRII+SRAM
- •Package: CCGA1284
- •Peak Power: 16W(80 percent of Peak Performance)
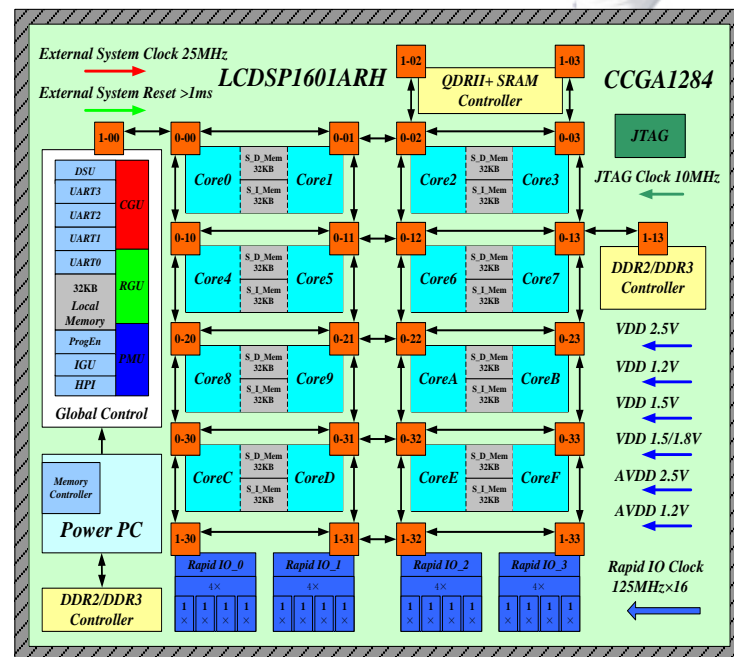


LCDSP1601ARH Block Diagram

## Feature

- •Parallel Access to computing and storage in Revealer-ISA Based on Hardware pipeline driven by Instruction
  - −27.56us for 1024-point FFT with 1 DSP(Single Precision Floating Point Complex)
  - −3.65us for 1024-point FFT with 10 DSP(Single Precision Floating Point Complex)
  - −31.6ms for image matching with 16 DSP(512×512,128×128)
- •Dynamic Reconfigurable ALU
  - −Supports Butterfly operation, Complex multiplication, Matrix operation, Vector operation, etc
- •Anti-irradiation Performance
  - −TID ≥150Krad(Si), LET ≥75MeV•cm$^2$/mg, SEU ≤1E-5Error/device·day
- • Peak Performance: 102.4GMACs@400MHz, 51.2GFLOPs@400MHz
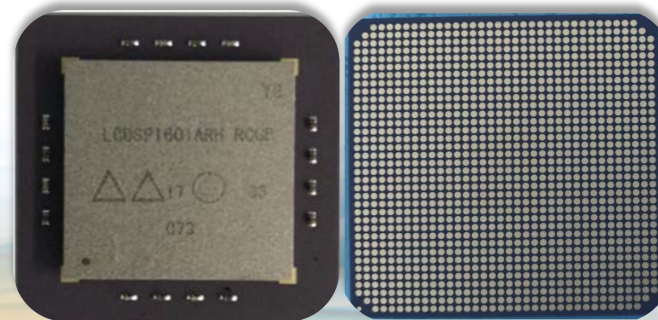


LCDSP1601ARH Chip

13

# Radiation-Hardened 65nm Platforms

## Description (LSP0201RH：A Radiation-hardened Dual-core PowerPC Processor)

### ➢ Processor Subsystem

- ✓ 32-Bit Embedded PowerPC 470 Superscalar
- ✓ 32KB L1 I/D Cache with Parity Check
- ✓ 256KB L2 Cache with 64+8 ECC
- ✓ Dual-Core SMP Architecture, 400MHz
- ✓ Fixed-Point Performance：2000 DMIPS
- ✓ Floating-Point Performance：171.4 MFLOPS

### ➢ Memory Subsystem

- ✓ DDR2/3, 4GB, with 32+8 ECC
- ✓ EMIF(SRAM/PROM/IO), 4GB, with 32+8 ECC
- ✓ On-Chip SRAM, 32KB, with 8+5 ECC



LSP0201RH block diagram

### ➢ Peripheral & Communication Subsystem

- ✓ 4-way SPI,4-way UART, 32-way GPIO, 2-way CAN, 4-way DMA
- ✓ 2-way 1553B with 1/4/10Mbps, 3-way SpaceWire with 200Mbps
- ✓ 4-lane RapidIO with 2.5Gbps/lane
- ✓ 2-lane PCIe with 5Gbps/lane
- ✓ 1-way Ethernet with 10/100/1000Mbps
- ✓ Multi-Processor Interrupt Controller(MPIC) with 128 Sources
- ✓ Hierarchy Interconnection with DCR and PLB

### ➢ Reliability Parameter

- ✓ TID ≥ 100krad（Si）
- ✓ LET ≥ 75MeV.cm$^2$/mg
- ✓ SEU ≤ 1E-5Error/device.day
- ✓ Operating Temperature：-55℃~125℃
- ✓ ESD ≥ 2000V

### ➢ Application Field

- ✓ Spaceborne intensive task control
- ✓ Real-time network communication and data processing

### ➢ Product Status

- ✓ 65nm CMOS technology
- ✓ Release time: 2019

14

# Radiation-Hardened 65nm Platforms

## Design Service for RH ASICs

We and our partner BMTI are willing to transfer our latest technology for customers to implement their radiation-hardened products, and can provide customers with licensed radiation-hardened libraries, IPs and experienced design services

**Design Services**

- IP License
  - Standard Cell Libs
  - IO/Interface IPs
  - Embedded IPs
- Design Service
  - FPGA to ASIC
  - ASIC/SOC
  - Customized Design

**Service Modes**

Input:
- SPEC
- RTL
- Netlist
- P&R
- Customized

→ Rad-Hard Platforms →

Output:
- IP
- Mask
- Wafer
- Prototype
- Flight Model

Service modes can be various with multiform inputs and outputs, and customers can choose any mode according to their situation

# Radiation-Hardened 65nm Platforms

## Design Service for RH ASICs

**Service Modes**

| Input | Rad-Hard Platforms | Output |
|-------|--------------------|--------|
| SPEC | | IP |
| RTL | | Mask |
| Netlist | | Wafer |
| P&R | | Prototype |
| Customized | | Flight Model |

➢ **Our ASIC service is not limited to design, but also includes services in wafer fabrication interface, package design, packaging, testing and screening per customers' request**

➢ **Several customers from Russia have shown their interests in our ASIC techniques and a few of them have been working with us on IPs and design service**

# Radiation-Hardened 65nm Platforms

## Design Service for RH ASICs

**Design Phase**

Customer

| RTL Source Code
Test Bench Code
(usually FPGA verified) |

Modification Suggestion

Customer &BMTI

Code Check

Fail

Pass

Customer or BMTI

Synthesis

db+verilog

DFT

BMTI's design kits are fully compatible with standard VLSI design flow and main-stream EDA tools

rc

Power Analysis

Customer and/or BMTI

| Physical Verification
• DRC/LVS
• DFM
• ESD |

Cdl+gds+Drc+lvs+ dfm+esd

| Post-layout Verification
• Formality
• Function
• Timing |

ccsm+verilog

Foundry

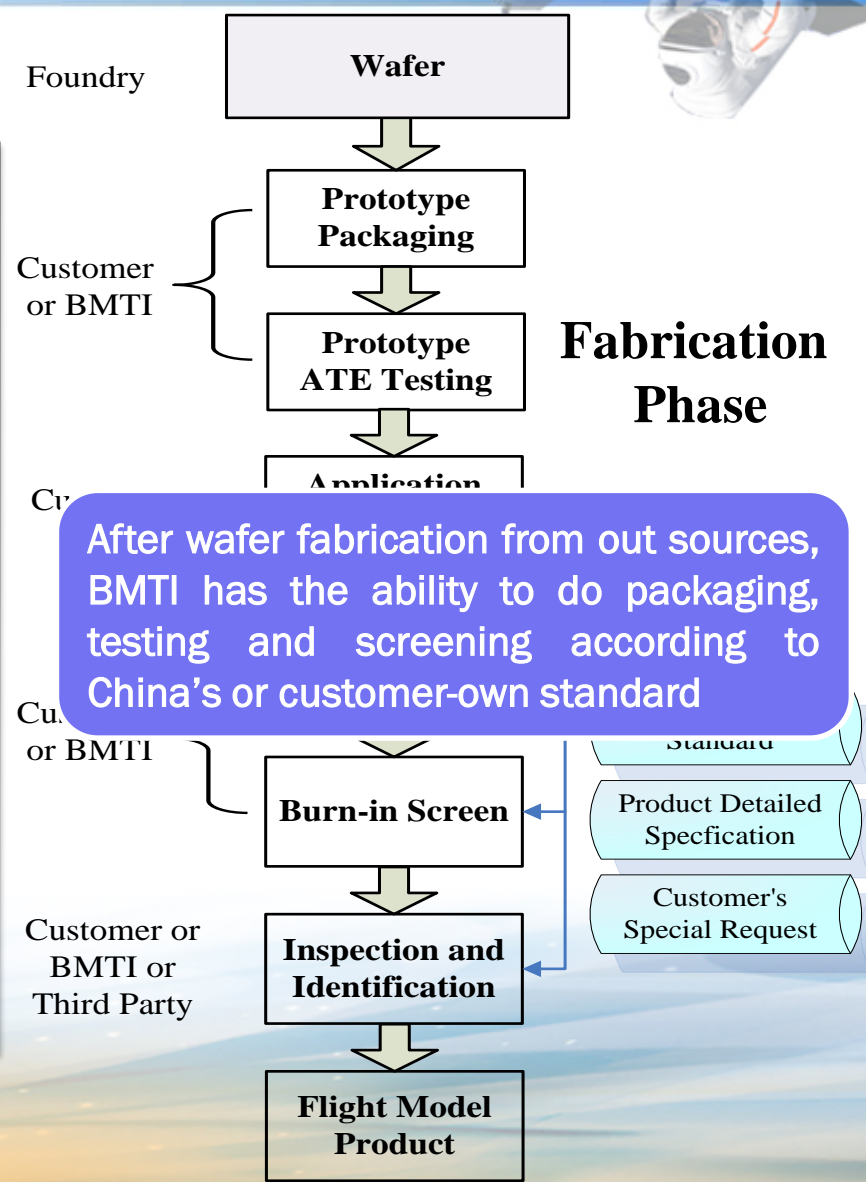Tape Out

GDSII

**Fabrication Phase**

Foundry

Wafer

Prototype Packaging

Customer or BMTI

Prototype ATE Testing

Application

After wafer fabrication from out sources, BMTI has the ability to do packaging, testing and screening according to China's or customer-own standard

Standard

Customer or BMTI

Burn-in Screen

Product Detailed Specfication

Customer's Special Request

Customer or BMTI or Third Party

Inspection and Identification

Flight Model Product

# 100V Input DC/DC

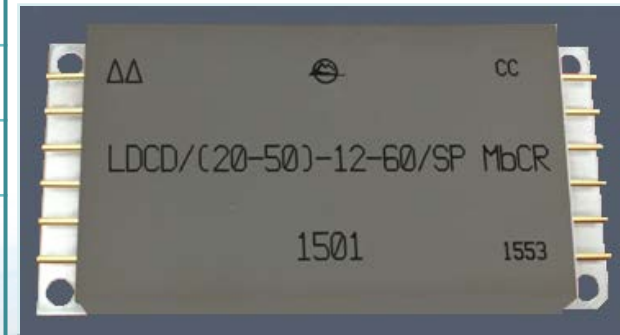The aerospace anti-radiation DC/DC converter consists of two series of 20-50V and 80-120V products, covering 28V, 42V and 100V input voltage bus, which can provide stable voltage and power for the spacecraft's electronic circuits

**Anti-radiation design technology**

- **Topology structure**
  - Single-end → No common mode turn-on risk, easy to integrate
  - Magnet-isolated feedback → operating point does not drift with the radiation

- **Die selection**
  - RH Die → Controller, VDMOS, operational amplifier
  - Radiation test assessment → Bipolar test：0.1rad/s MOS test：50rad/s

- **Compensation optimization design**
  - Error feedback → Offset voltage, offset current, impedance matching
  - Reduce electronic stress of transistors → Resonant reset and lossless absorption circuit

# 100V Input DC/DC

## ☐ Product Feature

| Product Type | 28V & 42V Series | 100V Series |
|---|---|---|
| Input voltage | 20~50V | 80~120V |
| Typical input voltage | 28V, 42V | 100V |
| Output power | 1.5W~65W | 5W~65W |
| Typical frequency | 500kHz | 300kHz |
| Output voltage | 3.3V、5V、12V、 15V、 ±5V、 ±12V、±15V、 5V&±12V、 5V&±15V | |
| Feedback | Magnetic isolated | |
| TID | ≥100krad（Si） | |
| LET | ≥75MeV·cm$^2$/mg | |
| Internal key die RH | PWM controller, VDMOS, operational amplifier, are radiation hardened | |



LDCD/100-12-5/D1 MCR
1403    1438

LDCD/100-5R-15/SP MCR
1406    1438

LDCD/(20-50)-12-60/SP MbCR
1501    1553

# SSPC (Solid State Power Controller)

The aerospace anti-radiation solid-state power controller (SSPC) is an intelligent switching device that integrates the conversion function of the relay and the circuit protection function of the circuit breaker.

- ➢ No contact, no electronic arc, no noise, fast response, long life, low electromagnetic interference

- ➢ High reliability and easy remote control

- ➢ Input voltage: 10～120V

- ➢ Output current: 1A、3A、10A、15A

- ➢ $I^2t$ overcurrent protection with thermal memory

- ➢ TID ≥ 100krad(Si)

- ➢ LET ≥ 65MeV·cm$^2$/mg
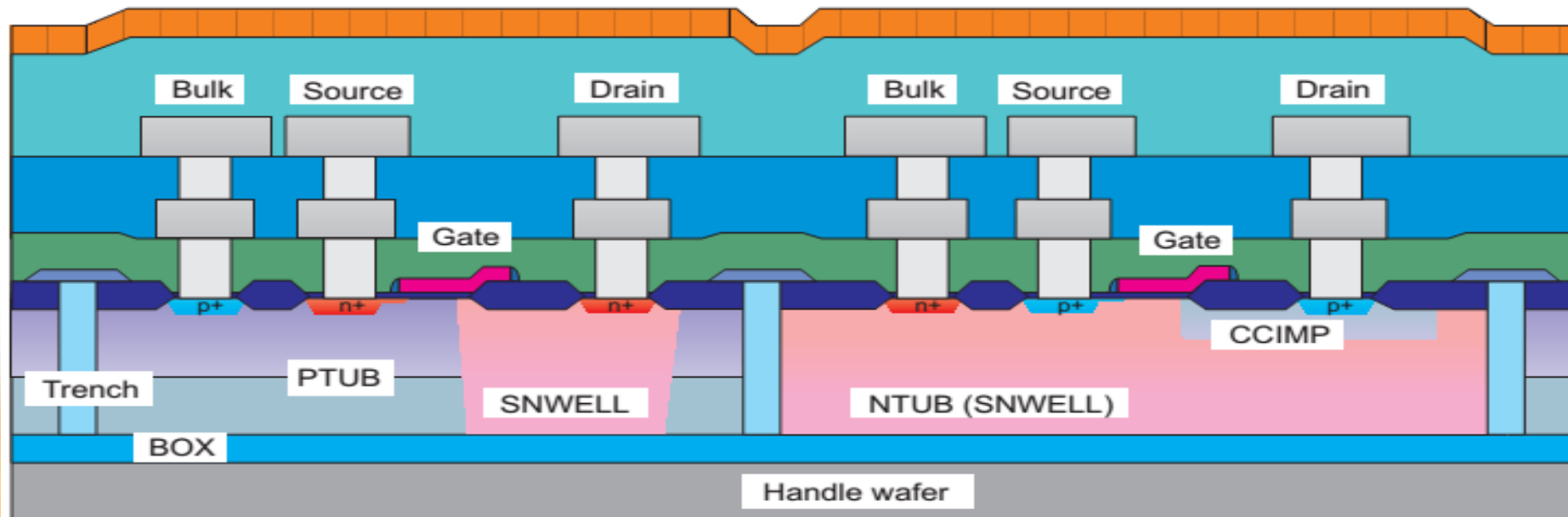
# High Voltage CMOS Technology

**Anti-radiation high-voltage integrated circuits developed by fully dielectric isolation SOI technology have many advantages.**

- Eliminate crosstalk and SEL
- Small isolation area and high integration
- Small leakage current & high temperature resistance
- Small parasitic capacitance & less parasitic effects

# High Voltage CMOS Technology

◆ **The part's gate and drain have a maximum operating voltage of 36V or higher**

◆ **leakage current under 30V leakage is less than 10pA/μm@125°C**

◆ **After 100 krad (Si) of total dose irradiation, the device functions normally and there is no significant change in leakage current.**
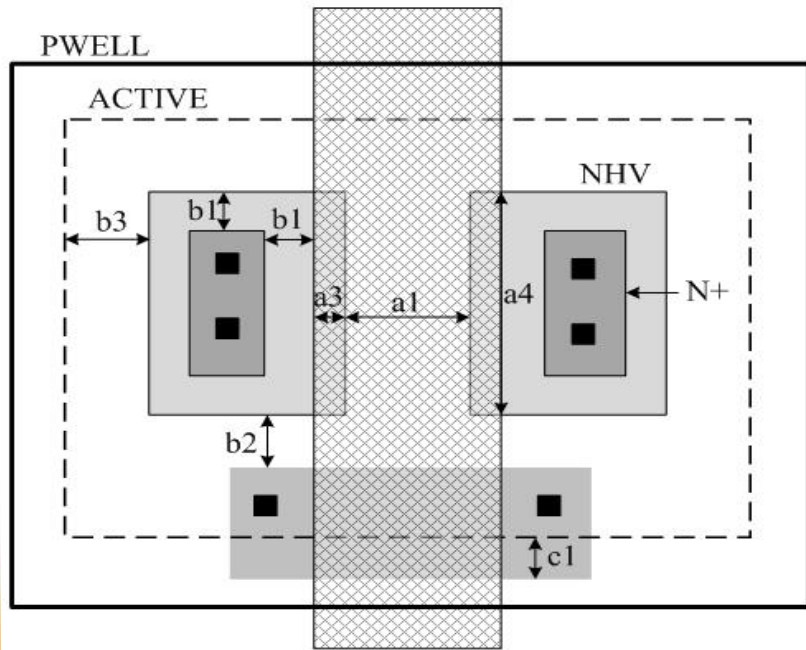


**Anti-radiation harden structure**



一次氧化+SIN淀积     Trench腐蚀     STI氧化

淀积多晶+多晶腐蚀后     多晶氧化     去SIN漂SIO2后
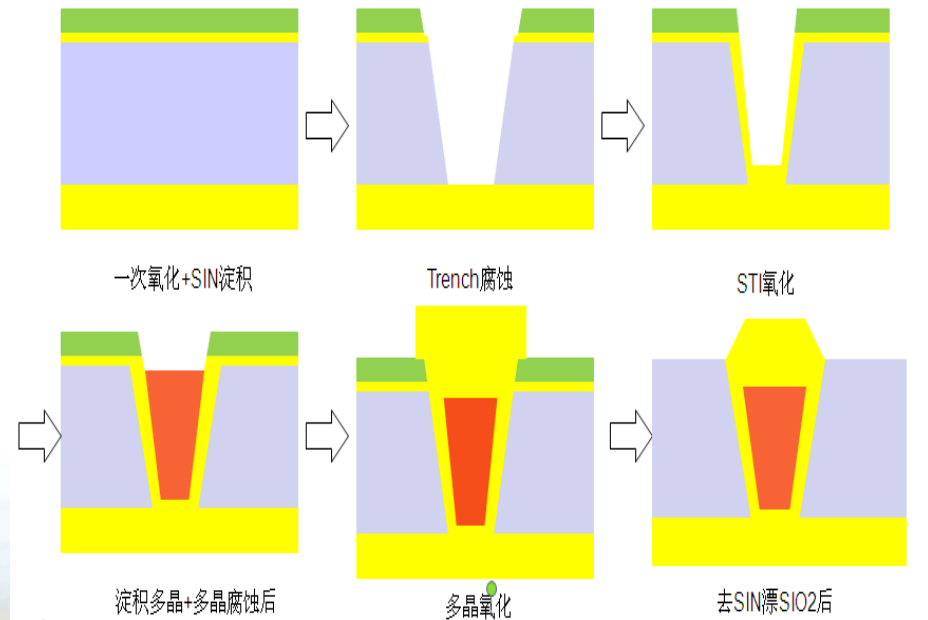
**fully dielectric isolation SOI process**

# High Voltage CMOS Technology

**12 part numbers have been developed and entered CAST PPL. Typical products are as follows:**

| Part No. | Function | Voltage | $R_{on}$ | $t_{on}$ | Over voltage protect | TID rad(Si) | SELMeV·c m²/mg |
|---|---|---|---|---|---|---|---|
| JHSR18XX | 16-ch | ±15V | ≤3kΩ | ≤1us | ±35V | 100K | 75 |
| JHSR05XX | Dual 8-ch | ±15V | ≤2kΩ | ≤1us | ±25V | 100K | 75 |
| JHSR05XX | 16-ch | ±15V | ≤2kΩ | ≤1us | ±25V | 100K | 75 |
| JHSR5XX | 8-ch | ±15V | ≤2kΩ | ≤1us | ±25V | 100K | 75 |
| JADR5XX | 16-ch with register | ±15V | ≤450Ω | ≤400ns | / | 100K | 75 |
| JHSR2XX | 4-ch SPST | ±15V | ≤100Ω | ≤130ns | ±17V | 100K | 75 |
| JHSR3XX | 双路DPST | ±15V | ≤75Ω | ≤500ns | / | 100K | 75 |
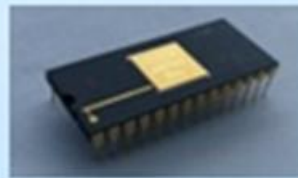
# CMOS Visible Light Image Sensor

**The LCIS64M has high quality optoelectronic properties, reliability and radiation resistance for spacecraft applications.**
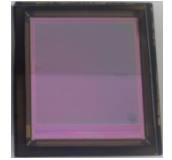
➢ **Property：**

- 8192×8192 active pixels on 5.67um pitch

- Frame rate 2.3frames/sec, 8 analog outputs

➢ **High reliability：**

- Quality Grade：C1 in GJB 5968-2007

- ESDs：≥ 1000V

➢ **High quality：**

- Dynamic range：＞67dB

- Dark current：＜30 pA/cm$^2$

➢ **High radiation resistance**

- TID：＞50krad(Si)

- SET: ＞ 99.8 MeV·cm$^2$/mg

---

The LCIS7P5M is a Back Side Illuminated CMOS visible image sensor .

- 2560×3072 active pixels on 7.5um pitch

- Frame rate 30frames/sec, global/rolling

- 21 pairs of LVDS digital outputs

- Release time: 2019

The LCIS225M is a Back Side Illuminated CMOS visible image sensor .

- 15000×15000 active pixels on 7.5um pitch

- Frame rate 6frames/sec, global/rolling

- 126 pairs of LVDS digital outputs

- Release time: 2019

# Contents

■ **Introduction**

■ **New technology or parts**

  ➢ **Anti-fuse parts based on MTM**

  ➢ **65nm RH design platforms**

  ➢ **100V Input DC/DCs**

  ➢ **High voltage CMOS technology**

  ➢ **CMOS visible light image sensor**

✔ **Quality assurance**

■ **Summary & about CACEC**
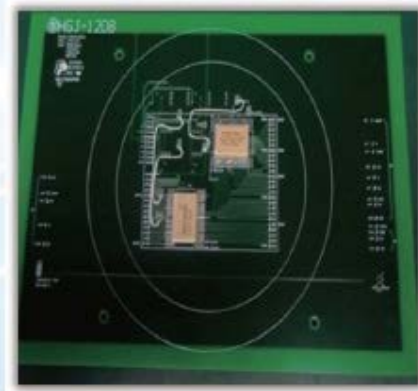
# Quality Assurance

☐ **Qualities of Monolithic ICs and Hybrid ICs**

➢ **The screen terms are done 100% according to GJB597B for monolithic ICs and GJB3438A for Hybrid ICs. The experiment methods are made reference to GJB548B. The qualities of the products are class S and B for monolithic ICs and class K and H for Hybrid ICs, respectively.**

➢ **Class S and B correspond to class V and Q of MIL-PRF-38535, and Class K and H correspond to class K and H of MIL-PRF-38534. And GJB548B is equivalent to MIL-STD-883.**

☐ **Application Validation**



Part-level **Test**    On-board **Test**    System-level **Test**

# Quality Assurance

## Application Validation

### Part-level

| Intrinsic function & performance | Construction analysis | Limited stress test | Accelerated life assessment |
|---|---|---|---|
| • Completeness of function<br>• Test coverage<br>• Consistency of parameters | • Design<br>• Manufacture process<br>• Materials | • Limited temperature test<br>• Limited electrical stress test | • 1000h<br>• 2000h |

**+**

### On-board & system level

| Function & performance of application | Environmental adaptability | Assembly adaptability | Adaptability to development environment | Comprehensive evaluation and typical application |
|---|---|---|---|---|
| • Basic functional performance<br>• Electrical characteristics of application<br>• Specific functional performance | • Electrical environment of application<br>• Thermal environment of application<br>• Mechanical environment of application<br>• Space radiation environment<br>• (SEU,SEL, TID)<br>• Combined space environment | • Assembly process features<br>• Assembly structural features | • Adaptability to development software<br>• Compiler adaptability | • Evaluation on aerospace availability<br>• Analysis of application notes<br>• Design of typical application |

# Contents

- **Introduction**

- **New technology or parts**
  - ➤ **Anti-fuse parts based on MTM**
  - ➤ **65nm RH design platforms**
  - ➤ **100V Input DC/DCs**
  - ➤ **High voltage CMOS technology**
  - ➤ **CMOS visible light image sensor**

- **Quality assurance**

- ✔ **Summary & about CACEC**

# Summary

◆ **In order to achieve autonomous control of aerospace components, we have developed a large number of new parts for space missions.**

◆ **According to our industry situation for space components R&D, In addition to take the ordinary quality assurance methods, we also conduct application validations for new developed parts to ensure the quality and reliability of space components.**

◆ **At present, we have already formed a certain ASIC development capability to meet the needs of the domestic space missions, and we can also provide ASIC customized services for other aerospace partners.**
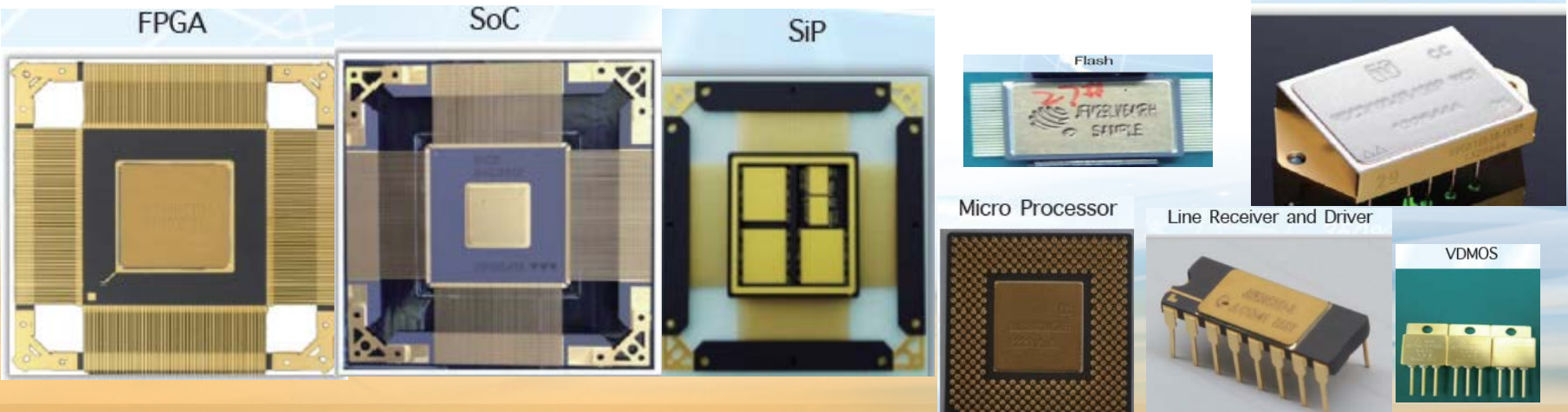
# About CACEC

China Aerospace Components Engineering Center (CACEC) ,founded in 1984, is affiliated with China Academy of Space Technology (CAST). CACEC has created an integrated service system on components engineering service and procurement service for 30 years, including **components selection, qualification, application validation, procurement, quality assurance** as well as logistics & storage. So far, CACEC has offered services for more than 130 spacecrafts both at home and abroad. Our objective is to be the **world-class service supplier of aerospace components.**

# About CACEC

## Main Products

**CACEC offers a wide range of products with more than 1,200 types, covering almost all categories of aerospace components. Most of the high-reliable components have been applied in Chinese satellite projects with successful flight experience, CACEC devotes to improve quality assurance services on newly developed components for space applications. Typical products: FPGA, DC/DC, SoC, SiP, VDMOS, ASIC, DSP, Line Receiver/Driver, Microprocessor, ADC&DAC, Memory, high power transistor.**



FPGA

SoC

SiP

DC/DC

Flash

Micro Processor

Line Receiver and Driver

VDMOS

# About CACEC

**Components procurement & supply service**

**FLOW**

Customers provide the requirement

↓

CACEC recommends components and offer the solution to customers

↓

Components qualification (If needed)

↓

Components procurement

↓

Quallty control and quallty assurance inspection

↓

Issue the COC

↓

Dellvery to customer, including data package

↓

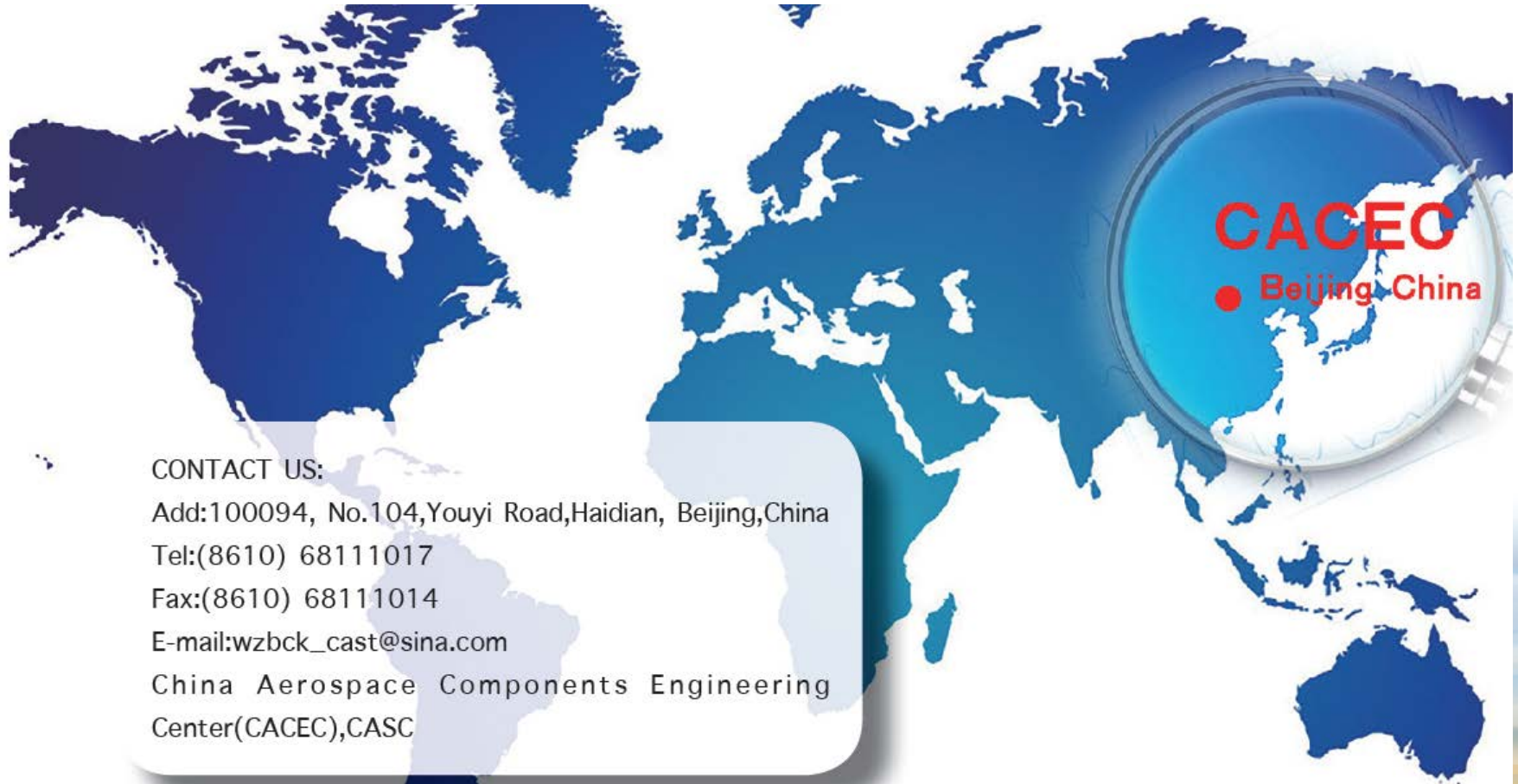Technical service after sale, including FA

# About CACEC

## Components procurement & supply service

**CACEC has both components engineering center and procurement center together in space application area. Service mode: One-stop shop solution**

CONTACT US:
Add:100094, No.104,Youyi Road,Haidian, Beijing,China
Tel:(8610) 68111017
Fax:(8610) 68111014
E-mail:wzbck_cast@sina.com
China Aerospace Components Engineering
Center(CACEC),CASC

CACEC
Beijing China

# Thank you for your attention