NX RHBD FPGA solutions For Today & Tomorrow Spaceborne applications

Joël LE MAUFF
Head of Marketing & Sales

Noordwijk, NL – 11th March 2019

Agenda

1- NX introduction

2- Space Market

3- RHBD FPGA solutions

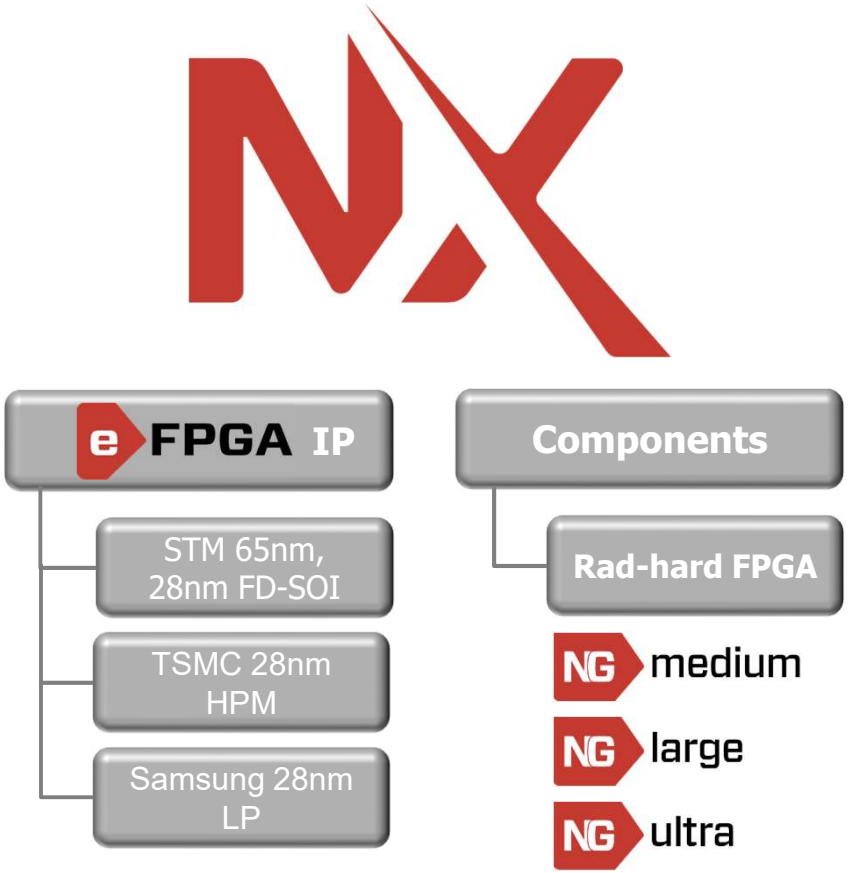
4 Packaging Technologies

5- NX Quality Flows

6- CONCLUSION

NanoXplore

NanoXplore Overview



- **Created in 2010** by three veterans of semiconductor industry with long experience in the design, test and debugging of FPGA cores.
- **Fabless** semiconductor company headquarter in France
- R&D engineers in two offices in France:
  - Sèvres: Hardware developments
  - Montpellier: Software developments
- **NanoXplore is a leader in the design of large scale programmable logic arrays for state of the art FPGA cores**
- The company is focusing on 2 main activities:
  - Offer hard block embedded FPGA core IP (NX-eFPGA)
  - Developing rad-hard FPGA qualified for space applications (from BRAVE contract)

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NanoXplore

Space Market

QA level

GEO

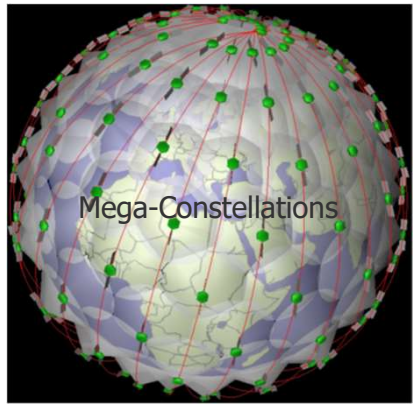
LEO

COTS

Ceramic / Class-1
QML-V

Organic / Class 1
ESCC PEM
(If justified by Delta Performances
Such as HSSL)

Ceramic / Class-2
(QML-Q)



Organic Class 2
B & M-grade

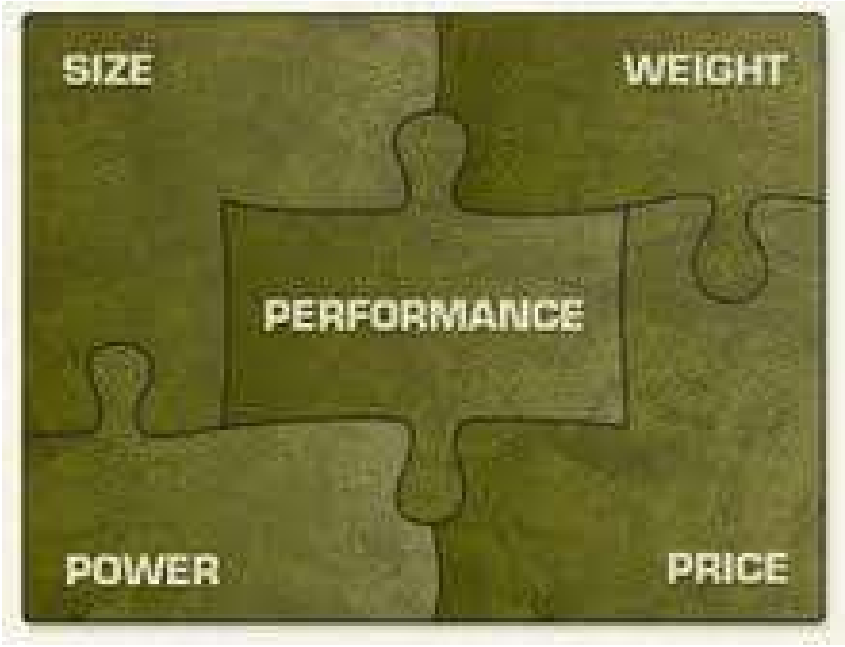
Other Small sat
M-grade
Even Com

Bubble area : Cost of ownership
Bubble density : Radiation Hardness

Quantity (typ)

1 10 100 1000

Space Trends



- **SWaP-C** *(Stands for Size, Weight and Power + Cost)*
  - ***Space EP or COTS+ components***
- Radiation-Tolerance/Hard solution
- ITAR-free components

Space Trends – What about FPGAs

Space requirements extracted from last ESA HEDPT workshop, dated 01/10/2018

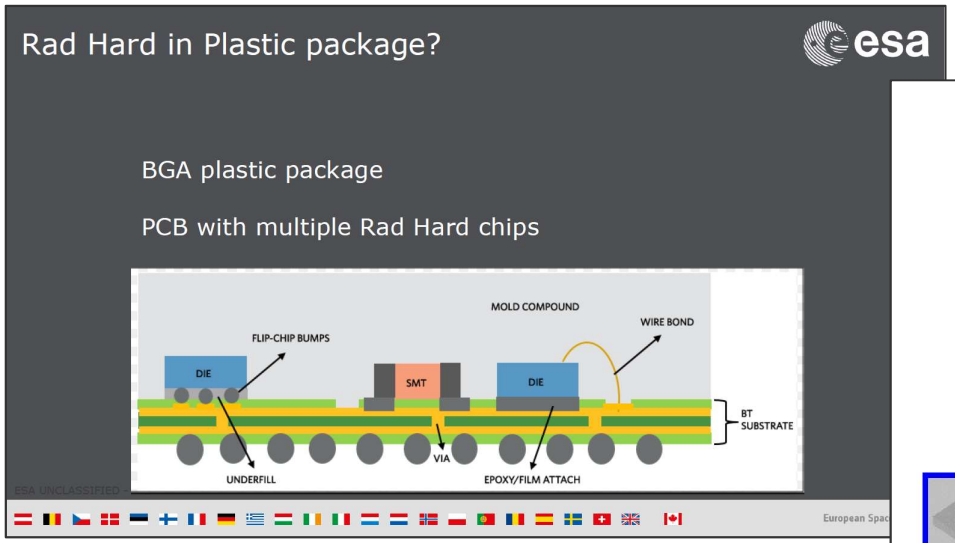
- All services in a single solution
- Gbps of data transfer rate
  - With ECC and Quality-of-Service
- Increased performance with Multicore systems
- Increased On-Board Processing
- Radiation Tolerance
- Lowest Power consumption
- High degree of coverage & Mission Re-Configurability during lifetime
- DSP techniques must be integrated
  - Filtering, multiplexing, demodulation, signal information extraction, performance optimization etc
- FPGA performing supervisory function of SSMM
- Rad-Hard in Plastic Package

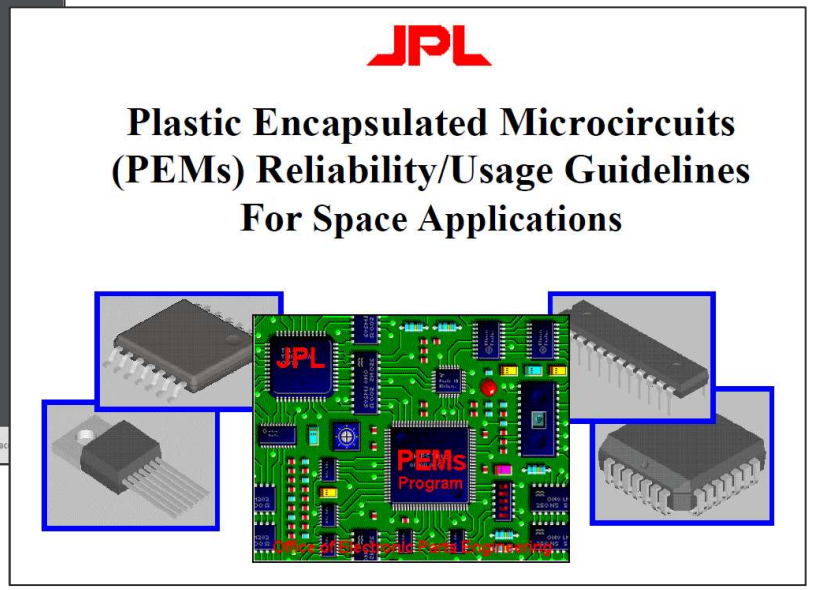
NG ultra

- System-On-Chip FPGA
- HSSL-12G: SpFi, ESIstream, SRIO,
- Quad-cores ARM Cortex-R52
- x1000 DSP blocks
- RHBD approach
- LP process technologies
- Partial Reconfiguration feature (Thanks to Sram architecture)
- DSP supported by NXcore & NXscope
- DDR2/3/4 interfaces
- RHBD PEM devices

RH PEM devices demand

Space requirements extracted from last ESA HEDPT workshop

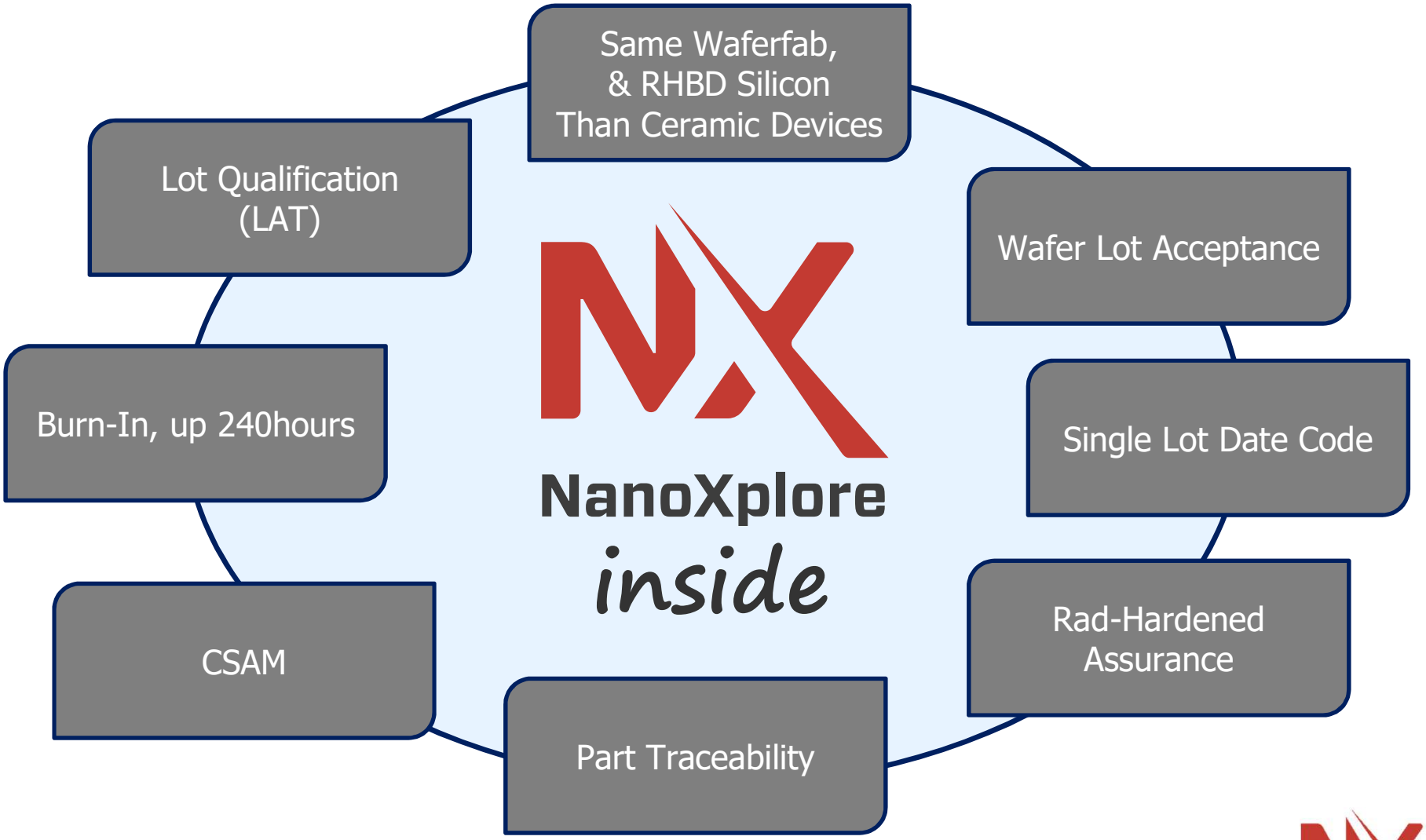




- For Users looking for
  - SWAP-C solutions,
  - Lower-cost, less heavy Packages,
  - Highest HSSL performances, etc.

NX proposes Space RHBD PEM FPGAs with QA level up ECSS Class-1 flow.

Space RH Plastic flow



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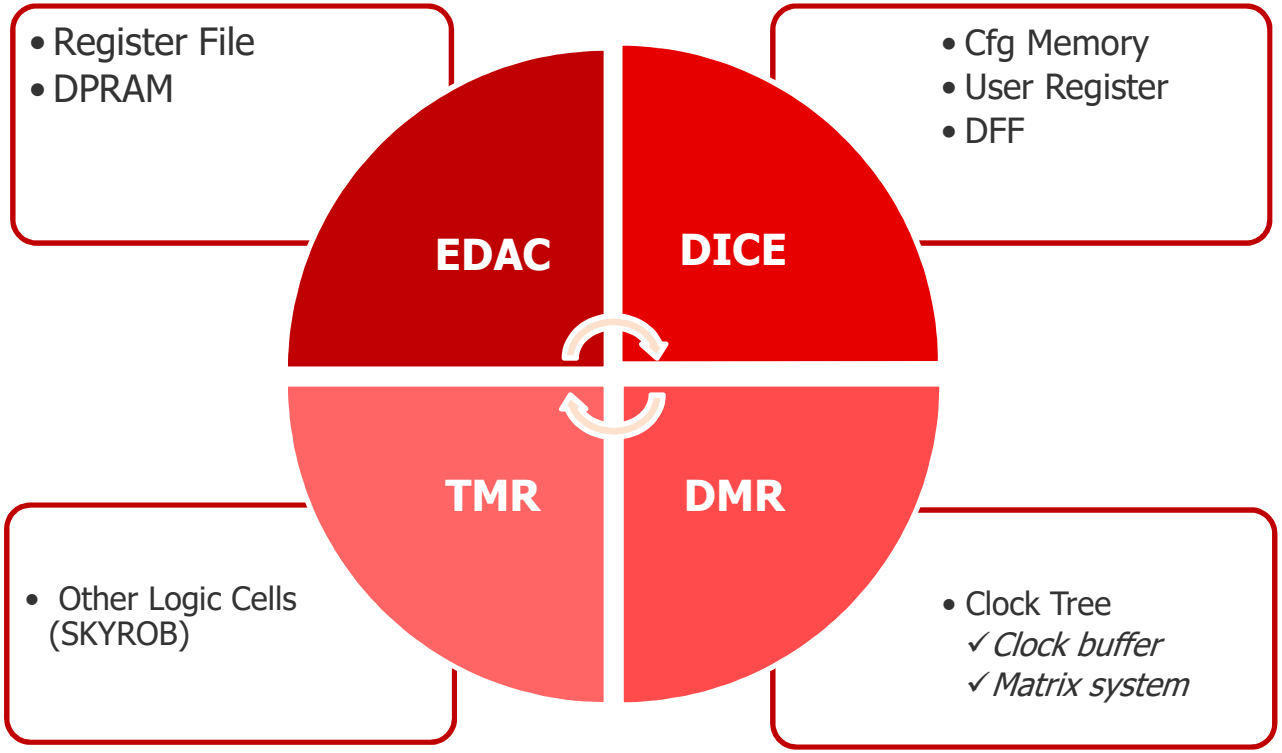
FPGAs are Rad Hardened

All logic of NX FPGAs is hardened by design (RHBD)
and simulated with TFIT software



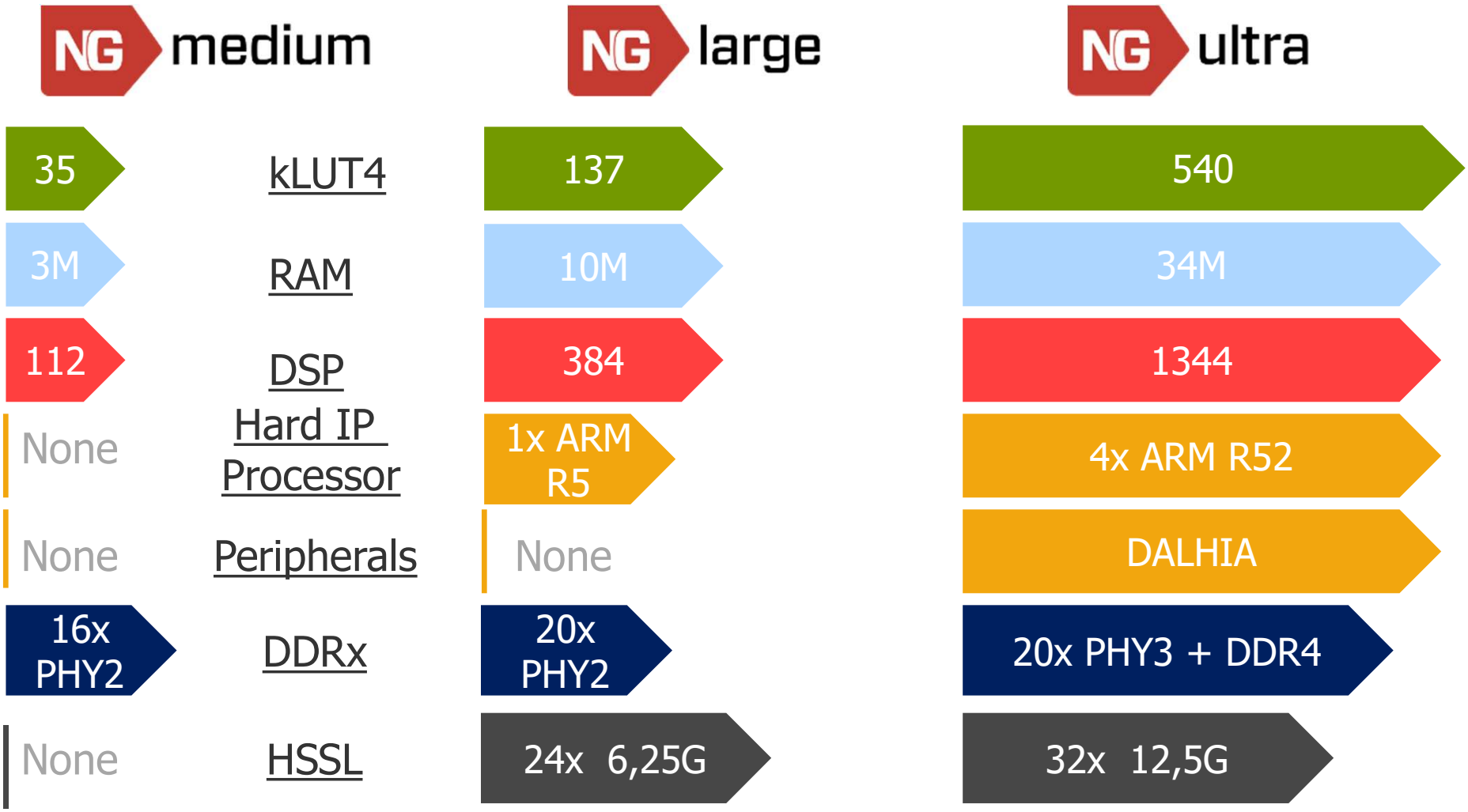
On top of it,
Embedded Configuration Memory Integrity Check ("CMIC")

Export Regulation

- NX RH FPGA devices are **ITAR & EAR-free** ➔ No Dependance to USA.
- Classified 3A001.a.2.c according (EC)2015/2420 rules.

US Dep't. of Commerce	US Department of State	US Department of Treasury
Bureau of Industry & Security	Directorate of Defense Trade Controls	Office of Foreign Assets Controls
•Export Administration Regulations •"Dual Use" products/ technologies •Items subject to EAR •Commerce Control List	•International Traffic in Arms Regulations •Inherently military products/ technologies •U.S. Munitions List	Administration of US economic sanctions & embargoes

RHBD FPGAs features



Embedded Processing solutions

NG medium

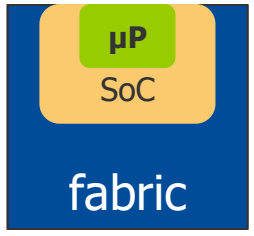
- 34K LUTs / 3Mb RAM
- A SoC can be mapped in the fabric.
- Leon3 based SoC has already been validated. (Max Freq.: ~40 Mhz)

NG large

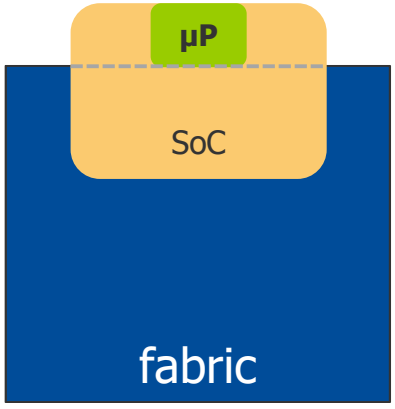
- 137K LUTs / 10Mb RAM
- ARM Cortex R5 Hard IP
- HSSL
- µP : 200 MHz

NG ultra

- 517K LUTs / 36Mb RAM
- µP : 600 MHz



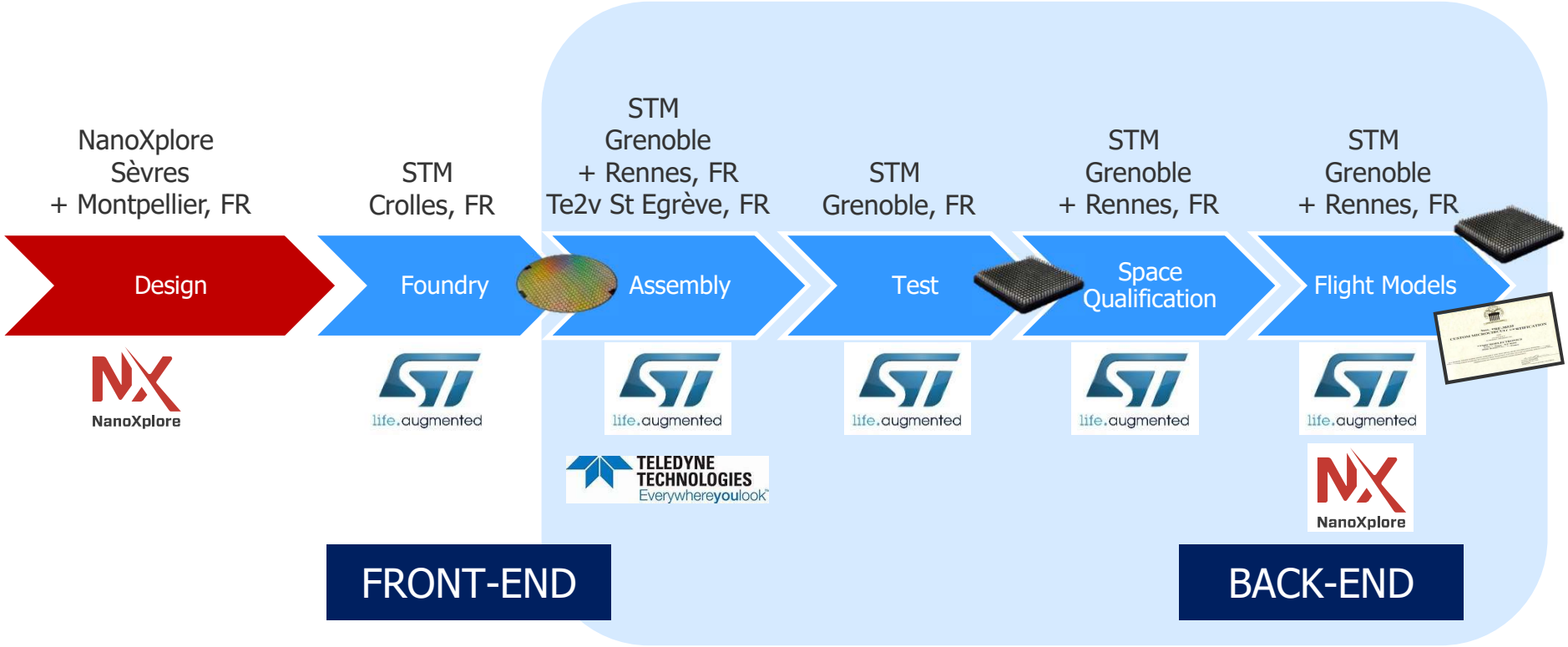
Low-End FPGA



Mid-End FPGA

High-End FPGA

– Space Supply-Chain



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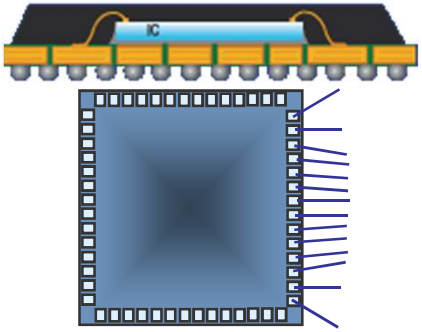
Packaging Technologies: WB vs Flip-Chip

NG medium

Wirebond



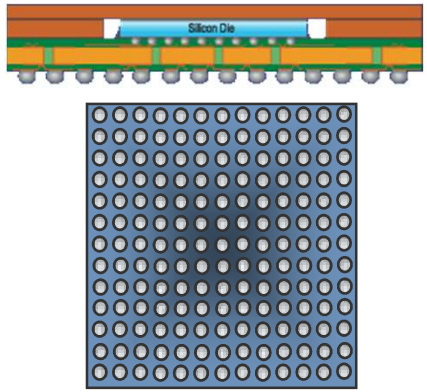
Typical Die with
Peripheral Bond Pads

Drivers

- Flip Chip offers Higher performance for high speed device
  - flip chip interconnect has lower inductance
  - direct power/ground access to core
- Flip Chip delivers better thermal performance
- Flip Chip addresses I/O Limitations of Wire Bond Interconnect

NG large
NG ultra

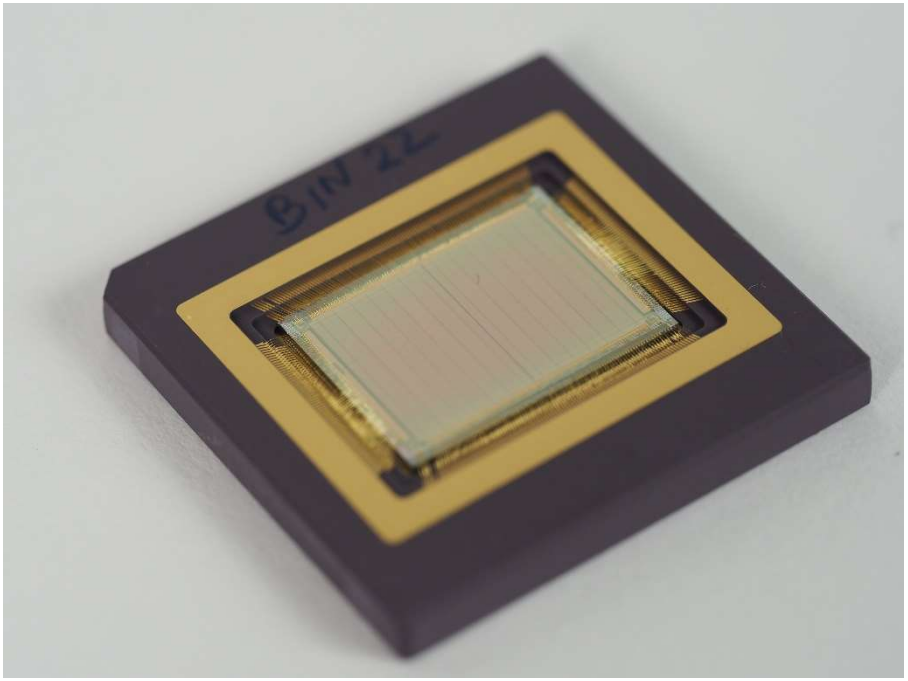
Flip Chip



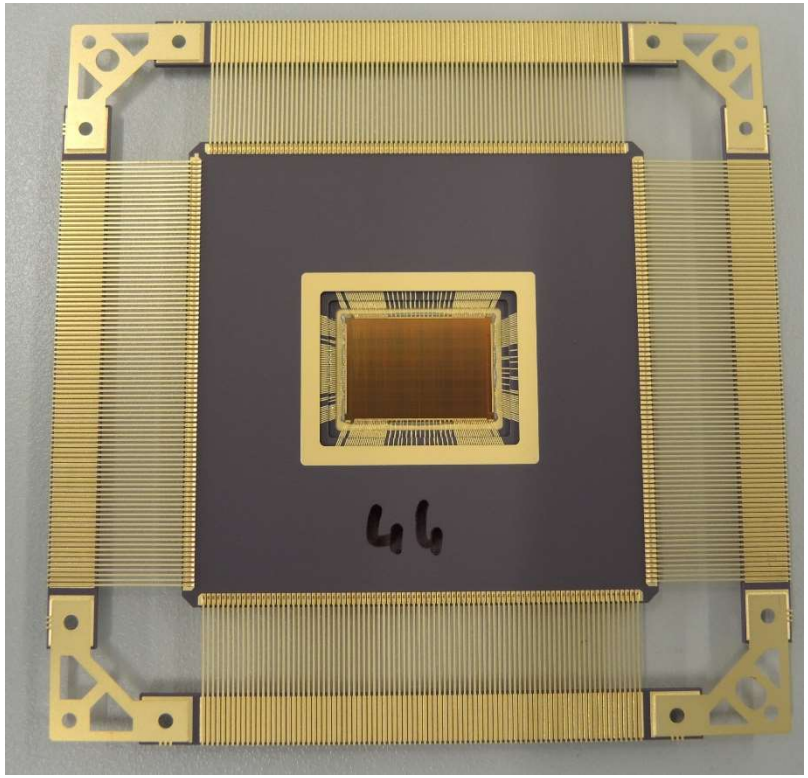
Flip Chip Die
Array Pads (Solder bumped)

NG medium Ceramic Packages (CQFP & LGA)

LGA625
29*29mm body, 1,00mm pitch

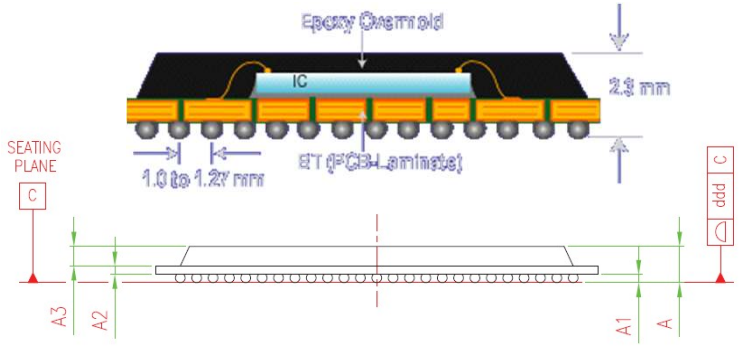


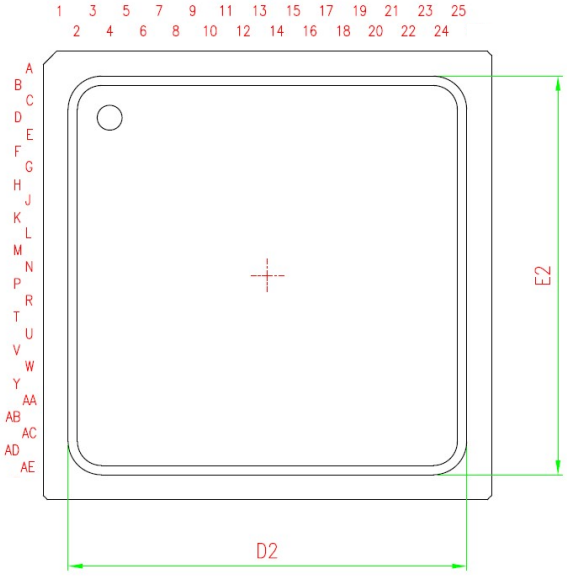
CQFP352
48*48mm body, 0,50mm pitch

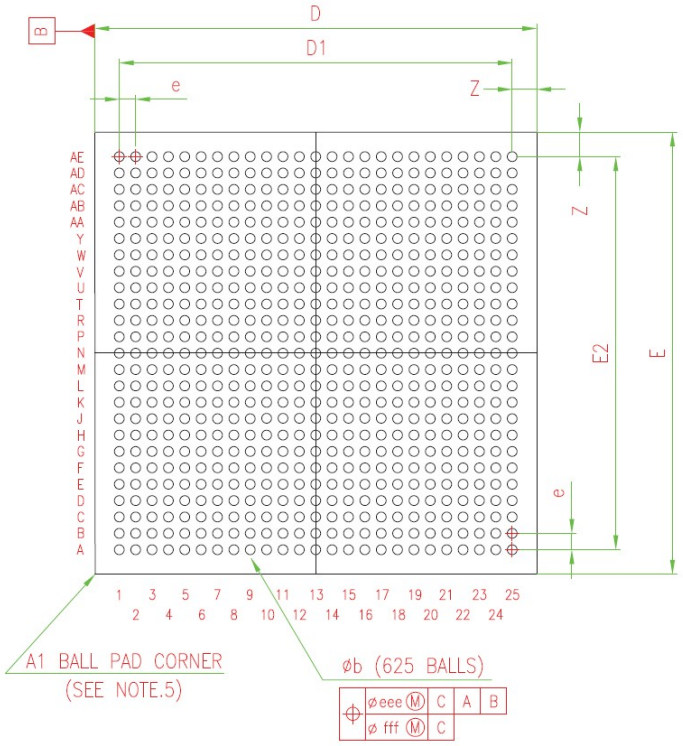


NG medium Organic Package (WB-PBGA)

PBGA625
27*27mm body,
1,00mm pitch
Lead-free Solder balls
SACN305 Diam 0,5mm







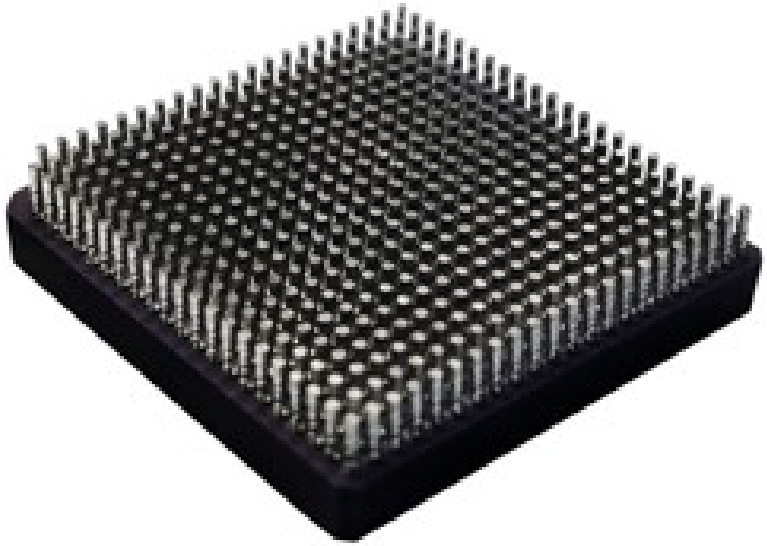
PACKAGE DIMENSIONS			
DATABOOK TABLE 1 PACKAGE DIMENSION (mm)			
SYMBOL	MIN.	NOM.	MAX.
A			2.39
A1	0.30		
A2		0.53	
A4		1.20	
b	0.50	0.60	0.70
D	26.80	27.00	27.20
D1		24.00	
D2		24.00	
E	26.80	27.00	27.20
E1		24.00	
E2		24.00	
e		1.00	
Z		1.50	

SYMBOL	TOLERANCE OF FORM AND POSITION
	DATABOOK (mm)
ddd	0.20
eee	0.25
fff	0.10

NG large & NG ultra Packages (LGA & FC-PBGA)

LG/CG1752

45*45mm body, 1,00mm pitch
Full populated
No Decoupling Capacitors



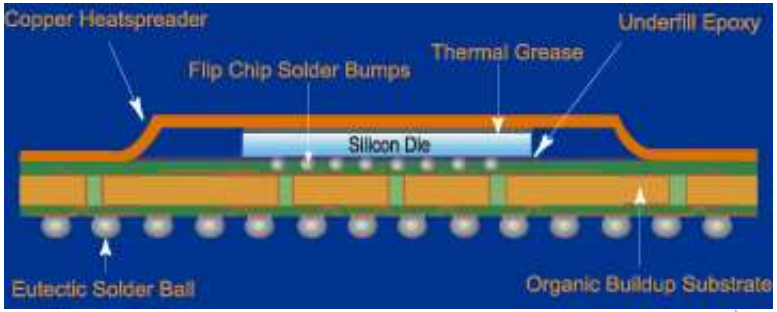
CGA package picture
Extracted from Internet

FF1752

42,5*42,5mm body, 1,00mm pitch

Key Attributes

- BT - Laminate Substrate
- Heat Spreader – Lowest Thermal Resistance (θja<12°C/W), (θjc <1°C/W)
- Superior Electrical Performance – with **HSSL capabilities**



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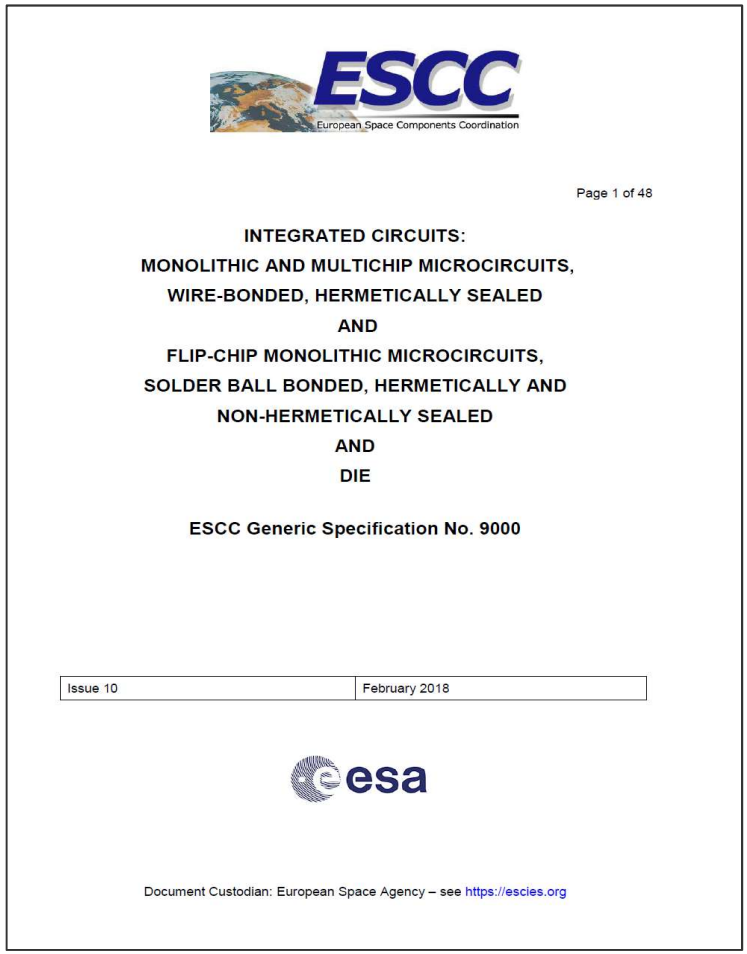
Space Quality Standards



ESCC
European Space Components Coordination

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INTEGRATED CIRCUITS:
MONOLITHIC AND MULTICHIP MICROCIRCUITS,
WIRE-BONDED, HERMETICALLY SEALED
AND
FLIP-CHIP MONOLITHIC MICROCIRCUITS,
SOLDER BALL BONDED, HERMETICALLY AND
NON-HERMETICALLY SEALED
AND
DIE

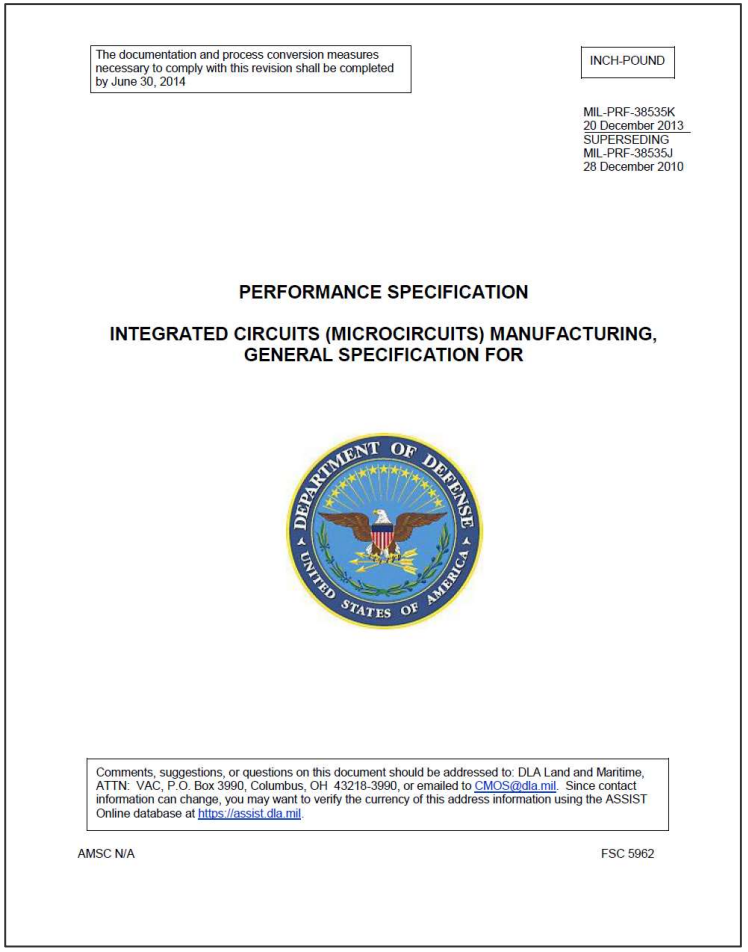
ESCC Generic Specification No. 9000

Issue 10	February 2018

esa

Document Custodian: European Space Agency – see https://escies.org

VS



The documentation and process conversion measures necessary to comply with this revision shall be completed by June 30, 2014

INCH-POUND

MIL-PRF-38535K
20 December 2013
SUPERSEDING
MIL-PRF-38535J
28 December 2010

PERFORMANCE SPECIFICATION

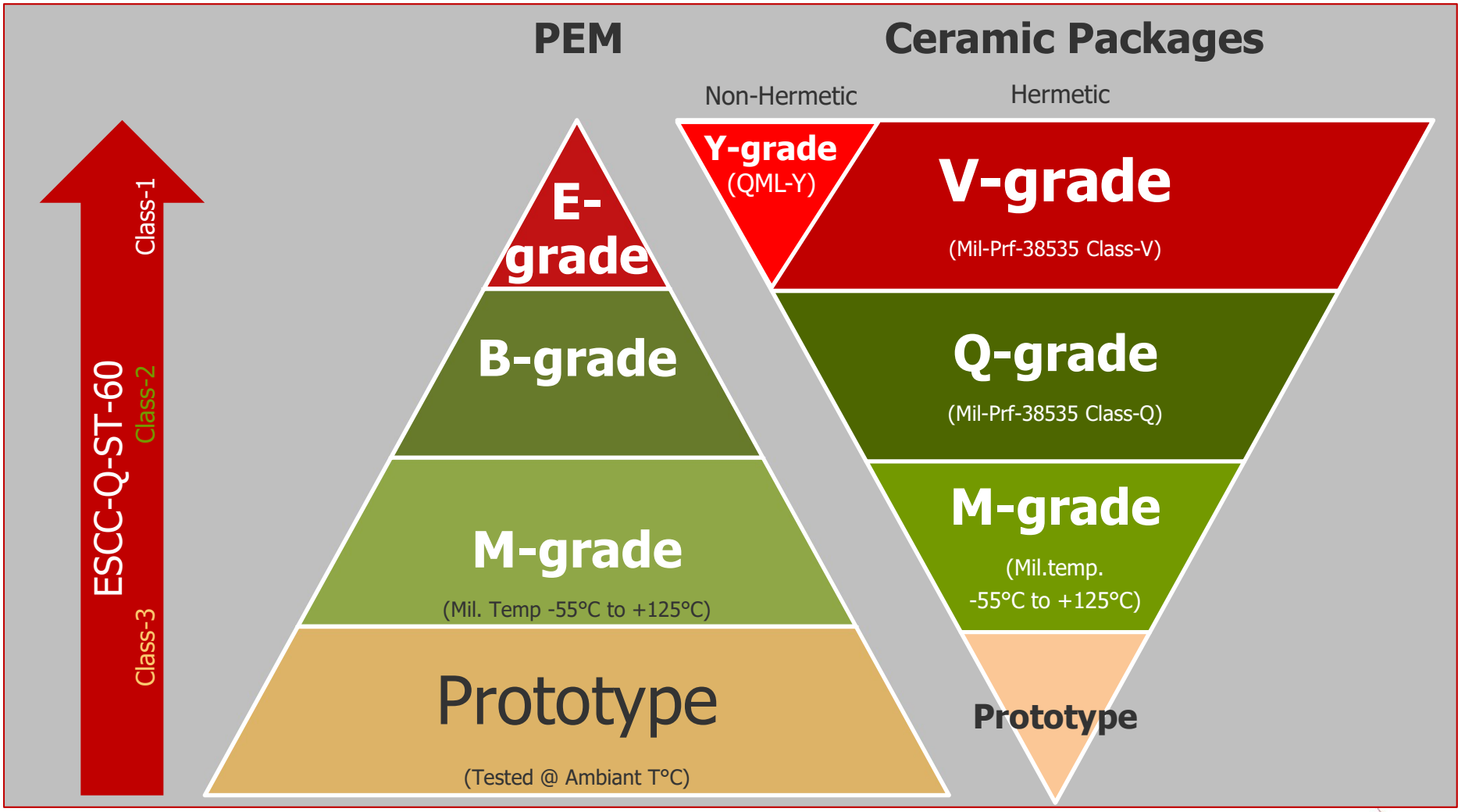
INTEGRATED CIRCUITS (MICROCIRCUITS) MANUFACTURING, GENERAL SPECIFICATION FOR

Comments, suggestions, or questions on this document should be addressed to: DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to CMOS@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A

FSC 5962

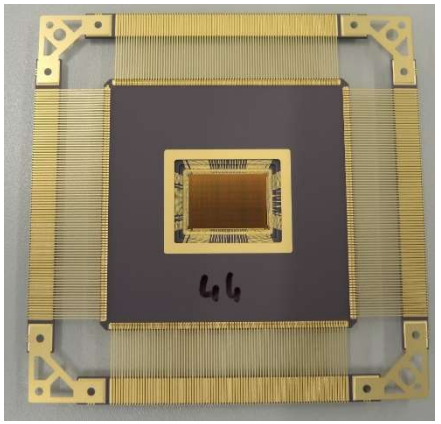
Quality Levels



Ceramic Devices QA level

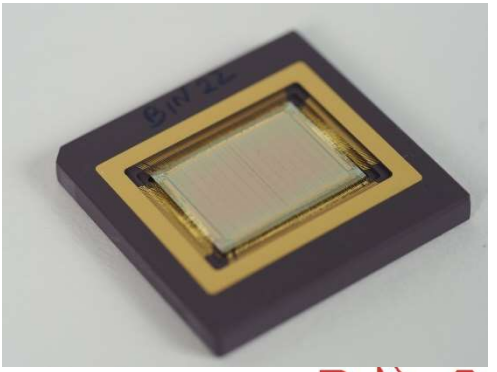
Grade	PR	M	Q	V
WLAT	✗	✗	✓	✓
TID / Report	✗	✗	✓ Yes	✓ Yes
SLDC	✗	✗	✓	✓
T/C	✗	✗	✓ 10cy	✓ 10cy
Internal Visual	STM policy	2010B Sampling	2010B 100%	**2010A 100%**
Pind-Test	✗	✗	On Request	✓ Yes
Serialization	✗	✗	✗	✓
Burn-In	✗	✗	✓ 160h 125°C	✓ 240h 125°C
PDA	✗	✗	5%	5%
Electrical Test	25°C	-55°C & +125°C	25°C then -55°C & +125°C	25°C then -55°C & +125°C R&R
QCI	✗	✗	✓ Yes	✓ Yes
External Visual	✗	Sampling	✓ 100%	✓ 100%
CoC	✗	✗	✓ Yes	✓ Yes

CQ352



LG/CG625

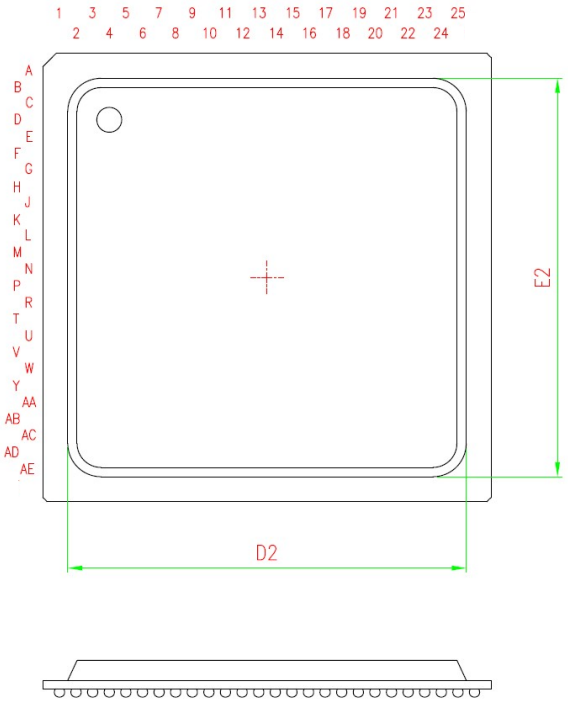
29*29mm body,
1,00mm pitch



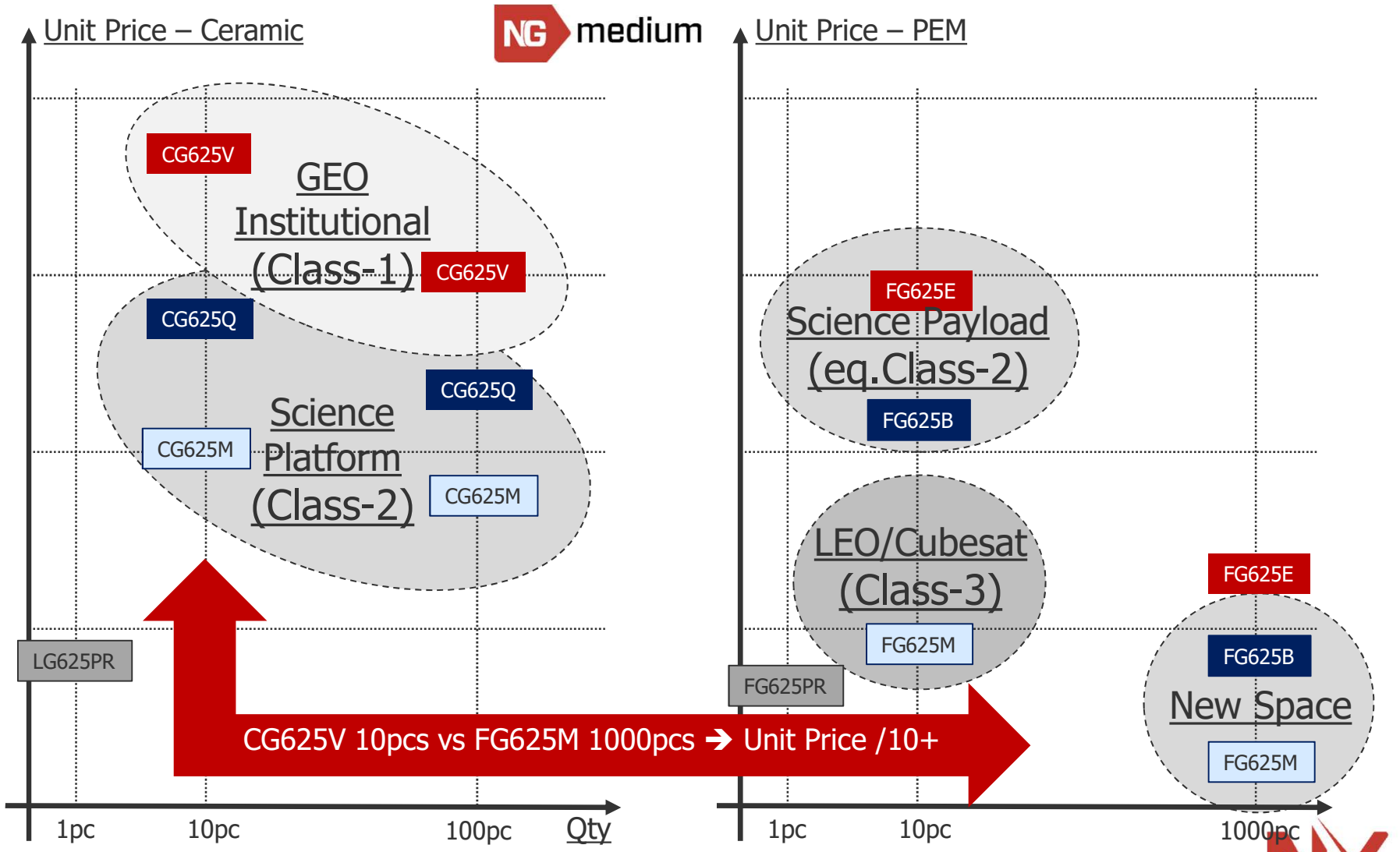
PEM QA level

Grade	PR	M	B	E
WLAT	✗	✗	✓	✓
TID / Report	✗	✗	✓ Yes	✓ Yes
SLDC	✗	✗	✓	✓
T/C	✗	✗	✓ 10cy	✓ 10cy
Internal Visual	STM policy	2010B Sampling	2010B 100%	2010A 100%
CSAM	✗	✗	✓	✓
Serialization	✗	✗	✗	✓
Burn-In	✗	✗	✓ 160h 125°C	✓ 240h 125°C
PDA	✗	✗	1%	1%
Electrical Test	25°C	-55°C & +125°C	+25°C then -55°C & +125°C	25°C then -55°C & +125°C R&R
LAT 1/2/3	✗	✗	✓	✓
External Visual	✗	Sampling	100%	100%
CoC	✗	✗	✓	✓
			ECSS Class-3	ECSS Class-2	ECSS Class-1

PBGA625
27*27mm body,
1,00mm pitch



Pricing vs Pkg & Qty



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Thanks for your attention


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