Agenda

1- NX introduction
2- Space Market
3- RHBD FPGA solutions
4 Packaging Technologies
5- NX Quality Flows
6- CONCLUSION
NanoXplore Overview

- **Created in 2010** by three veterans of semiconductor industry with long experience in the design, test and debugging of FPGA cores.

- **Fabless** semiconductor company headquarter in France

- R&D engineers in two offices in France:
  - Sèvres: Hardware developments
  - Montpellier: Software developments

- **NanoXplore is a leader in the design of large scale programmable logic arrays for state of the art FPGA cores**

- The company is focusing on 2 main activities:
  - Offer hard block embedded FPGA core IP (NX-eFPGA)
  - Developing rad-hard FPGA qualified for space applications (from BRAVE contract)
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Space Trends

- SWaP-C *(Stands for Size, Weight and Power + Cost)*
  - Space EP or COTS+ components
- Radiation-Tolerance/Hard solution
- ITAR-free components
Space Trends – What about FPGAs

Space requirements extracted from last ESA HEDPT workshop, dated 01/10/2018

- All services in a single solution
- Gbps of data transfer rate
  - With ECC and Quality-of-Service
- Increased performance with Multicore systems
- Increased On-Board Processing
- Radiation Tolerance
- Lowest Power consumption
- High degree of coverage & Mission Re-Configurability during lifetime
- DSP techniques must be integrated
  - Filtering, multiplexing, demodulation, signal information extraction, performance optimization etc
- FPGA performing supervisory function of SSMM
- Rad-Hard in Plastic Package

- System-On-Chip FPGA
- HSSL-12G: SpFi, ESIstream, SRIO,
- Quad-cores ARM Cortex-R52
- x1000 DSP blocks
- RHBD approach
- LP process technologies
- Partial Reconfiguration feature (Thanks to Sram architecture)
- DSP supported by NXcore & NXscope
- DDR2/3/4 interfaces
- RHBD PEM devices

Space requirements extracted from last ESA HEDPT workshop, dated 01/10/2018
RH PEM devices demand

Space requirements extracted from last ESA HEDPT workshop

- For Users looking for
  - SWAP-C solutions,
  - Lower-cost, less heavy Packages,
  - Highest HSSL performances, etc.

NX proposes Space RHBD PEM FPGAs with QA level up ECSS Class-1 flow.
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FPGAs are Rad Hardened

All logic of NX FPGAs is hardened by design (RHBD) and simulated with TFIT software

On top of it, Embedded Configuration Memory Integrity Check ("CMIC")
Export Regulation

- NX RH FPGA devices are **ITAR & EAR-free** ➞ No Dependance to USA.
- Classified 3A001.a.2.c according (EC)2015/2420 rules.

<table>
<thead>
<tr>
<th>US Dep’t. of Commerce</th>
<th>US Department of State</th>
<th>US Department of Treasury</th>
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<td>Office of Foreign Assets Controls</td>
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<td>- International Traffic in Arms Regulations</td>
<td>Administration of US economic sanctions &amp; embargoes</td>
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<td>- Inherently military products/technologies</td>
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<td>- U.S. Munitions List</td>
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<td>- Commerce Control List</td>
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## RHBD FPGAs features

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<th>medium</th>
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<th>ultra</th>
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<td>20x PHY3 + DDR4</td>
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<tr>
<td>2x</td>
<td>HSSL</td>
<td>24x 6,25G</td>
<td>32x 12,5G</td>
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Embedded Processing solutions

**medium**
- 34K LUTs / 3Mb RAM
- A SoC can be mapped in the fabric.
- Leon3 based SoC has already been validated. (Max Freq.: ~40 MHz)

**large**
- 137K LUTs / 10Mb RAM
- ARM Cortex R5 Hard IP
- HSSL
- μP : 200 MHz

**ultra**
- 517K LUTs / 36Mb RAM
- μP : 600 MHz

---

Low-End FPGA

Mid-End FPGA

High-End FPGA

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Packaging Technologies: WB vs Flip-Chip

**Wirebond**

Drivers

- Flip Chip offers Higher performance for high speed device
  - flip chip interconnect has lower inductance
  - direct power/ground access to core
- Flip Chip delivers better thermal performance
- Flip Chip addresses I/O Limitations of Wire Bond Interconnect

**Flip Chip**

Typical Die with Peripheral Bond Pads

Flip Chip Die Array Pads (Solder bumped)
LGA625
29*29mm body, 1,00mm pitch

CQFP352
48*48mm body, 0,50mm pitch
Organic Package (WB-PBGA)

PBGA625
27*27mm body, 1,00mm pitch
Lead-free Solder balls
SACN305 Diam 0,5mm

PACKAGE DIMENSIONS

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TOLERANCE OF FORM AND POSITION

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**Large & Ultra Packages (LGA & FC-PBGA)**

- **LG/CG1752**
  - 45*45mm body, 1,00mm pitch
  - Full populated
  - No Decoupling Capacitors

- **FF1752**
  - 42,5*42,5mm body, 1,00mm pitch

**Key Attributes**

- BT - Laminate Substrate
- Heat Spreader – Lowest Thermal Resistance ($\theta_{ja} < 12^\circ C/W$), ($\theta_{jc} < 1^\circ C/W$)
- Superior Electrical Performance – with HSSL capabilities
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Space Quality Standards

INTEGRATED CIRCUITS:
MONOLITHIC AND MULTICHIP MICROCIRCUITS,
WIRE-BONDED, HERMERICALLY SEALED
AND
FLIP-CHIP MONOLITHIC MICROCIRCUITS,
SOLDER BALL BONDED, HERMERICALLY AND
NON-HERMERICALLY SEALED
AND
DIE

ESCC Generic Specification No. 9000

The documentation and process control measures
necessary to comply with this revision shall be completed
by June 30, 2014

The Department of Defense
A United States of America

Comments, suggestions, or questions on this document should be addressed to: DLA Land and Maritime,
ATTN: VAC, P.O. Box 2060, Columbus, OH 43216-2060, or emailed to VAC-IGD@dlainc.com. Since contact
information can change, you may want to verify the currency of this address information using the ASD/SBIST
Online database at https://dsdd.tdp.dla.mil

AMSEC N/A
FSC 5905
Quality Levels

ESCCON-Q-ST-60

Class-1

E-grade

(Mil. Temp -55°C to +125°C)

Prototype

(Tested @ Ambient T°C)

ESCCON-Q-ST-60

Class-2

B-grade

M-grade

(QML-Y)

Y-grade

(Mil-Prf-38535 Class-V)

V-grade

(Mil-Prf-38535 Class-Q)

Q-grade

(Mil.temp. -55°C to +125°C)

M-grade

Non-Hermetic

Hermetic

Ceramic Packages

Prototype

PEM
## Ceramic Devices QA level

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<td>✔</td>
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**CQ352**

*29*29mm body, 1,00mm pitch*
# PEM QA level

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<tr>
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<td>2010B 100%</td>
<td>2010A 100%</td>
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**PBGA625**
27*27mm body, 1,00mm pitch
Pricing vs Pkg & Qty

Unit Price – Ceramic

- CG625V
- CG625Q
- CG625M

Unit Price – PEM

- FG625E
- FG625B
- FG625M

New Space

- LEO/Cubesat (Class-3)
- Science Payload (eq. Class-2)
- Institutional (Class-1)

CG625V 10pcs vs FG625M 1000pcs ➔ Unit Price /10+
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CONCLUSION

Joël LE MAUFF - Tel +33 (0)6 83820053 - joel.lemauff@nanoxplore.com
Thanks for your attention