What is changing in radiation hardness assurance ?

THE CHALLENGE OF TECHNOLOGY EVOLUTION

R. Ecoffet, CNES

cnes
CENTRE NATIONAL
D'ÉTUDES SPATIALES

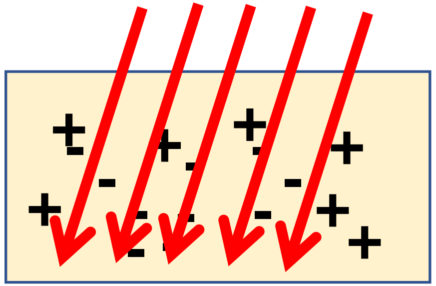
Introduction and some in-flight feedbacks

Radiation effects on electronics

Destructive

Cumulative

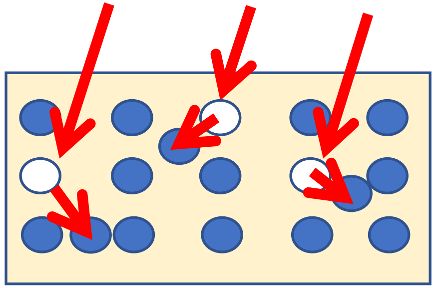
All technologies



Electron-hole pairs

Ionizing dose

Optoelectronics
Bipolar



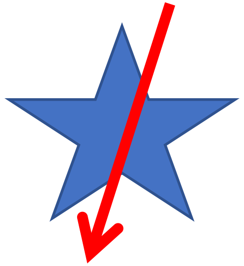
Vacancies - interstitials

Displacement damage

Parametric drift
Functional failure (lifetime)

Single event

CMOS bulk,
power MOSFETs,
Power diodes



Short-circuit or dielectric breakdown
SEL, SEB, SEGR

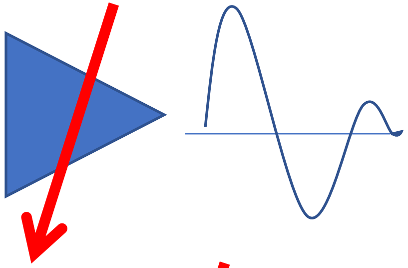
Possible immediate destruction

Radiation effects on electronics

Non destructive

Single event effects

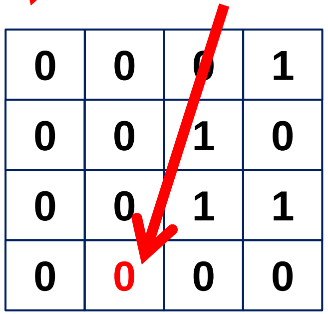
Analog



False signal SET

- Disjunction
- Redundancy swapping
- De-synchronization
- Gain change,…

Digital

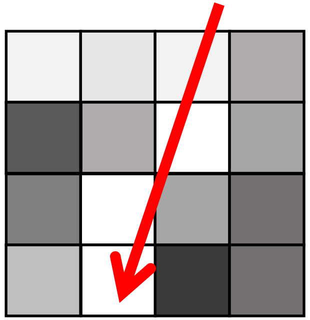


0	0	0	1
0	0	1	0
0	0	1	1
0	0	0	0

False information SEU, MBU

- False data
- Program errors
- Processor crash,…

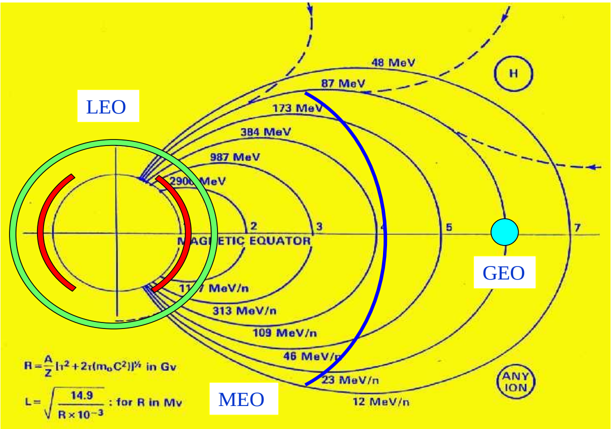
Detectors Imaging

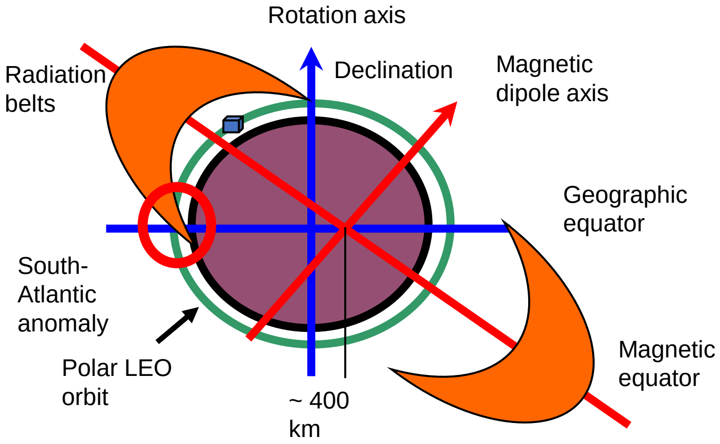


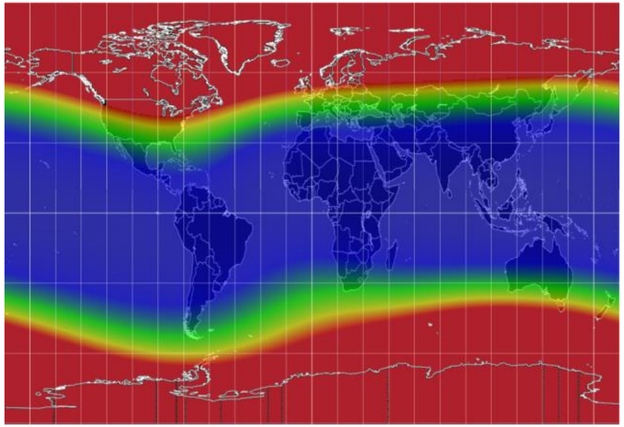
False pixel

- False stars
- Degraded images
- Saturated pixels
- Oscillating pixels,…

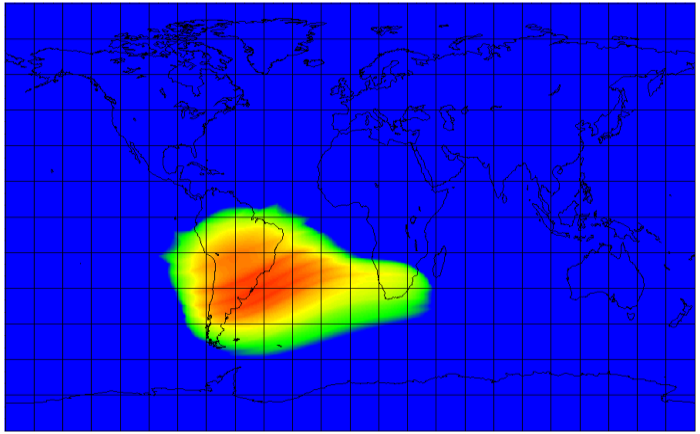
Hazard zones in low Earth orbit





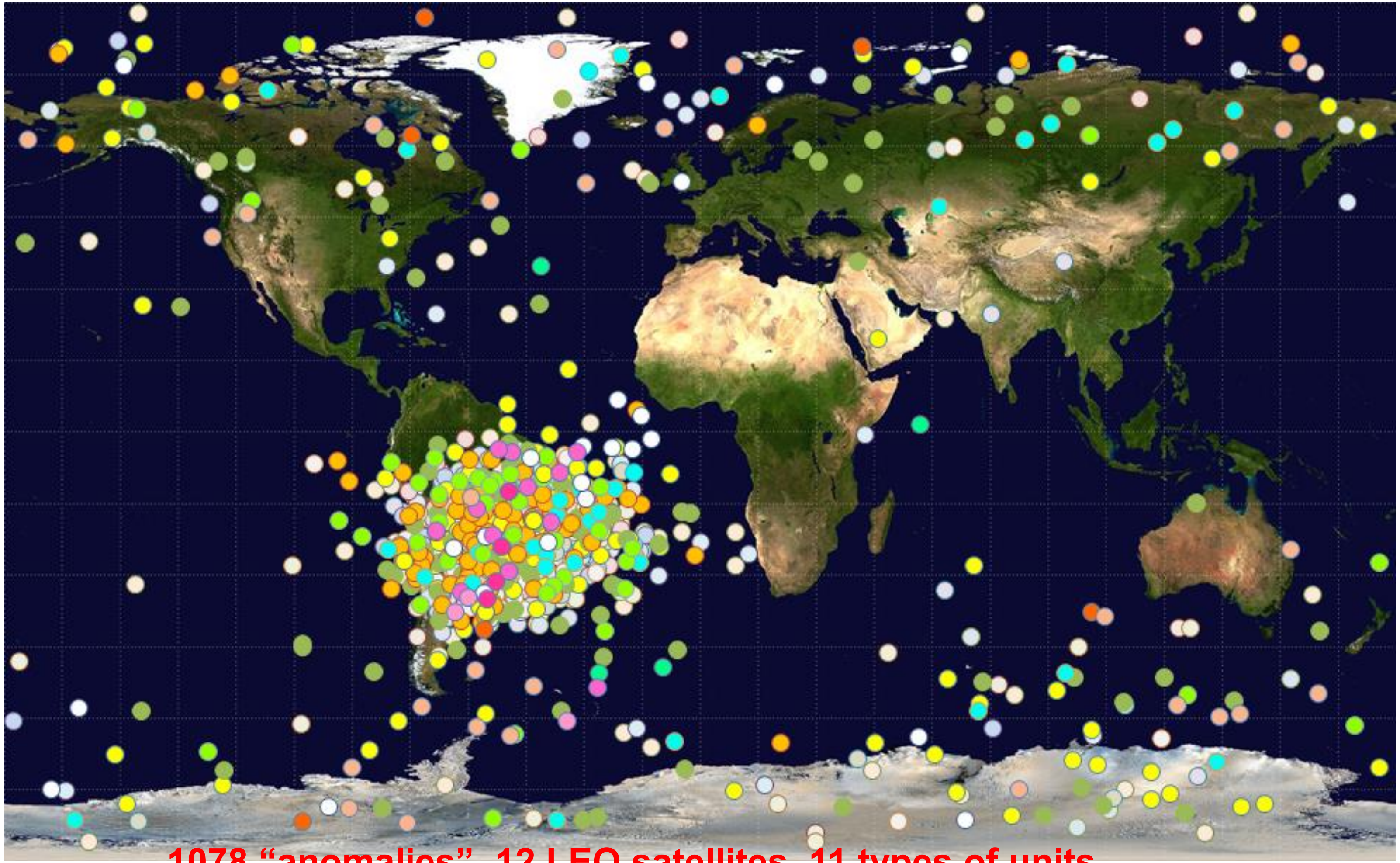


Increased risk from solar events and cosmic rays



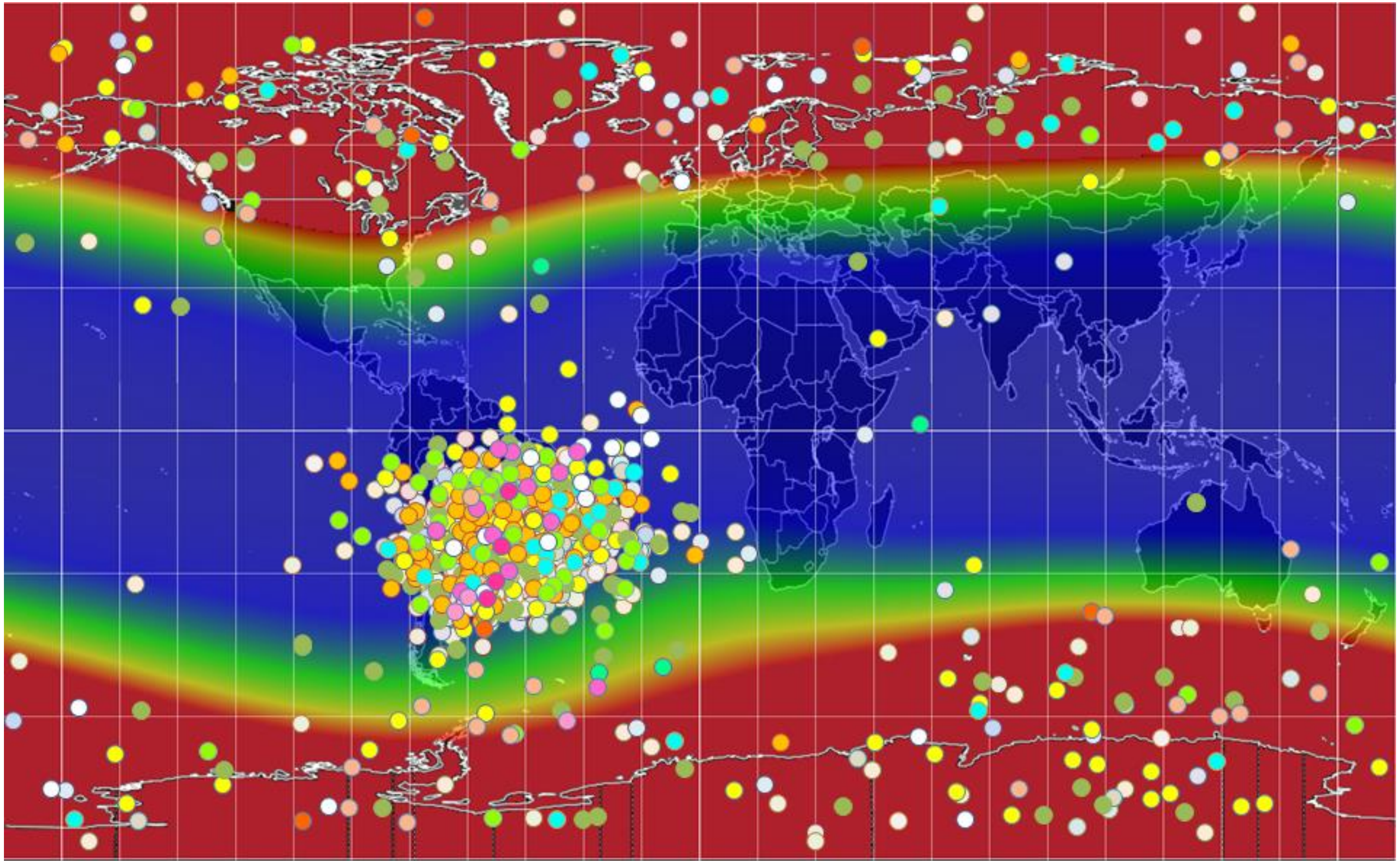
Increased risk from trapped protons

Low Earth Orbit in-flight feedback

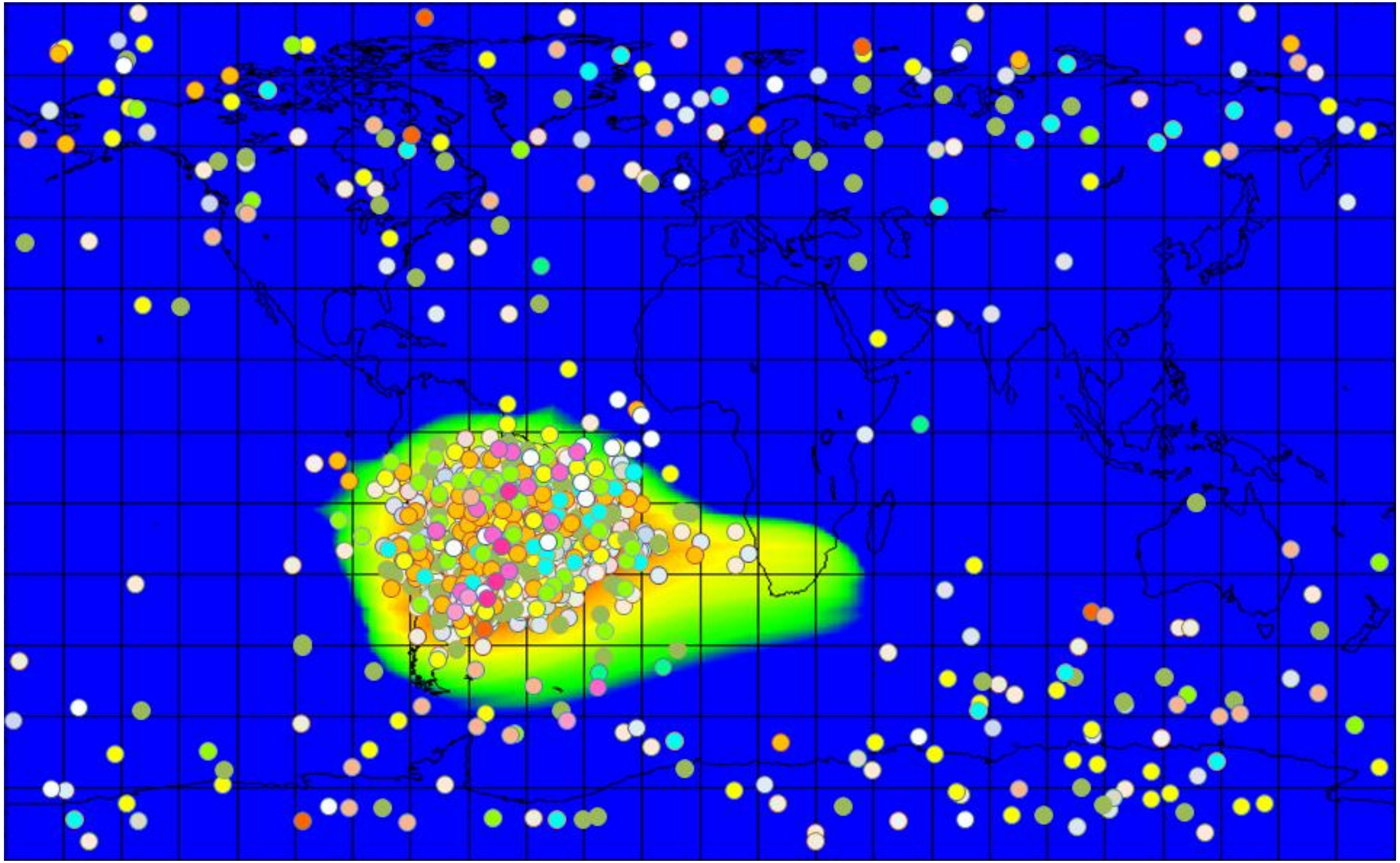


1078 “anomalies”, 12 LEO satellites, 11 types of units

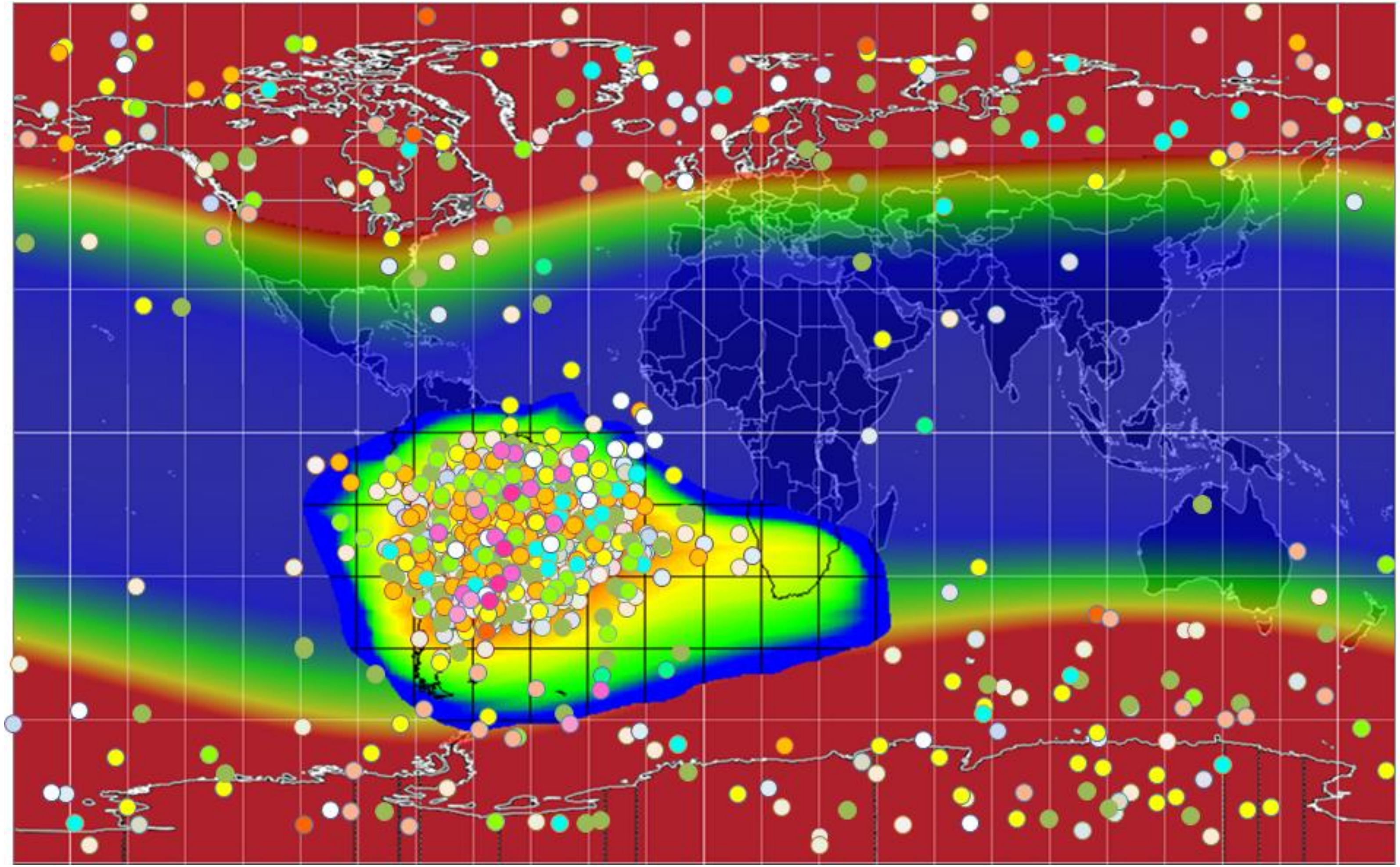
Low Earth Orbit in-flight feedback



Low Earth Orbit in-flight feedback



Low Earth Orbit in-flight feedback



Lifetime

Satellite	Built for - by	Designed for	Survived	Received vs Specification	End of service
Spot-1	CNES – Matra Espace	5 years	17 years	x3	Not because of radiation
Hipparcos	ESA – Matra Espace	5 years in GEO	5 years in GTO	x7	Because of radiation
Inmarsat-2 F1	Inmarsat – Matra Espace British Aero.	10 years	22 years	x2	Not because of radiation
Jason-1	CNES - TAS	5 years	11 years	x2	Not because of radiation
Integral	ESA – Alenia Spazio	5 years	15 years	x3	Still in operation

x2, x3 mission levels → can survive
x7 mission level → failure
Gives an idea of the real safety margin
- At least for satellites built with 1980-2000 technologies -

Dose calculations - yesterday

GEO

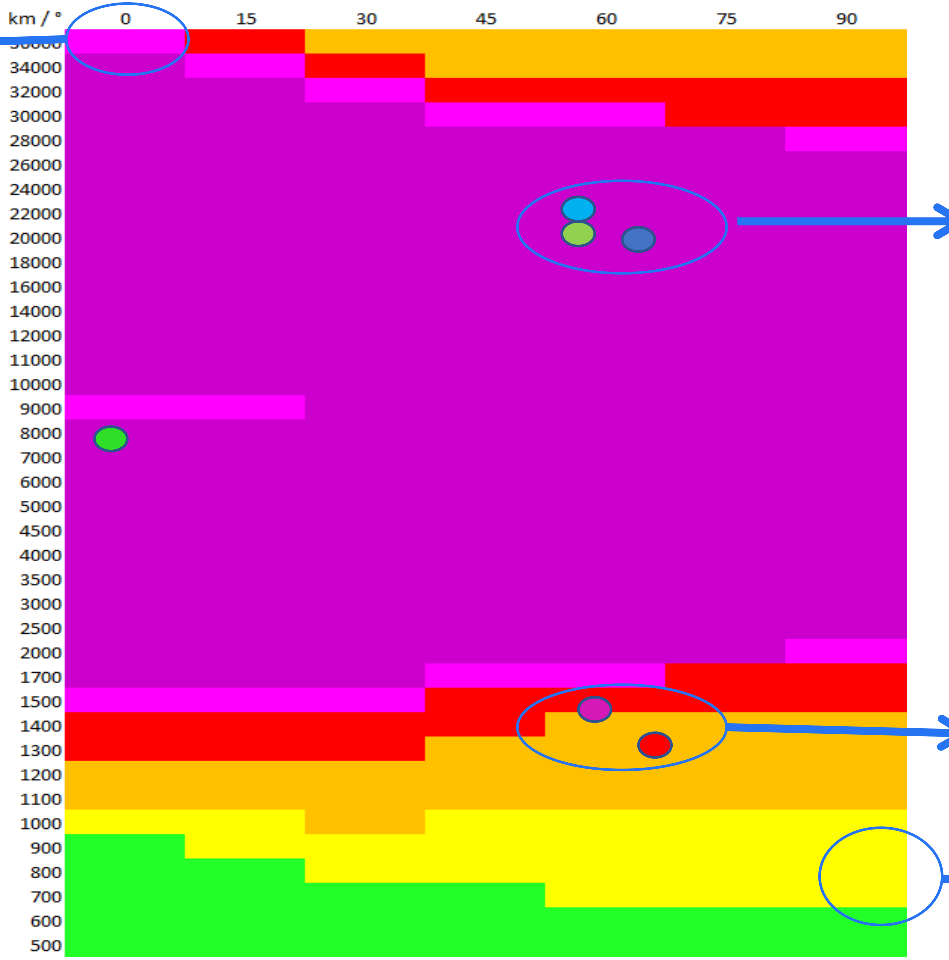
~20 krad / year
15 years : 300 krad

Outer electron belt

🟩	< 1 krad / year
🟨	1-3 krad / year
🟧	3-10 krad / year
🟥	10-20 krad / year
🟪	20-30 krad / year
🟪	> 30 krad / year

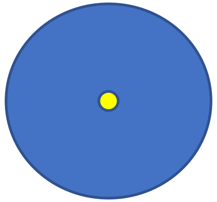
Proton belt and inner electron belt

- ● GALILEO
- ● GPS
- ● GLONASS
- ● O3B
- ● GLOBALSTAR
- ● JASON



AE8 Max / AP8 Min - Circular Orbits

MEO
Navigation



Center of a
1 g/cm² (3.7 mmAl)
solid sphere

LEO
Constellations

LEO Observation
Constellations

Dose calculations - today

GEO

~1 krad / year
15 years : 15 krad

Outer electron belt

- 🟩 < 1 krad / year
- 🟨 1-3 krad / year
- 🟧 3-10 krad / year
- 🟥 10-20 krad / year
- 🟪 20-30 krad / year
- 🟪 > 30 krad / year

Proton belt and inner electron belt

- ● GALILEO
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- ● GLONASS
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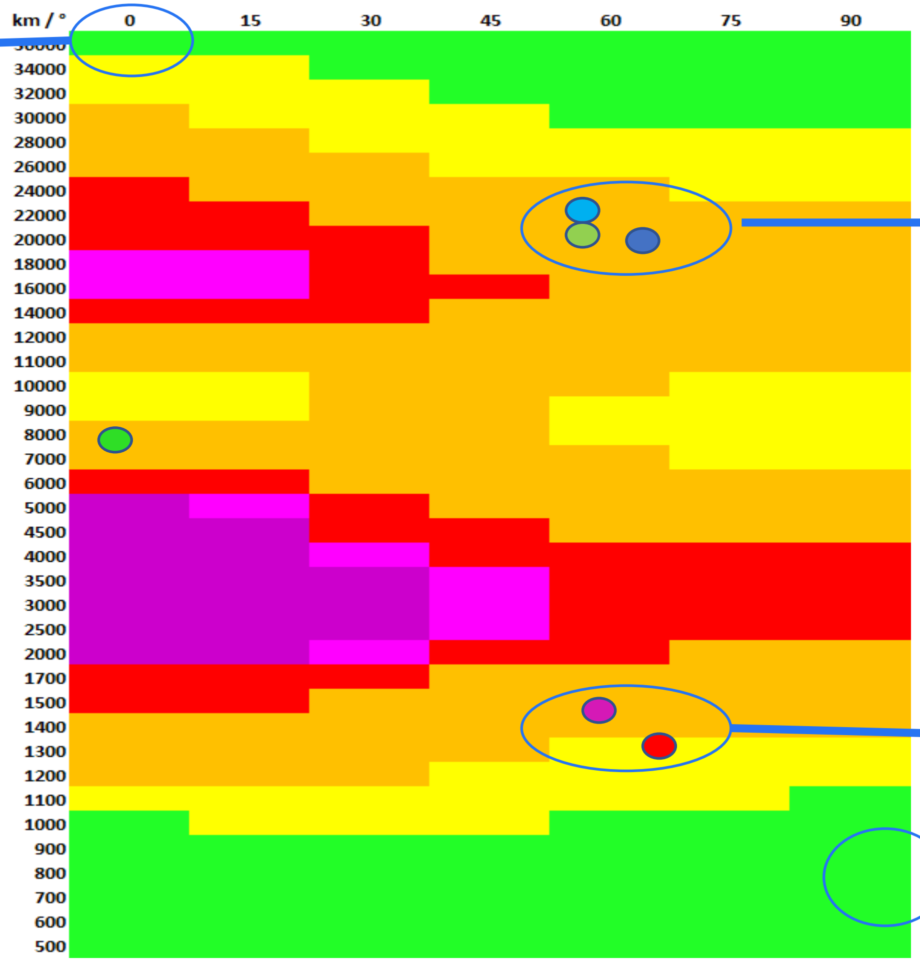


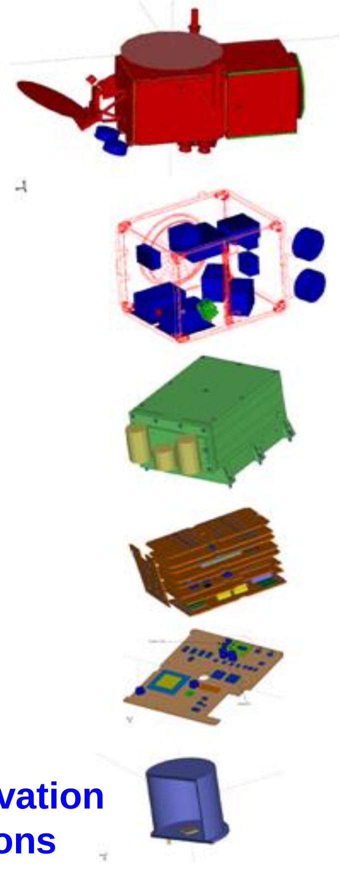
AE8 Max / AP8 Min - Circular Orbits

MEO
Navigation

PMOS dosimeter
CARMEN-2
JASON-2

LEO
Constellations

LEO Observation
Constellations



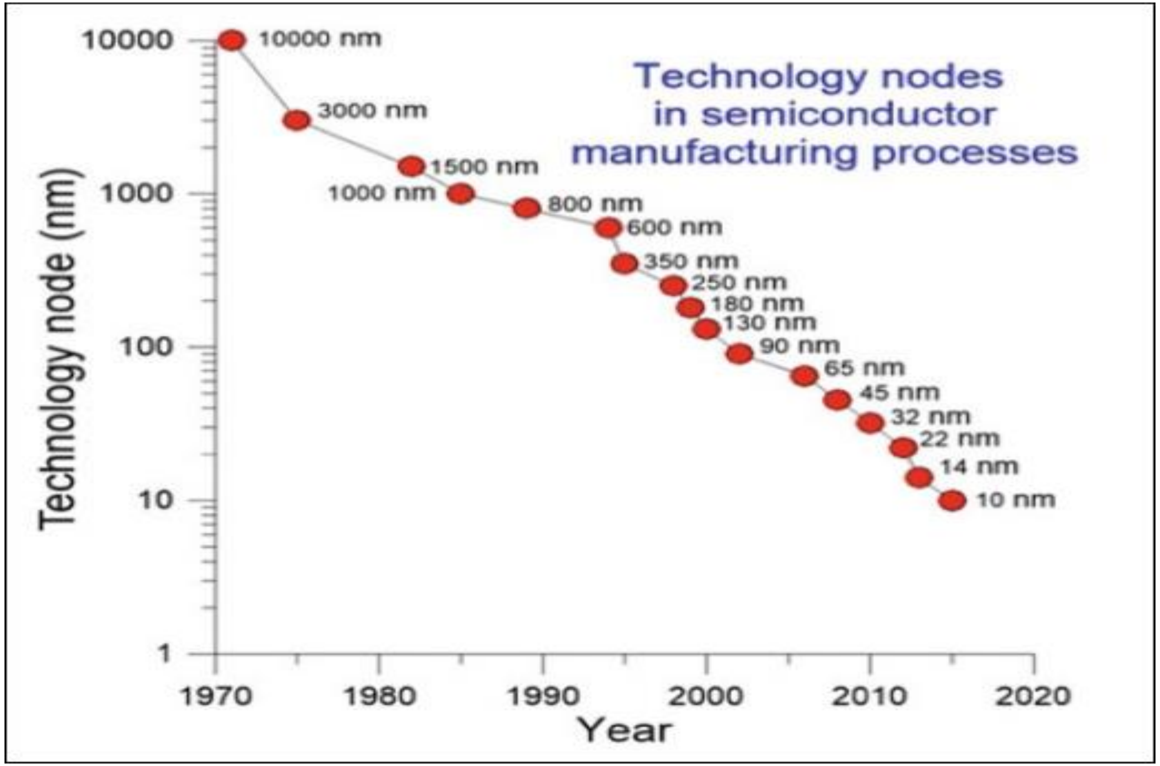
Lessons learned

- **Ionizing dose**
  - Hidden margins : environment models, shielding description, application temperature, annealing
  - In Earth orbit, except in very particular cases, there is always a solution to dose
- **Single event effects**
  - Are an issue – one of the major causes of spacecraft “anomalies”
  - And new technologies may bring additional challenges (next slides)

Electronic technologies today and in the near future

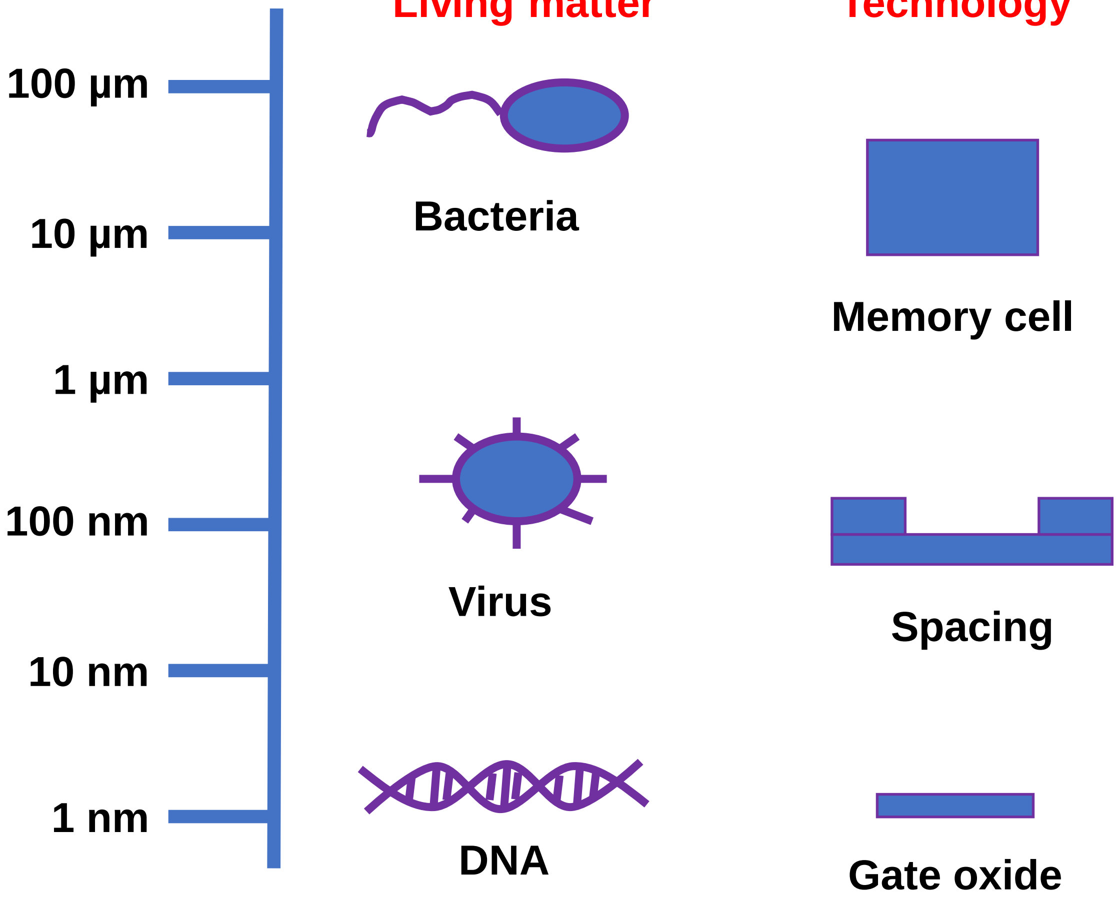
Miniaturization

- **Steady trend**
  - **Up to now, every prediction of a limit has been contradicted**



http://www.spinograph.org/blog/why-nanoelectronics-better-microelectronics

Dimensions



100 µm

10 µm

1 µm

100 nm

10 nm

1 nm

Living matter

Bacteria

Virus

DNA

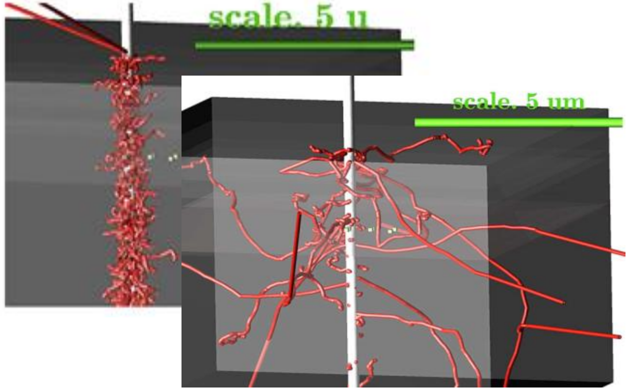
Technology

Memory cell

Spacing

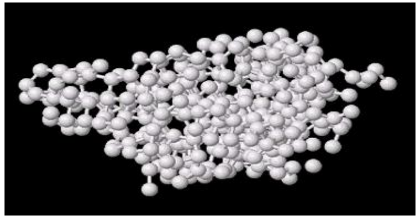
Gate oxide

Radiation



King, 2013, © IEEE

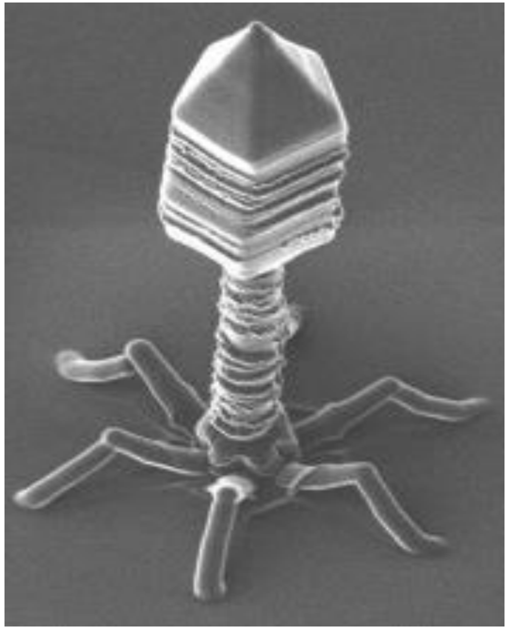
Ion track “radius”

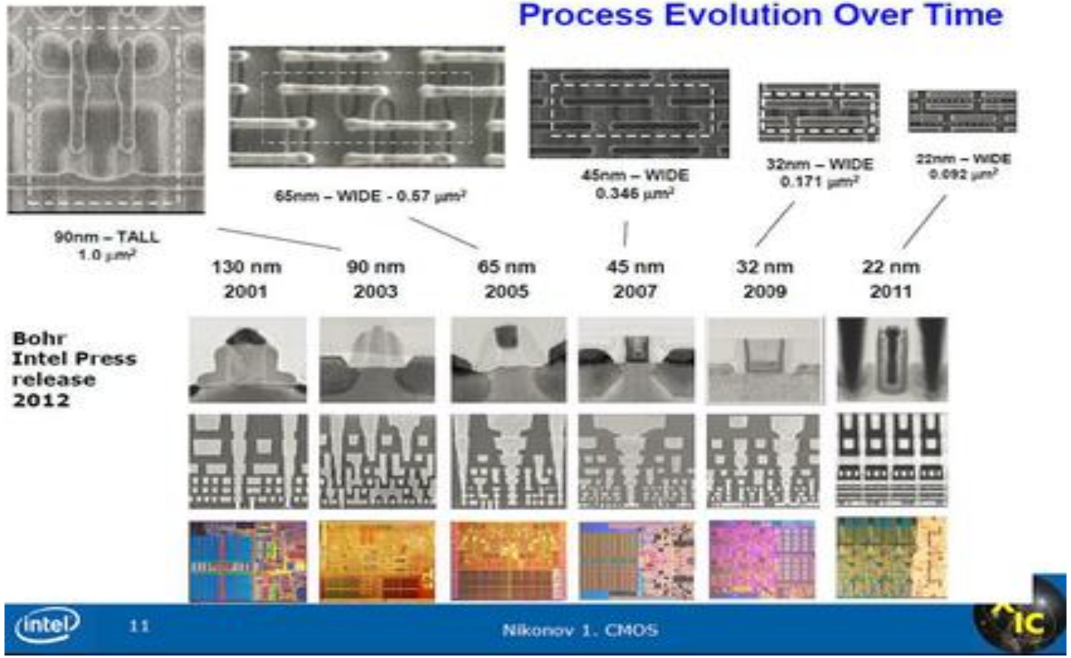


Defects cluster

Dimensions

About the same scale of structuration than elementary living matter





Process Evolution Over Time

90nm – TALL
1.0 µm²

65nm – WIDE - 0.57 µm²

45nm – WIDE
0.346 µm²

32nm – WIDE
0.171 µm²

22nm – WIDE
0.092 µm²

130 nm	90 nm	65 nm	45 nm	32 nm	22 nm
2001	2003	2005	2007	2009	2011

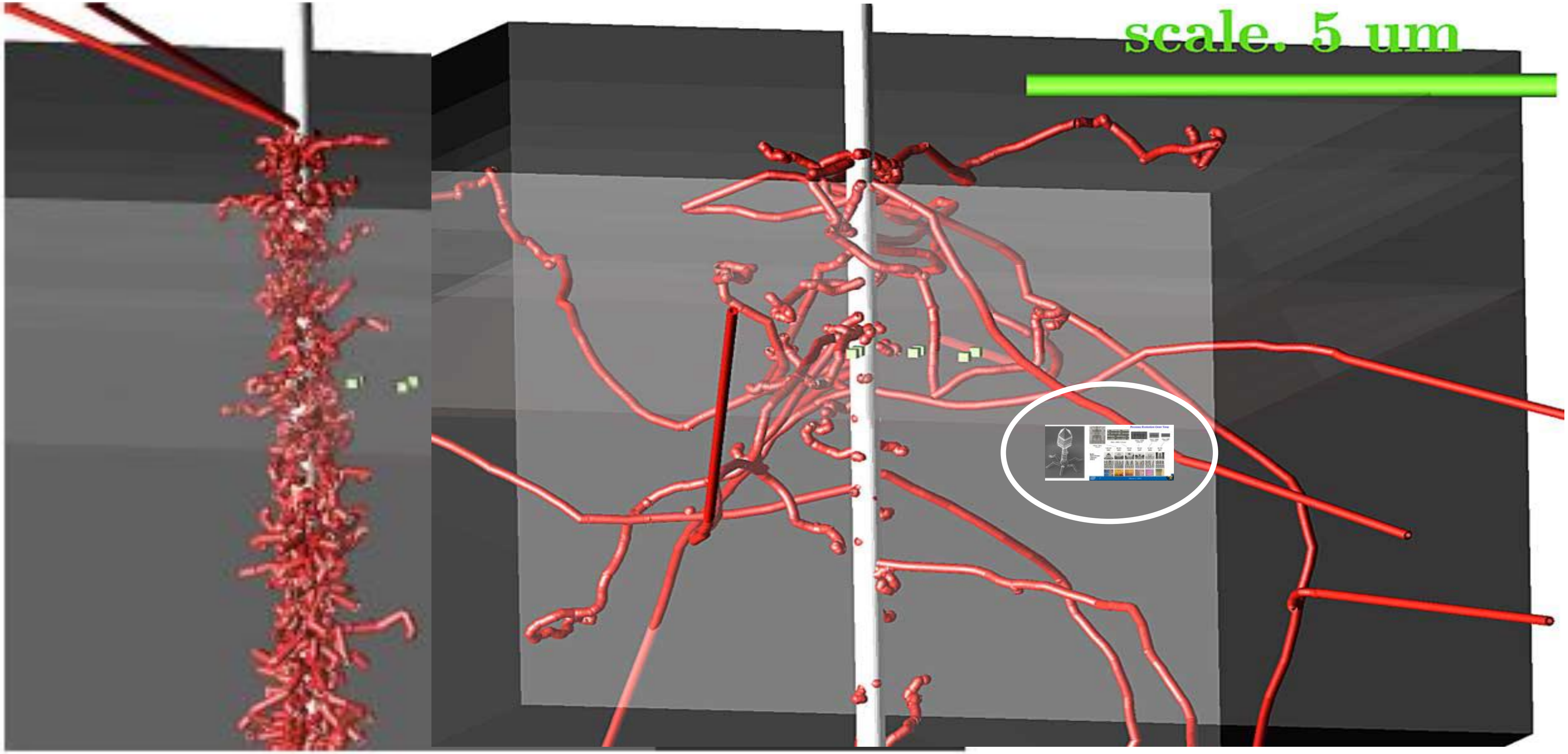
Bohr
Intel Press
release
2012

This virus (bacteriophage) is about 200 nm tall and 65 nm wide

Compared dimensions

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 57, NO. 6, DECEMBER 2010

KING *et al.*: THE IMPACT OF DELTA-RAYS ON SINGLE-EVENT UPSETS IN HIGHLY SCALED SOI SRAMS

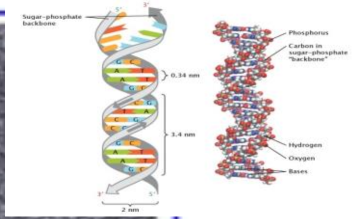


280 MeV Fe

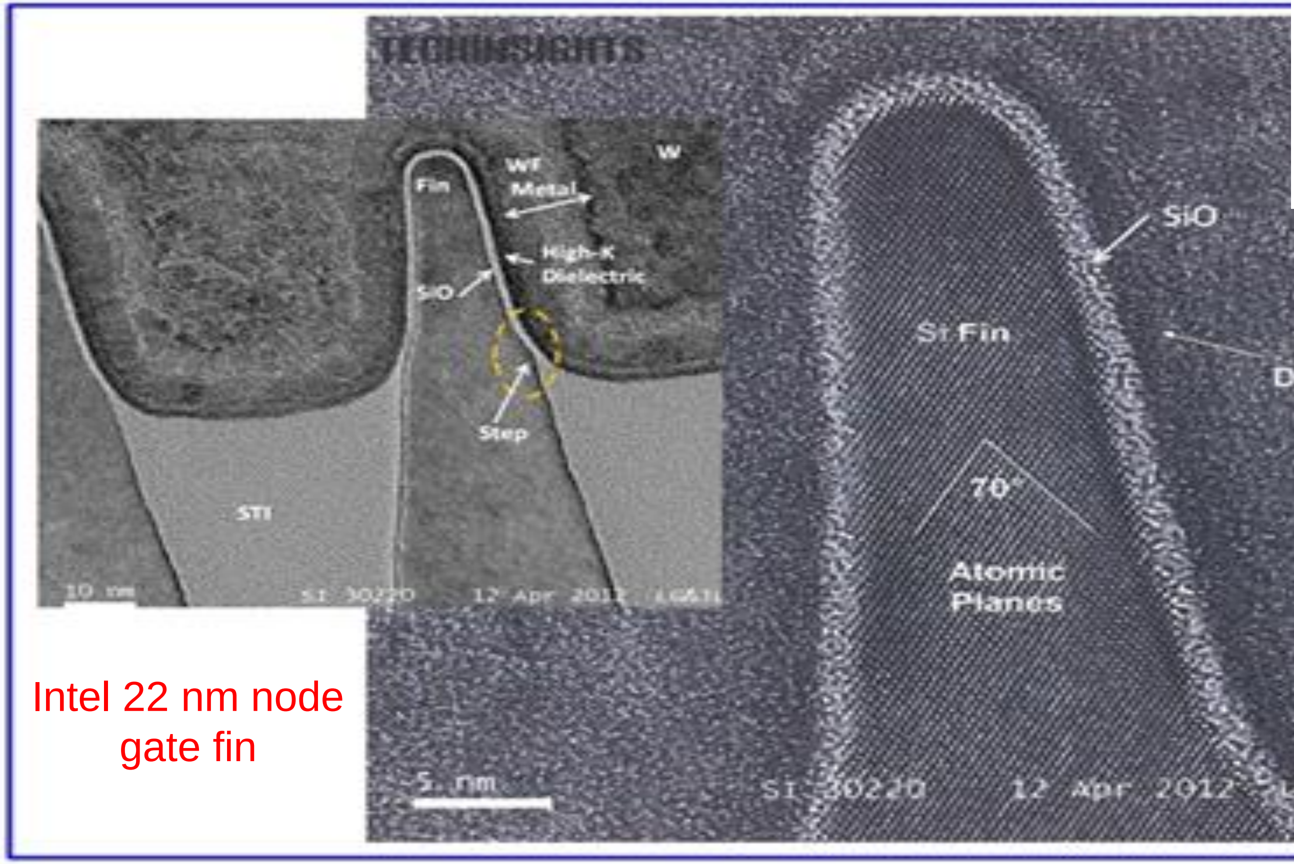
28 GeV Fe

Dimensions

Width of DNA helix ~2 nm



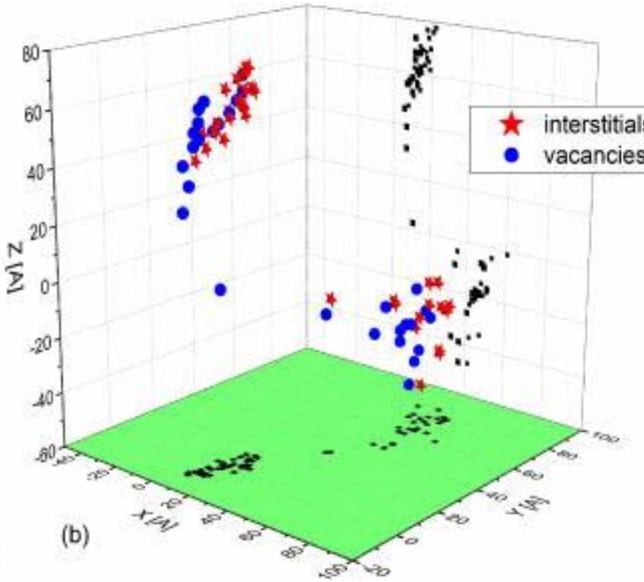
www.nature.com



Intel 22 nm node
gate fin

http://www.edn.com/Home/PrintView?contentItemId=4395587

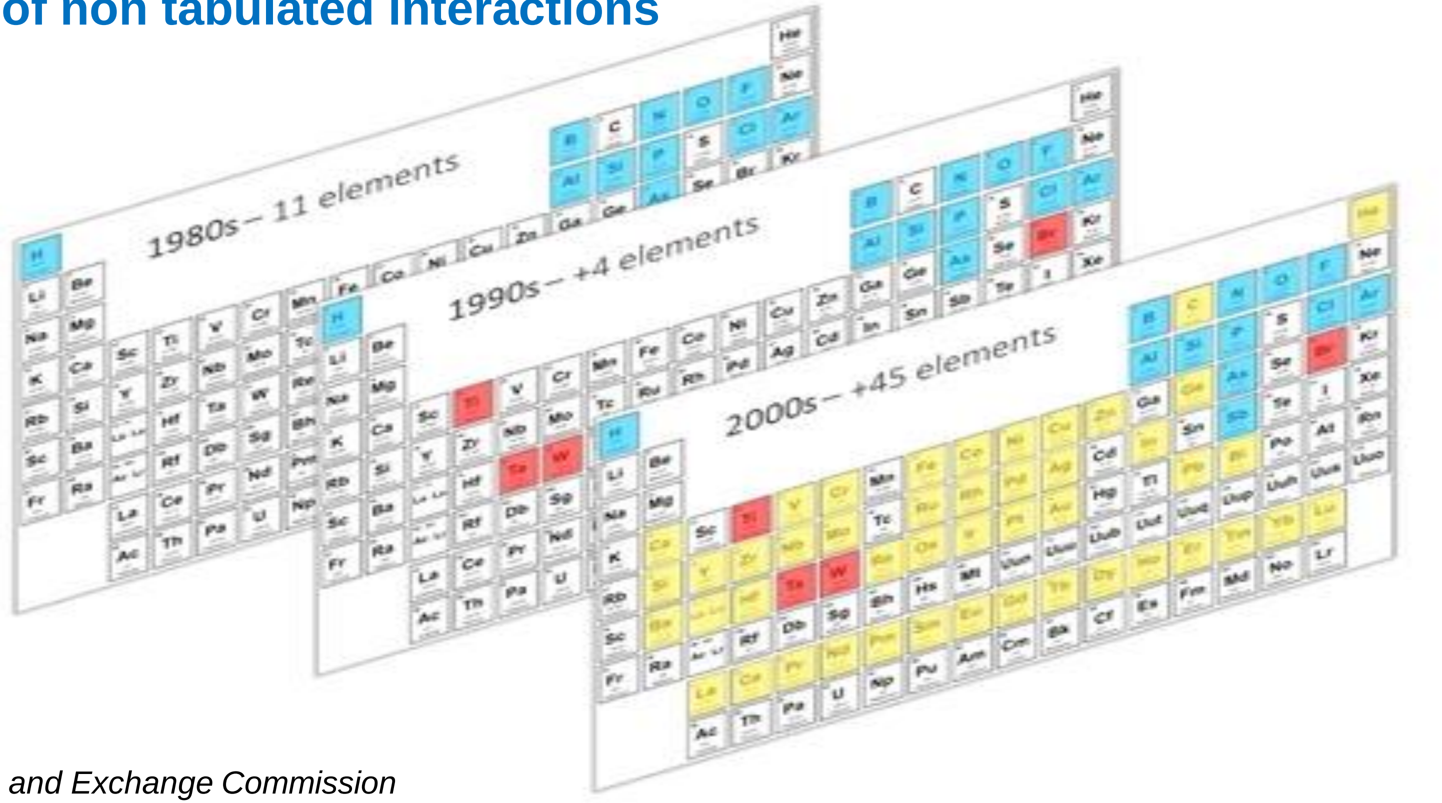
Cascade from 20 keV PKA



Investigation of point and extended defects in electron irradiated silicon—Dependence on the particle energy: Journal of Applied Physics: Vol 117, No 16

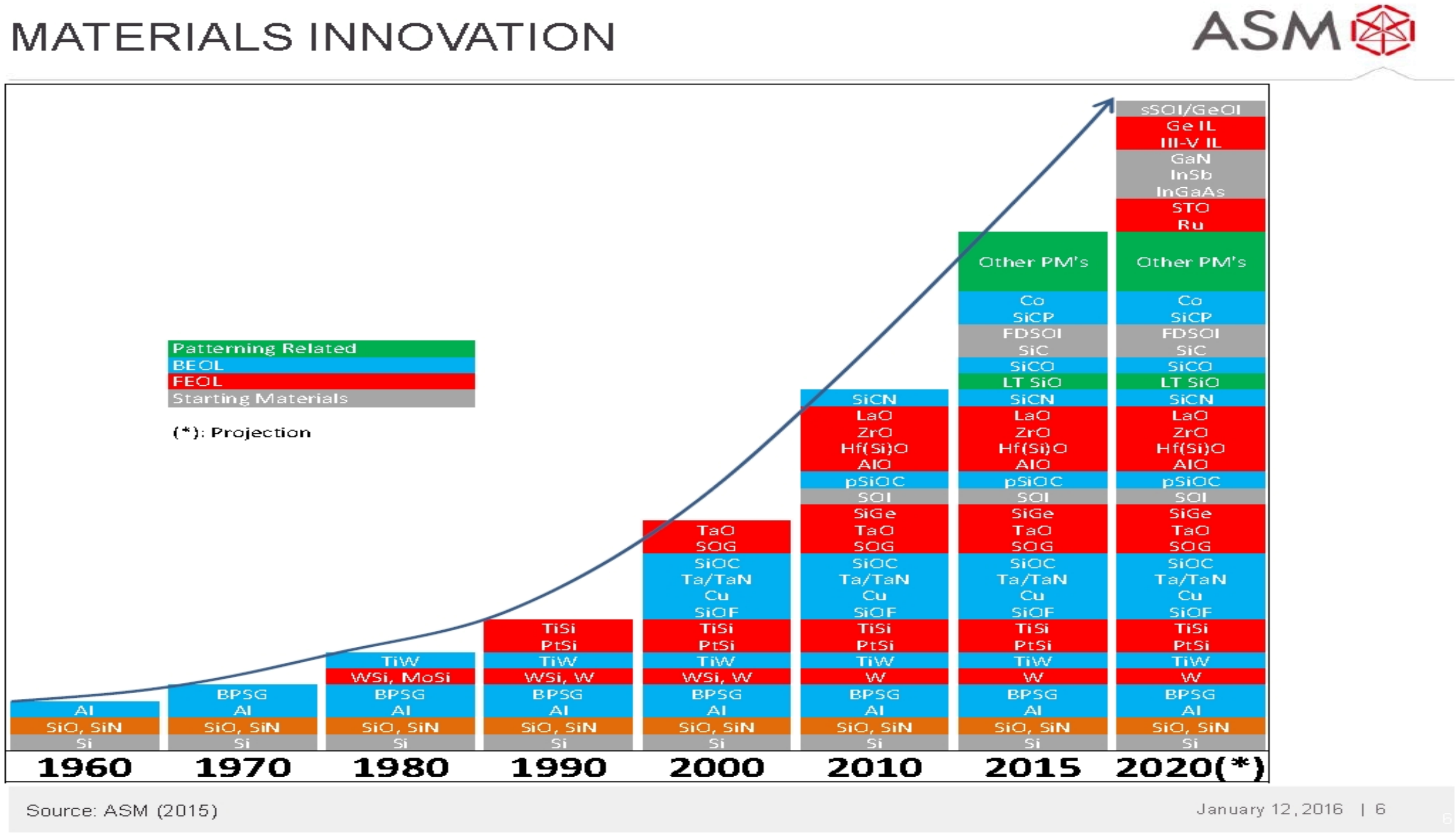
“New” materials : elements

- A large part of the periodic table is now used in technology
  - May become a strategic procurement issue (+ ethical and environmental issues)
  - Large part of non tabulated interactions



US Securities and Exchange Commission
https://www.sec.gov/Archives/edgar/data/1101302/000119312516645958/d225180dex991.htm

“New” materials : compounds



MATERIALS INNOVATION

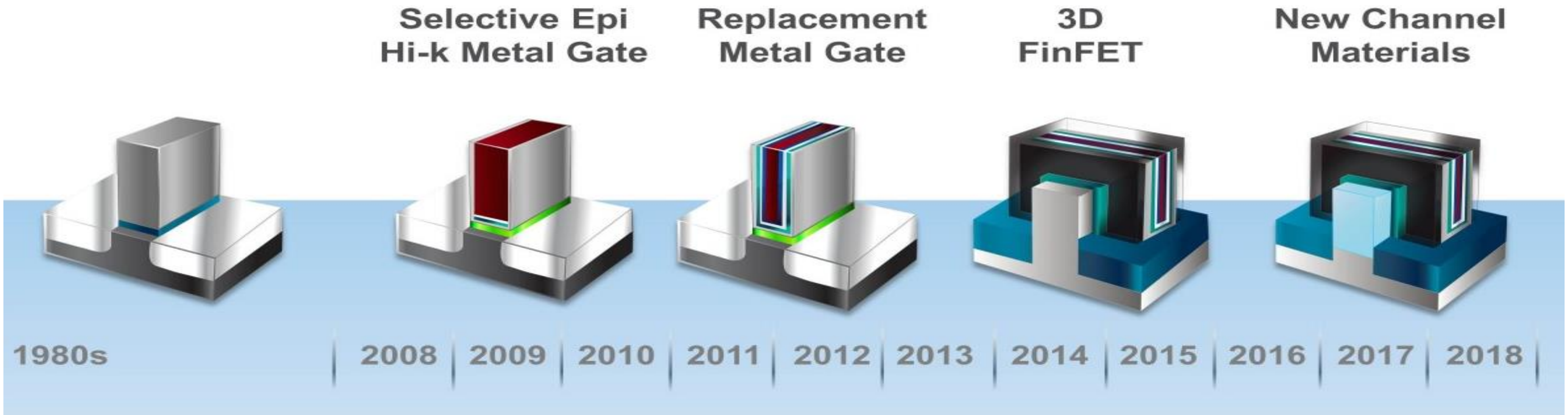
ASM

Source: ASM (2015)

January 12, 2016 | 6

ASM International (American Society for Metals), Electronic Materials Handbook

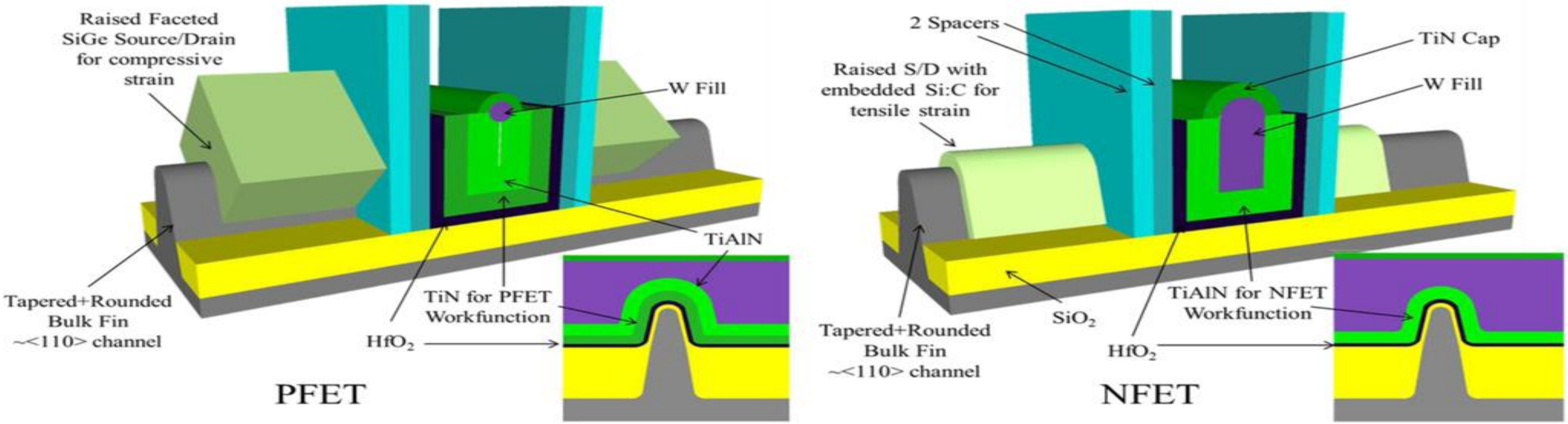
Micro-structuration :
example of transistor gate evolution



Adapted from : http://semimd.com/applied/files/2013/12/Transistor_Blog_2.jpg

Micro-structuration : today

- **Intel 22 nm node**
  - **9 Cu metal layers, W contacts, Ge and C implants**

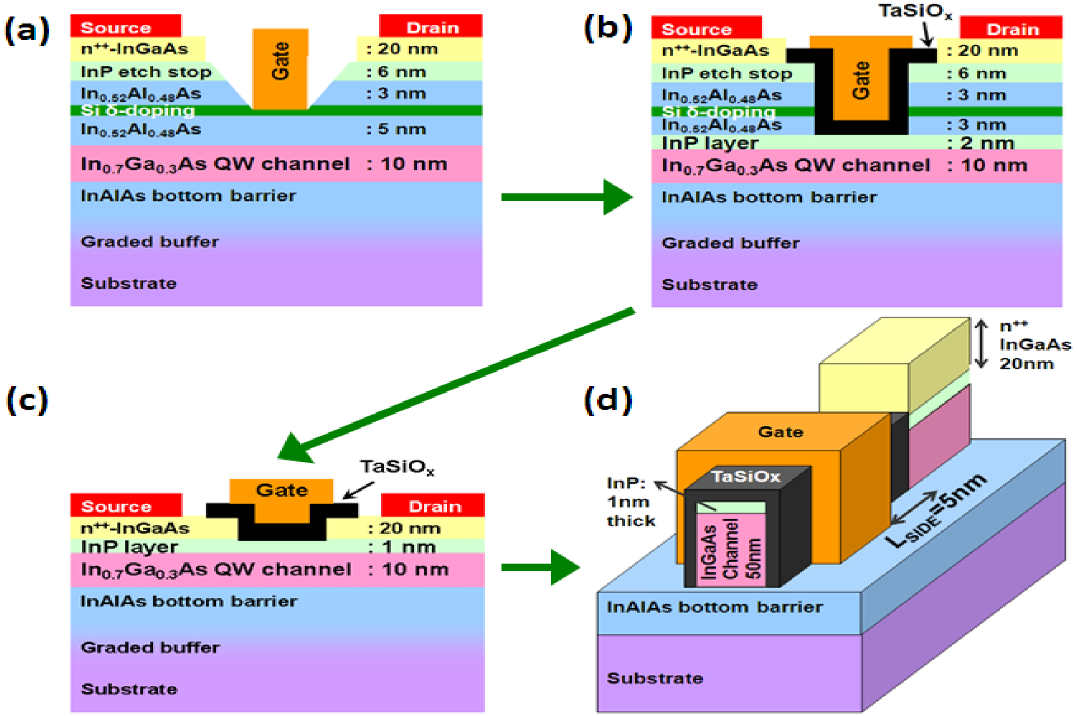


Those technologies are already in your smartphone

Robert D. Clark, Emerging Applications for High K Materials in VLSI Technology, Materials 2014, 7(4), 2913-2944; doi:10.3390/ma7042913

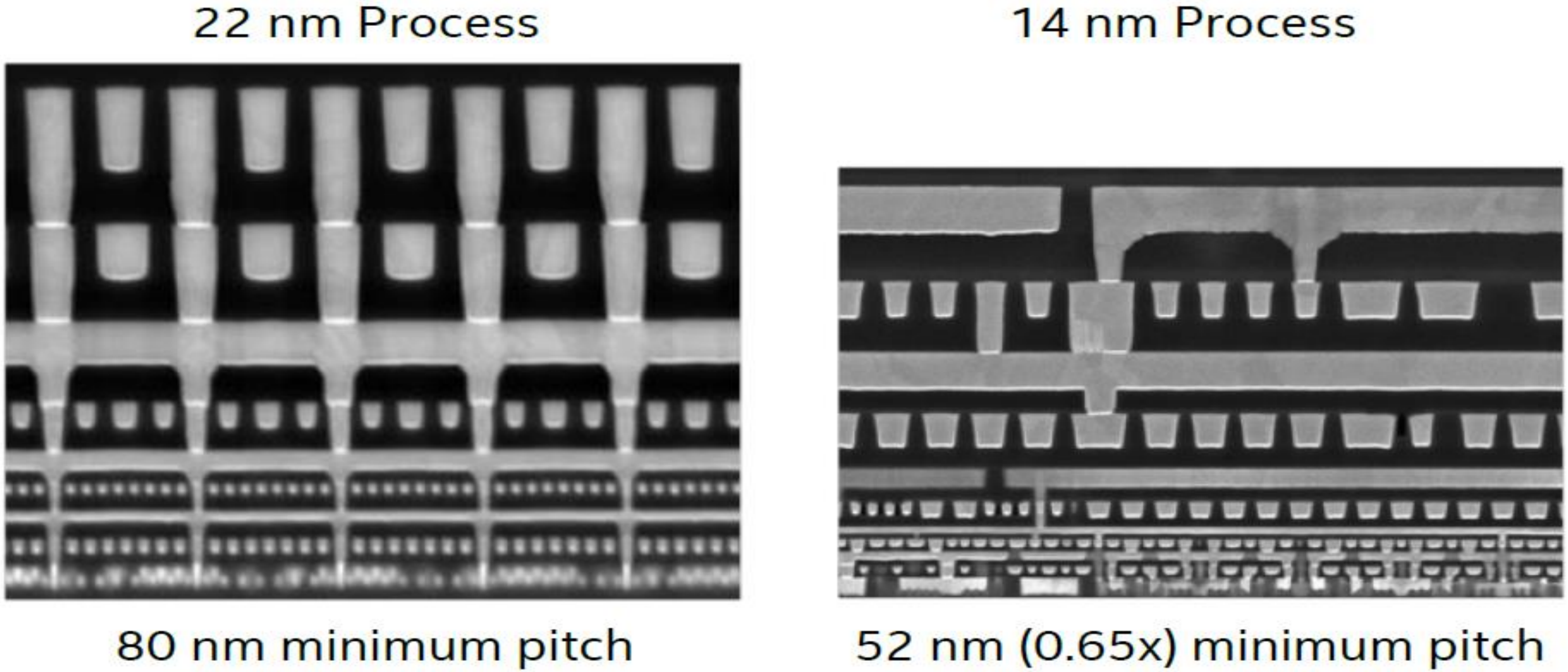
Micro-structuration : foreseen future

Quantum well transistors



M. Radosavljevic et al. (Intel), Non-Planar, Multi-Gate InGaAs Quantum Well Field Effect Transistors with High-K Gate Dielectric and Ultra-Scaled Gate-to-Drain/Gate-to-Source Separation for Low Power Logic Applications, Fig. 1: Evolution of InGaAs QWFET from planar to non-planar, multi-gate architecture, IEDM10-126, 978-1-4244-7419-6/10/$26.00 ©2010 IEEE

Complexity : interconnections



9 interconnection layers

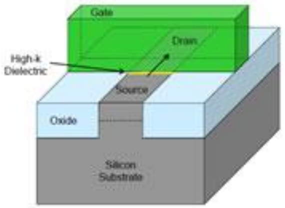
11 interconnection layers

Intel 22 and 14 nm processes

http://www.intel.com/content/dam/www/public/us/en/documents/pdf/foundry/mark-bohr-2014-idf-presentation.pdf

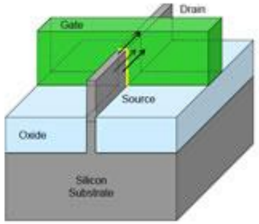
Complexity : 3D patterns

Traditional Planar Transistor



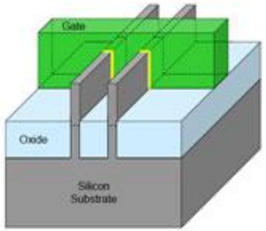
Traditional 2-D planar transistors form a conducting channel in the silicon region under the gate electrode when in the "on" state

22 nm Tri-Gate Transistor



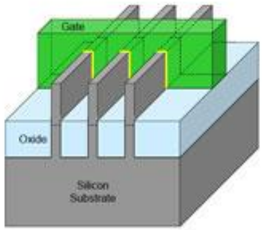
3-D Tri-Gate transistors form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

22 nm Tri-Gate Transistor

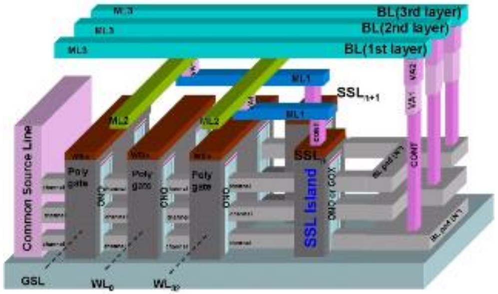


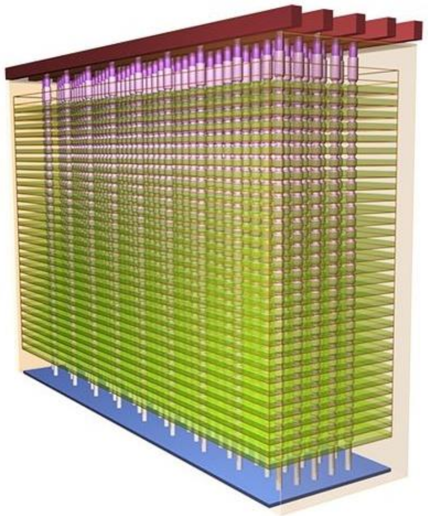
Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance

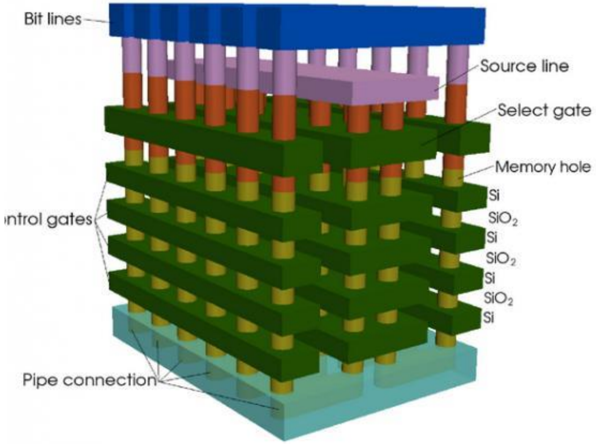
22 nm Tri-Gate Transistor



Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance

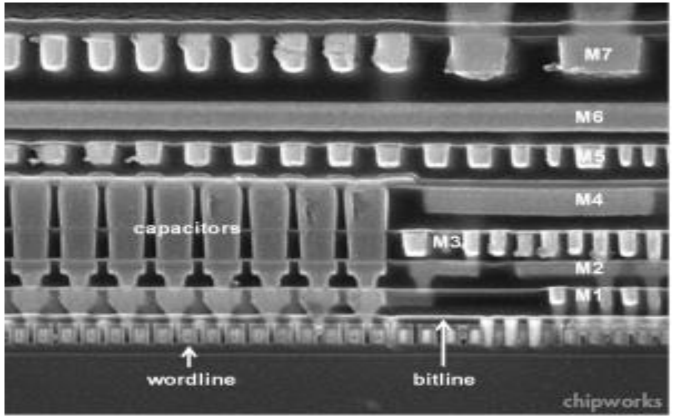




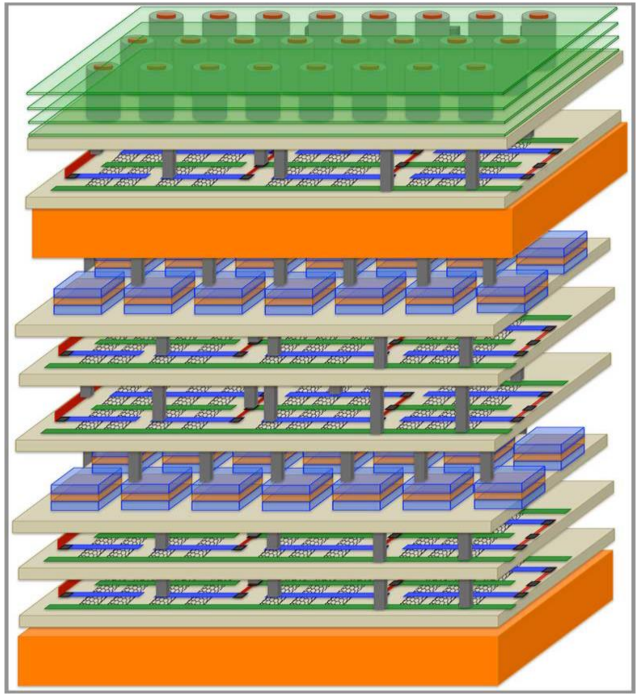


https://electroiq.com/2012/09/horizontal-channels-key-to-ultra-small-3d-nand/
http://www.eenewsanalog.com/news/toshiba-takes-3d-nand-96-layers-4-bits-cell
https://www.notebookcheck.net/Micron-intros-its-first-3D-NAND-memory-for-mobile-devices.171198.0.html

Complexity : 3D patterns



Intel’s 22-nm embedded
DRAM stack

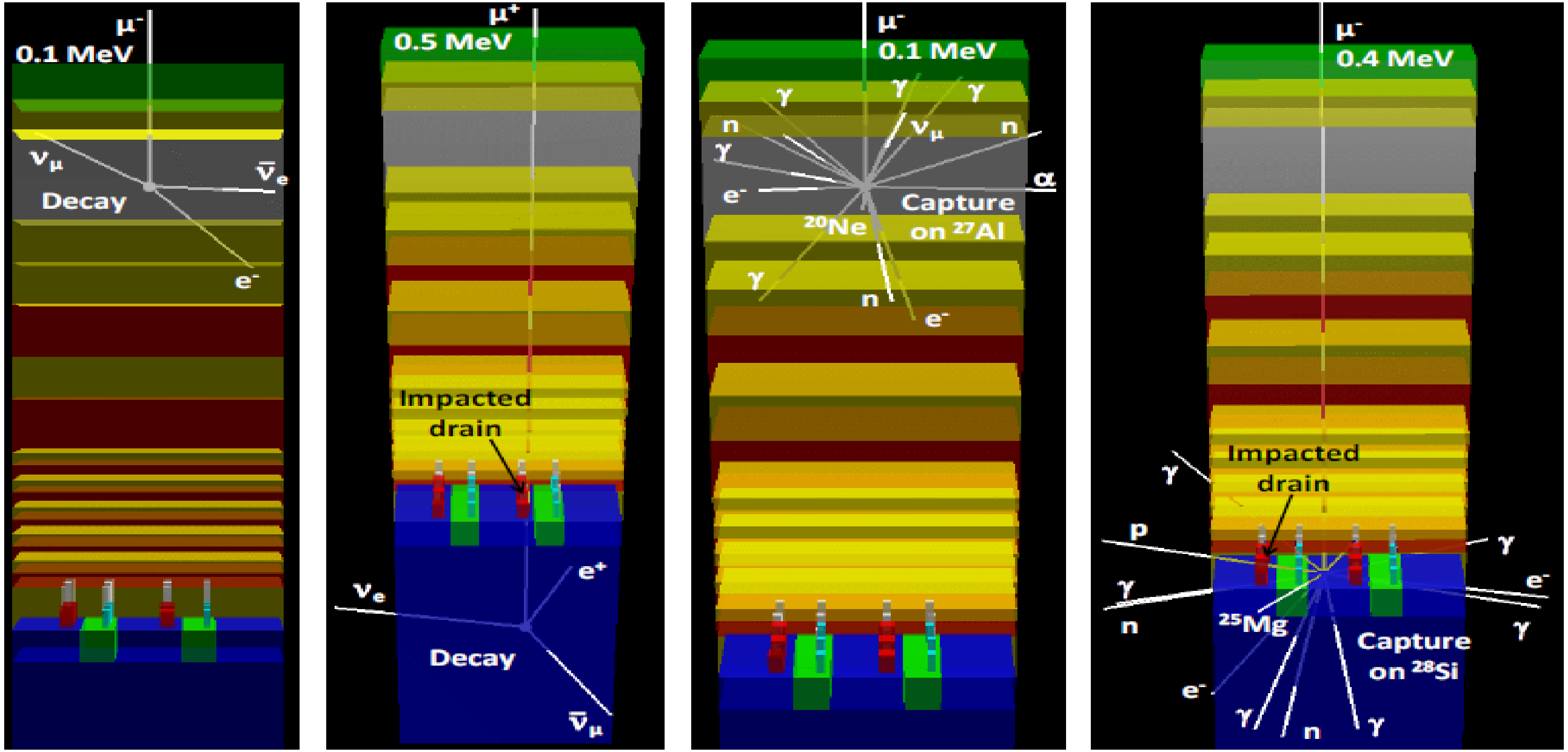


Stanford’s Nano-Engineered Computing
Systems Technology (N3XT)

MEMS

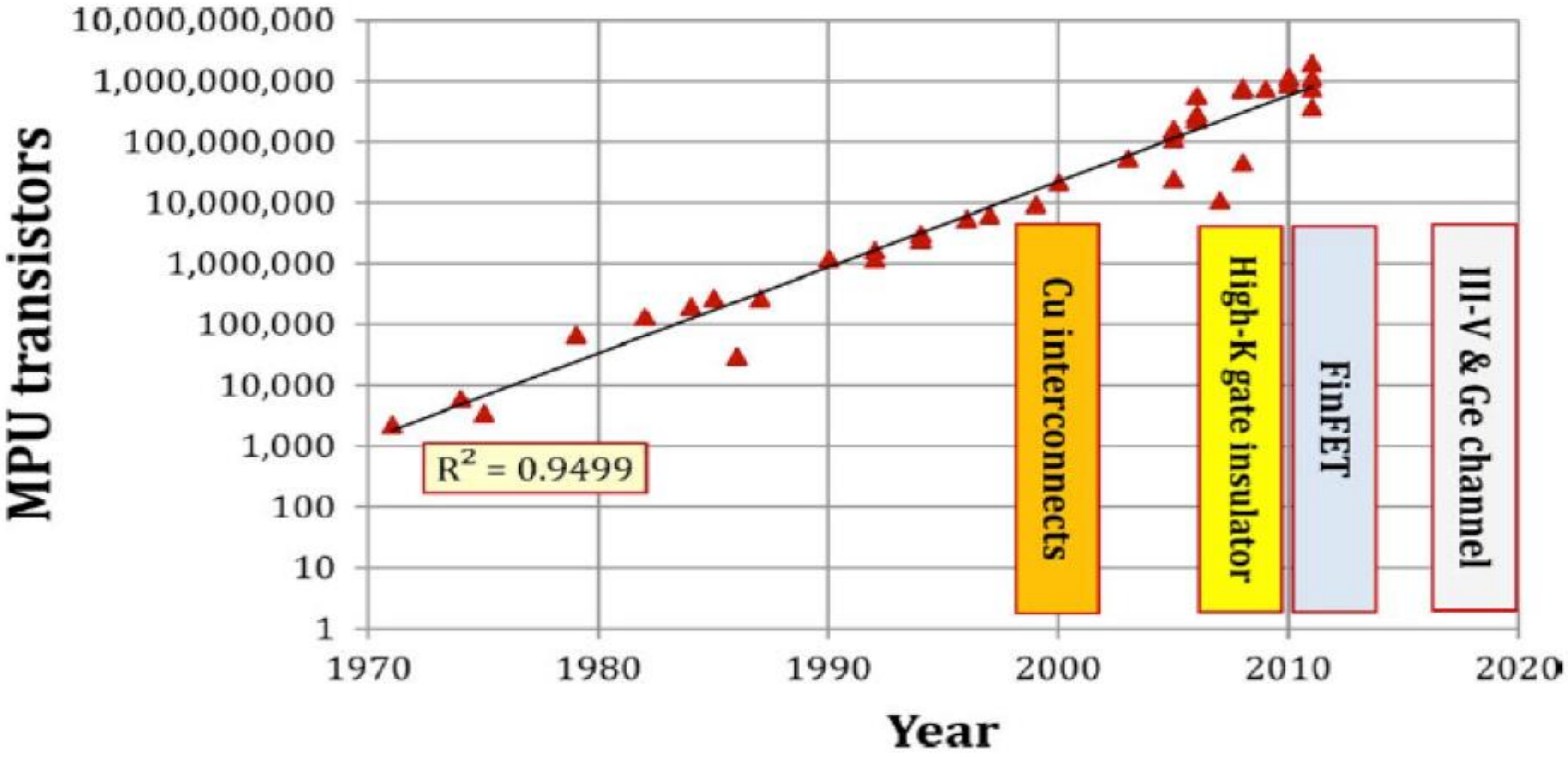
http://chipworksrealchips.blogspot.fr/2014/02/intels-e-dram-shows-up-in-wild.html
http://news.stanford.edu/2015/12/09/n3xt-computing-structure-120915/
http://www.memx.com/

Impacts on radiation effects : more interactions



Courtesy Jean-Luc Autran, RADECS 2013 Short Course

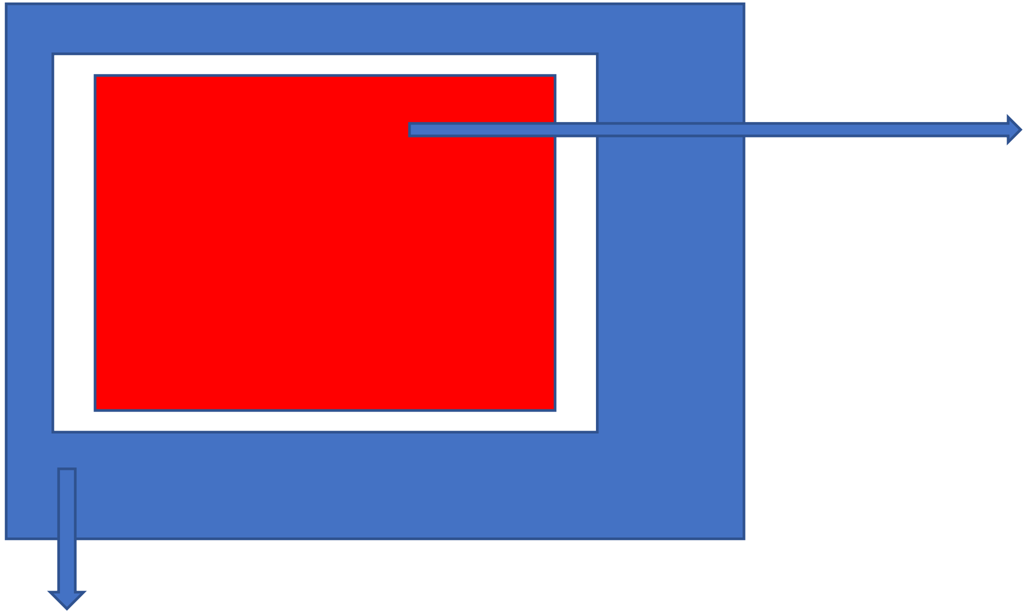
Complexity : transistors per chip



Number of transistors in a microprocessor

http://www.spinograph.org/blog/why-nanoelectronics-better-microelectronics

Complexity : technology mixing



Core

New memory concepts (*)

MEMS
- Quite hard

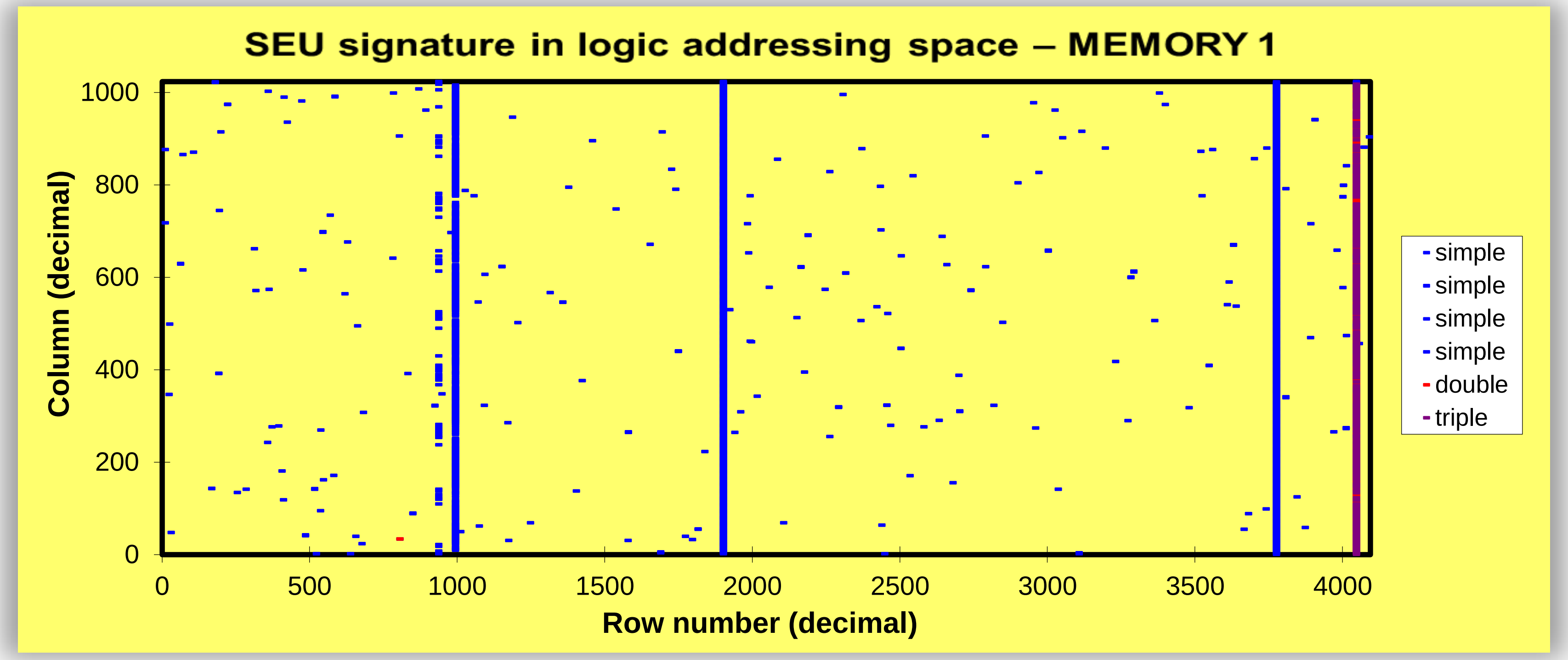
CMOS imagers
- Transients
- Hot pixels, RTS
- TID
- DDD

Periphery : CMOS usually

Will drive the radiation performance
- Quite soft
- Latch-up, SET, SEU

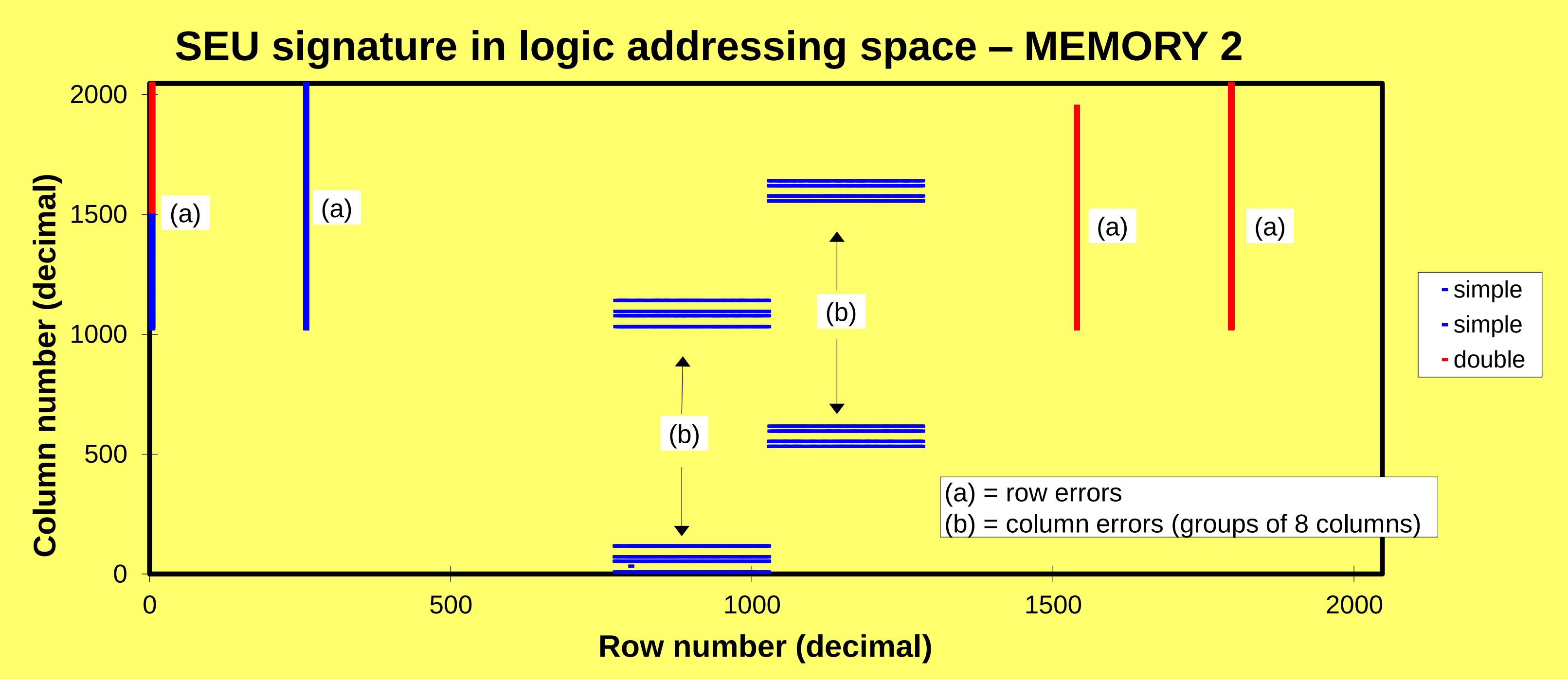
(*) Magnetic RAM, Spin Transfer Torque RAM (STTRAM), Phase Change RAM (PCRAM), ReRAM (Redox or Resistive RAM), Valence change memory (VCM), Electrochemical memory (ECM), Thermochemical memory (TCM),…

Complexity : event signatures



Same « technology node », different circuit architecture

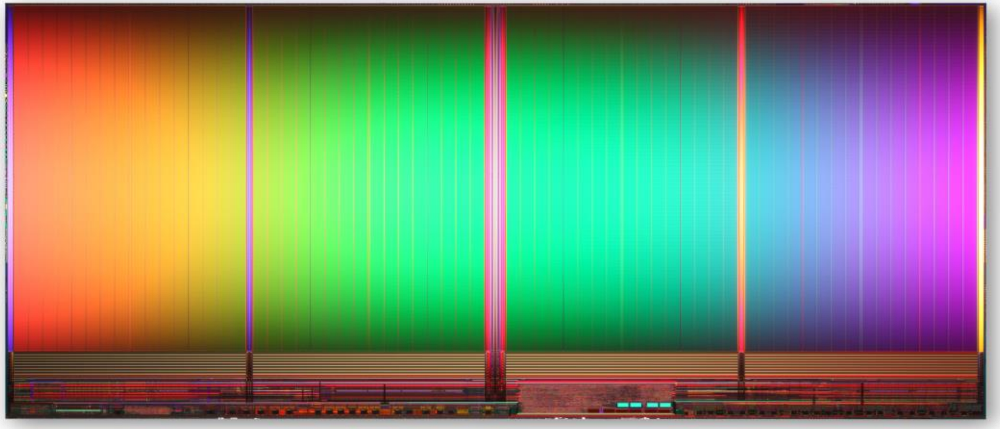
Complexity : event signatures



Same « technology node », different circuit architecture

Complexity : final word

© NASA JPL



Intel-Micron 25-nanometer (nm) 8 gigabyte (8GB) NAND flash memory

More transistors now in a single chip than in whole 1980's spacecraft designs

(GALILEO Jupiter probe for example)

http://www.intel.com/pressroom/archive/releases/2010/20100201comp.htm

Consequences for radiation hardness assurance

New elements

- **Recoil of heavy elements**
  - Max recoil LETs in MeV/mg/cm² in Si : Si = 15, Cu = 31, W = 83
  - Proton SEUs can be induced on high-LET threshold devices, incl. rad-hard (seen in space)
- **Physical sciences – radiation / matter interaction**
  - As surprising as it may appear, proton NIEL for example is still largely unknown for elements such as As, Ga, In,…

Smaller dimensions

- **Particle track larger than device features**
  - Multiple node collection will generalize
  - MBUs (incl. SOI), possibly SEFIs or other conflicts in the state machine
- **Induced defects comparable or larger than device features**
  - Could in principle completely jam a DSM gate oxide
- **High electric field across oxides**
  - Electric field across a gate oxide of 2 nm under 1 V is about 5 MV/cm closing SiO2 minimum dielectric breakdown field, such as for power MOSFETs in the past
  - This has lead to the introduction of high-k dielectrics (e.g. HfO2)
  - But still possible impact on RILC (radiation induced current leakage) or even SEGR

Smaller SEE thresholds (critical charge)

- **SEEs induced by proton direct ionization**
  - Observed in testing for nodes smaller than 45 nm
  - From estimations would contribute to a few 10% of in-orbit LEO rate, to date
  - But still no agreed test method and a fortiori flight rate estimation technique
- **SEEs induced by electrons**
  - First observed through MBUs in SOI technologies, which was supposed impossible
  - Due to high-energy electrons ejected along ion track and ballistic crossing of the oxide between two cell
  - Would also possibly be created by primary electrons from the space environment
  - CNES and ESA studies on <=45 nm devices : really appears above 10 MeV from nuclear reactions, not an issue now for Earth orbit

Smaller dimensions and SEE thresholds

- **Some proton – substrate nuclear reactions can produce several recoils**
  - In the past, only the heavier one was of significant importance (classical proton SEE)
  - The thresholds being lower now, the lighter ones may also deposit enough energy for an SEE
  - The distances being shorter many of the recoils may reach a sensitive volume
  - Another possible source of multi-node charge collection
  - The multiplication of chemical elements implies more interaction possibilities

Complexity

- **Single event functional interrupts (SEFI)**
  - SEFI is a functional manifestation, not a physical effect
  - The term extends to any “critical effect”, and has to be detailed in test reports : a SEFI cross section curve without description of the “SEFI” is of little use
  - Tends to generalize to about any digital or digital/analog circuits
  - Complex signatures, possibly very harmful events (e.g. µP erases its EEPROM array)
  - It is not impossible that multi-node charge collection plays a role in the generalization of SEFI because it may induce strong disturbances into the state machine

Some still unexplained effects

- **Weakened cells**
  - Observed in space after the first mission days, observed in testing
  - Cell is intermittently stuck at 0 or 1, may defeat classical mitigation techniques
  - Occurs in SDRAMs, DDR
  - Still badly understood, likely to be due to DDD
  - No agreed test method and a fortiori in-orbit estimation technique
  - *RTS and possibly weakened cells are supposedly due to DDD, but the link between microcosm (energy states of defects) and the macrocosm (current measured in the laboratory) is still not understood*
- **High current events (HCE)**
  - Observed on some FPGAs, FlashEPROM, MRAM,…
  - Micro-latch-up ? Damage and induced leakage ? Internal bus conflicts ?
  - May be resettable, may need ON/OFF, may not anneal

Discussion : test challenges

- **Most of heavy-ion tests are made on delidded devices and normal incidence**
  - More and more difficult and expensive to open parts to expose the die
  - Will become nearly impossible with 3D technologies
  - Particles coming sideways may be more harmful (tri-gate FinFET, “tower” Flash,..)
  - Roll and tilt testing will probably be necessary
  - Access to very high energy ion beams not easy, especially in Europe
- **Possible test artifacts**
  - High flux / fluence experiments may induce “new” artifacts
  - E.g. gate oxides can be damaged by 10^7 heavy ions / cm^2, but in space the real fluence will be a couple or a few tens of these ions → ???
  - Or, beam degradors and everything that is in the ion beam path can generate neutrons, but there will not be a significant ion-induced neutron generation in space
- **Testing a billion transistor circuit is a challenge by itself**

Conclusions

- Device features are now comparable or smaller than radiation interaction characteristics, this complicates very much the problem
- In terms of electrical testing, complexity becomes a real challenge (testability, test coverage)
- Tests procedures and facilities may need to be revisited to avoid artifacts (flux, fluence) and improve representativeness (high energy beams, tilted irradiation)
- R&D still needed in physics (radiation / matter interaction, physics of defects) and in understanding of basic mechanisms (RTS, weakened cells, HCE)
- The generalization of SEFI, HCE, weaken cells will impact on mitigation techniques
- The paradigm of “we don’t care about radiation effects, a priori mitigation works” of the good old days of simple SEUs and easily detected latch-up is over
- Links between radiation, component and system engineers more than ever needed