ESCC

APPLICATION FOR ESCC QUALIFICATION APPROVAL

Component Title: **Integrated Circuits, Silicon, Monolithic, CMOS, Cell-Based Array, based on Type ATMX150RHA – Ph2 Digital Only 22Mgates 5ML+Thick Metal MMT Assy**

Executive Member: CNES Date: 11/04/2019

Appl. No. 359

1 Components (including series and families) submitted for Qualification Approval

ESCC COMPONENT. NO.	VARIANTS	RANGE OF COMPONENTS	BASED ON	TEST VEHICLE / S	COMPONENT SIMILAR
9202083	All	ASIC (Digital only, 22Mgates, 5ML+Thick Metal, 3.3V IO, 2.5V IO, MMT assembly)	ATMX150RHA technology	002OP, 002MS, 02FT, 002NY, 002FU, 002NX	

2 Component Manufacturer

MICROCHIP TECHNOLOGY NANTES (ex-ATMEL NANTES)

3 Location of Manufacturing Plant

MCHP Nantes (design & test)
UMC Taïwan (wafer fab 8C)
MMT Thailand (assembly)
HCM La Rochelle (column mounting)

4 ESCC Specification used for Qualification

Generic: ESCC 9000
Issue
Detail/s: ESCC 9202/083
Issue

5 Qualification Report Reference and date:

ATMX150RHA Qualification Test Report 2018-IC-384_QTR_rev1.0

Date: 05/11/2018

6 **PID** used for manufacturing Qualification Lot

Ref No: ATMX150RHA PID 0037
Issue: Rev D
Date: 12/04/2019

7 **PID** changes since start of qualification

None ☐
Minor* ☒ (* Details not published, provided in confidential annex 2.)
Major* ☐

8 Current **PID** Verified by CNES (D. Dangla)

Name of Executive Representative

Ref No: ATMX150RHA PID 0037 – Rev D – 12/04/2019

MMT PID FOR MCHP NANTES – 1G-QM-0105 – 04/02/2019

HCM Colums manaufacturing & Assembly on CLGA PID 11 issue E – 09/01/2019

9 Current Manufacturing facilities surveyed by:

CNES (D. Dangla, F. Malou) & ESA (F. Martinez) 15/10/2018

(Name of Executive Responsible) (Date)

Report Reference - ESCC validation audit of MMT assembly for ATC18RHA and ATMX150RHA ASICs ESCC QML - DSO/AQ/EC-2018.19112, 29/10/2018

Satisfactory: Yes ☒ No ☐ Explain

10 Quality and Reliability Data

Evaluation testing performed Yes ☒ No ☐

Report Ref. No.: MMT assembly line - Qualification Tests Report 2017-EC-212 rev2 Date: 16/08/2018

Equivalent Data:

Certification:

Failure analysis, DPA, NCCS available Yes ☒ No ☐

(supply data)

Ref Nos. and purpose:

Construction analysis report done by MCHP: CA18-10948
Constrruction analysis reports done by CNES: DSO/AQ/LE-2018.0010689 on multi-decks & DSO/AQ/LE-2019.0003248 on flat-substrates

11

The undersigned hereby certifies on behalf of the ESCC Executive, that the above information is correct; that the appropriate documentation has been evaluated; that full compliance to all ESCC requirements is evidence except as stated in box 13; that the reports and data are available at the ESCC Executive and therefore applies for ESCC qualification status to be given to the component(s) listed herein.

Date: 17/04/2019

JP. BUSSENOT

(Signature of the Executive Coordinator)

12

Continuation of Boxes above: (Only non-confidential comments)

[5] ESCC QML qualification of UMC 8C wafer fab with MMT assembly based on: ATMX150RHA Qualification Test Report 2018-IC-384_QTR_rev1.0 and associated reports:

- ATMX150RHA Synthesis characterization Report 150nm PD-SOI Technology UMC fab 8C – Reference: 2019-EC-446 rev 1.0
- ATMX150RHA Wafer Level Reliability qualification report – Reference: 2018_IC_393_rev1.6
- ATMX150RHA Electrical Latch-Up qualification report – Reference: 2018-IC-398 Electrical Latchup rev1.2
- ATMX150RHA ESD report – Reference: 2018-IC-392 ESD rev1.3
- ATMX150RHA Validation of life test at 150°C instead of 125°C Package/Assembly integrity verification report – Reference: 2018-IC-391 Package integrity after lifetest 150°C rev0
- ATMX150RHA Endurance qualification test report (High Temperature Operating Life test) 150nm on SOI UMC Fab 8C – Reference: 2018-IC-397 Life-test rev1.0
- ATMX150RHA Package/Assembly qualification test report 150nm on SOI UMC Fab 8C – Reference: 2018-IC-396 Pack-Assy reliability rev1.0
- ATMX150RHA Total Ionizing Dose qualification test report 150nm on SOI UMC Fab 8C – Reference: 2018-IC-394 TID1 rev1.4
- ATMX150RHA Single Evaluation Circuit 002MS Total Ionizing Dose qualification test report 150nm on SOI UMC Fab 8C – Reference: 2018-IC-394 TID1 rev1.4 & Reference: 2018-IC-399 TID2 rev1.1
- ATMX150RHA Single Event Effects qualification report 150nm on SOI UMC Fab 8C – Reference: 2018-IC-395 SEE rev1.5
- ATMX150RHA Construction analysis – Reference: CA18-10948.pdf
- MMT Assembly Line Qualification Test Report – Reference: 2017-EC-212 rev2
- MMT domain extension Wafer back-grinding – wafer sawing – Die inspection Qualification Test Report – Reference QTR_2018-IC-355_rev1
- CRS 17-0771 MMT assembly line – extension of Assembly qualified domain with INK marking Markem4489 Qualification Test Report – Reference: QTR3240 Markem4489 2017-IC-294 rev1
- CRS 17-0824 Lid finish – process change Qualification Test Report – Reference: QTR lid finish 2018-IC-366 rev1.0

[7] PID changes:

ATMX150RHA PID 0037

03/03/2015 – Rev 0: Creation
30/11/2015 – Rev A: Update
14/01/2016 – Rev B: Update taking into account CNES comment
29/11/2016 – Rev C: MCGA replacement by CCGA with european columns. Change name : FEPE group to Tech devt Specification table update, Fab process info update and minor corrections
12/04/2019 – Rev D: Extension to 22Mgates – Assembly in MMT, Thailand

[8] MMT PID exclusions:
- the use of 18u wire is not authorized for ESCC product
- Multi-dice devices in flat substrate packages are not authorized for ESCC product

[9] Audits and Surveys
Last ESCC QML Annual Quality Meeting held in June'18, ref. CNES/DSO/AQ/EC-2018.0010779

13

Non compliance to ESCC requirements:

No.:	Specification	Paragraph	Non compliance

14

Additional tasks required to achieve full compliance for ESCC qualification or rationale for acceptability of noncompliance:

15

Executive Manager Disposition

Application Approval: Yes ☑ No ☐

Action / Remarks:

Date:

B. Schade, Head of ESA Product Assurance and Safety Department

ANNEX 1: LIST OF TESTS DONE TO SUPPORT QUALIFICATION

16

Tests conducted in compliance with: **ESCC 9000**

- ESCC 9000 generic specification; Chart F4 (for ESCC/QPL parts);
- Or PID-TFD (for ESCC/QML parts)

Tests vehicle identification/description:

002OP CQFP-352	Standard Evaluation Circuit (SEC) - Transistors to cover a domain up to 22 Mgates (equiv. NAND2) - Thick top metal layer to avoid voltage drop issues - Set of compiled memory blocks with and without EDACs - Cold Sparing Buffers - High Speed LVDS Buffers 655Mbps - PCI Buffers - PLL 002OP shall be used for radiation testing (TID,SEU,SEL,SET), process stability and reliability monitoring, performance characterization
002MS CQFP-352	Test Vehicle Same than 002OP but NO Thick Metal Layer 002MS will be embarked on quarterly MPW (Multi-Project Wafer) instead of OO2OP when embarked ASIC's do not need thick metal layer. If so, 002MS shall be used for reliability quarterly monitoring
02FT/002NY CQFP-352	Buffers Test Vehicle - Standard IO33 buffers (supply 3.3 or 2.5V). - Specific IO33 buffers (LVDS,PCI) - PLL for performance evaluation - Set of ring oscillators made of different library cells, set of interconnect lines 002NY is a 5 metal layers with thick metal option. It shall be used for ESD tests. 002FT is the same test vehicle but without thick metal option, it shall be used for electrical latch-up, which is a test only depending on front-end process, there is no impact of the presence of thick metal option or not.
002FU CQFP-256	This test vehicle, of 5 Metal Layers, has been designed in compliance with the requirements of the MIL-PRF38535 §H.3.4.3, in terms of functionality, design, fabrication and packaging, but embarks less transistors (19 Million of devices instead of 44 Million in the 002MS). Il shall be used in conjunction with the 002MS for group E initial qualification.
002NX CQFP-352	This test vehicle, 5 Metal layers, have been designed for specific SEU tests on shift registers.

Subgroup	Test	Tick when done	Conditions	Date Code Diffusion Lot	Tested Qty	No. of Rejects	Comments if not performed. Comments on Rejection
Environmental/Mechanical Subgroup	Mechanical Shock	☒	MIL-STD-883, Test Method 2002	002MS D9Q3JA227X Si-lot DC1712	15	0	
	Vibration	☒	MIL-STD-883, Test Method 2007		15	0	
	Constant Acceleration	☒	MIL-STD-883, Test Method 2001		15	0	
	Seal (Fine and Gross Leak)	☒	MIL-STD-883, Test Method 1014		15	0	
	Intermediate and End-Point Electrical Measurements	☒	Intermediate and End-Point Electrical Measurements in the Detail Specification		15	0	
	External Visual Inspection	☒	ESCC Basic Specification No. 20500	002OP DA57MA229V Si-lot DC1712	15	0	MIL-STD-883, Test Method 2009
	Thermal Shock	☒	MIL-STD-883. Test Method 1011		15	0	
	Moisture Resistance	☒	MIL-STD-883, Test Method 1004		15	0	
	Seal (Fine and Gross Leak)	☒	MIL-STD-883, Test Method 1014		15	0	
	Intermediate and End-Point Electrical Measurements	☒	Intermediate and End-Point Electrical Measurements in the Detail Specification	00OP DAANTA22KU Si-lot DC1730	15	0	
	External Visual Inspection	☒	ESCC Basic Specification No. 20500		15	0	MIL-STD-883, Test Method 2009

Subgroup	Test	Tick when done	Conditions	Date Code Diffusion Lot	Tested Qty	No. of Rejects	Comments if not performed. Comments on Rejection
Endurance Subgroup	Operating Life	☒	MIL-STD-883, Test Method 1005	2000h @150°C			
	Intermediate and End-Point Electrical Measurements	☒	Intermediate and End-Point Electrical Measurements in the Detail Specification	002MS D9A5G.1 Si-lot DC1712	45	0	
				002MS D9Q3JA227X Si-lot DC1712	45	0	
				002OP DCGLL.1A Si-lot DC1752	45	0	
	Seal (Fine and Gross Leak)	☐	MIL-STD-883, Test Method 1014				
	External Visual Inspection	☐	ESCC Basic Specification No. 20500				
Assembly Capability Subgroup	Permanence of Marking	☐	ESCC Basic Specification No. 24800				Covered by ATC18RHA ESCC qualification tests Application n°357, 28/03/2019
	Terminal Strength	☐	MIL-STD-883, Test Method 2004				
	Internal Visual Inspection	☐	ESCC Basic Specification No. 20400				
	Bond Strength	☐	MIL-STD-883 Test Method 2011				
	Die Shear or Substrate Attach Strength	☐	MIL-STD-883 Test Method 2019 or 2027				
Additional Tests	Electrical Characterization	☒		02FT D7N0F.1 Si-lot DC1442	10	0	
				002NX D8WYK.1 Si-lot DC1537	10	0	
	Package integrity after Life-Test @150°C	☒		002OP DAANTA22KU Si-lot DC1730	4	0	
	Electrical Latch-Up	☒	JEDEC78	02FT D7N0F.1-7 Si-lot DC1442	6	0	
	ESD (HBM & CDM)	☒	MIL-STD-883 Test Method 3015.9	002NY D9KQ8-14A	15	0	ESD HBM level is class 1B (500 volts to 999 volts)
			ESDA S5.3.1-2009	Si-lot DC1633	9	0	ESD CDM levels is class C3 (250 volts to 499 volts)

	Construction Analysis	☒		002OP DAANTA22FV Si-lot DC1730	5	0	
	Radiation Tests	☒	TID ESA/SCC 22900 MIL-STD-883 Test Method 1019	00FU 3 Si-lots: D7N0F.1-4A DC1436 D7N0G.1-1 DC1440 D84HRA23Q2 DC1510 002MS D8FQFA23PU Si-lot DC1536	11 11 11 22	0 0 0 0	The TID RHA capability of 100krad (Si) (1000Gy (Si)) is demonstrated and qualified the ATMX150RHA offer, using the AT77K9RHA technology. This qualification is compliant with both DLA and ESCC systems, at a RHA-R level. The TID RHA capability of 100krad (Si) (1000Gy (Si)) is demonstrated and qualified the ATMX150RHA offer, using the AT77K9RHA technology 22 Mgates. This qualification is compliant with both DLA and ESCC systems, at a RHA-R level.
			SEE ESA/SCC 25100 EIA/JESD57	002FU D799T.1-3 Si-lot DC1410 002NX D8WYK.1 Si-lot DC1543 002FU D7NOG.1-1 Si-lot DC1440	3 8 3	0 0 0	SEL: No SEL events have been observed up to a LET of 78 MeV.cm²/mg @Vccmax @125°C. SEU: The SEU threshold LET (LETth) is upper than 18.5 MeV.cm2/mg for hardened DFF. The LETth is 3.0 MeV.cm2/mg for the standard DFF. The LETth is 1 MeV.cm2/mg for the Virage memories so below the standard DFF, and at a value in line with the CMOS 0.18 µm technologies. No SEU event has been noticed on standard DFF with TMR hardening.

Note : All lots date codes up to 16xx were assembled at e2v and are shown for characterization purpose. All lots date codes from 17xx were assembled by MMT.

Note: additional test evidence related to packaging aspects is available as part of Qualification with certificate No. 357

NOTES ON THE COMPLETION OF THE APPLICATION FORM FOR ESCC QUALIFICATION APPROVAL

ENTRIES

Form Heading	shall indicate:— the title of the component as given in its detail specification or the name of the series or family; — the entering date; — the serial number and the suffix of the form.
Box 1	shall provide details given in table; in particular there shall be listed - the variants or range of variants; the range of components by using the ESCC code for values tolerances, etc.; the designation given in detail specification as 'based on'; —under Test Vehicle enter either a cross or the specific characteristic capable to identify the component tested; — under component similar enter a cross.
Box 2 and 3	Manufacturer's name and location of plant where the components were manufactured and tested.
Box 4	Generic and detail specifications used during qualification program.
Box 5	Reference to test report(s) submitted in support of application.
Box 6	Enter details to identify the PID that was applicable at the time the qualification lot was manufactured.
Box 7	If the PID was evolved after qualification lot manufacture, adequate details of such evolution shall be provided together with reasons for changes. Major changes shall be clearly marked.
Box 8	The box serves to identify the current PID and the Executive Representative that has verified it together with the date of this occurrence.
Box 9	This box can be completed only after a physical visit to the plant to confirm that the practices, procedures, materials, etc. used in manufacturing the components are as described in the PID. This survey shall be carried out in accordance with the requirements of ESCC Basic Specification No. 20200 and its findings shall be recorded.
Box 10	Details entered shall be sufficient to evidence that an evaluation program according to ESCC Basic Specification No. 22600 has been performed and that the results thereof are summarized in the survey and test reports. If the evaluation program has not been carried out according to established ESCC documents, the applicant Executive Representative shall provide alternative data and declare its assessed degree of satisfactory compliance with the ESCC basic requirements. Reference shall be made to the reports on Destructive Physical Analysis (DPA), Failure Analysis and Non conformance (NCCS) issued during the Evaluation and/or Qualification Phase.
Box 11	Enter the name of the Executive Coordinator and the signature.
Box 12	To be used when there is a need to expand any of the boxes from 1 through 10. Identify box affected and reference the Box 12 in the relevant Box. Box 12 can be broken into 12a, 12b, etc. if several Boxes have to be expanded.
Box 13	Fill table as requested.
Box 14	Fill in any additional tasks required to achieve full compliance.
Box 15	All Executive recommendations on the application itself, special conditions or restrictions, modifications of the QPL or ESCC QML entry, letters to the manufacturer, etc. shall be entered clearly in Box 15, signed by the ESA Representative.
Box 16	Fill in Table as requested.
Box 17	Confidential details of PID changes shall be provided.
Box 18	State noncompliance with reference to specification(s) and paragraph(s). To simplify reference in Box 18 each nonconformance shall be sequentially numbered. If relevant state 'None'
Box 19	Any additional action deemed necessary by the Executive Representative to bring the submitted data to a standard likely to be accepted by the ESCC Executive should be listed herein or the reason(s) to accept the nonconformance.
Box 20	Additional Comments