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MEMO

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To	Companies having ESA Approved Summary Tables or under verification programme, ESA skills training school, ESA recommended outsourcing companies, ESA PA Managers,	**Copy**	G. Corocher, E. Peraud, J. Hokka, T. Ghidini, K. Lundmark, A. Pesce, L. Marchand, Th. Battault

Subject: Devices that have shown anomalies during assembly on laminates or during verification programme as per ECSS-Q-ST-70-38

This memo is the update of the TEC-QT/2012/206/CV and the ESA-TECQTM-MO-1143 issue 1.

The changes between the different issues are highlighted in blue.

During the past years some failures on solder joints or in devices have been identified at the completion of the environmental testing performed in compliance with the ECSS-Q-ST-70-38C.

Those failures while present may not have been noticed in past verifications in compliance with ESA-PSS-01-738 and ECSS-Q-ST-70-38 due to the reduced number of parts being microsectioned and as the quality of the microsectioning may not have been sufficient to detect such cracks.

The intention of this memo is to allow all parties to be aware of the possible anomalies. This memo can be considered as informative except for the number of microsections required to confirm that assembly is compliant to ECSS. The objective is that each company will compile and maintain its own list of sensitive devices.

The assembly of the devices is considered sensitive when:

-The crack in the solder joint is longer than 75% of acceptable crack or when other anomalies have been identified after assembly and/or at the completion of the verification programme.

-The failure in the solder joints and/or in the devices has been noticed in many occasions by different end users.

Some of these listed sensitive devices may require higher number of devices to be verification tested (see Table 1).

The list of the devices is not exhaustive. This list may be updated once new anomalies are identified. The list of devices for which anomalies have been observed is uploaded on the escies website (www.escies.org).

Component	Package type	Type of failure	Possible cause of the failure	Number of parts to be assembled/ microsectioned per assembly configuration	Possible preventive action
Chip Resistor	R1206, R2010, R2512	Cracks in the solder joint	CTE mismatch between PCB and component	5 assembly/5 microsections	- To increase the stand off. Such corrective action may not be sufficient.
Chip resistor network	Resistor network	Cracks in the solder joint	CTE mismatch between PCB and component	5 assembly/5 microsections	- To increase the stand off. Such corrective action may not be sufficient.
Ceramic Chip Capacitors	Any of ceramic of type 2 when assembled by hand and or pretinned	Crack in the ceramic initiated at the end termination	-Thermal shock that may be caused during pretining and or assembly, - Assembled part having been reworked	5 assembly/5 microsections	-Preparation and assembly procedures to be compliant to component manufacturer recommendations (preheating of the board, device and limited delta temperature between iron tip and component), - Due to the sensitivity to thermal shock ESA does not accept pretining and/or rework on such devices. Therefore in case of non conform solder joint the device shall be changed.

Ceramic Chip Capacitors	Any of ceramic of type 2 when assembled by collective assembly for parts smaller than C1825	Crack in the ceramic initiated at the end termination	-Thermal shock that may be caused during pretining	-5 collective assembly (VP, Convection..) / 1 microsection	-To avoid excessive solder (Component manufacturer recommendations) -Recommendation to verify absence of cracks in the ceramic at component level
Ceramic Chip Capacitors	Any ceramic of type 2 whatever assembly method to be used	Crack in the ceramic initiated at the end termination	Presence of crack in the ceramic from procurement		-Recommendation to verify absence of cracks in the ceramic at component level for parts from which procurement specification allow cracks. -Those cracks may propagate during assembly or at later stage
Chip capacitors	Size C1825 and bigger type 1 and type 2	Cracks in the solder joint	-CTE mismatch	5 assembly/5 microsections	To increase the solder stand off when possible only in case assembly without artificial stand off fail due to cracks in the solder joint
Chip package (capacitors, resistors, castellation ...)	Any size	Risk of poor wetting, damage of the part due to high solder duration...			It is not recommended to assemble with artificial solder stand off when no previous assembly verification failed due to cracks in the solder joint. Artificial stand off could be limited to parts that fail assembly verification due to excessive cracks in the solder joints. Artificial stand off is recommended for sensitive parts due to potential cracks in the solder. It is recommended to verify the assembly with and without artificial solder stand off (chip resistors bigger or equal to 1206, chip capacitors bigger or equal to 1825,...)

Stacked chip capacitors CH for through hole and SMT assembly		Crack in solder joint	-CTE mismatch with stiff terminals	3 assembled / 1 microsection	-Lap connection -To verify absence of cracks in the ceramic chip capacitors during microsectioning
Active component s	LCCs	Crack in the solder joint	CTE mismatch between PCB and component	5 assembly/5 microsections	-Degolding/ pretinning and soldering temperature used need to be compliant to the component manufacturer datasheet to avoid damage of the device, - To increase the stand off -Increase of stand off may not be sufficient and may cause poor wetting of the component termination underneath the device (risk of poor wetting due to high thermal dissipation), -Another possible alternative is to solder the device upside down and add gull wing terminations (need of verification in compliance with ECSS). In this case the change of solder footprint is needed. - To solder upside down and have long wiring implemented. -The assembly by hand when assembled upside-down using a solder iron requires to be verification tested to demonstrate presence of acceptable cracks in the solder joints AND absence of damage in the package due to thermal shock during assembly using solder iron.

Active components	LCCs upside down	Crack in the solder joint or in the ceramic	Mishandling or excessive thermal stress		-The assembly by hand when assembled upside-down using a solder iron requires to be verification tested to demonstrate presence of acceptable cracks in the solder joints AND absence of damage in the package due to thermal shock during assembly using solder iron.
Tantalum capacitors	CWR06	Crack in the device. Crack in the epoxy between the tantalum and the terminal.	Component technology	3 assembly/1 microsections	-It is recommended to use TAJ/ CWR packages other than CWR06as these parts are less sensitive to package damage. - To avoid not needed thermal stress on the device (e.g. pretinning)

	SMDs with a metal plane termination (eg. TO 276) (SMD0.5, SMD1, SMD2, SMD5C, SMD0.2)	Crack in the ceramic	CTE mismatch between PCB and component	5 assembly/ 3 microsections of each manufacturer	-Procurement of package with leaded terminations. - Assembly upside down using thermal adhesive and addition of wires or ribbons . -The assembly by hand when assembled upside-down using a solder iron requires to be verification tested to demonstrate presence of acceptable cracks in the solder joints AND absence of damage in the package due to thermal shock during assembly using solder iron. This configuration may not be adapted for high thermal dissipation need. -The verification of the assembly of the SMD0.5 is currently resulting to a high number of failures due to the presence of cracks in the ceramic. This has also been noted after reduced number of thermal cycles (less than 20). -Recommendation to perform a verification programme with limited temperature thermal range in order to reduce the CTE mismatch between the part and the substrate. Such reduced temperature range shall include the max and min operational and non operational temperature that could see the package during ground and mission phase.
	SMDs with ribbons assembled upside down	Crack in the ceramic	Component construction	5 assembly/ 1 microsection of each manufacturer	-Minimum degolding and pretinning temperature to be applied -Soldering with hot air the ribbons onto the terminals.

	SMD0.22	Crack in the solder joint	CTE mismatch between PCB and component	5 assembly/ 5 microsections of each manufacturer	-Artificial stand off -This package is similar to LCC package as metallization directly on ceramic.
	SMDs (eg. SMD0.2) with a non metal plane termination (termination plated directly on ceramic)	Crack in the solder joint	CTE mismatch between PCB and component	5 assembly/ 5 microsections of each manufacturer	-Pending of the manufacturer this package may be as SMD2 with metal terminals or with bottom terminations directly on the ceramic (similar to LCCs, chip capacitors…). -Artificial stand off
Oscillator	JLCC4 with bottom brazed terminals	Crack in the solder joint	CTE mismatch/ component design Failure due to excessive stiffeness in the leads that does allow any stress relief during environmental test	3 assembly/ 1 microsection of each manufacturer	-To wire the connection (functional impact shall be evaluated) -Use of an alternative package
Stacked devices	SOP from 3D+	-Crack in the solder joint -Unacceptable solder height at heel when hand soldering	CTE mismatch/ component design	5 assembly/ 3 microsections (in case cracks in the solder joint above 75% of the critical area the 5 components to be microsectioned)	-The parts can be procured with shortened leads that allow better solder flow and allow proper solder at heel fillet. -The non conformance of solder height or wetting at heel when assembled by hand can be avoided by the increase of soldering temperature (Max soldering T has changed from 280C to 310C max)

Stacked devices	SOP from 3D+	-poor staking on the sides when made on varnished parts -Possible degradation of the active part when staking is made on it	Identified in the document 3641_0790 from 3D+.		-Use of scotch tape tape on the side of the package is forbidden by the manufacturer -Parts can be procured varnished or not. The part shall be procured with sides staking not varnished when the part is staked on the side. -When active areas are on the four sides of the package the staking is forbidden.
Stacked capacitors	CNCXX	- poor wetting due to finish type 10 (Ag 98%)	Component technology	3 assembly/ 1 microsection	- To pre-tin the device
Photo transistor	Pill from micropac	- Cracks in the solder joint of the two small terminals	CTE mismatch between PCB and component	3 assembly/ 1 microsection	- To degold and pretin at temperature compliant to the component manufacturer recommendations. - Not to solder the bottom part on the PCB but to make a wiring connection.
Inductor	Coilcraft inductor AE235 type	Poor wetting of the terminals	Component technology	3 assembly/ 1 microsection	-To request coilcraft for additional cleaning of the terminal to remove the contamination from the enamel present on the terminal.
	Enamel wire	Short due to damaged enamel			-To inspect the wire to ensure absence of any damage in the insulation, -Procurement of a double enamel layer is recommended to reduce the risk of short, -Another prefered alternative is to add an insulation (kapton, brady label, filled varnish…) between the wire and the metallic part to avoid direct contact with metallic traces.

Bottom terminated chip device	QFN	Cracks in the solder joint	CTE mismatch between PCB and component	5 assembly/ 5 microsections	-To increase stand off -To ensure correct wetting by NDA.
Tantalum capacitor	CWR, TAJ, TBJ,…	Damage of tantalum			Wiring directly on the component termination shall not be performed due to possible damage within the component when the component is added to the design.
Chip capacitor type 2					Wiring directly on the component termination (eg. Component bonded on PCB and wiring connection made) and wiring made on the same PCB pad than the capacitor (modification after component assembly) shall not be performed due to possible damage within the component such as crack in the ceramic. It is recommended either to use a patch board with separate pads for the wiring (for addition of a capacitor) or to replace the capacitor during the wiring (modification applied after assembly)
Removal of conformal coating using solvent					Removal of conformal coating shall not be removing using as solvent.

Table 1: List of devices that have shown anomalies during the assembly verification as per ECSS-Q-ST-70-38C on PCB laminates.

Change logs:

Reference/ Issue	Changes implemented
ESA-TECQTM-MO-1143 issue 2	-New criteria for sensitive parts to be compliant to ECSS-Q-ST-70-38C Rev1 -Addition of the number of parts to be assembled and to be microsectioned per assembly configuration -Addition of recommendation to verify for chip capacitors

	type 2 the absence of cracks in the ceramic at procurement level -Addition of chip capacitor T1 with size bigger or equal to C1825 as sensitive part -Recommendation not to implement solder artificial stand off when not needed -Addition of staked chip capacitors as sensitive part -Addition of SMD0.22 and SMD0.2 as sensitive part when terminal in contact with ceramic package (similar termination than LCC) -Addition of QFN as sensitive part -Not allowed wiring on chip capacitors type 2 and tantalum chip components -Not allowed removal of conformal coating using solvent