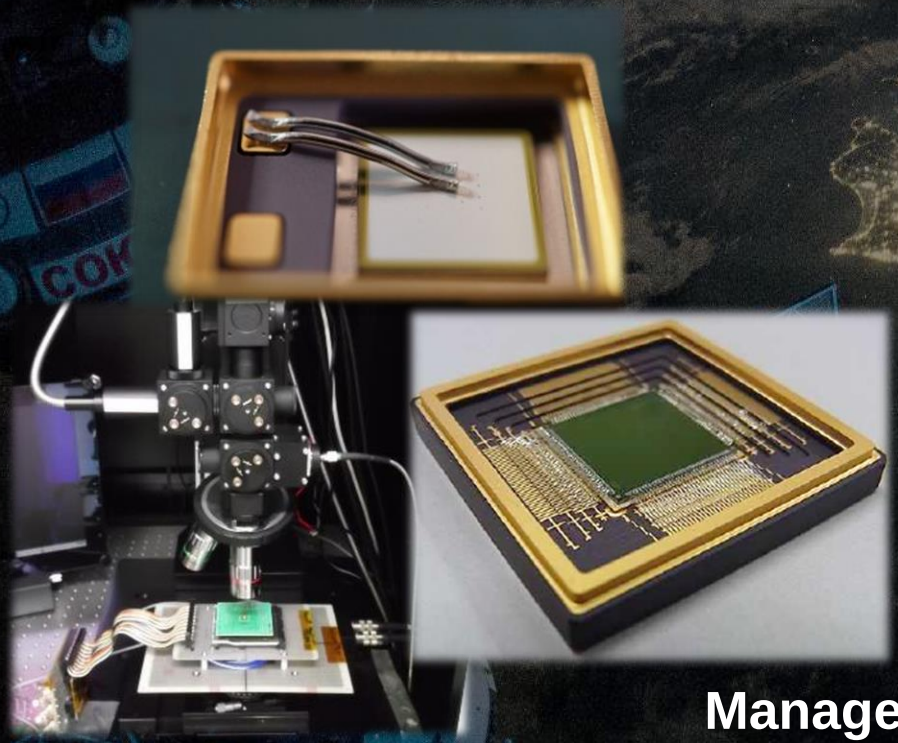
ESCCON 2021

JAXA's EEE parts R&D update



Mar. 9 - 11, 2021

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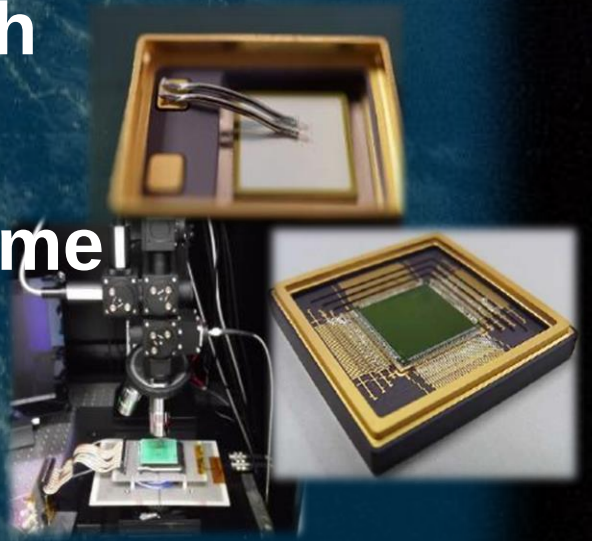
(shindou.hiroyuki @ jaxa.jp)

Manager for EEE parts technology research
R&D directorate, JAXA

Topics: On-going activities

- ✓ Nano-scale CMOS RHBD methodology for next generation ASIC/MPUs.
- ✓ Atom switch based non-volatile FPGA.
- ✓ Wide bandgap devices for space.
- ✓ Printed-wiring board with high heat dissipation structure.
- ✓ Brand new high-mix low-volume IC production.



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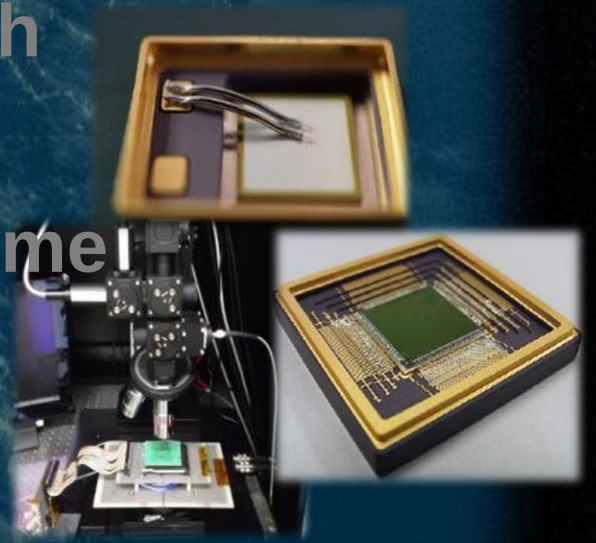
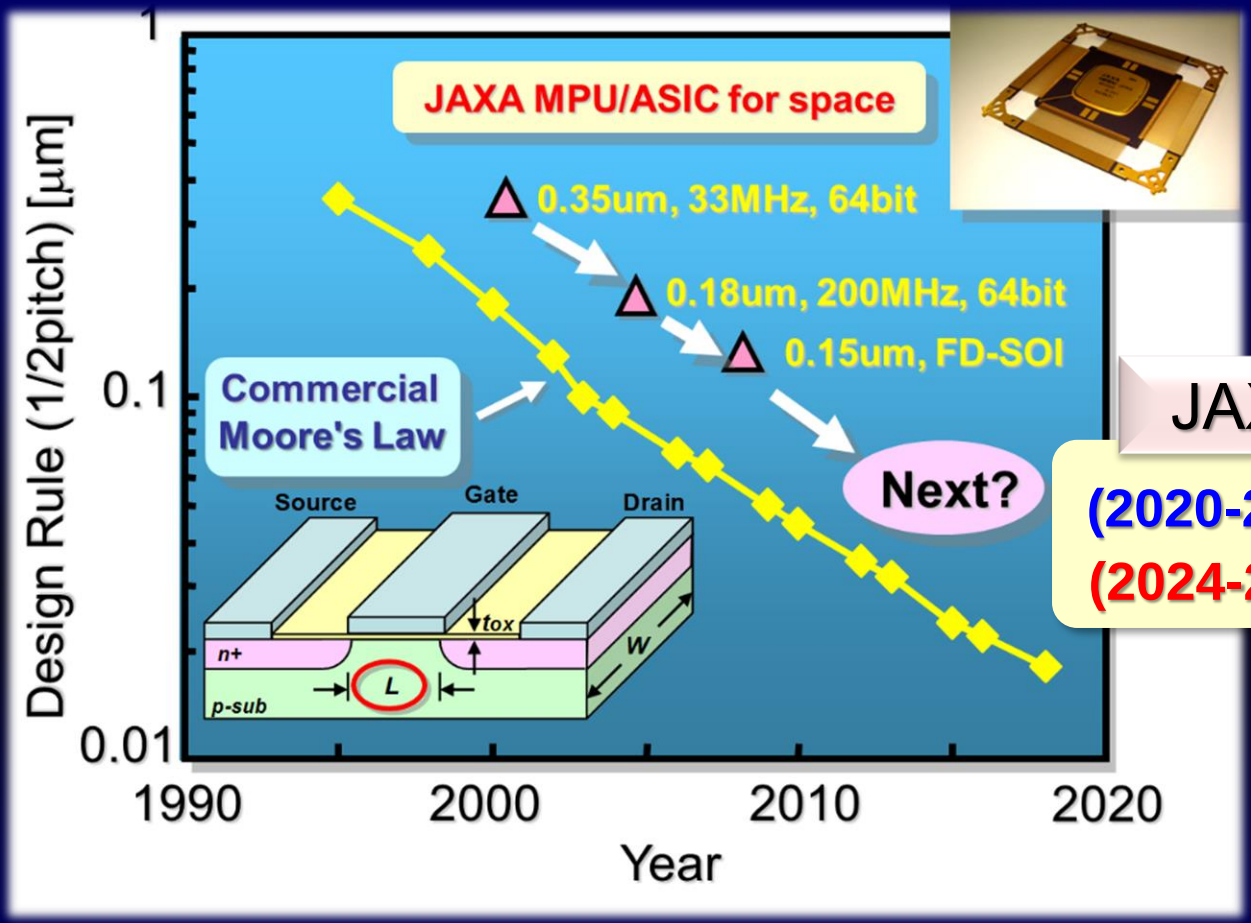


CMOS scaling and JAXA's future target



64bit Microprocessor
(0.15um CMOS-SOI)

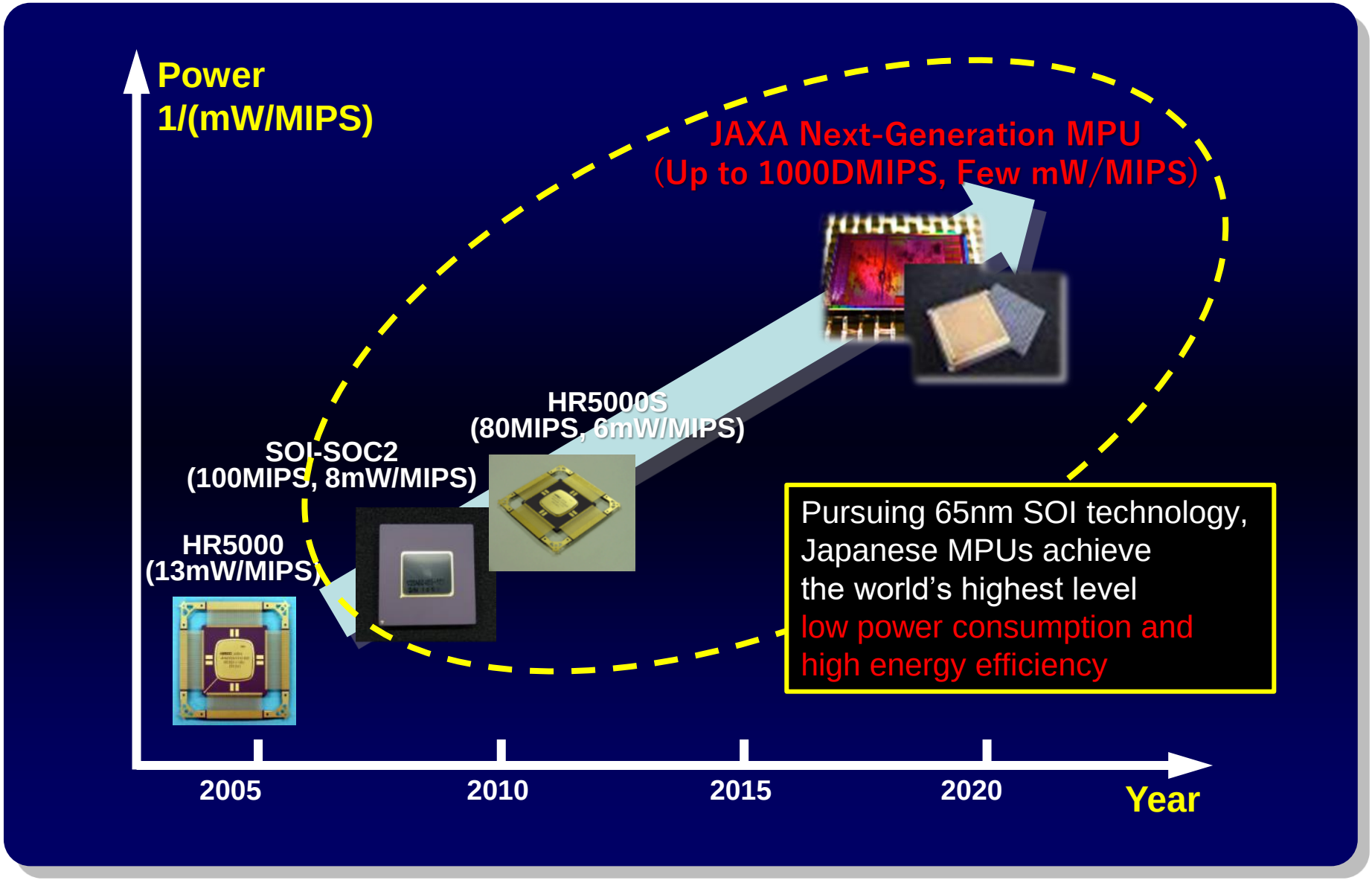
JAXA's R&D target

(2020-2021) : 65nm

(2024-2025) : 16nm Fin-FET

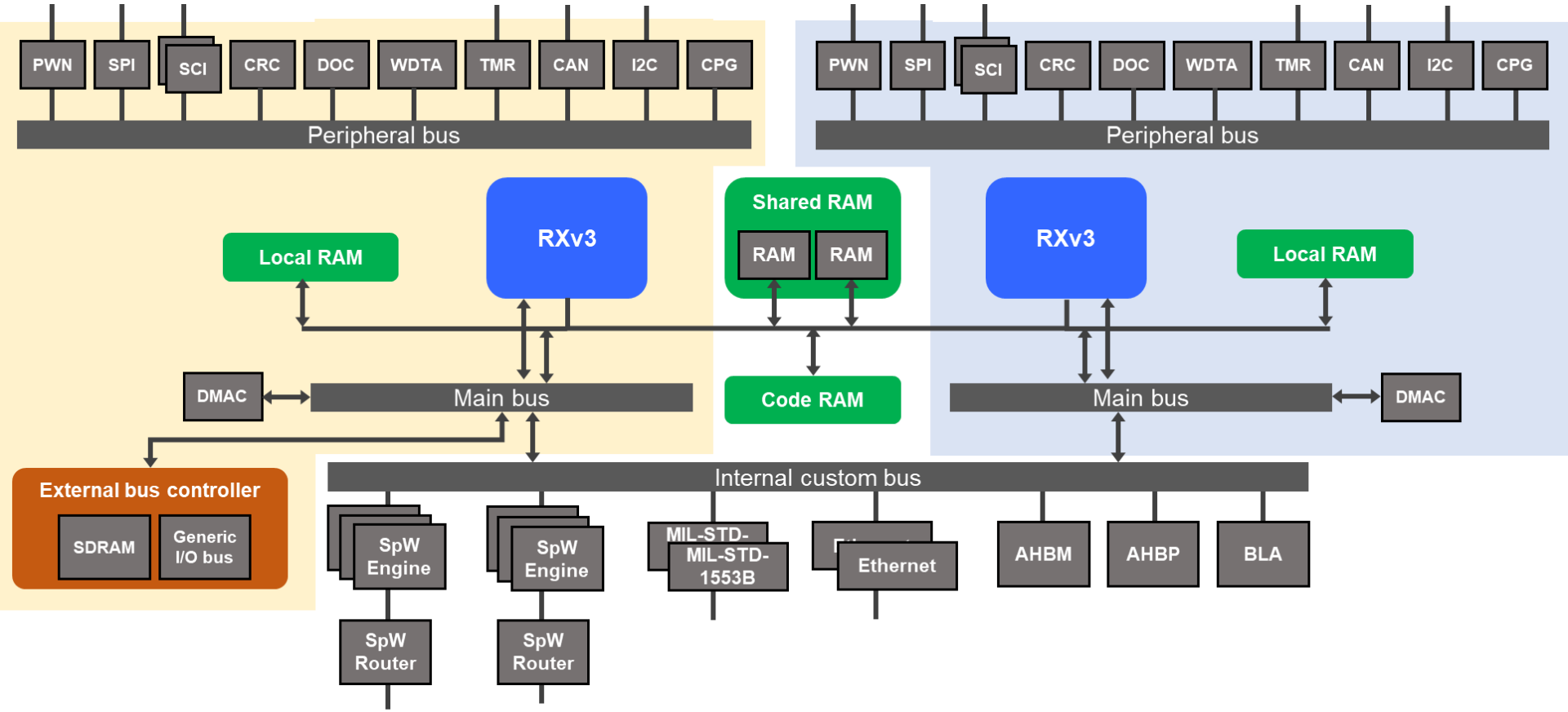
Recently, due to the requirements for higher density integration and device scaling, the logical circuits have been designed with <100nm design rule. SEE become serious problems for those integrated circuits.

Next Generation Microprocessor

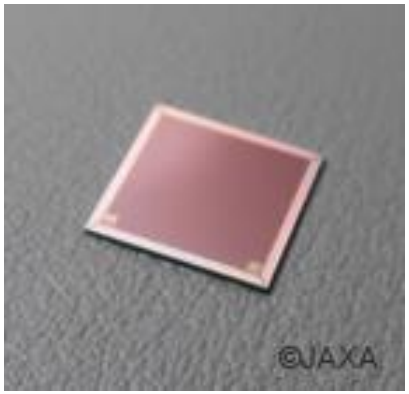


Next Generation Microprocessor

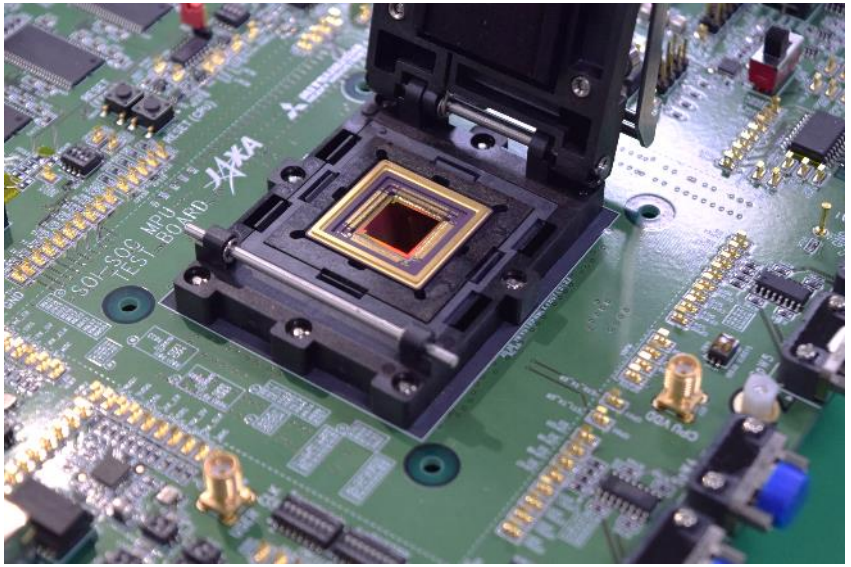
Function block diagram



Next Generation Microprocessor



Engineering Model Silicon die

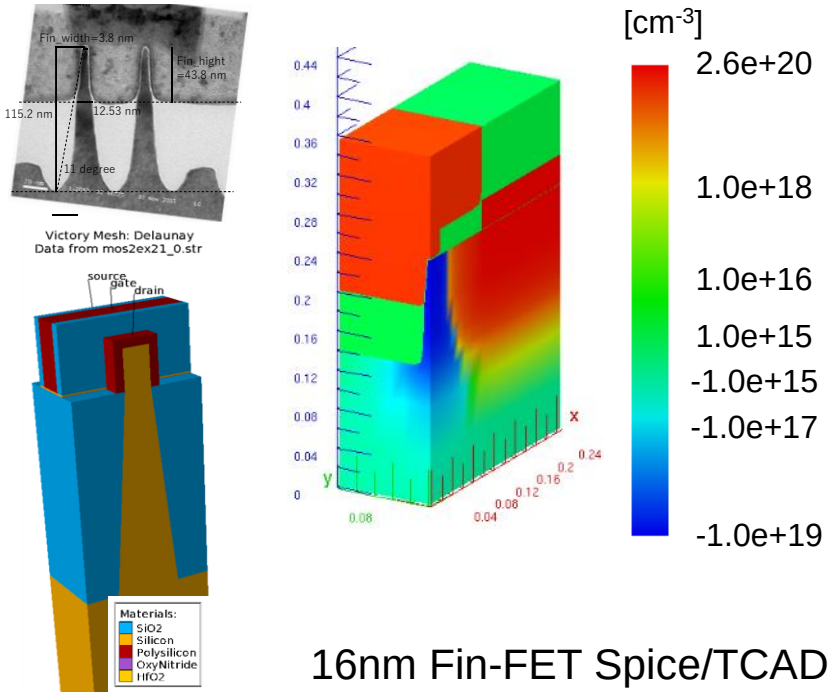


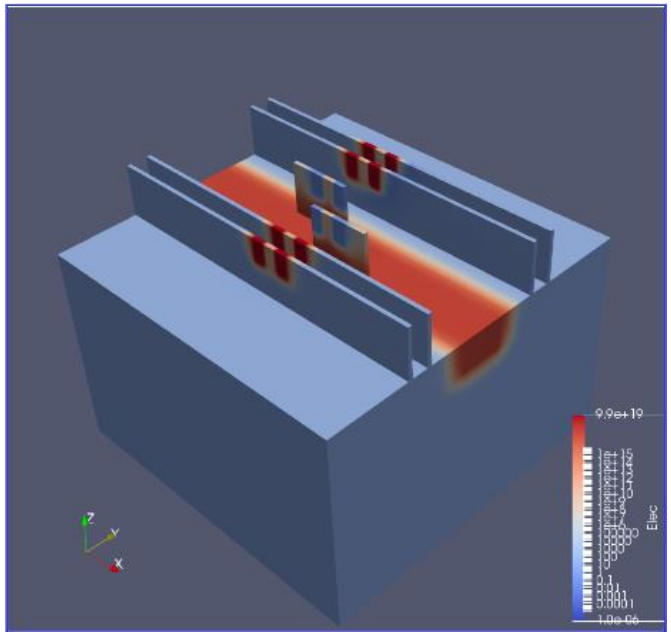
EM model evaluation results

Evaluation	Result	Comment
Frequency	280 MHz (max.) @PVT=Typical	Benchmark program (CoreMark)
Performance [CoreMark@250MHz]	800 ~ 1200	Depending on the operating configuration
Power Consumption	0.787 W @PVT=Typical	CPU0: CoreMark CPU1: Space Wire
Radiation	• SRAM w/ RHBD: 40 MeV/(mg/cm^2) • SRAM w/ EDAC: 40 MeV(mg/cm^2) • SEL: ≧ 80 MeV/(mg/cm^2) @ 125°C • EM-chip: ≦ 100FIT	

RHBD modeling for 16nm Fin-FET

Now we are constructing Spice/TCAD simulation model for 16nm Fin-FET technology to realize RHBD element circuit suitable for this technology. Now we are evaluating our new patent pending RHBD circuits by using TCAD simulation and test chips designed by JAXA.





16nm Fin-FET Spice/TCAD Simulation model.

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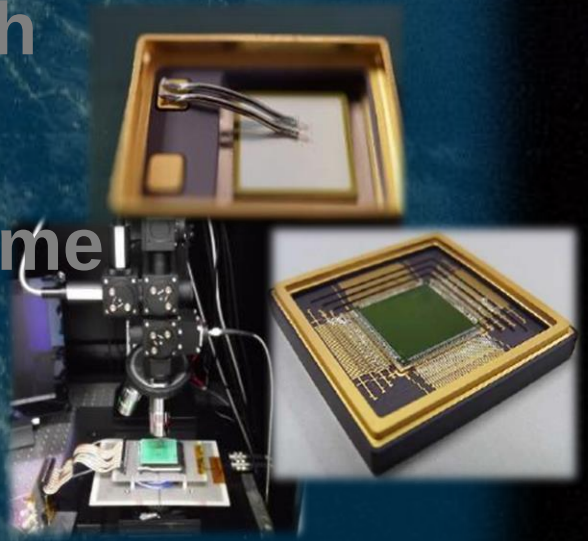
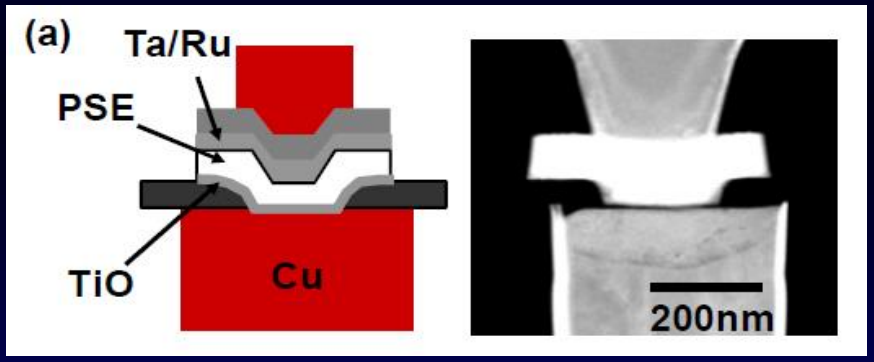
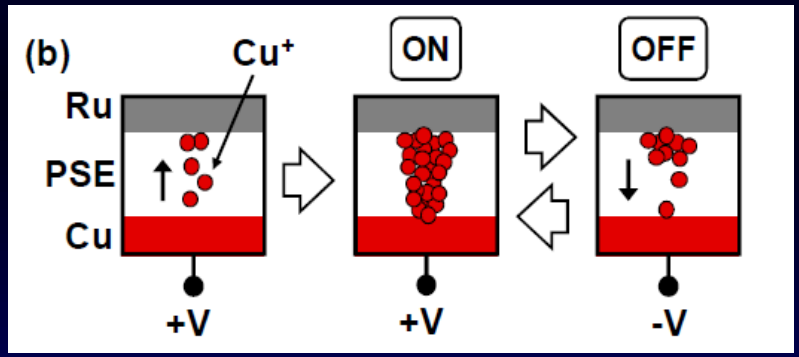


“Nano-bridge FPGA”
= Atom switch based non-volatile FPGA

Atom switch : A nano-scale switch which controls connection/disconnection of Cu^+ ion bridge electrochemically.

- ✓ Atom switch has features of low power, small area and non-volatility for the memory applications. In addition, it is also expected to replace a conventional SRAM/Pass-Tr. switch for a reconfigurable LSI.

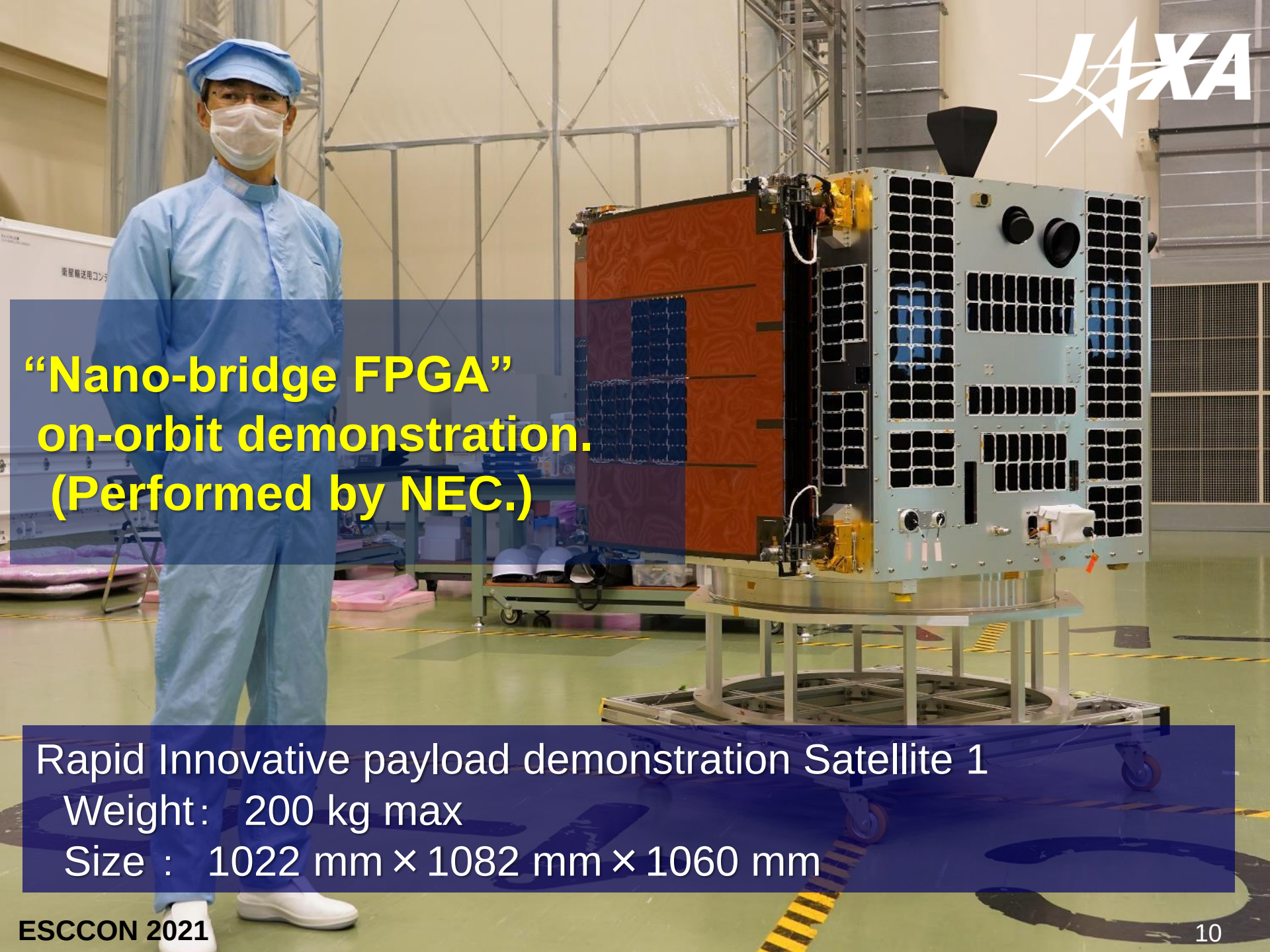




PSE: Poly Solid Electrode

Fig. (a) Cross sectional illustration (left) and TEM image (right) of atom switch cell, (b) Schematic diagrams of switching mechanism.

Ref: K. Okamoto et al., “Conducting mechanism of atom switch with polymer solid-electrolyte,” Tech. Dig. Int. Electron Devices Meet. IEDM, vol. 1, pp. 279–282, 2011.



“Nano-bridge FPGA” on-orbit demonstration. (Performed by NEC.)

Rapid Innovative payload demonstration Satellite 1
Weight： 200 kg max
Size ： 1022 mm × 1082 mm × 1060 mm

“Nano-bridge FPGA” on-orbit demonstration

Uchinoura Space Center
January 18, 2019, 9:50:20（JST）
Epsilon Launch Vehicle #4
Sun synchronous orbit

JAXA

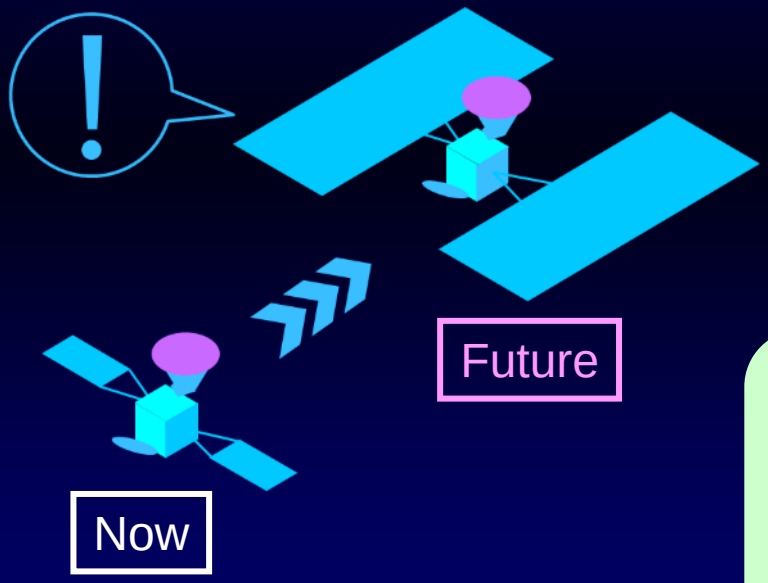
Nano-bridge FPGA

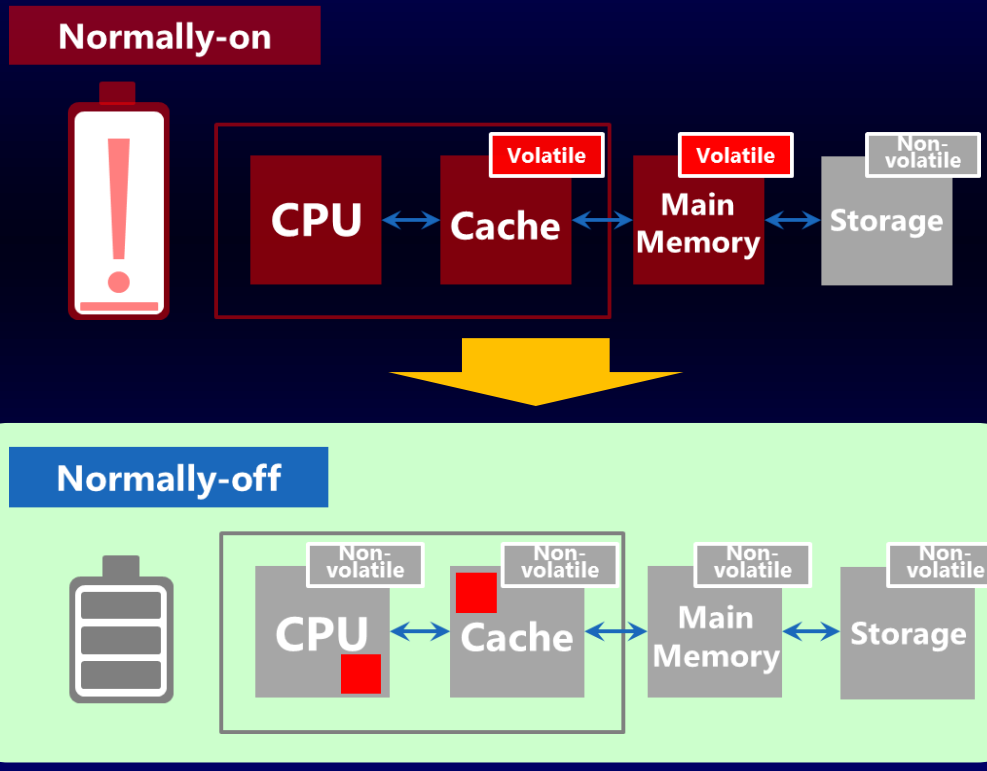
Photograph taken by monitor camera for paddle deployment confirmation. This image has been compressed by NB-FPGA and transferred by test radio wave.

JAXA

Atom switch will be a key technology to realize “Normally-off computing”

- ✓ Explosion of power consumption in orbit would be inevitable.
- ✓ Huge solar paddles and power cells will be required to keep the satellite systems in the near future.
- ✓ Normally-off computing: To shut the power down whenever not being used.





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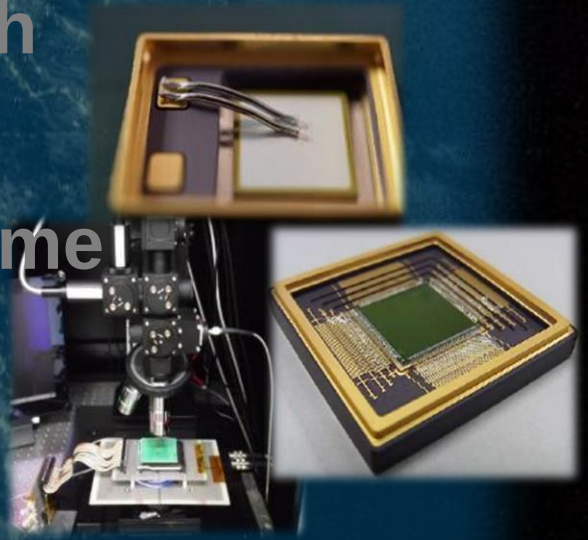
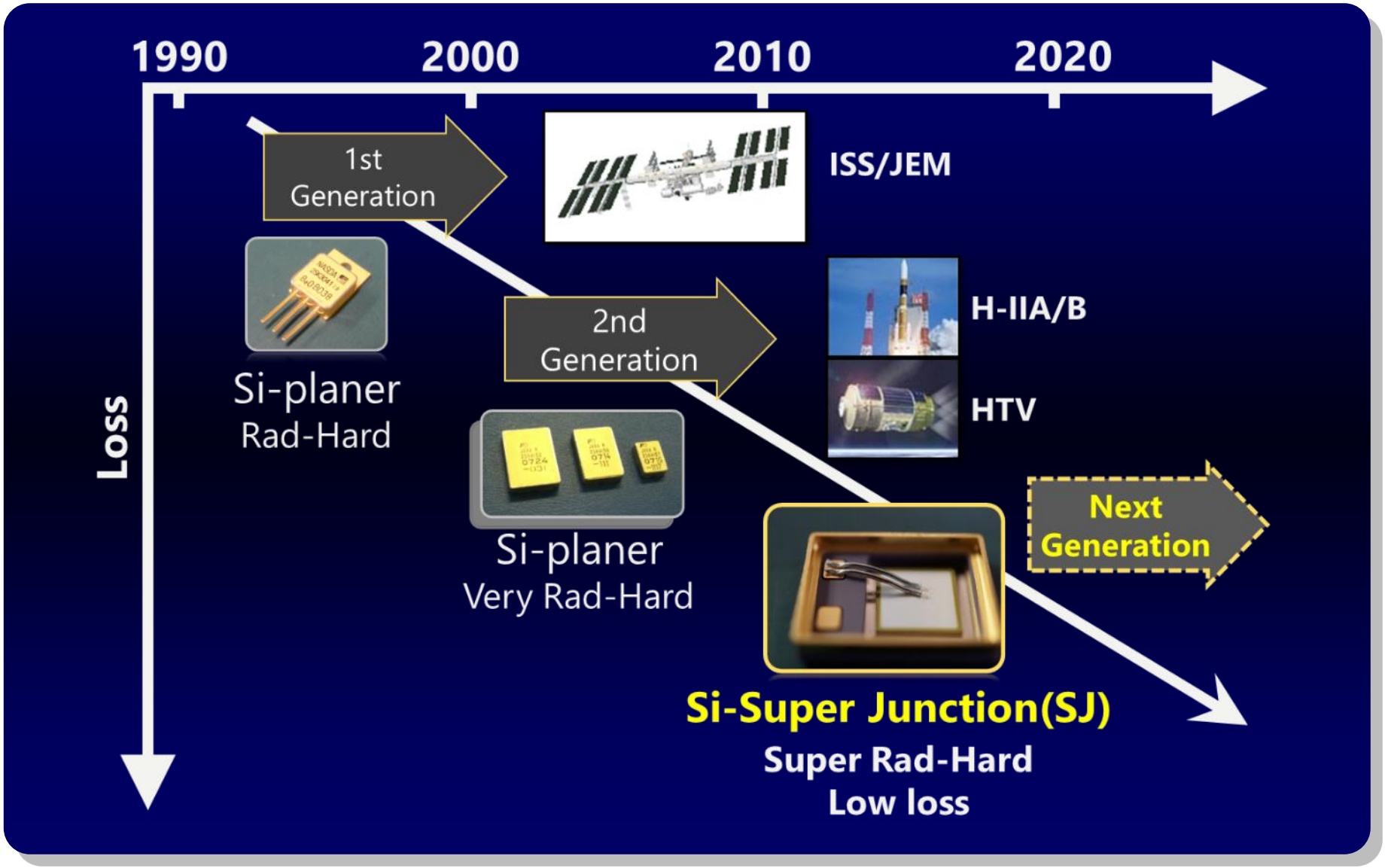


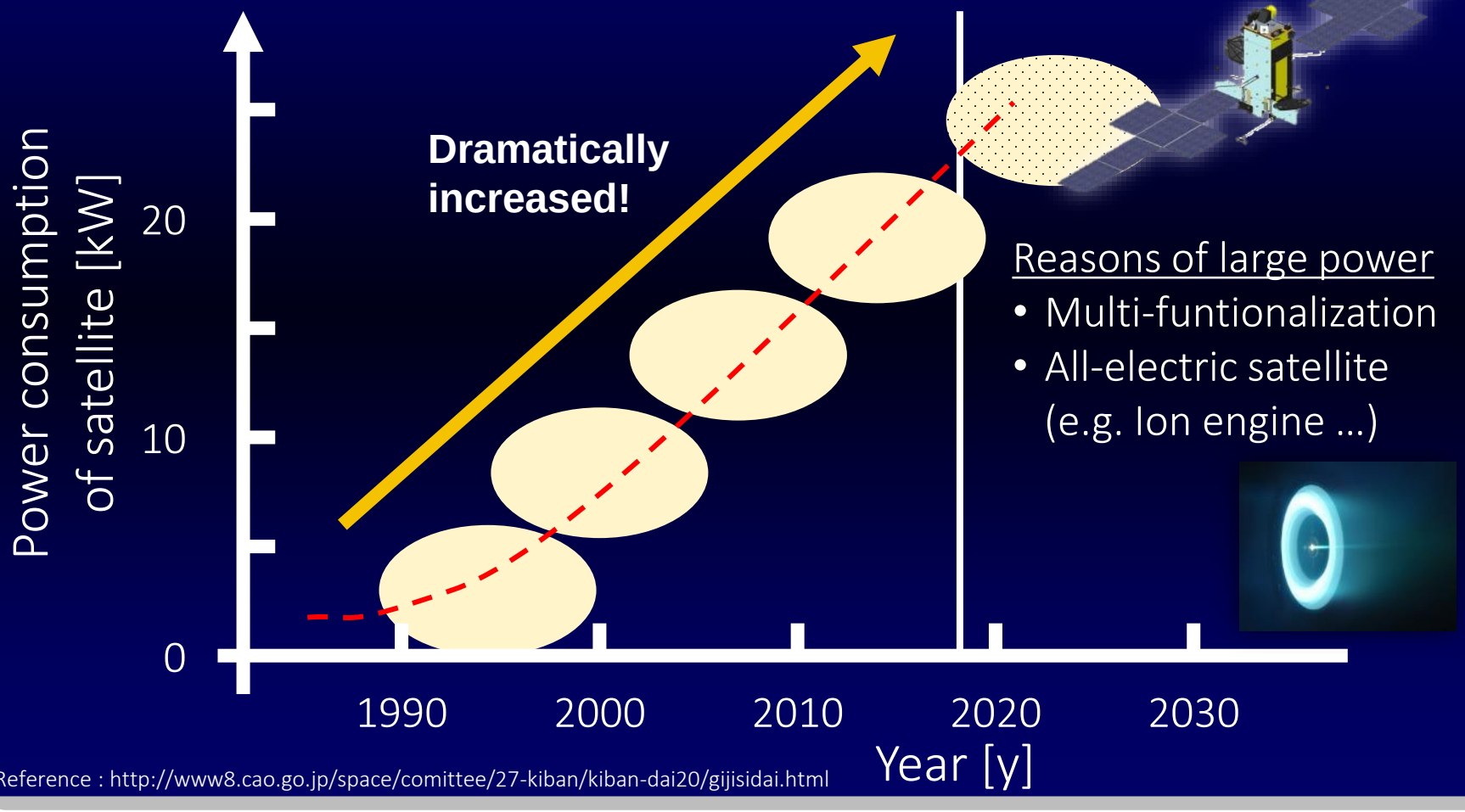
Power MOSFETs for space



Prediction of Satellite Power Consumption

As the satellite becomes multifunctional, power consumption tends to increase. GaN / SiC devices are strongly required !

However mechanisms about SEB/SEGR failure mode should be clarified.



Reasons of large power

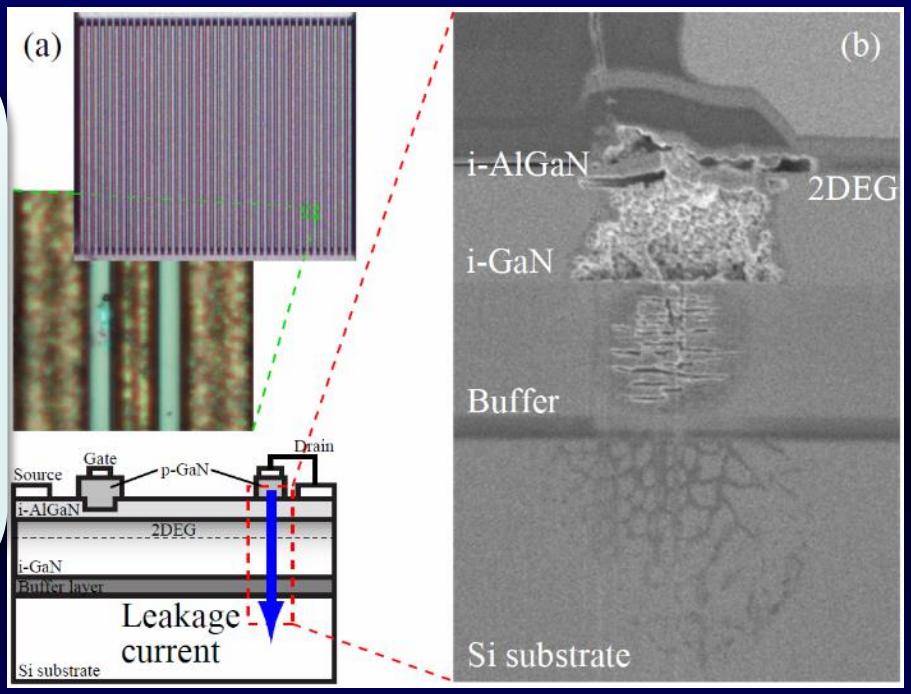
- Multi-funtionalization
- All-electric satellite (e.g. Ion engine …)

Reference : http://www8.cao.go.jp/space/comittee/27-kiban/kiban-dai20/gijisidai.html

Destructive SEE observed in GaN HEMT

Some types of new destructive SEE mode have been identified in GaN and SiC devices.

Now we are trying to analyze mechanisms about these failure mode to realize Rad-hard wide-bandgap devices.



Drain – Substrate leakage mode

E. Mizuta et al, IEEE Trans. Nucl. Sci., Volume 65, Issue 8, pp.1956-1963, 2018

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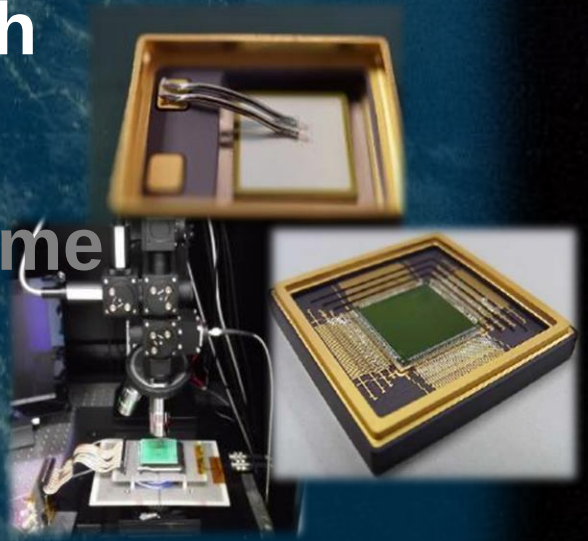
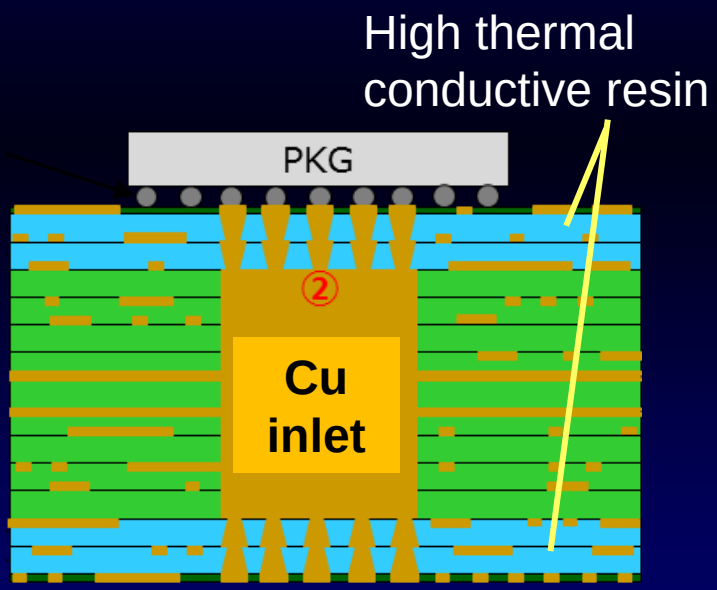
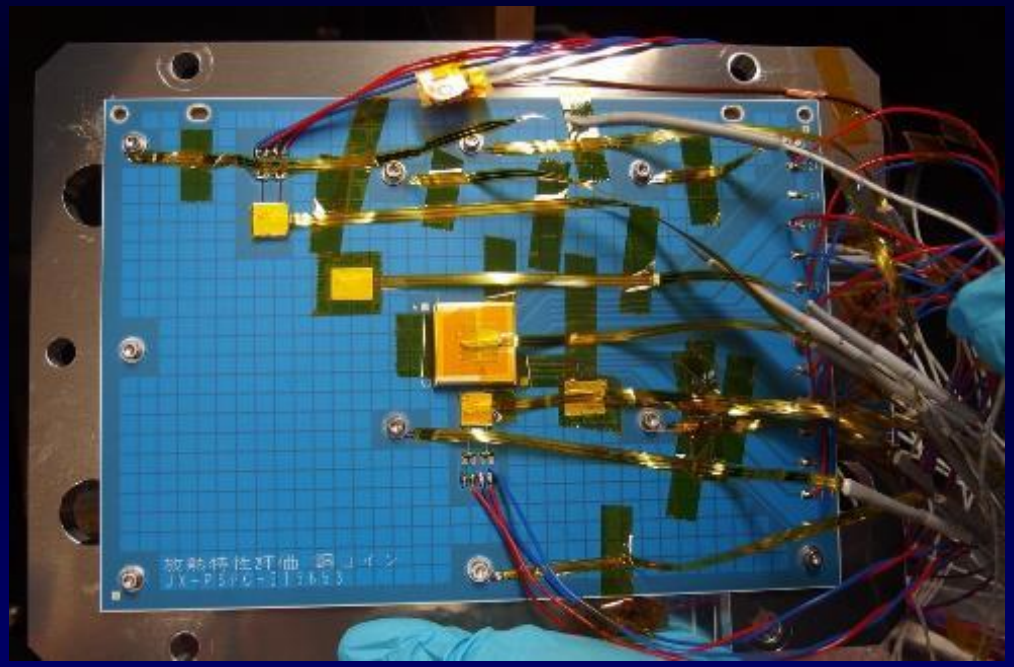


PWB with high heat dissipation structure

The feature of this PWB is a combination of usage of high-thermal conductive resin and metal foil or inlet. Preliminary thermal analysis was conducted to estimate the performance of heat dissipation of the partial model of PWB with several different structures. Now we are EM board evaluation phase to demonstrate the effectiveness of this structure.





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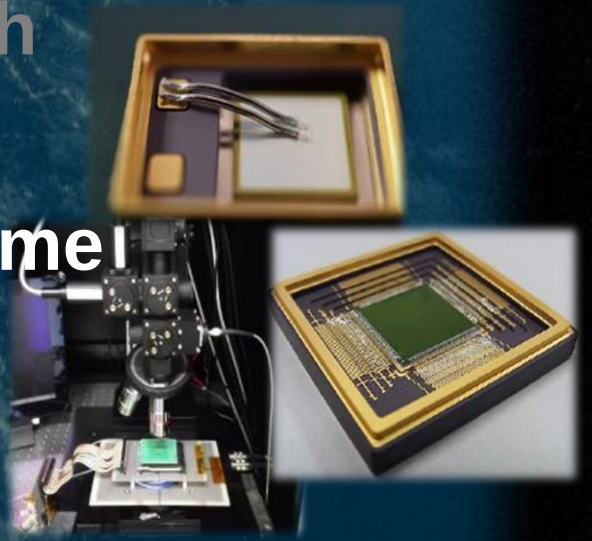


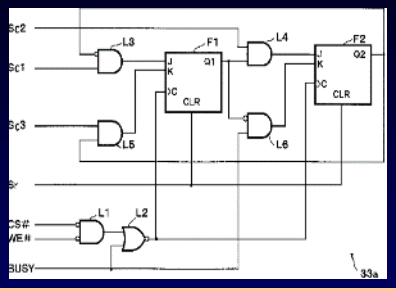
High-mix low-volume IC production

Feasibility study about a brand new high-mix low-volume IC production system based on “Minimal Fab”.

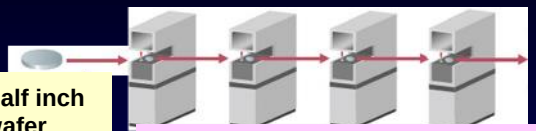
“Minimal fab” is the small quantity and multi-breed oriented technology which is developed by National Institute of Advanced Industrial Science and Technology (AIST).

Now we are demonstrating this brand new high-mix low-volume manufacturing system by prototyping several types of logic ICs.

Only 3-5 days !!



Circuit Design Data



Half inch wafer

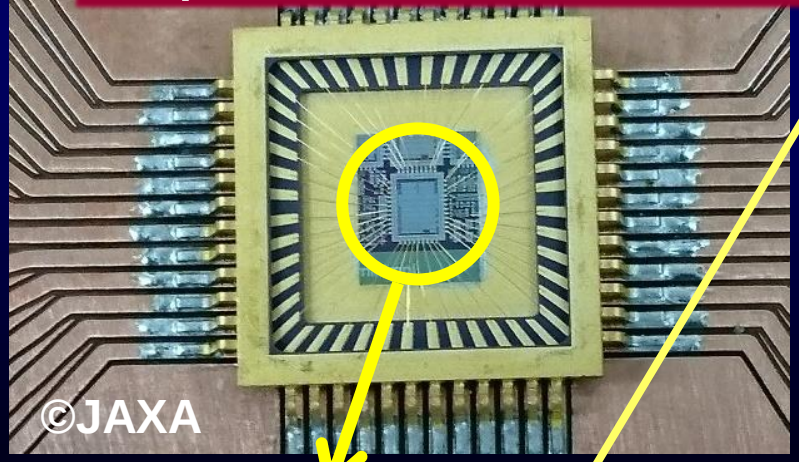
“Minimal Fab”

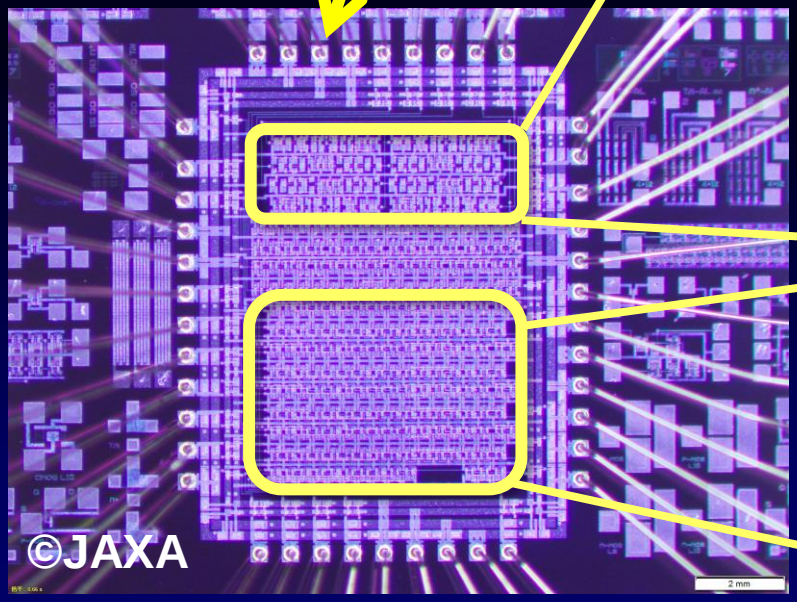
Half inch wafer Φ12.5mm

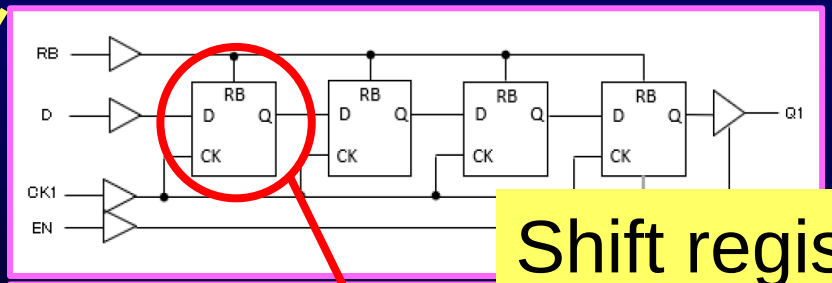
Minimal shuttle

High-mix low-volume IC production

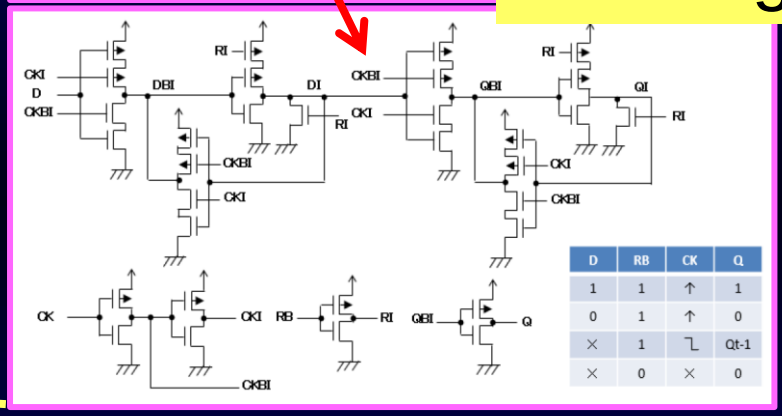
Expected functionalities have been confirmed.

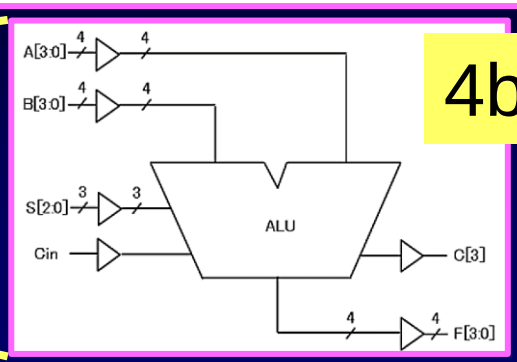






Shift register





4bit ALU


Thank you for your attention !
Any questions or comments?