



ESCCON 2021
ESTEC 11-13 March 2021

CNES Strategic Components activities

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CNES Budget

Actors

Key technologies and Supply chain

COTS radiation assessment

R&T –Microtechnologies, Components, Expertise axis

- **Activities on all electronic components & technologies**

- Survey & Assessment of COTS
- Innovative assembly & mounting solutions, PCB
- New technologies (UDSM, GaN, SiGe, optical connectors, etc.)
- Radiation studies : Environment, Effects on components, Test means ...
- Expertise lab

TRL
2→5

3M€/year

30 to 200k€/activity

RCS – Strategic Components

- **Key technologies Development, Evaluation, Market introduction**
- **Supply chain audit**

- ASICs (ATMEL-MICROCHIP, STMicroelectronics)
- FPGA NG (NanoXplore, STMicroelectronics)
- MicroProcesseurs (ATMEL-MICROCHIP)
- Data Conversion (E2V-TELEDYNE)
- Standard Products STMicroelectronics (diodes, transistors, LSI,...)

TRL
4→7

2,8M€/year

100k€ to 1M€/activity

COORDINATION

CTB (ESCC) → roadmaps

EDA / DGA

COSPACE/SGDSN

Multipartenariat (MOIs-F)

International (JAXA)

OBJECTIVES

European Non dependance

Europe's industrial competitiveness

Components offer adapted to customers needs (HiRel, NewSpace) to ensure manufacturers competitiveness

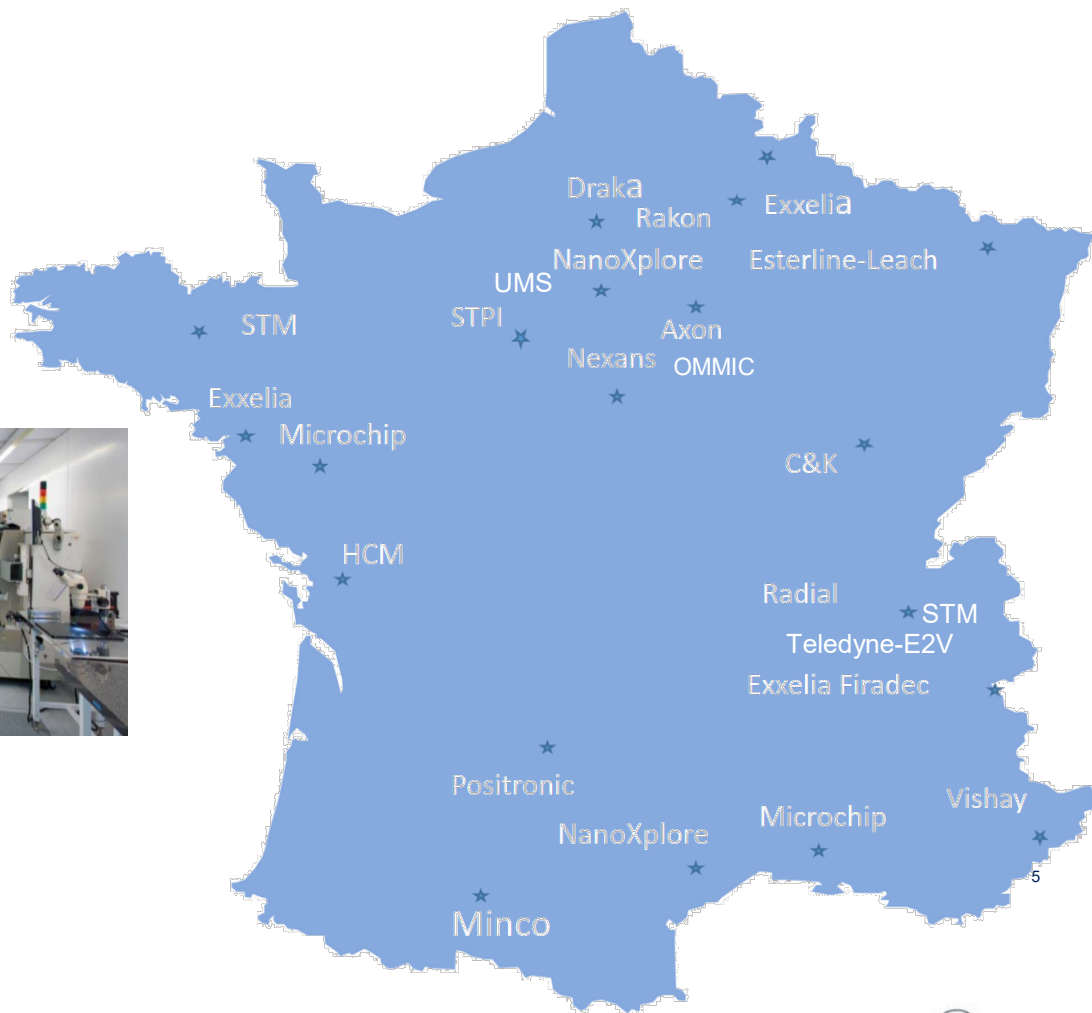
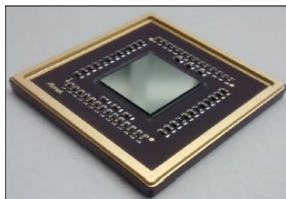
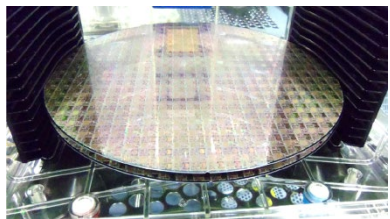
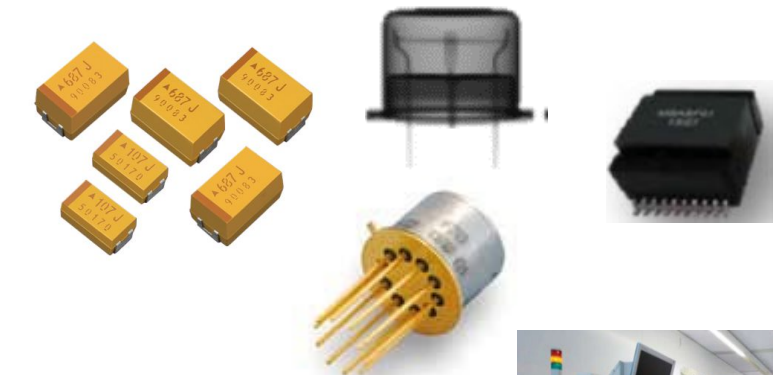
European/French sustainable supply chains for critical techno

Space qualification of existing commercial/automotive techno

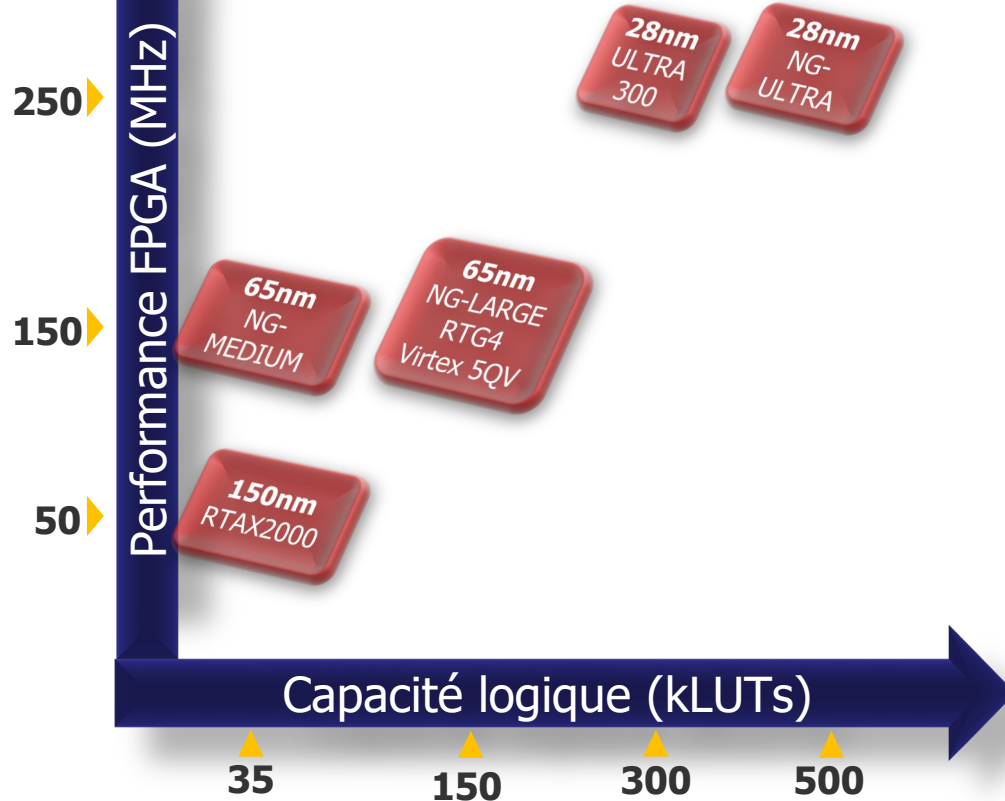
Performances & Key technologies

Components Manufacturers in France

➤ Wide range of products

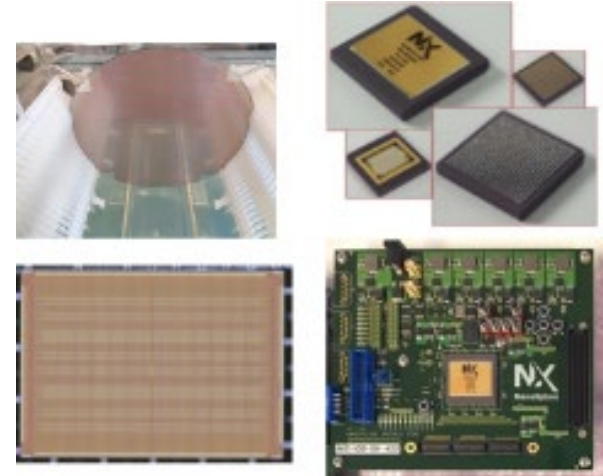
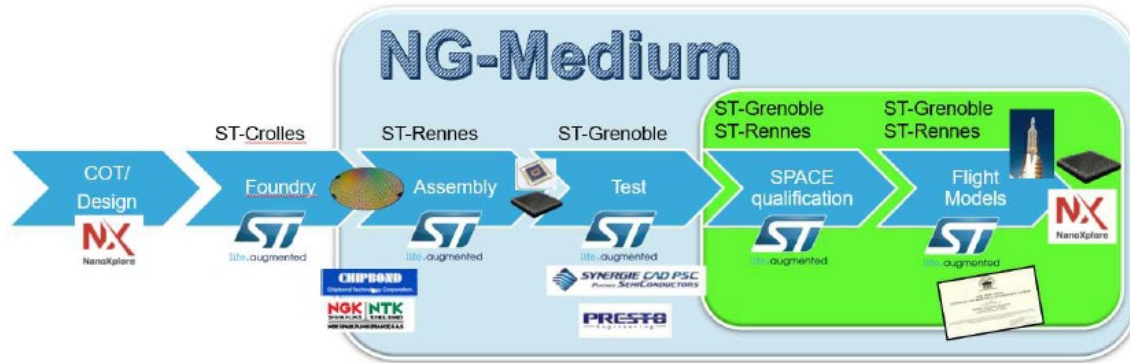


FPGA-NG : NanoXplore offer



		NG medium	NG large	NG ultra	ultra300
FPGA	DEVICE	NX1H35AS	NX1H140TSP	NX2H540TSC	NX2H300TSA
	TECHNOLOGY	CMos Planar	CMos Planar	FDSOI	FDSOI
	Process Lithography	65nm	65nm	28nm	28nm
	ASIC Gates	550 000	1 900 000	8 000 000	4 000 000
	LOGIC MODULES				
	Register	32 256	129 024	505 344	273 408
	LUT4	34 272	137 088	536 928	290 496
	Carry	8 064	32 256	126 336	68 352
	EMBEDDED RAM	2,8Mb	9,7Mb	33,9Mb	21,8Mb
	DPRAM	2 688	9 216	32 256	21 504
SoC	Core Register File	168	672	2 632	1 424
	Core Register File bits	168kb with ECC	672kb with ECC	1480kb Hardened	801Kbit Hardened
	CLOCK Domains / PLL	24 / 4	32 / 4	50 / 7	50 / 7
	ADDITIONAL FEATURES				
	SpaceWire PHY (8 IOBs)	16	20	20	20
	DDR PHY (11 IOBs)	16	20	20	20
	DSP Blocks (S)	112	384	1344	896
	SpaceWire link I/F 430 Mbps	1	1	1	1
	SERDES Tx/Rx (T)	-	24	32	16
	Hard IP Processor core (P)	-	1	4	-
IOBs	SoC Peripherals (C)	NO	NO	YES	NO
	ADC / DAC (A)	-	-	-	4 / 4
	DESIGN SECURITY	NO	NO	YES	YES
	INPUTS/OUTPUTS	374	674	740	544
	I/O Simple Bank	5	14	4	4
	I/O Complex Bank	8	10	10	10
	I/O Service Bank	1	1	1	1
		-	-	1	2
		-	-	2	1
		-	-	-	-
PACKAGING	PACKAGES	4#	3#	3#	4#
	CQFP-352	192	-	-	TBD
	CLGA-484 / CCGA-484	-	-	-	TBD
	PBGA-484	-	-	-	TBD
	CLGA-625 / CCGA-625	374	-	-	544
	PBGA-625	374	-	-	544
	CLGA-1752 / CCGA-1752	-	674	740	-
	FCBGA-1752	-	674	-	-
	FCBGA-1760	-	-	740	-
		-	-	-	-

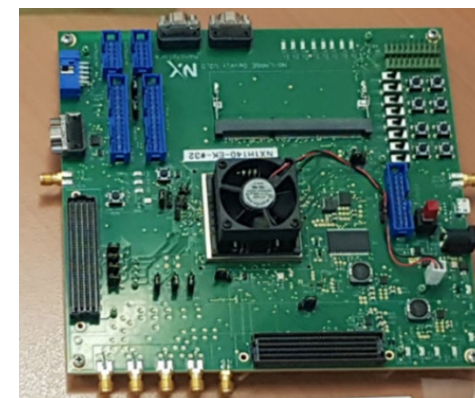
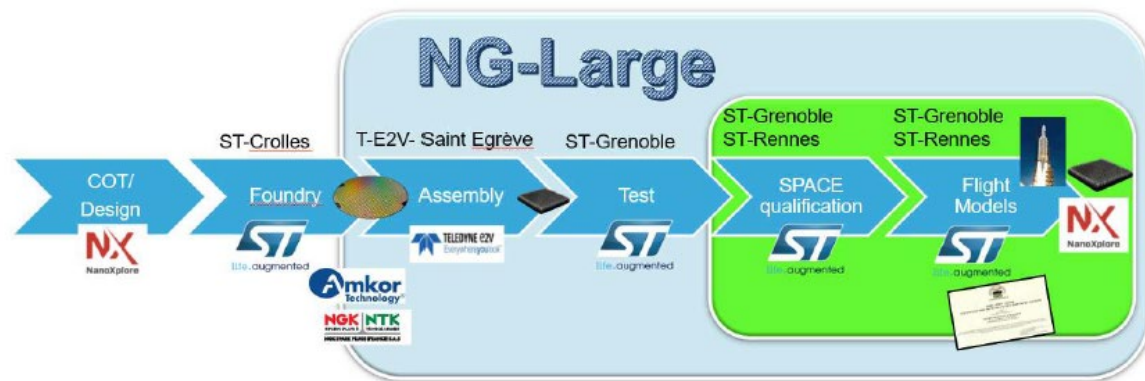
- Rad-Hardened by design SRAM-Based FPGA
- NX design, C65SPACE ST techno, CQFP-352 & CCGA-625
- Supply chain :



- CQFP-352 Flight models available

- Rad-Hardened by design SRAM-Based FPGA
- NX design, C65SPACE ST techno, CCGA-1752

- Supply chain :



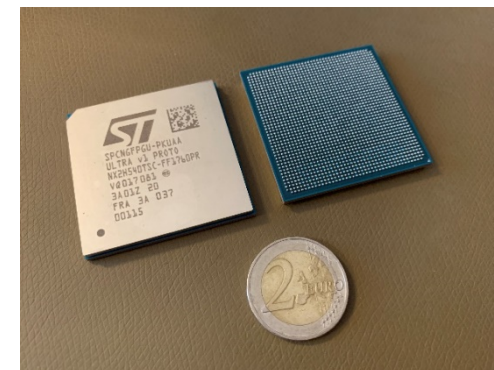
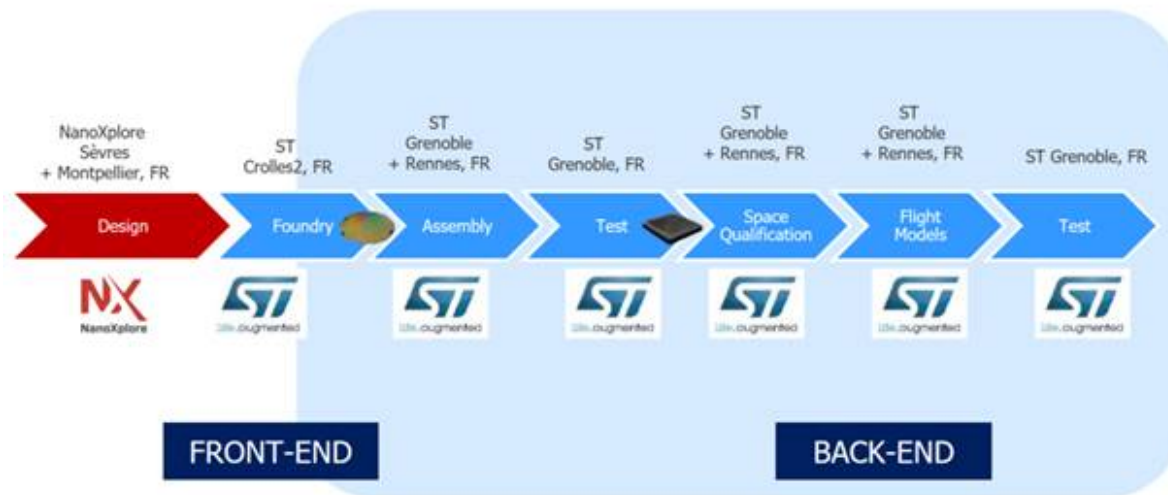
NG-LARGE Eval kit

- Eval Kit bring-up done
- Derisking Hermetic Flip-Chip assembly : Good results

→ Next : Qualification (H2020 OPERA)

- Rad-Hardened by design SRAM-Based FPGA
- NX design, ST 28FDSOI techno, ST Non-hermetic Flip-chip BGA1752
- Supply chain :

The NG-ULTRA is based on SME technology from NX but 100% industrialised by a fully trusted space supply chain from ST



➤ Development strategy with 2 Tape-Out:

➤ NG-Ultra V1:

- Launched in fab in February 2020,
- **First prototypes received on September 21st,**
- **Bring-up on-going by NX/ST, CNES, end-users**

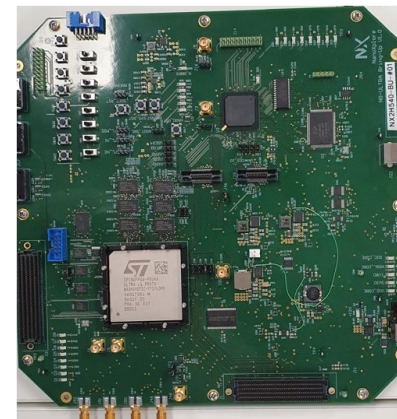
➤ NG-Ultra V2:

- To be launched in fab in Q2/2021,
- **FM equivalent (screened parts): July 2021**
- End of Qualification:
 - Organic Flip-Chip FF1752: Q1/2022
 - Ceramic hermetic Flip-Chip CCGA-1752: Q2/2022

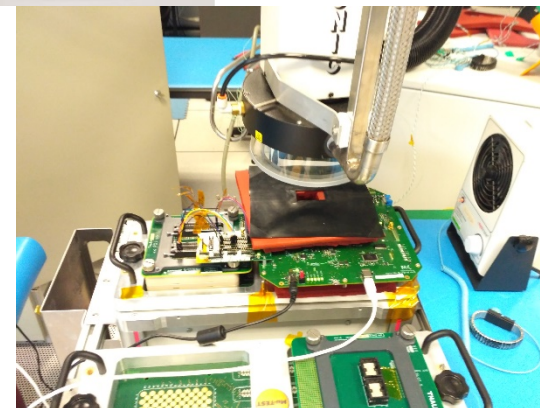
➤ Derisking Non Hermetic Flip-Chip assembly in progress

➔ Next :

- FPGA Programming Tools improvements
- NG-ULTRA Qualification (ARTES & H2020 HERMES)
- NG-ULTRA-300 intermediate capacity : Tape-out in Q1/21



CTB RM : Si17



NG-ULTRA Eval kit during CNES bring-up

CTB RM : Si115

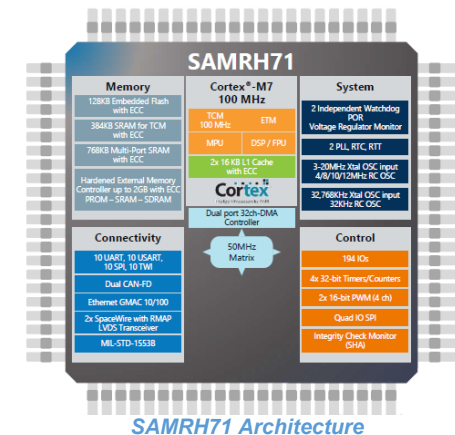
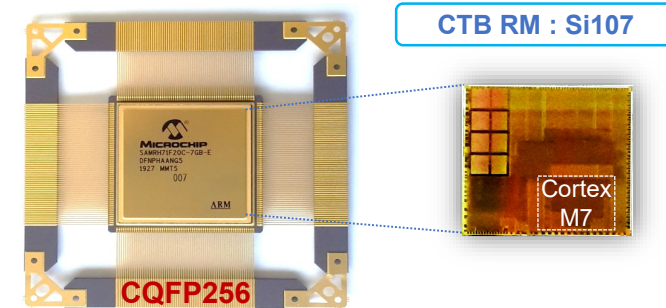
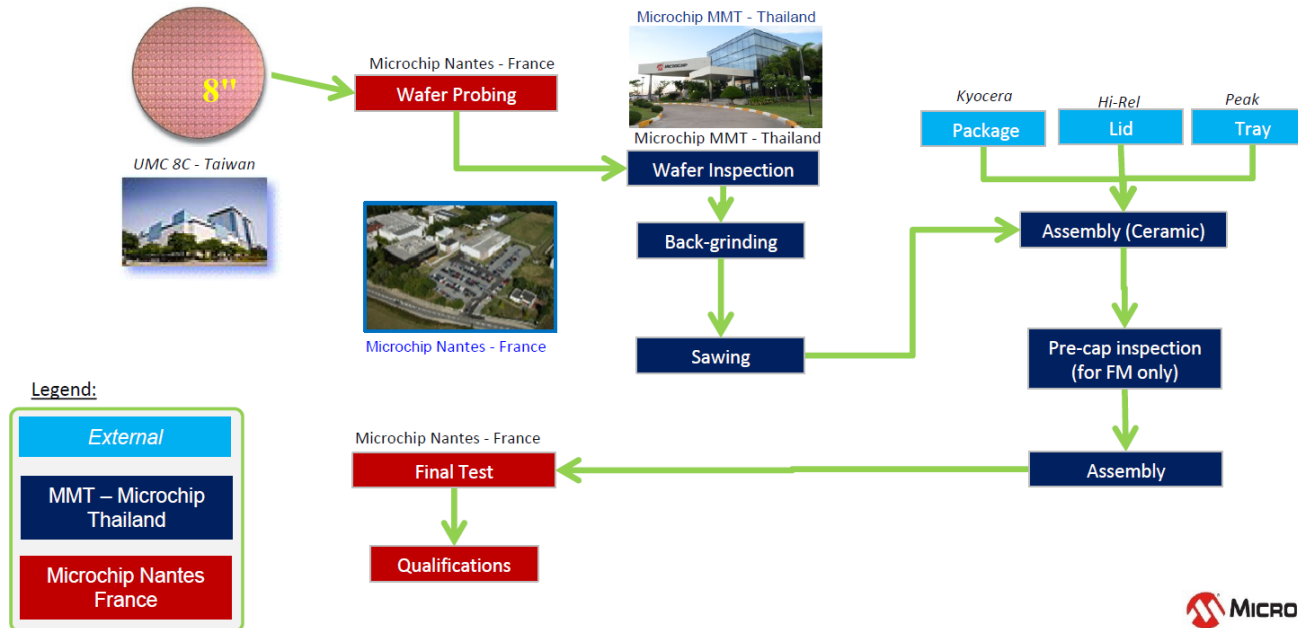
CTB RM : Si18

CTB RM : Si72

Microchip Microprocessors



- **SAMRH71 : First Rad-Hard by design ARM Cortex M-7μP**
- **MCHP design, 150nm ATMX150RHA techno, CQFP256**
- **Supply chain :**



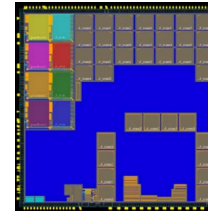
- **ESCC evaluation completed : Good results**
- **Flight models available**

Radiations
TID 150krad (Flash limited to 20krad)
SEL immune up to 62 MeV
SEU LET >20Mev.cm2/mg (Xsection <10-9 cm2/word)

→ Next :

- SAMRH71 in plastic version

CTB RM : Si107



- SAMRH707 development and evaluation (ESA)
- Next generation multi-core ARM Rad-Hard μ P development on UDSM technology

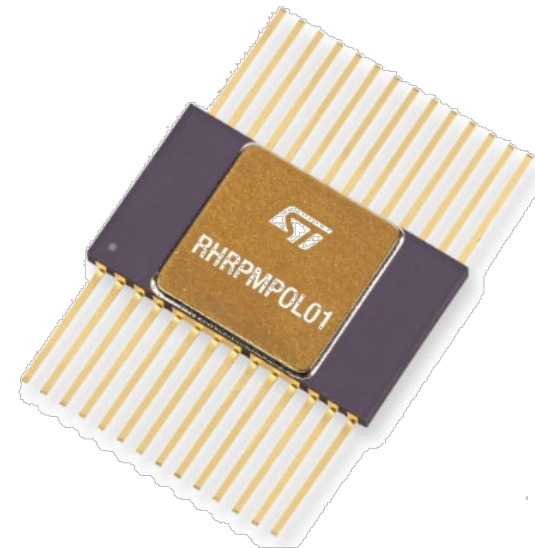
CTB RM : Si99, Si100

CTB RM : Si109

➤ **RHRPMPOLS01 : Rad-hard 7A point-of-load synchronous step-down regulator**

ESA contract for product development ; CNES contract for ESCC evaluation

- ❖ Monolithic silicon step-down regulator based on **BCD6s-SOI** technology
- ❖ 3V to 12V input voltage range (radiation performance guaranteed at **VCC up to 7 V**)
- ❖ **0.8V** to (0.85xVIN) output voltage range
- ❖ **Up to 7A** output current
- ❖ Integrated N-channel MOSFETs ; overcurrent & overvoltage protection
- ❖ **Flat-28 CuW** hermetic package
- ❖ **Radiation report available on demand :**
 - Total ionizing dose up to **100krad** ; **ELDRS-free**
 - **SEL-free** up to 70MeV/mg.cm² (@ VCC up to 7V)
 - **SEU-SEFI** characterized up to VCC=7V
 - **No performance degradation** due to **SET**
- ❖ **QML-V qualified : SMD 5962-20208, Flight models available**



Designed to supply FPGA, DSP, MCU and ASICS for space use

Teledyne E2V- Direct conversion solution

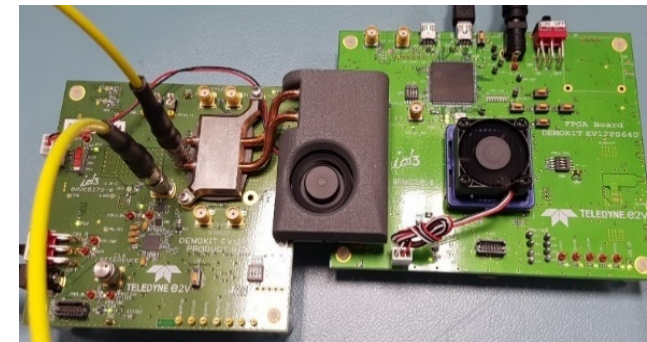
➤ Proof-of-Concept of Direct Conversion to address new challenges :

- To design a data converter up to Ka band with more than 6.5 effective bits (ENOB at FS) with a very low power consumption
- To develop Die-Package Co-design skills
- To realize first SiP in Non-hermetic SiP Flip-chip assembly
- Based on new TH design + 2 EV12AQ600 ADCs
- **Validation of the Concept on Eval kit**

➤ Next : AS940 Direct conversion module

- Design in progress → CDR : Q2/21
- Performances to reach : Ka BW, 12Gsps, 2.5W...

➤ Supply chain :



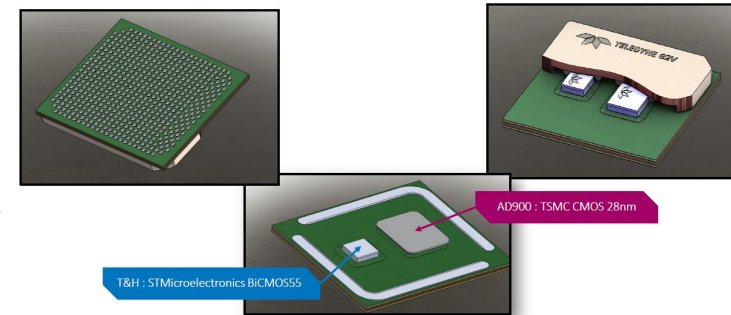
PoC Eval kit during CNES bring-up

CTB RM : Si74

CTB RM : Si06

AS940 : What it looks like

First 3D views

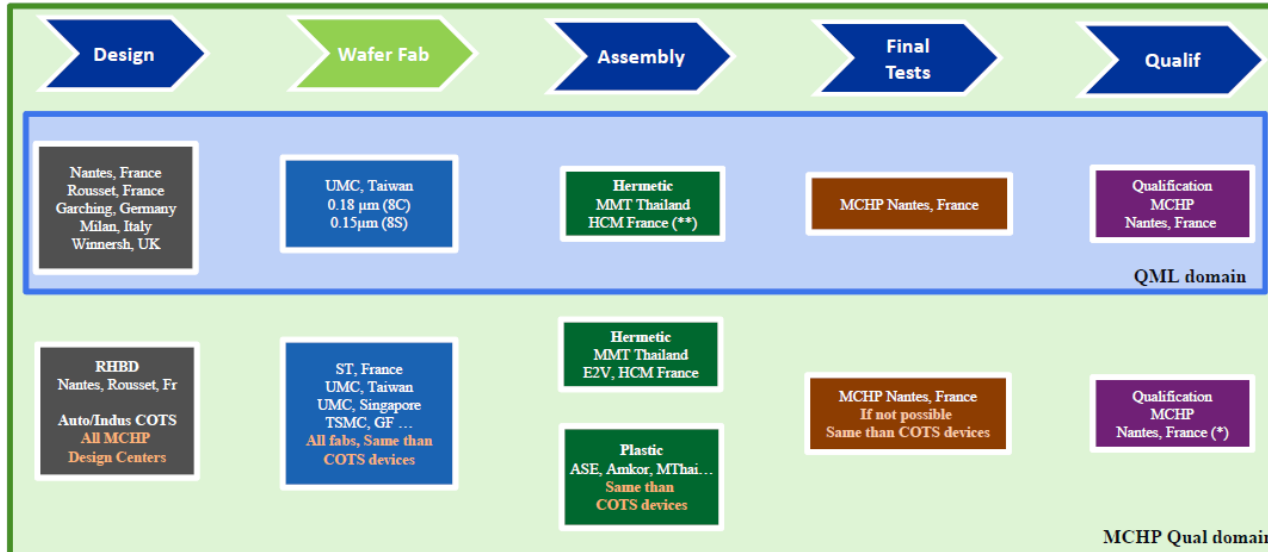
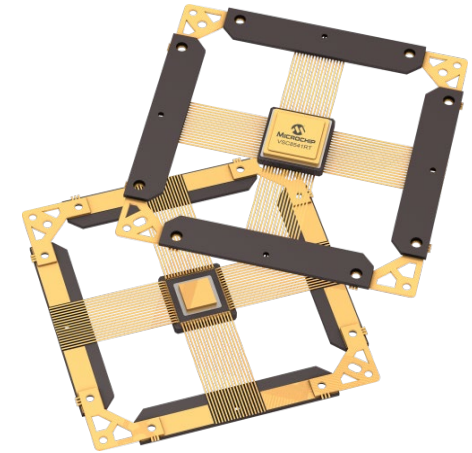
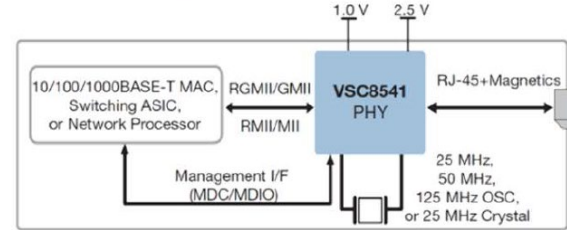


New Space : Microchip Rad-Tol Ethernet solution

- Rad-Tolerant products from MCHP COTS catalog : Low cost offer
- Radiation evaluation & Qualification up to « New Space » levels (SEL free, 50krads min)
- Qualification according Space standards

- **VSC8541RT Mbit/Gbit Ethernet PHY**
→ Samples & Flight Models available

- Supply chain :



- Rad-Tolerant products from ST : Low cost offer
- Radiation evaluation & Qualification up to « New Space » levels (SEL free up to 45MeV/mg.cm², 50krads)
- Qualification according ST specification

❖ LOGIC:

- LEOAC14, 00, 244 Flight Models available
- Coming soon : LEOAC74,32, 08

❖ LVDS transceiver

- LEOLVDSRD FM available

❖ Analog to Digital Converter

- LEOAD128 FM available

❖ Power supply

- Next : LEO3910 & LEOPOL01



CP	Function
LEOAC14	HEX SCHMITT INV
LEOAC00	QUAD 2-in NAND
LEOAC244	BUS TRANSCEIVER
LEOLVDSRD	LVDS <u>Dver/Rver</u>
LEOAC74	DUAL D FLIP FLOP
LEOAC32	QUAD OR
LEOAC08	QUAD 2-in AND



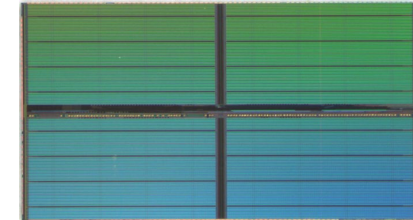
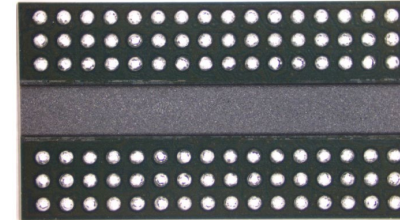
➤ Radiation assessment of DDR4 COTS Memories

➤ SEE and TID tests

	Référence	Description	Boîtier	Mfr.
1 bis	MT40A256M16LY-062E IT:F	DDR4 4Gbit (x16)	FBGA-96	Micron
2	K4A4G165WE-BITD (CL19)	DDR4 4Gbit (x16)	FBGA-96	Samsung
3 bis	H5AN8G6NCJR-VKI	DDR4 8Gbit (x16)	FBGA-96	Hynix
4	NT5AD256M16D4-HRI (CL19)	DDR4 4Gbit (x16)	FBGA-96	Nanya
5	MT40A512M16JY-075E AIT:B	DDR4 8Gbit (x16)	FBGA-96	Micron



- Most of the parts are SEL free
- SEU sensitive, Stuck bits observed
- SEFI sensitive
- Good behaviour under TID up to 100Krad



→ Detailed Results will be published at RADECS21

➤ Radiation assessment of FPGA SoC COTS

- See CNES presentation « Feedback on radiation test on SoC Components which can be very challenging regarding the complexity of such devices »

➤ SEE Radiation assessment of GH15-10

- GH15-10 is based on SiC substrate and is well-suited for a wide range of applications up to 35GHz. It enables the design of high power, high linearity and high PAE products.

On state : 32.5V @ 200 mA/mm demonstrated

Off state : 47.5V demonstrated: probably limited by the capacitor placed on the drain of the DEC

CTB RM : MW054

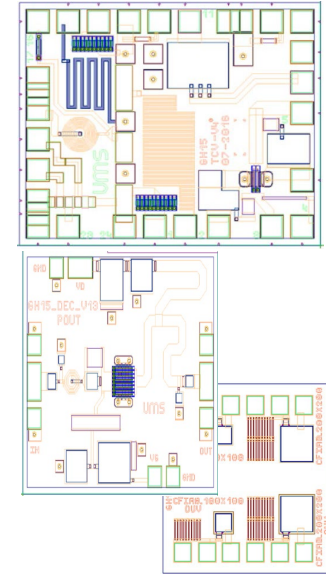
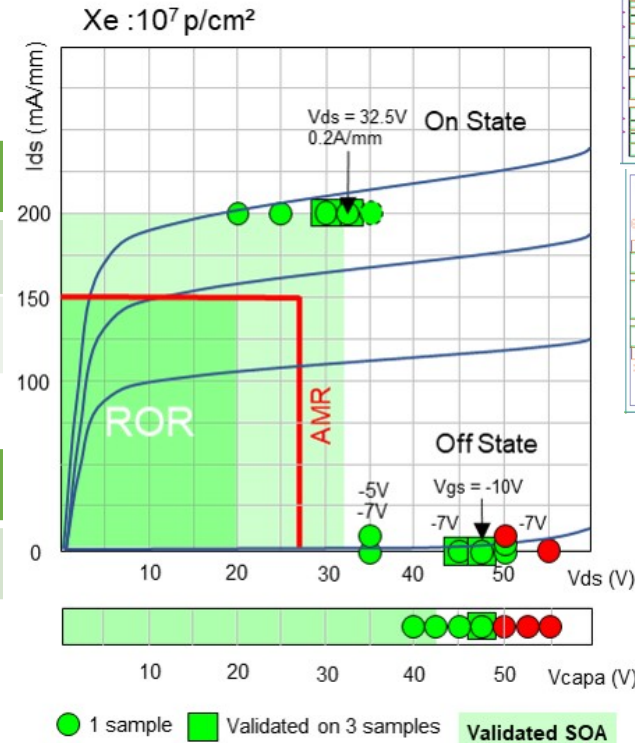
Biasing conditions	SEB - failure	SEB validated	ROR	AMR
On state (Vds / Ids)	No failure up to 35V	32.5V @ 0.2A/mm	20V @ 0.15A/mm	27V @ 0.15A/mm
Off state (Vds / Vgs)	1st failure at 50V/-7V	47.5V /-10V Vdg = 57.5V	Vgs = -15V Vdg = 65V	Vgs = -15V Vdg = not defined

Standard Transistor Rad Hard Operating Area and Maximum Rating

Electrical parameter	SEB - failure	SEB validated	Max rating for space	ROR	AMR
Capacitor voltage	1st failure at 48.5V	47.5V	42.5V	80V	130V

MIM capacitor Rad Hard Operating Area and Maximum Rating

➔ Next : EPPL Listing



Test structures used

Thank you for your attention !