

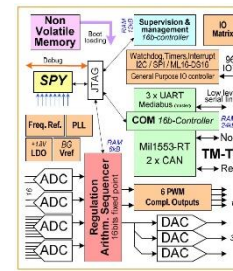
ASIC/FPGA ECSS standard evolution

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09/03/2021

ECSS ASIC/FPGA WG

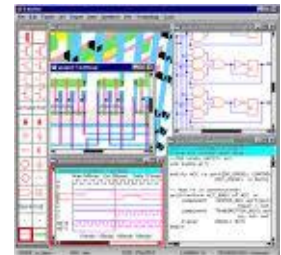
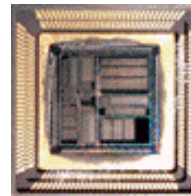
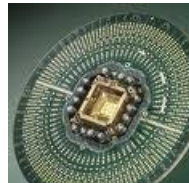
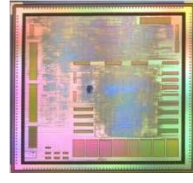
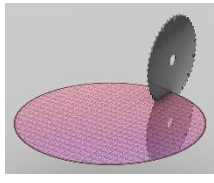
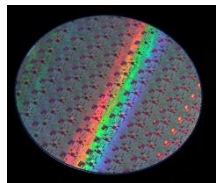
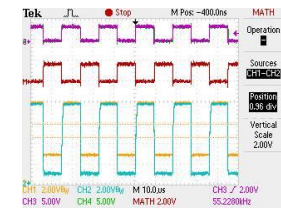
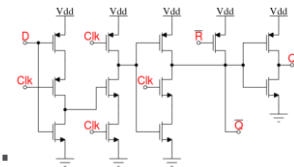
PURPOSE and SCOPE



- 1 - new **ECSS-E-ST-20-40** : engineering requirements
- 2 - revised **ECSS-Q-ST-60-02** : quality assurance requirements

end-to-end multi-phase development flows,
from specification of requirements to validation tests of prototypes of :

- **ASICs** (digital, analogue and mixed-signal)
- **FPGAs** (SRAM, FLASH and anti-fuse)
- IP Cores (building blocks for ASICs and FPGAs)



New risks and challenges due to evolution and changes in ASICs and FPGAs MANUFACTURING PROCESSES, METHODS and TOOLS for DESIGN and TEST, higher functional and technology complexities (> 20 Million of transistors in one chip).

more and **clearer engineering requirements and development flows** for the different ASICs (digital, analogue and mixed-signal) and FPGAs (SRAM, Flash and anti-fuse) types

CHALLENGES

- design for **test** (timing and stuck-at faults, built-in self-tests)
- design for **manufacturability** (smaller nodes 65, 28, 22nm, manufacturing design rules)
- design for **signal integrity** (noise, cross-talk and parasitic effects)
- design for **power** (power islands, ground bounce effects, etc.)
- design for **connectivity** (optimal layout floor-planning and place and route)
- design for **timing and speed** (synchronizing clock domains, signal propagation delays and racing problems)
- design for **radiation effects** (mitigation techniques at multiple levels)
- System-on-Chip with **embedded microprocessor cores using SW** -> HW-SW co-design
- **IP cores (re)use**
- multiple abstraction levels of **Hardware Description Languages** and iterative **tool chains** to create integrated circuit topologies (basic circuit elements and interconnects)
- “**criticality classes**” and “**tailoring**” (as done in other engineering domains, such as software engineering).
- **Naming conventions** for milestone names – avoiding wrong interpretation, confusion

Starting points: existing standards, related handbooks (ESA,NASA)



origin	DOC name	release date	access
ECSS	ECSS-Q-ST-60-02C ASIC/FPGA Development	Jul-08	https://ecss.nl/standard/ecss-q-st-60-02c-asic-and-fpga-development/
ECSS	ECSS-Q-HB-60-02C Techniques for radiation effects mitigation in ASICs and FPGAs handbook	Sep-16	https://ecss.nl/hbstms/ecss-q-hb-60-02a-techniques-for-radiation-effects-mitigation-in-asic-and-fpgas-handbook-1-september-2016-published/
ECSS	ECSS-E-ST-40C Software general requirements	Mar-09	https://ecss.nl/standard/ecss-e-st-40c-software-general-requirements/
ECSS	ECSS-Q-ST-80C Software product assurance	Feb-17	https://ecss.nl/standard/ecss-q-st-80c-rev-1-software-product-assurance-15-february-2017/
ESA TEC-EDM document	ESA IP Core Technical Requirements (TEC-EDM/2010.61/KM)	Apr-15	https://amstel.estec.esa.int/tecedm/ipcores/ESA_IP_Core_tech_guide.pdf
NASA Tech Std System	NASA Complex Electronics Handbook for Assurance Professionals	02/02/2016	https://standards.nasa.gov/standard/nasa/nasa-hdbk-873923
NASA Tech Std System	Programmable Logic Devices (PLD) Handbook	2013-12-02 Revalidated 2016-01-19	https://standards.nasa.gov/standard/nasa/nasa-hdbk-4008
Radio Technical Commission for Aeronautics "RTCA".	RTCA/DO-254, Design Assurance Guidance for Airborne Electronic Hardware	Apr-00	https://www.rtca.org/ and http://www.do254.com/

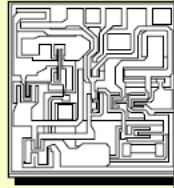
Preparation of an ECSS Standard for ASIC Development		
Timeframe / Milestones		
Milestone	Date	
Kick-off	January 2000	
First issue of draft specification	April 2000	
Coord. Meeting at ESTEC, 2 nd issue of draft	June, July 2000	
Distribution of draft ECSS Standard to industry	January 2001	
Technical meetings with selected vendors	March 2001	
Analysis of Comments	August 2001	
Distribution of third issue of draft ECSS Std.	November 2001	
Industrial Review Meeting	January / 2002	
Preparation of fourth issue of draft ECSS Std.	February / 2002	
Preparation of final ECSS approved Standard	March / 2002	



CHART 4

Released
2007 !!!

ECSS-Q-ST-40-02C
31 July 2008

**Space product
assurance**

ASIC and FPGA development

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Division
Noordwijk, The Netherlands

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85% !!

15% is product / quality assurance , dependability

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starting point 1 - overview ECSS-Q-ST-60-02 - figures

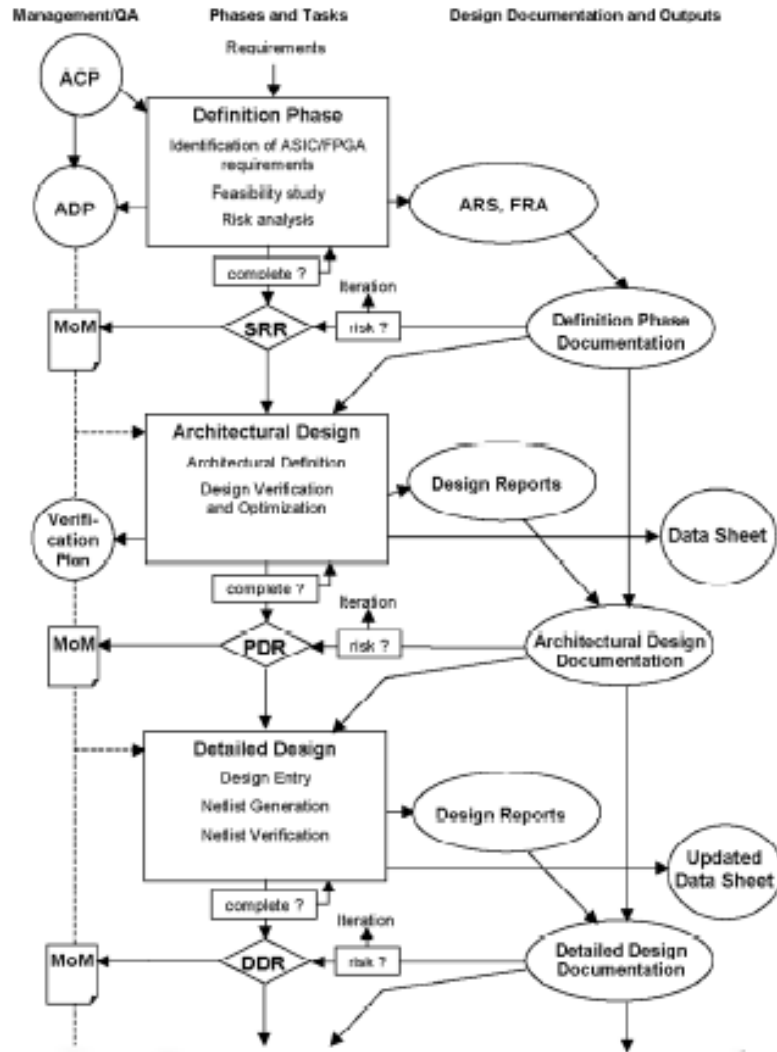


Figure 5-1: Development flow (example)

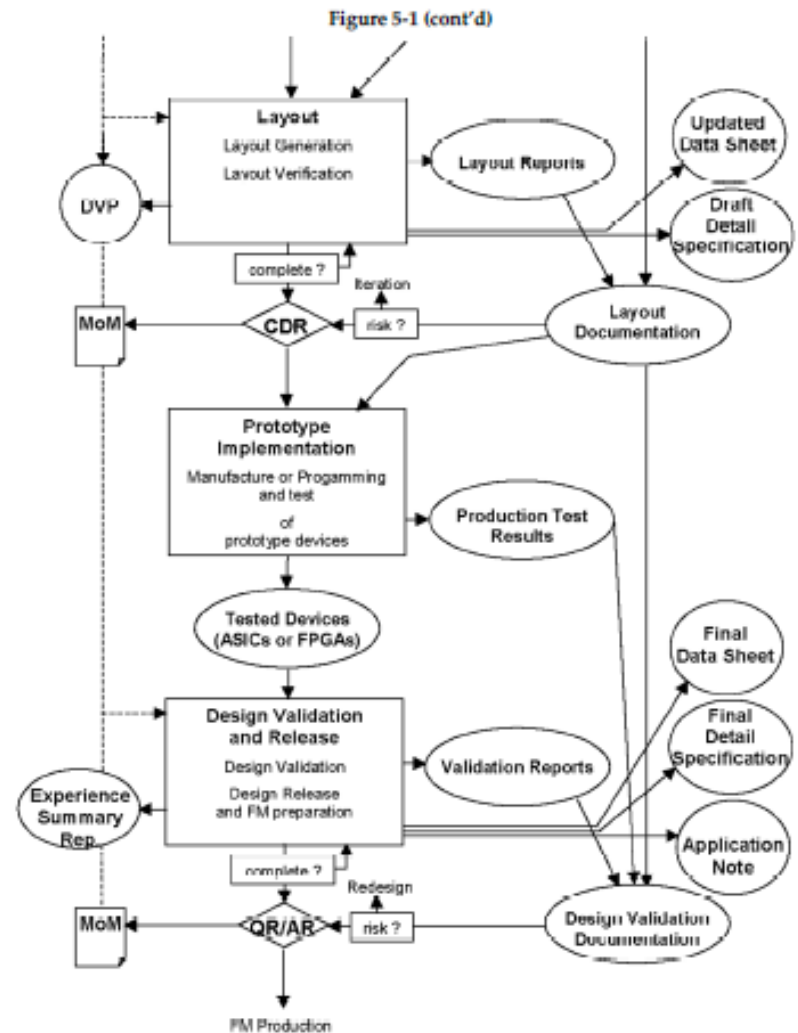


Figure 5-1: Development flow (example) - continued

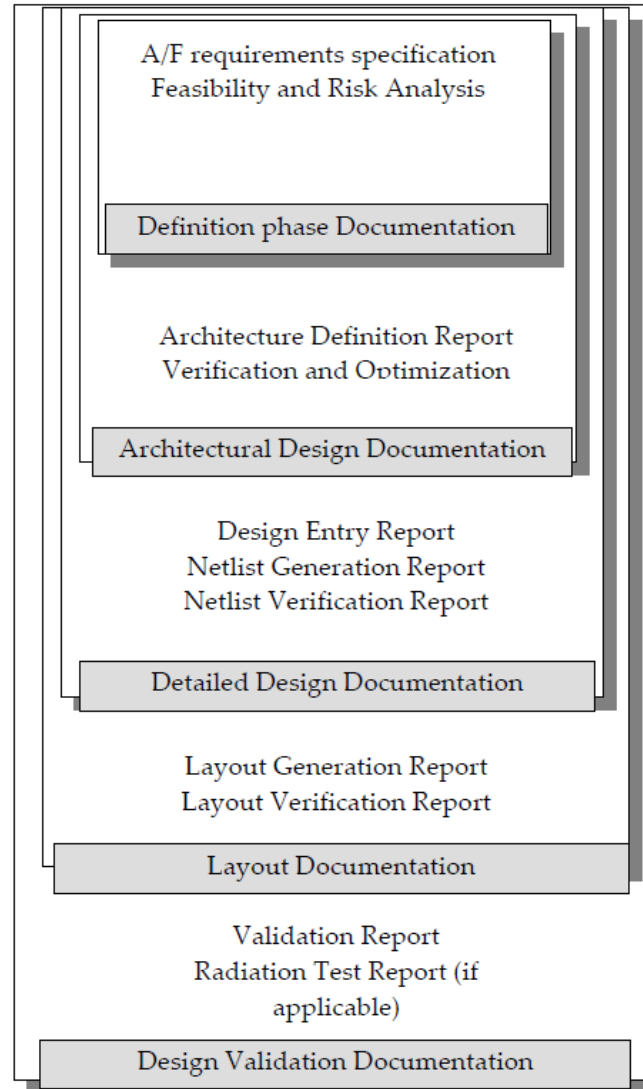


Figure 7-1: Design documentation

1. ECSS-Q-60-02 ASIC/FPGA Development (2007)
2. ESA-TECEDM-MIN-009225 "ECSS-Q-ST-60-02 improvements - preliminary feedback from Industry experts" MoM (**12-April-2018**). This document collects **42 change requests** proposed by ASIC/FPGA 11 experts from European companies and institutes (including TAS, ADS, RUAG, Arquimea, Cobham Gaisler, TESAT, IMEC, CNES.)
3. ESA-TECEDM-CR-011384 "ECSS-Q-ST-60-02: preliminary list of **28 Change Requests** proposed by ESA Microelectronics Section (TEC-EDM, **August 2017**)".
4. ECSS-CR-overview_ECSS-Q-ST-60-02C (25 October 2018), **4 CRs** submitted to ECSS on-line system.
5. 12 years of accumulated experience applying and using ECSS-Q-60-02 standard – Working Group and supporting experts!

New standard's content and format challenges



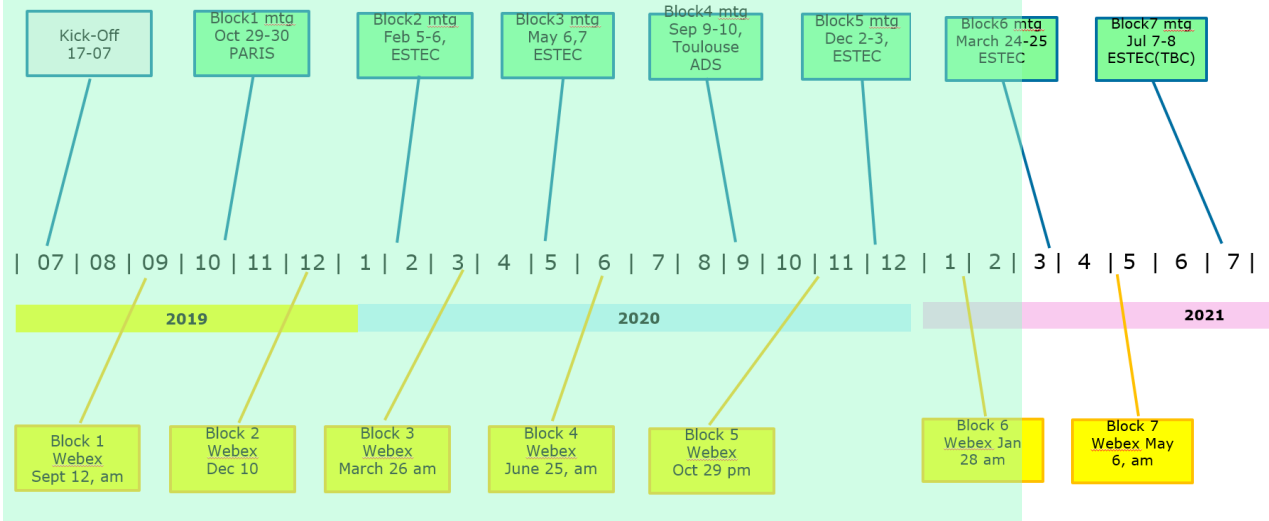
- **higher clarity**, simplicity
- covering different flows for **ASIC** (digital and analog), **FPGA** and **IP Cores**
- **better definitions** of Specifications, Development, Verification and Validation Plans
- **parallel/serial** submodule developments, iterations, additional intermediate reviews or fewer reviews (according to device complexity and criticality)
- special attention to **HW-SW co-engineering** (coordinated with ECSS-E-ST-40 SW engineering WG), when using embedded processing cores using Software
- consistent **terminology** , also wrt new SW ECSS-E-ST-40 /Q-ST-80 stds
- special attention **Analogue/Mixed ASICs** requirements and flow
- new Annexes and figures with **pre-tailoring** of flows/requirements per device type and its criticality
- Compatible with evolving IC technologies, higher functional complexities, CAD tools
- Efficient separation of **engineering** (E-ST-20-40) versus **quality assurance** requirements in revised Q-ST-60-02

ECSS-E-ST-20-40 WG – March 2021 status (1/2)



- 2.5** years of total work planned to have **2** drafts for public review by **Dec 2021**
- 36** mtgs planned, **3** face-to-face 2-days mtgs, and **33** half day webexs.
- 11** WG members (ESA, CNES, ADS, TAS, IMEC, Ariane Group, GMV, RAL)
- 22** WG experts (TESAT, ADS, ESA Microelectronics section, BSC, Cobham, TAS, E040 WG)
- 132 requests for changes** gathered between 2017 and 2020 from industry and agencies

22 meetings, BLOCK1-6 covered = **290** requirements agreed
(63 are new)



BLOCK1- Overall structure, Terms, definitions

BLOCK2 – General req, Definition Phase

BLOCK3 – Architectural Design Phase

BLOCK4 – Detailed Design Phase

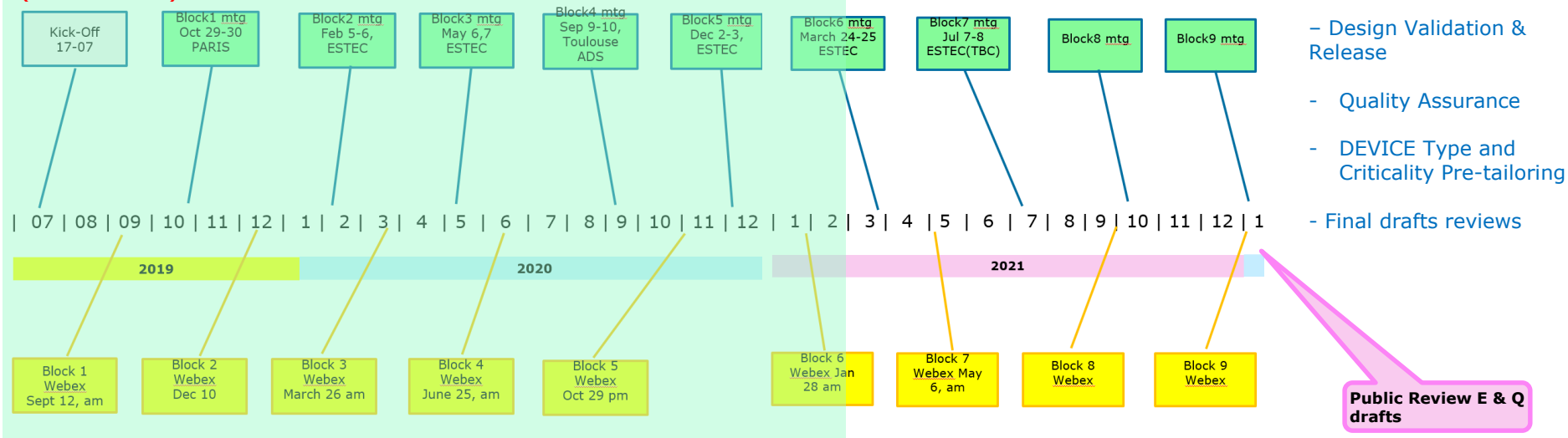
BLOCK5 – Layout Phase

BLOCK6 – Proto Implementation Phase

BLOCK7 – Design Validation & Release

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coordination with **ECSS-E-ST-40C** Software Engineering standard and **ECSS-Q-ST-80C** SW PA

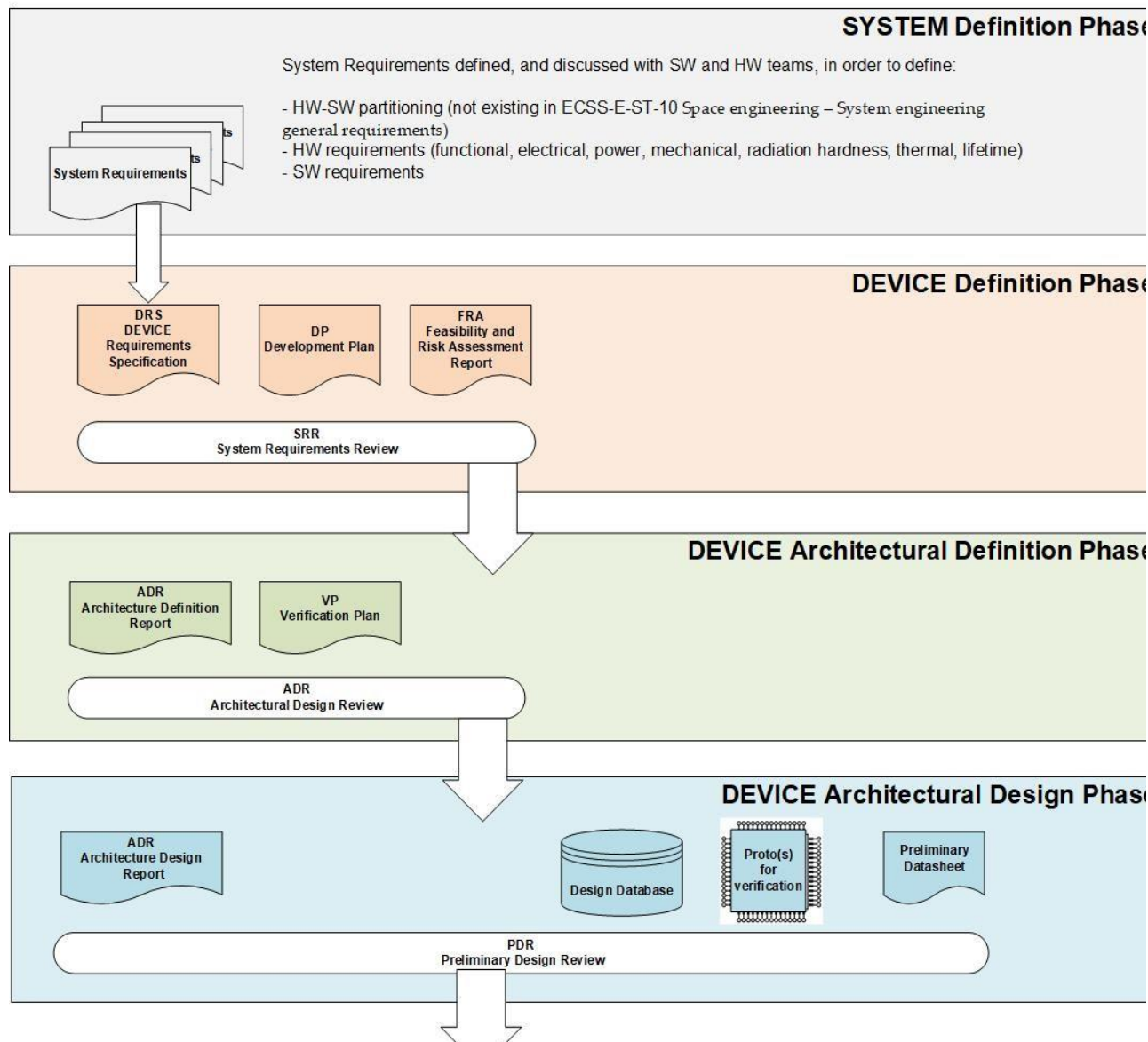


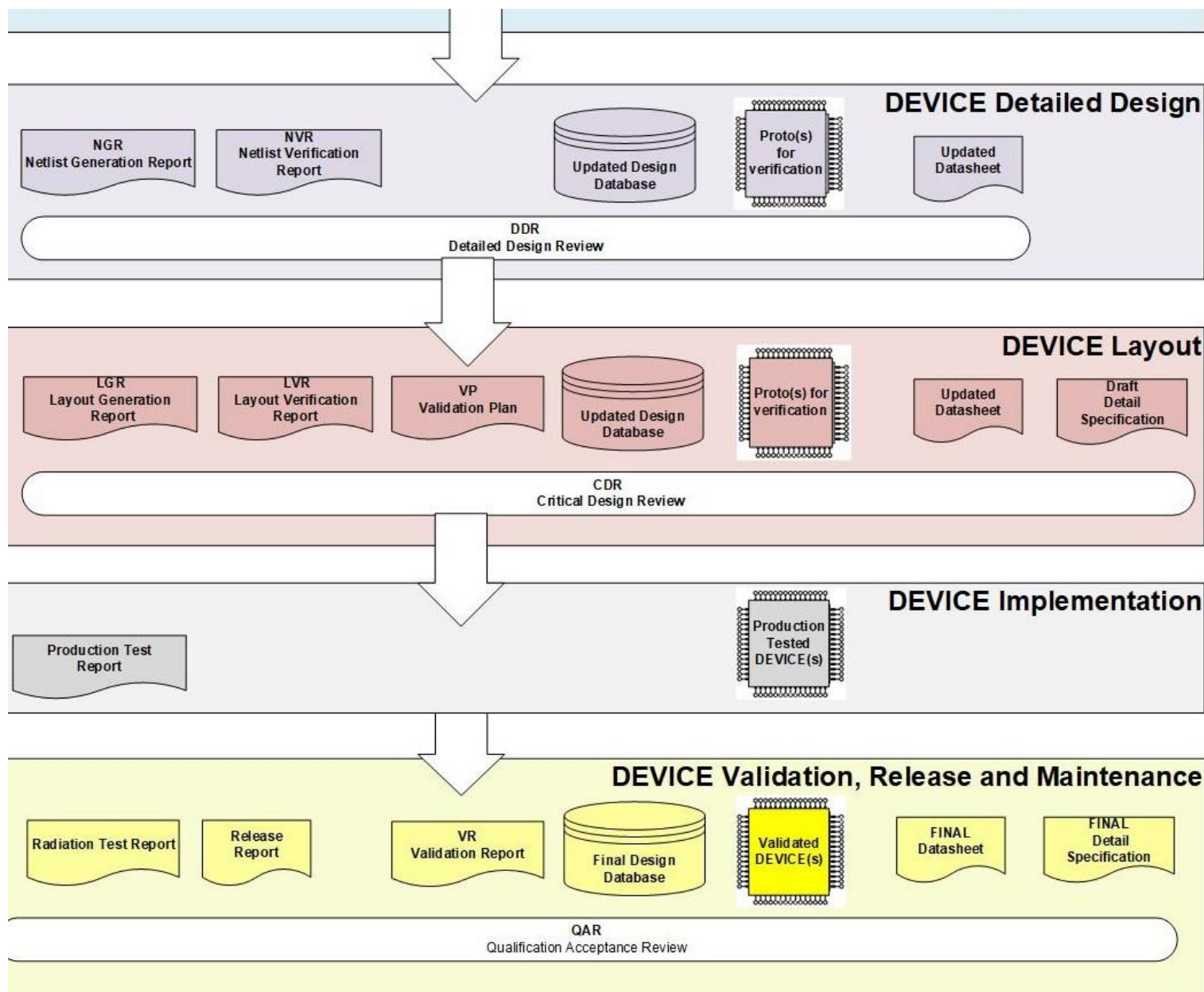
to ensure coherence and synergy in the definition and applicability of **requirements** and **terminology** used for certain ASIC/FPGA development phases:

1. creation and verification of files of code
2. HW-SW systems co-design requirements.

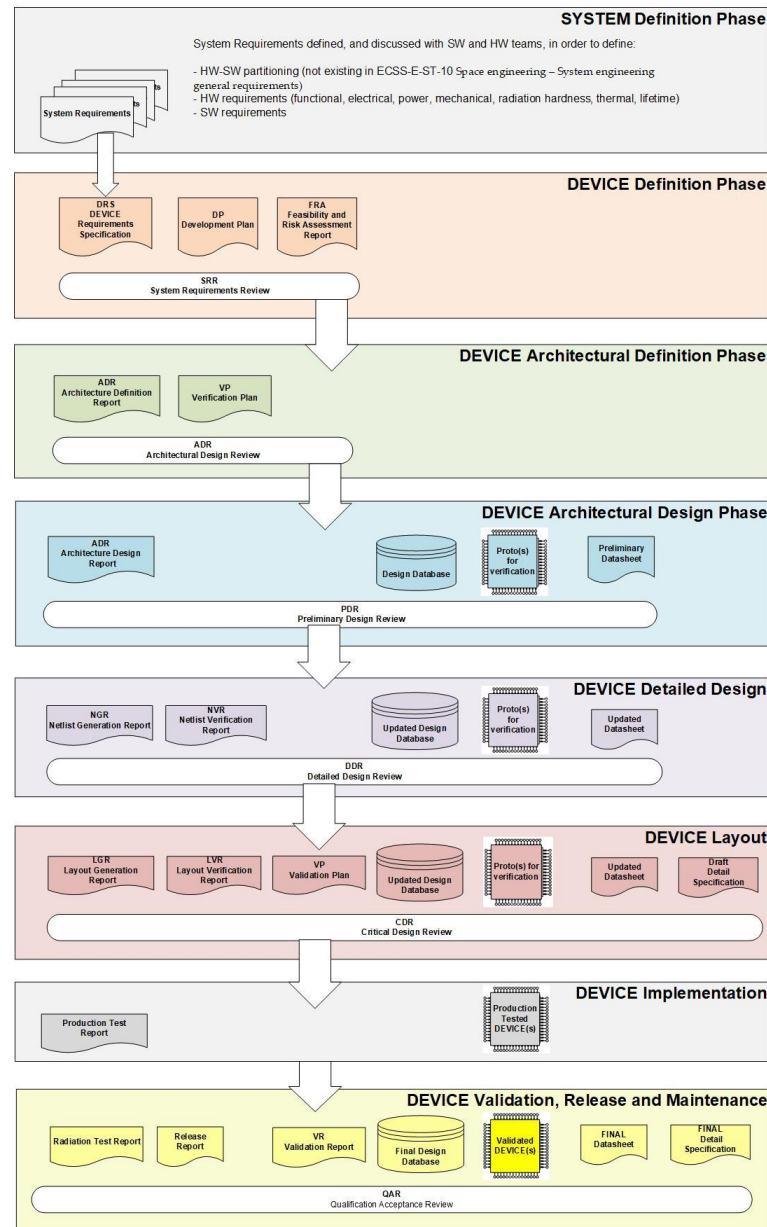
DEVICE (ASIC/FPGA/IP) DEVELOPMENT FLOW

ECSS-E-ST-20-40 new standard





ECSS-E-ST-20-40 new standard



Thanks !

Questions ?