Radiation Testing at System Level

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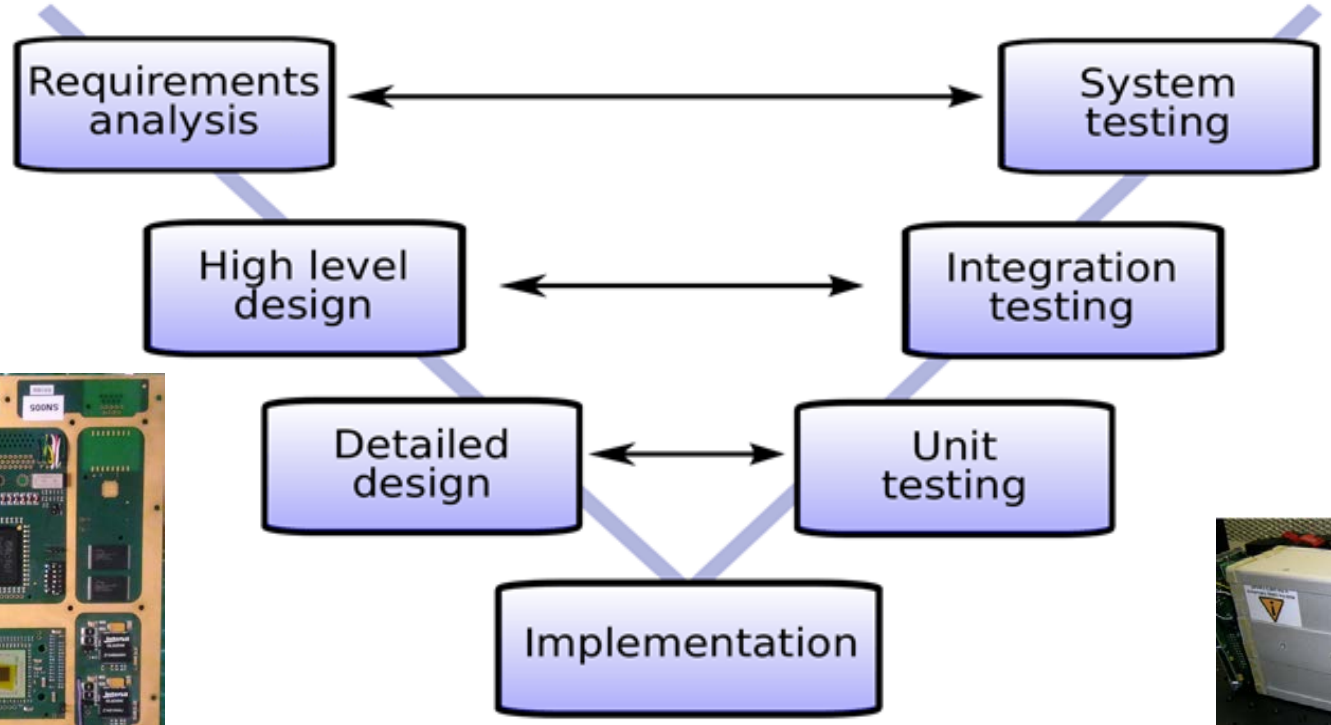
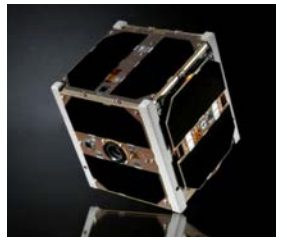
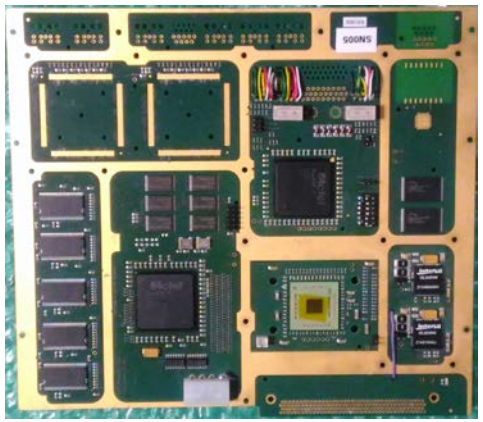
Outline

- Scope
- TID System/Board Level Testing
  - Advantages and Disadvantages
- Single Event Effect System/Board Level Testing
  - Advantages and Disadvantages
- Conclusion

System Level Testing, What Are We Talking About?





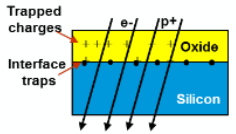


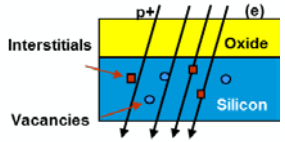
System Level Testing: Board(s) testing (breadboard or EM) or COTS unit

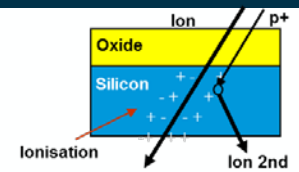
System/Board level testing is not a new technique (common practice in some ISS applications)

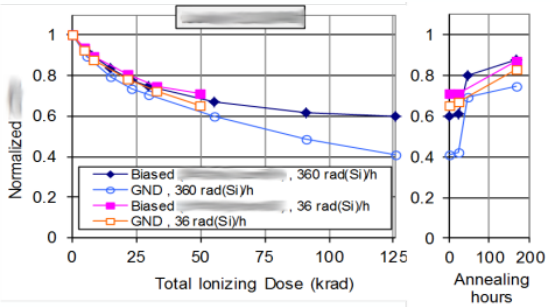
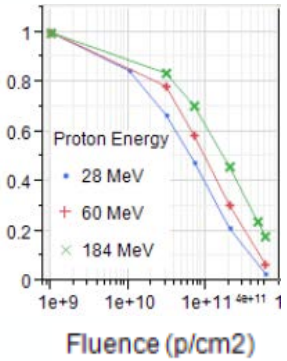
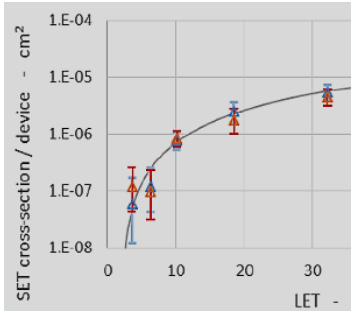
Radiation Effects Testing – In a Nutshell

(*Adapted from Muschitiello & Costantino, SERESSA 2018*)



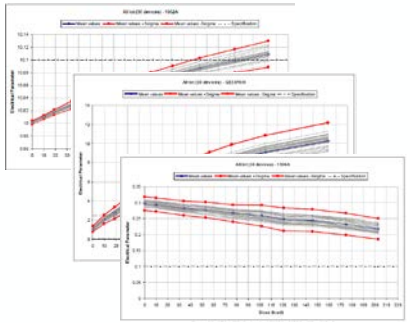




Total Ionising Dose	Displacement Damage	Single Event Effects
Cumulative effect: Gradual global degradation of device parameter		Probabilistic effect: transient, permanent or static errors.
PERFORMANCE DEGRADATION as function of :		CROSS SECTION (=Probability of SEE occurrence) as function of:
Total dose [rad(Si)] [Gy(Si)] – **Co-60**	Fluence [p/cm^2] – **protons** Displacement Damage Dose [MeV/g]	Linear energy transfer [MeV/mg/cm^2] – **ions** Energy [MeV] - **protons**
		
Other irradiaton test parameters: Dose rate [rad(Si)/s] [Gy(Si)]	Other irradiation test parameter: Proton Energy [MeV], Flux [p/cm^2/s]	Other irradiation test parameter: Flux[p/cm^2/s] , particle range [um]

Total Ionizing Dose Testing

Part Level Testing



Radiation data on parts
(worst case bias)

PART	PARAM	AGING	RADIATION	
		Drift	Design Dose (Krad)	Drift
RH1014	Voffset	±0,1mV	100	±1,4mV
HS9-139 RH	V_{OFFSET} I_b I_{OFFSET}	±0,1mV +1,8% ±9%	100	±1mV 150nA ±16nA
RH118W	GBWP V_{OFFSET}	-4,4% ±0,2mV	100	-10% ±0,75mV
OP467F	V_{OFFSET} I_b I_{OFFSET} Min Gain	±0,2mV +1,8% ±9% -1,8%	15	1mV 1µA 0,3µA 0
PE9601	Kφ	±2%	100	-
DAC08-498AF	INL Full Range Current	0% 0%	60	±0,25LSB -0,555%
SOC 2N2907	β V_{BE}	-4,4% +1,8%	70	-55% -55%

Worst-case analysis
Estimation of function degradation

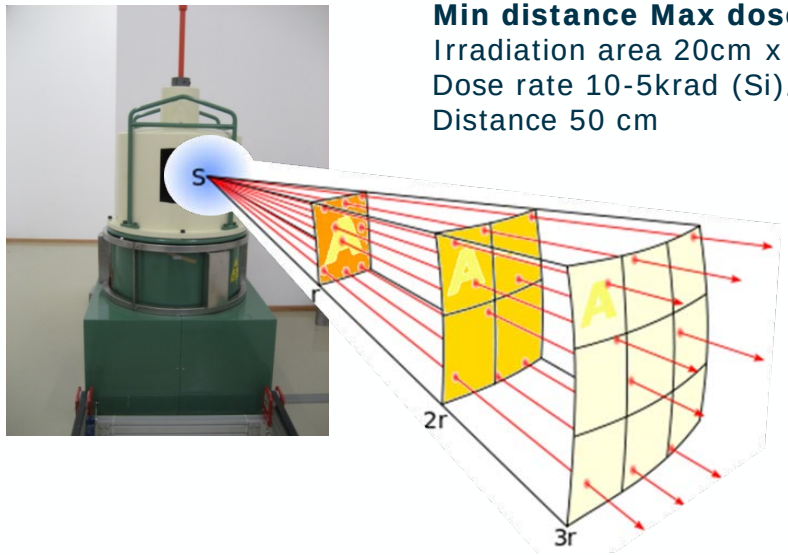
Design Validated

Board Level Testing

Measurement of Function(s) degradation

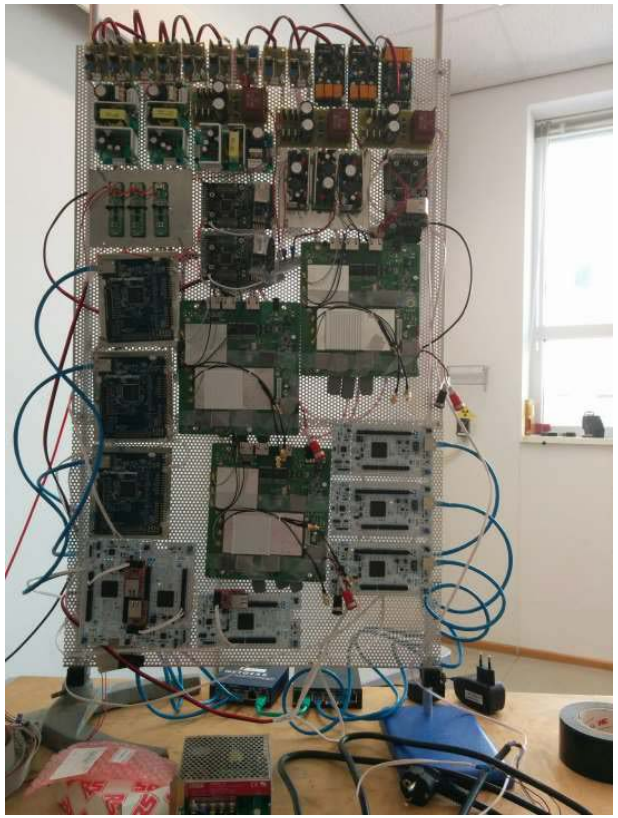
TID Board Level Testing

- Board tolerance will the tolerance of the most sensitive part(s) in the board for their particular function(s)
- The approach is commonly used for RHA of hybrid devices and authorized in RHA ECSS standard
  - DC-DC converters, oscillators,…



Min distance Max dose rate
Irradiation area 20cm x 20 cm
Dose rate 10-5krad (Si)/h
Distance 50 cm

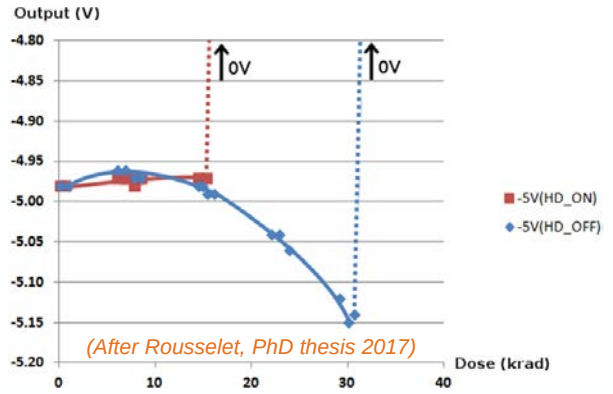
Max distance Min dose rate
Irradiation area 3.6 m x 3.6 m
Dose rate 40-20 rad (Si)/h
Distance 7.5m

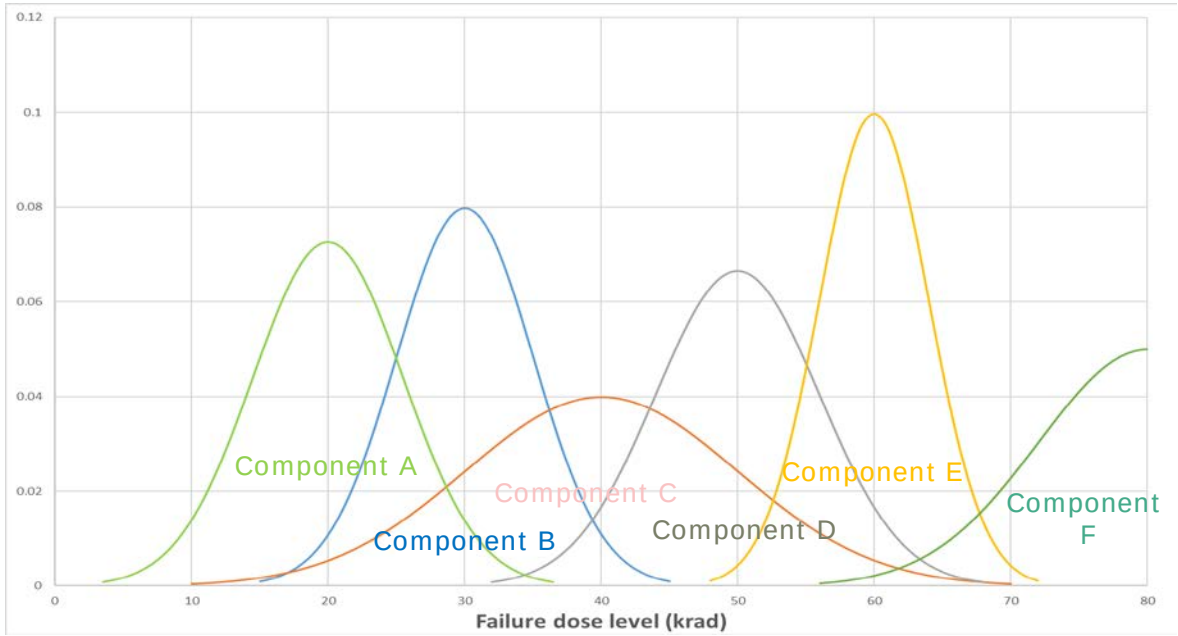


TID Board Level Testing

- Advantage
  - Test time is reduced
  - Parts are tested in application conditions
- Disadvantage
  - Observability is reduced,
    - *Test up to failure level is recommended*
  - Complicated test sequences
  - Significant loss of RHA quality if sample size is low

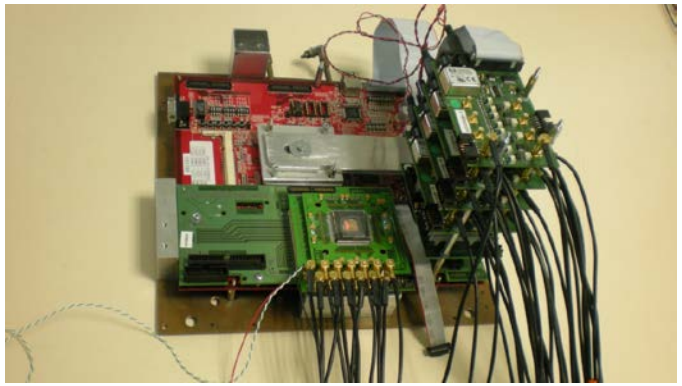
    (1 board = 1 sample per device type in some cases)
    - *Maybe compensated with higher margins?*
  - If a single part is changed, whole board may have to be tested again
  - Results cannot always be used for another application
    - Component level is done for worst case bias condition
  - Results come late in the design phase





Single Event Effect Testing

Component Level Testing



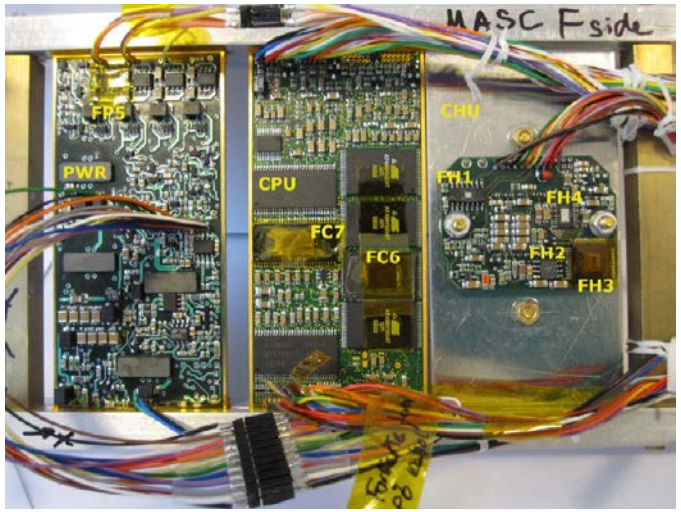
Measurement of SEEs cross-sections of each part used

SEE criticality analysis
(analysis of function response to SEE in parts)

SEE rate calculation

Design Validated

Board Level Testing



measurement of SEE cross sections

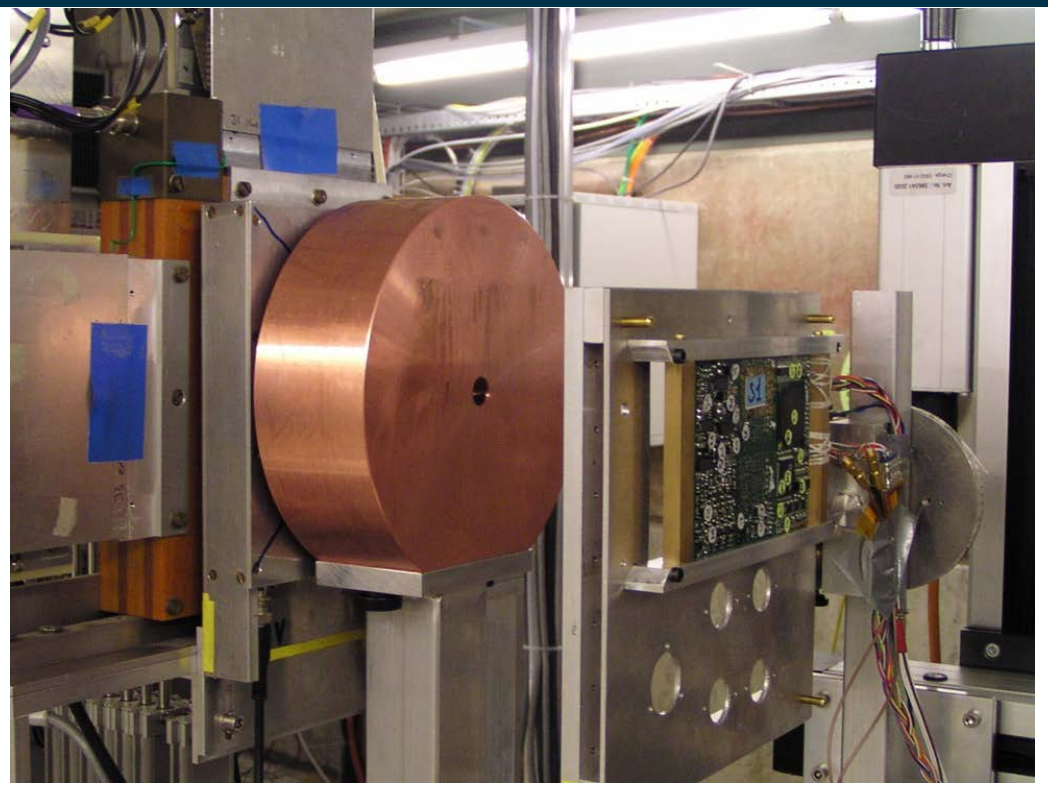
Observation of effects of SEE in parts to the function

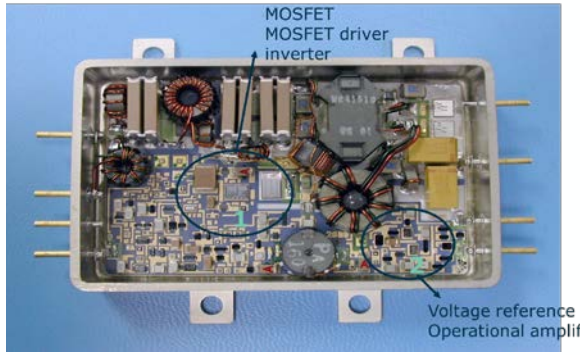
SEE rate calculation

SEE Board Level Testing

In most cases one component is irradiated at a time even when several components on a board shall be tested

- Max beam area in common facilities is generally limited
  - Ions ~ 2*2 cm
  - Protons ~8*8 cm
- In flight, probability of hitting 2 components on a board at the same time is negligible
  - GCR flux ~4 ions/s-cm^2
- Irradiation test conditions vary in function of tested component (flux, fluence, LET,..)





There is little gain in test and beam time when doing board level SEE testing

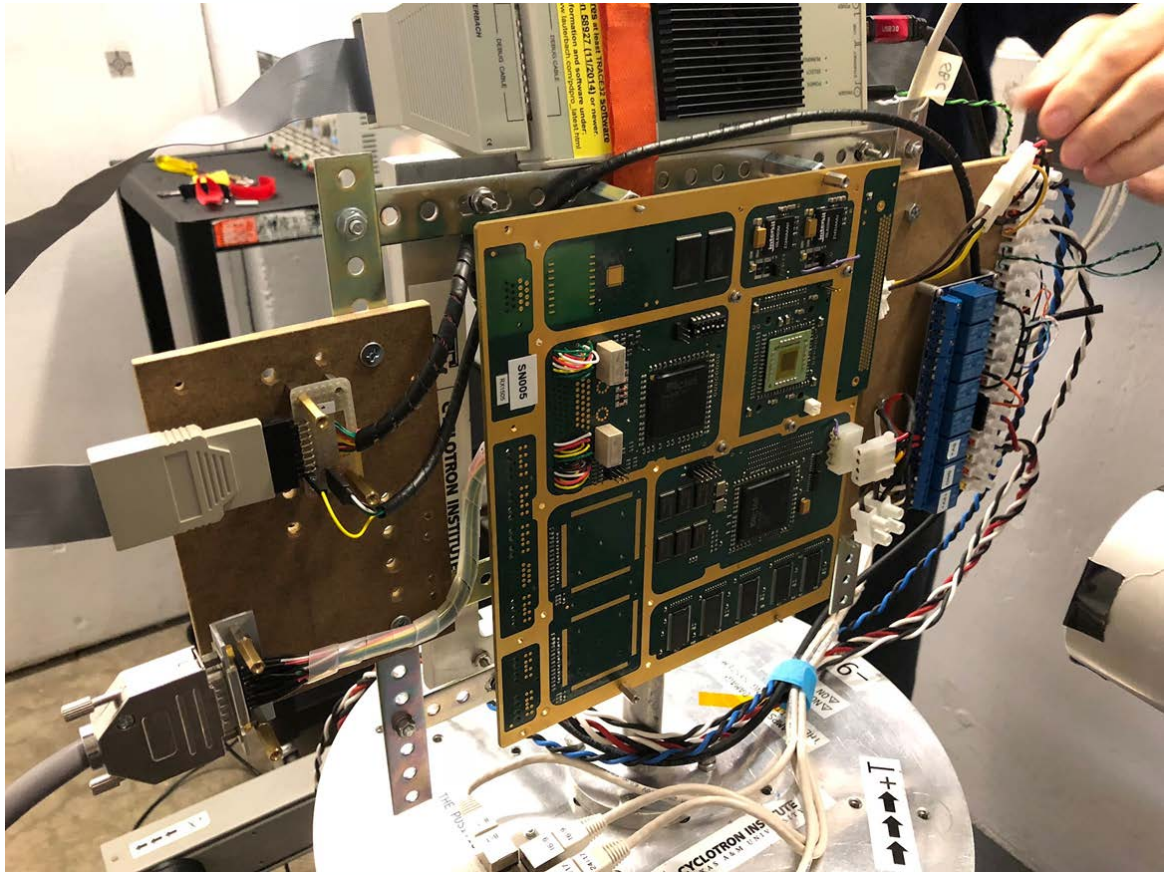
SEE Board Level Testing

- Advantages
  - Board Testing allows testing in application conditions
    - Final design (FPGA, ASIC)
    - Application software (processors)
    - Test of mitigations (SEL, EDAC, TMR. scrubbing, SET filtering..)
    - Analog SETs
- Disadvantages
  - Complicated test sequence
    - Test order, Different test programs per part,..
  - Mitigated designs (ie TMR) can only be tested at low flux
    - Use of a lot of beam time
      - Can be improved with adaptation of setup (scrub frequency,…)
  - Long testing (lot of parts) with often unexpected results
    - A single test campaign is often not enough to obtain complete and satisfactory results
  - Test results for a part may not always be used for another application (ie. analog SETs)
  - Results come late in the design phase

Conclusion

- Board level testing could guarantee a good quality of RHA when it is done right
  - Sufficient sample size and margin for TID
  - Ion and proton testing for SEE with sufficient statistics

- Board level testing is a risky approach
- A mixed approach between component level and board level could be the optimal approach
  - SEE board level testing to test ASICs, FPGAs in their final design, and processors or SoCs with their application software is essential



Useful Reading

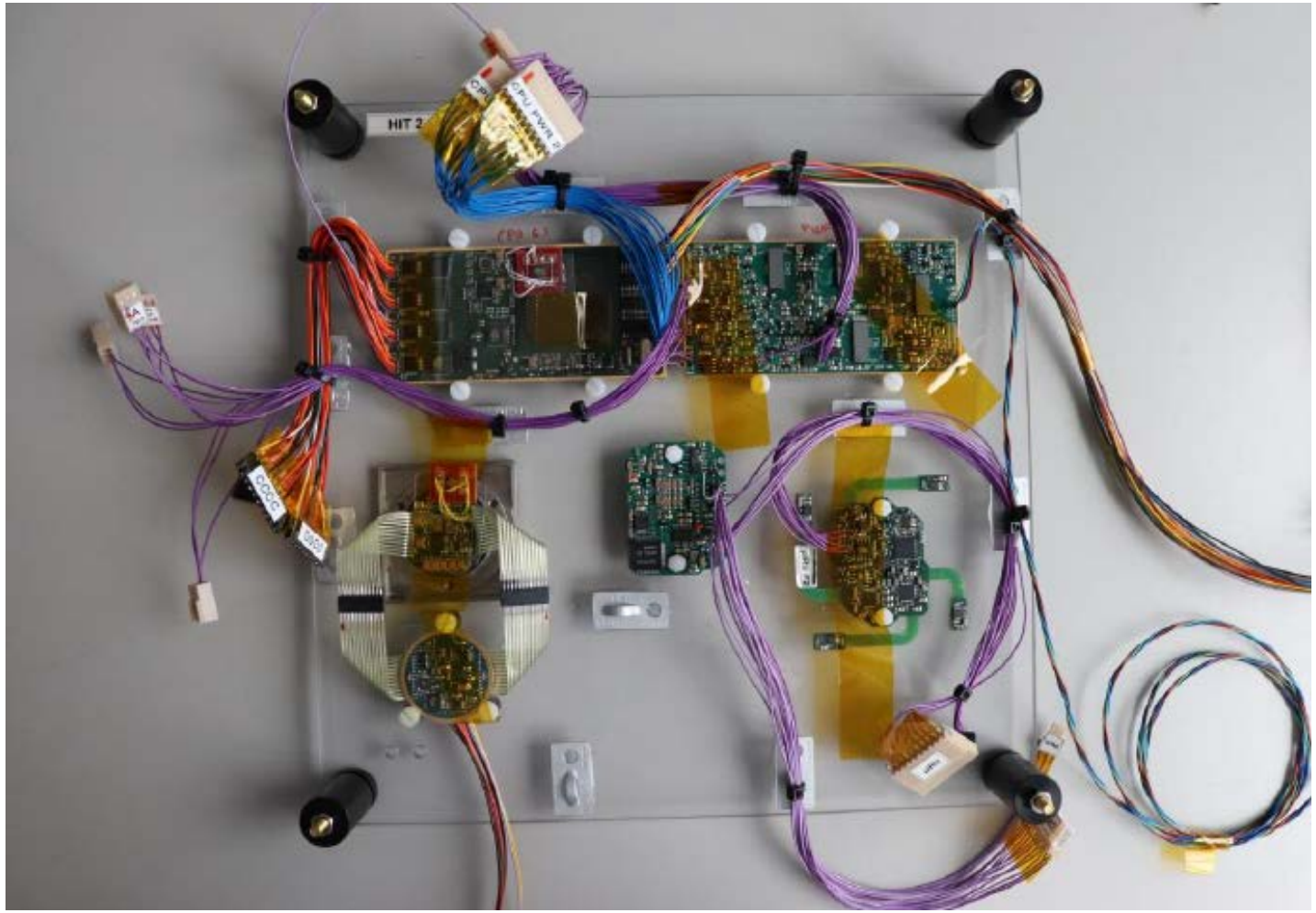
- “RADSAGA System-level Testing Guideline for Space Systems,” CERN Publication, EDMS 2423146, 2020

- “Board Level Proton Testing Book of Knowledge for NASA Electronic Parts and Packaking Program,” S. Guertin & al., JPL Publication 17-7 11/17, http://nepp.nasa.gov

- “Guidelines for SEE Testing of COTS Electronics Using Proton Board Level Testing,” S. Guertin & al., NASA WBS: 724297.40.49 , http://nepp.nasa.gov

Back-up slides

SEE Board Level Testing - Example



SN74LVC2G34DRLR (PbF)	1&2	µ	16	SET/SEL	Program 7	A
NDS355AN	1&2	H	23	SEB/SEGR	Program 7	A
Program 1: Star tracking using external CHU with stimulator on Port-B The instrument is connected to a CHU with a star stimulator. The instrument operates in a stimulator update mode. Special probes included in test software: • The debug output of ECC_MONITOR is enabled in order to get extended information of RAM bitflips. • The exception handling is set to debug output (to log information of trapped SEUs) by removing the assembler flag (EXCP_BOOT) • The watchdog timeout is decreased to 2s to enable rapid recovery after a trapped SEU.						
S-102T(PbF)	1&2	P	17	SEB/SEGR	Program 1	B
S-301T(PbF)	1&2	P	18	SEB/SEGR	Program 1	B
Program 2: Power cycling the instrument This test focuses on the events taking place while the instrument is starting up. It includes reading from the PROM (containing the bootstrap and safe-mode software) and the FLASH (containing the application mode software). During the irradiation, the instrument is automatically rebooted continuously. After irradiation, the instrument is subjected to a final reboot to confirm the final state. Special probes included in test software: • Upon transmission of an attitude packet, a call to handleBootTC() is inserted. This gives the system amble time to power up and send the two power up reports. Typically, 1 or 2 housekeeping packets will also appear before the restart (power up reports). • The exception handling is set to debug output (to log information of untrapped SEUs) by removing the assembler flag (EXCP_BOOT)						
SI4963BDY-T1-E3 (PBF)	1&2	P	20	SEB/SEGR	Program 2	B
Program 4: Verifying telemetry quality This test verifies primarily the line driver. It is activated continuously during the irradiation using memory dump, and the performance results can be assessed from the number of checksum errors. In order to maintain maximum statistics, the telemetry packet size is set to very low. The debug channel is furthermore configured to MIRROR to get maximum statistics (only possible for the Maxim driver circuits). Since attitude determination is not required, the startup mode is set to STANDBY. Special probes included in the test software: • The exception handling is set to debug output (to log information of trapped SEUs) by removing the assembler flag (EXCP_BOOT) • The watchdog timeout is decreased to 2s to enable rapid recovery after a trapped SEU. • The telemetry packet size is changed to 100 bytes (~75 bytes of memory data).						
FIN1031MX	1&2	C	21	SEL/SEFI	Program 4	B

TID Board Level Testing - Example