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Feedback on radiation test on SoC Components which can be very challenging regarding the complexity of such devices

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Introduction

A System on Chip (SoC) is a device who contains various components, such as:

- Processor(s)
- Memories
- Interface/memory drivers
- FPGA
- …

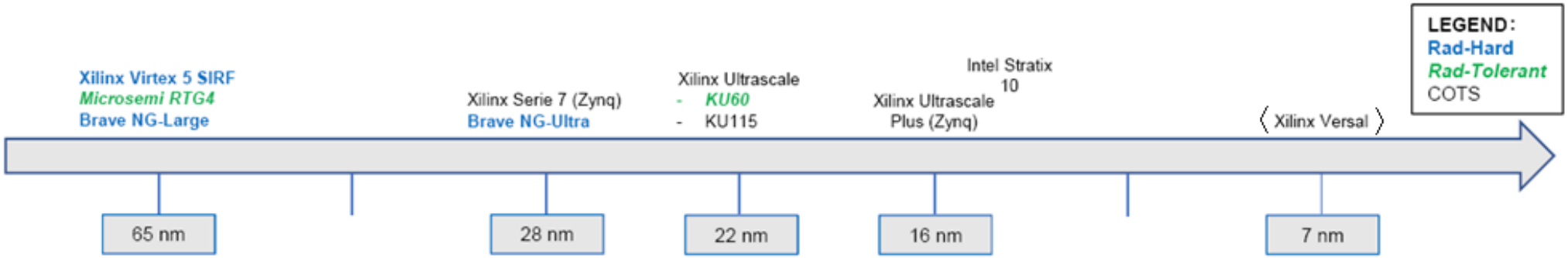
There are plenty on SoC on the commercial market which is driven by Apple, Intel, Samsung, Nvidia, AMD, Xilinx...

Each manufacturer has his own design specification with an associated market

Most of them are not suitable for space application (in terms of functionalities)

Most of them are not procurable on the commercial market

2 main commercial manufacturers:

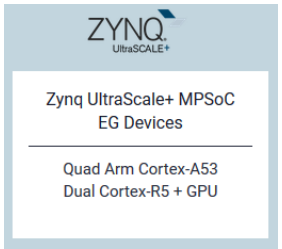


The node size translate the performance in consumption by logic cell.

Performance ≈ 1 / node²

CNES studies : **Chosen on performance and/or on cost basis**

FPGAs

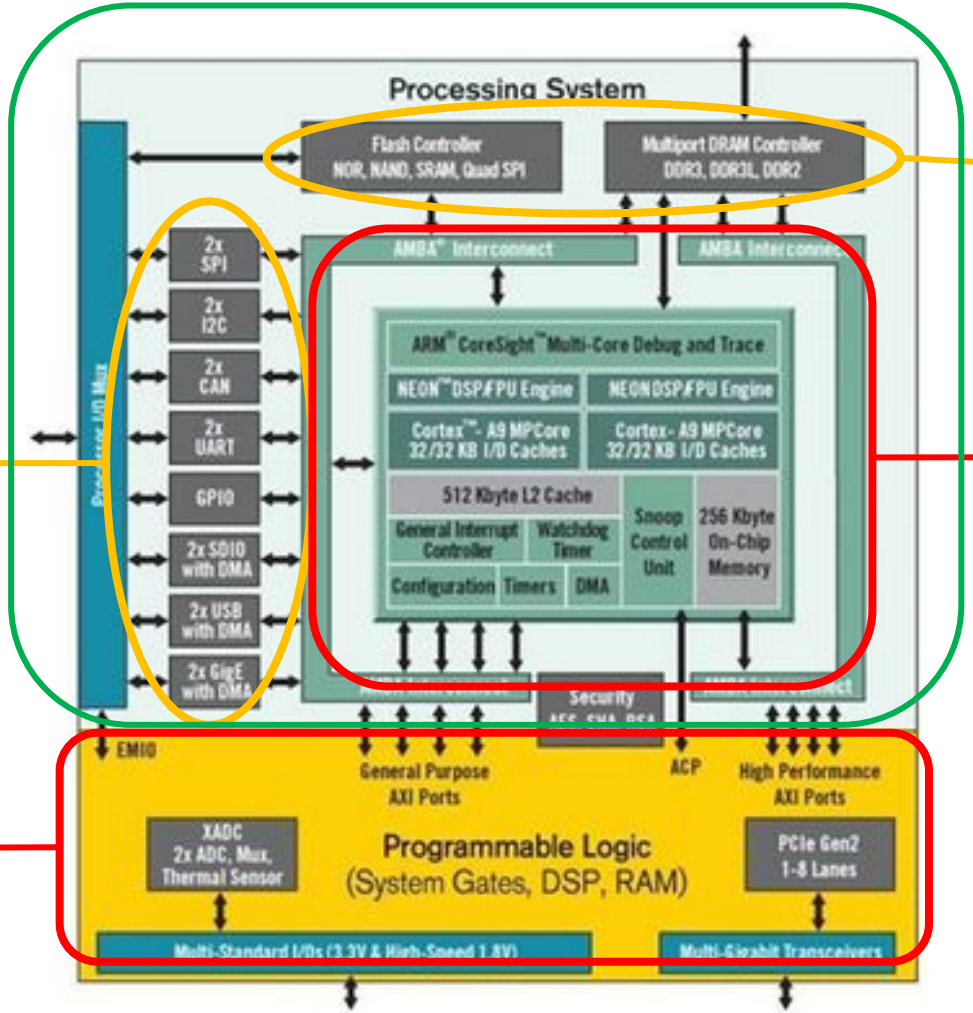


2014 2018 2021

Study on XC7Z030

Generic architecture

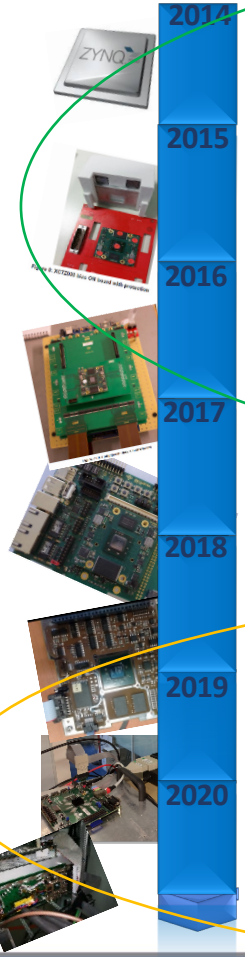
Peripherals



Memory controllers

Dual-Core ARM
Cortex-A9
MPCore Up to 1GHz

FPGA
equivalent to a Kintex-7
125K logic cells



Evaluation of the component
for the future missions vs
radiation effects

5 radiation test campaigns
At component level (HI, TID)

SEL tests
SEU tests in PL and PS

Funded by R&T programs

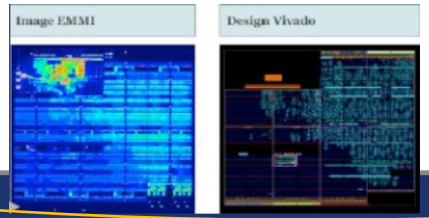
CNES Guideline for mitigation technics in Zynq 7000 series

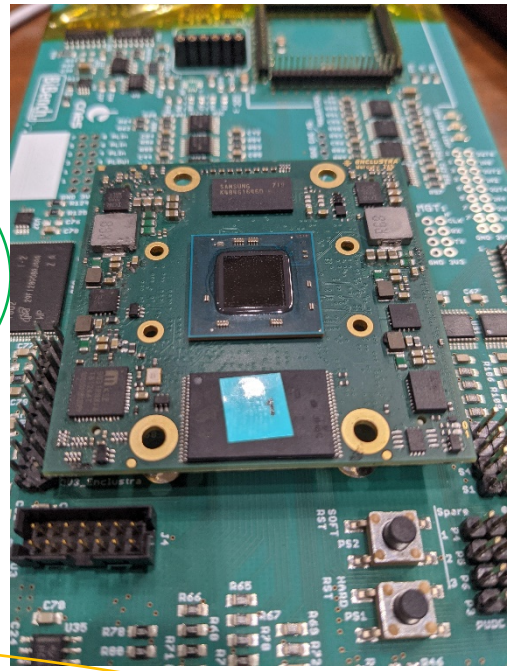
Systems validation

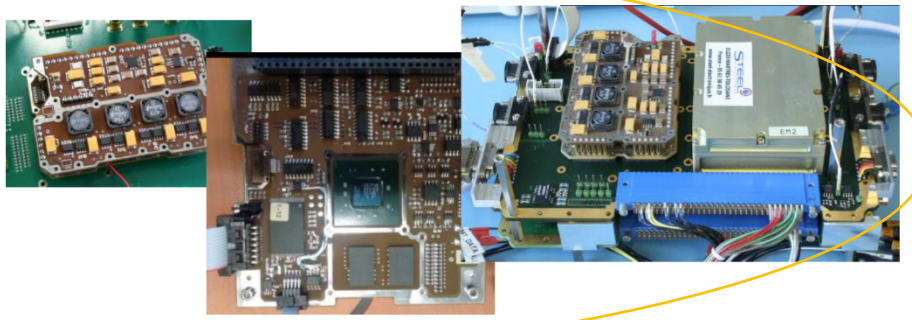
7 validation test campaigns
At system level

- **EMC**
- **Fault injection**
- **Radiation**

Funded by a project
or R&T programs







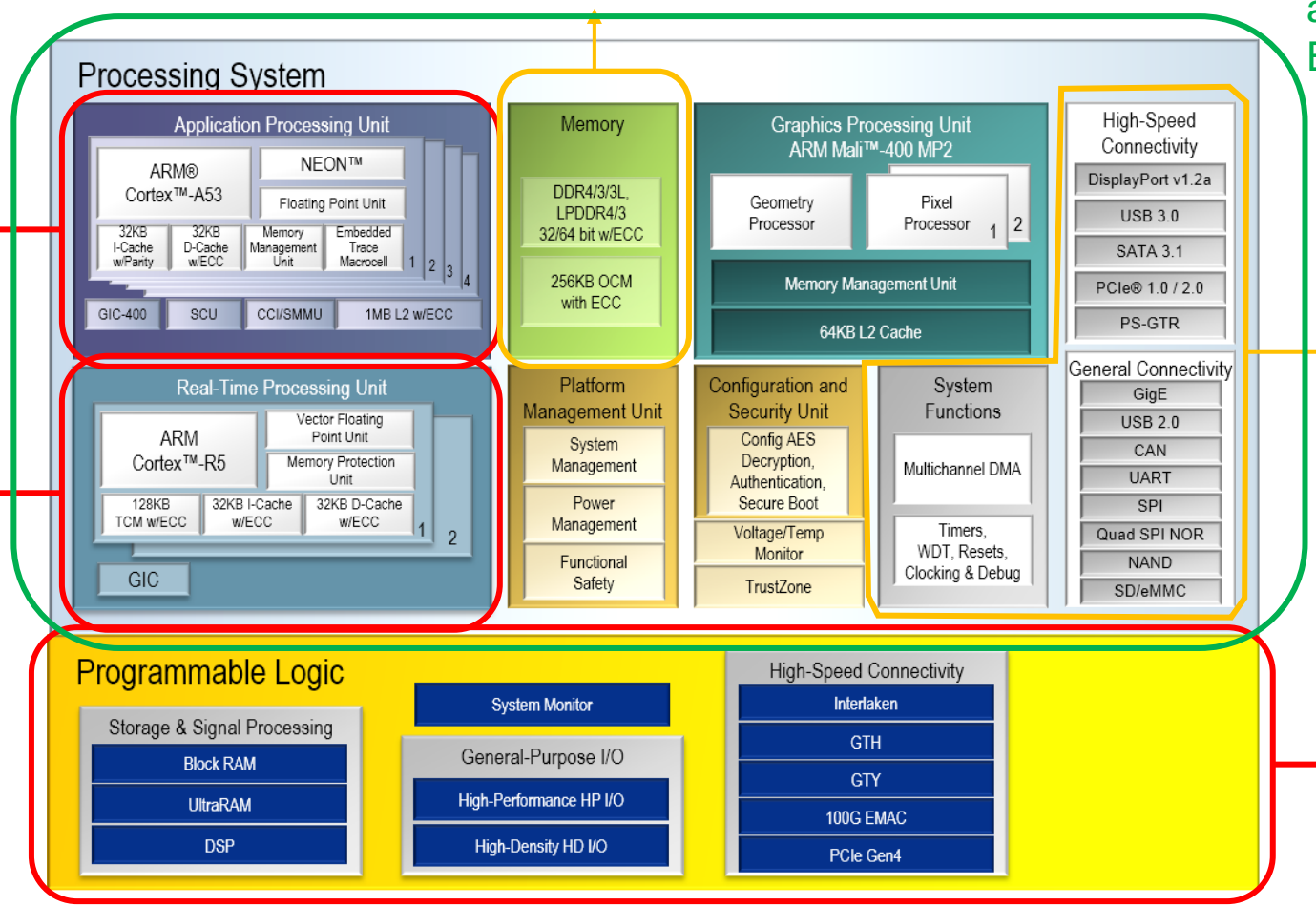
Study on XCZU19EG & XCZU15EG

Memory controllers

Generic architecture for EG version

Quad-core ARM Cortex A53 Up to 1.5GHz

Dual-core ARM Cortex-R5 Up to 600MHz

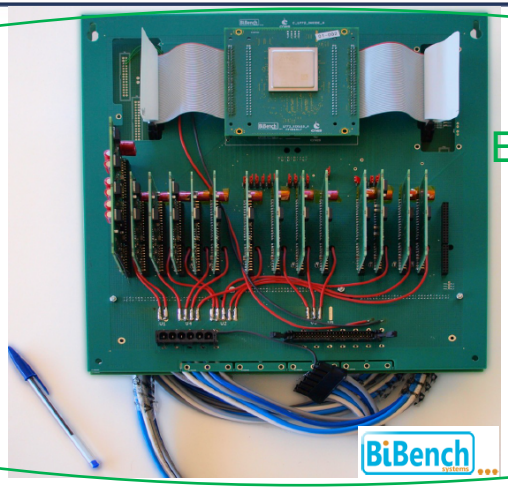


Peripherals

FPGA
ZU15:
747K logic cells
ZU19:
1143K logic cells

2018
2019
2020
2021
2022
2023
2024

5 radiation test campaigns
At component level
(Jyvaskyla, KVI)



Evaluation of the component for the future missions vs radiation effects

→ SEL sensitive

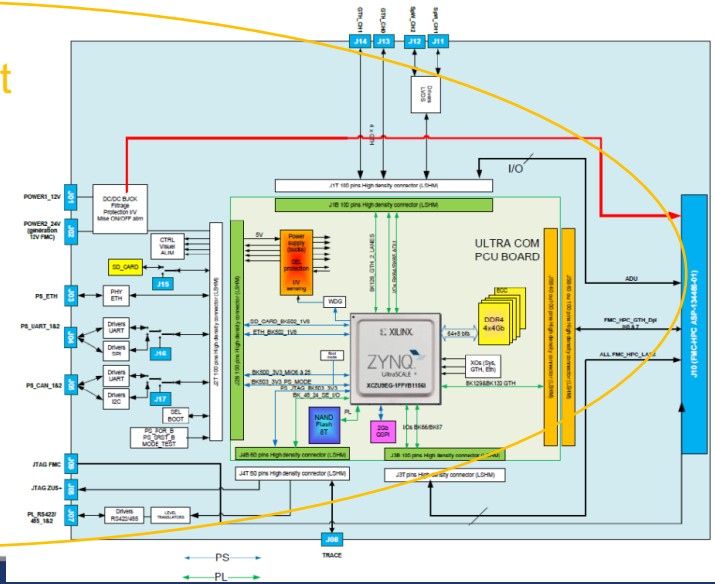
Funded by R&T programs

UltraCOM baord
Integrate all needed peripheal ICs & SEL protections

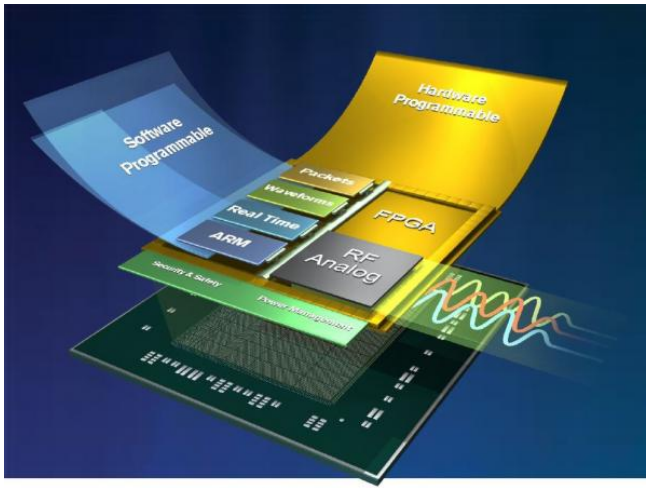
Funded by a project or R&T programs

XX tests campaigns
At system level

Test of use cases and mitigation technics

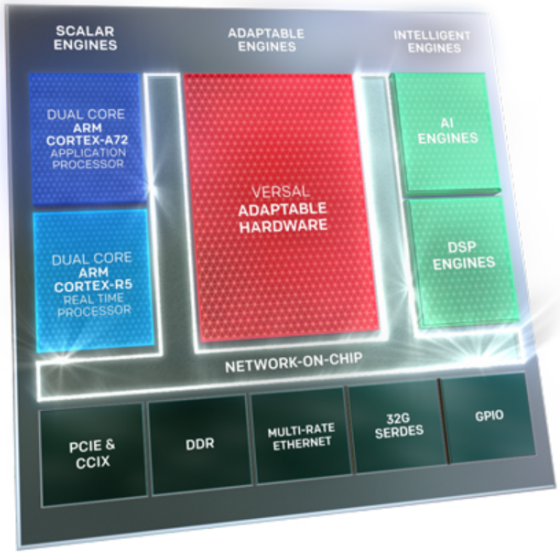


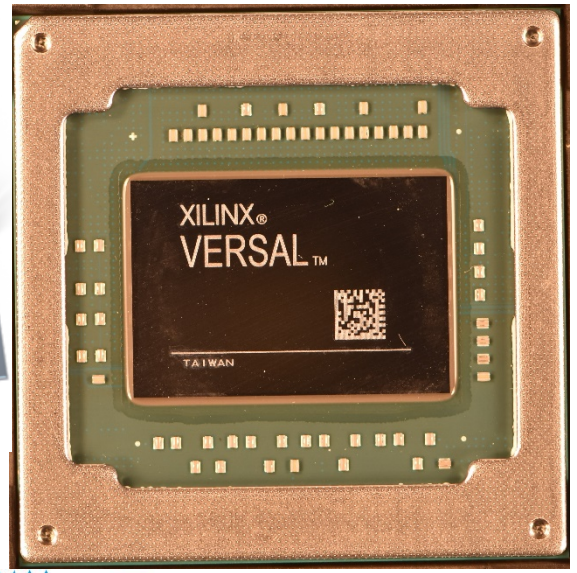
Zynq Ultrascale + RFSoC



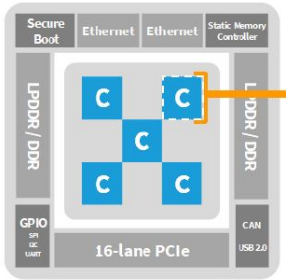
Similar with Zynq Ultrascale +
With additional ADC DAC
for RF processing

2020
2021
2022
2023
2024
2025
2026

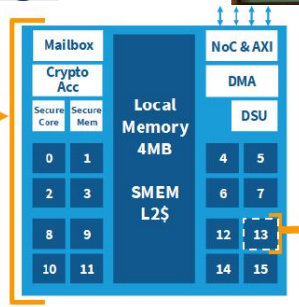




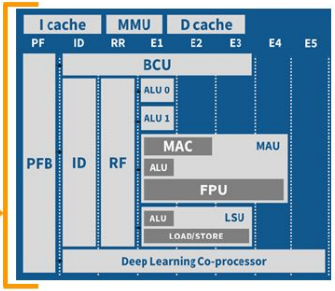
Kalray MPPA Coolidge



MPPA® Manycore Processor
(5 clusters = 80 cores)



Compute Cluster
(16 cores)



64-bit 3rd Generation
VLIW Core + Accelerators

Future is coming

Lessons learned

- Increase of the capacity and of the numbers of components inside the devices
- The architecture are more and more complex at for each new generation
- Increase of the data rates and available interfaces
- Constant increase of the power supply needs with
  - Plenty of power domains
  - Various independent power lines
- Complexity of the test for SEU and integrated components
  - Required a large amount of beam time
  - Custom test code needs to be developed
  - Access to all the memory blocks are not always feasible
- Difficult to clearly understand what's really happen inside the device without support from the manufacturer
- Time is needed between each test campaign to really understand what's happened
- Ecosystem grows in parallel of the tests/developments

Conclusion

- **Characterization of SoC is complex and cannot be done on a single radiation test campaign**
- **Tests required skills in various domains**
  - Hardware
  - Software
  - System
  - Test bench
  - …
- **Anticipate as much as possible your next test campaign with preliminary tests**
- **Keep tests simple.**
  - *If the test is too complex it will be difficult to develop the test setup and errors will be difficult to analyze*
- **A global system validation is needed to validate your mitigations technics**
  - A global validation is a project in a project framework
  - A validation with a good coverage is long and complex