SiC: First attempt of introducing SiC based power devices in space application

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BACKGROUND

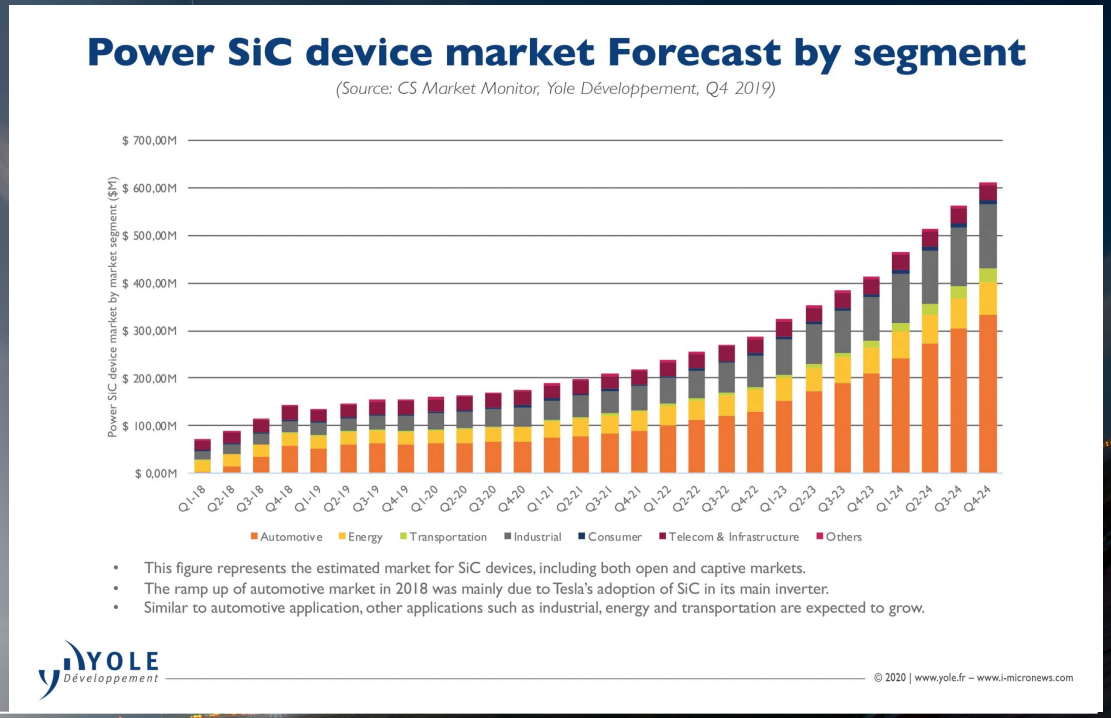
- From a niche market to a volume market: the supply chain of SiC has developed faster than forecast in the last 10 years thanks mainly to hybrid vehicle market
- Most popular application for SiC devices : HV On board charger, HV inverter, dc/dc conversion
- Starting in 2005, the industry began to ramp up SiC power devices in 100mm (4-inch) fabs. Then, from 2016 to 2017, SiC device makers completed the migration from 100mm to 150mm fabs. Today, 150mm is the mainstream wafer size in SiC.And now they are moving towards 200mm (8-inch)

See REACTION project part of Horizon2020

- Full European supply chain is available
- Availability of new generation devices:

ST is already in the 3rd generation, Infineon has Trench SiC MOSFET

- Availability of a rich catalogue of automotive qualified SiC diodes and MOSFET
- Stable manufacturing processes with good intrinsic reliability data



OUTLINE

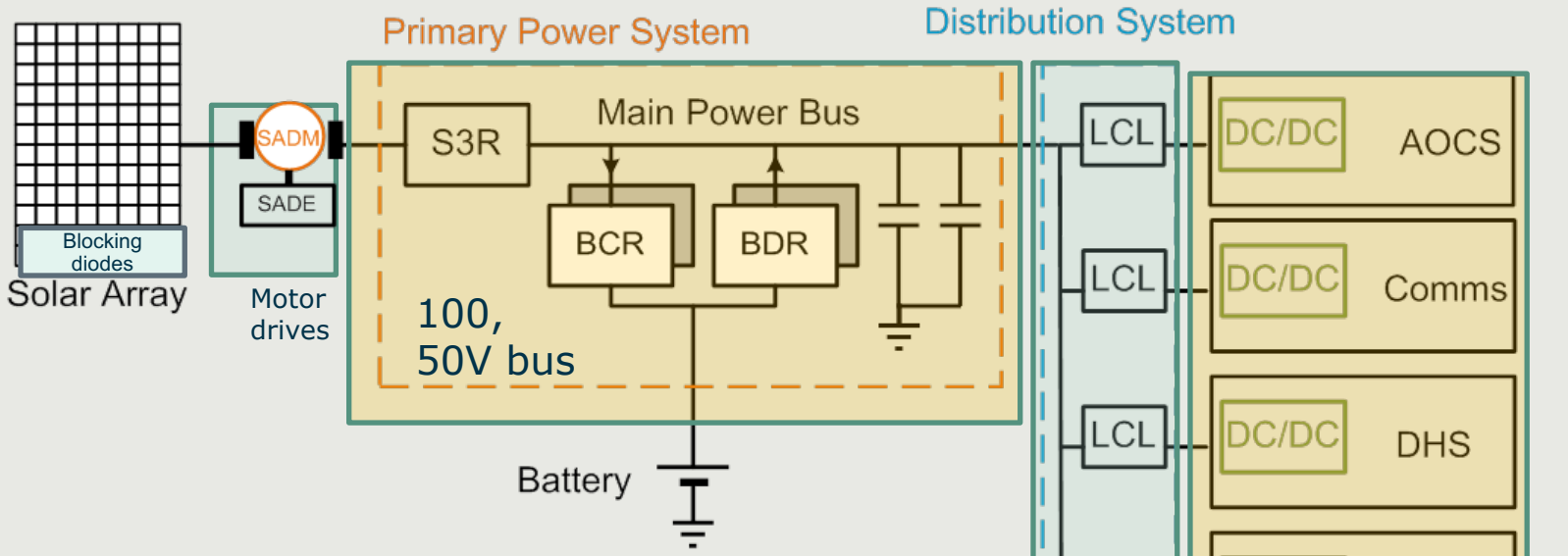
- WHERE SiC IN SPACE POWER APPLICATION

- WHERE SiC HAS BEEN USED
  - In orbit: Bepicolombo and Solar Orbiter
  - Baseline but still on ground: Juice GALA instrument
  - Future application under analysis: COMET I - MANIAC
- TRP studies main conclusions

- WHERE TO MOVE forward: Roadmap for introduction of SiC devices

WHERE SiC IN SPACE APPLICATION

Typical satellite Power System



GaN Low-Medium voltage 20-300V, medium power
F_{sw} ≈100KHz to 5MHz, good efficiency, miniaturisation

SiC High voltage ≥300V, high power (e.g. IGBT replacement)
Fsw ≈ 10-200 KHz, good efficiency, good thermal performance

DC/DC Electrical Propulsion

WHERE SiC IN SPACE APPLICATIONS

High power system trend: 300V power bus

- All future super high power applications that the primes are envisaging point at power levels above **80 kW**
- In this scenario the envisaged solution is a **300V power bus**
- The main power processing unit will need to deal with a total current value above **260 A**
- To minimise the number of power modules in parallel, a **high power efficient switch operating at 300 V and managing 50 A** will be needed. In this scenario around 6 modules in parallel will be needed, depending on the application
- **Electric Propulsion would benefit of HV power bus**: Dual Active Bridges (DAB) are now being baselined for PPU applications. In this case, the input bridge would operate at 300 V and the output bridge between 500 V and 2000 V. In terms of current level, the trend is to develop more and more powerful EP systems. It is plausible to have a power need per thruster in the order of 5 kW to 10 kW.

- NICHE APPLICATION: Instruments application when it is needed fast switching at high voltage to detect signals

WHERE SiC HAS BEEN USED: BEPI and SOLO blocking diode

- Development in the frame of Bepicolombo TDA, performed by CNM and Alter under TAS-I Turin – contract
- Schottky diode to be used as blocking at the end of a string of cells on solar panel for Bepicolombo mission: nominally forward biased and reverse biased in case of short circuit, polarized in reverse at V_R = other strings open circuit voltage
- Extremely harsh environment:
  - Sun intensities up to 10.7 times higher than in Earth's orbit lead to a operating range up to 270°C with 20°C of qualification margin
  - Eclipses during Mercury orbiting lead to more than 5000 cycles during operating life between -170°C and +270°C
  - Operative stresses induced by PCDU control technology, that is repetitive forward and reverse surge pulses. **$I_{rep\ pulses\ MAX}$=15A**

WHERE SiC HAS BEEN USED: BEPI and SOLO blocking diode

Requirements derived from typical application conditions:

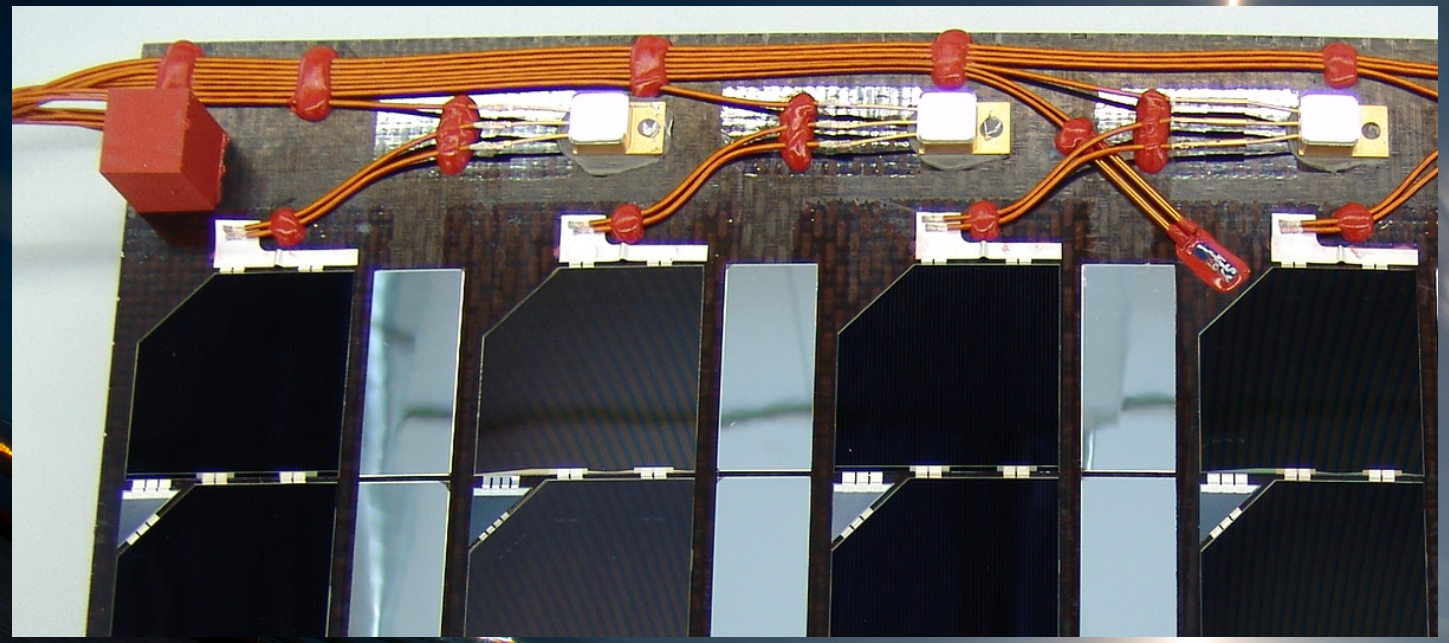
- The blocking diode is permanently forward biased when the Solar Array is illuminated:
  $I_{F\ max}$=5A
- **Reverse current Irev<150uA over the temperature range (-170C to +270C)**
- The package of the diode is **hermetically encapsulated** and **electrically isolated** compatible with the wide temperature range
- Assembly technique compatible with solar cell panel assembly technology
- Maximum reverse voltage in case of failure: **$V_{R\ MAX}$= 300V**

Programmatic challenges:

- Test set up adequate to reach such a wide temperature range
- Tight schedule

WHERE SiC HAS BEEN USED: BEPI and SOLO blocking diode

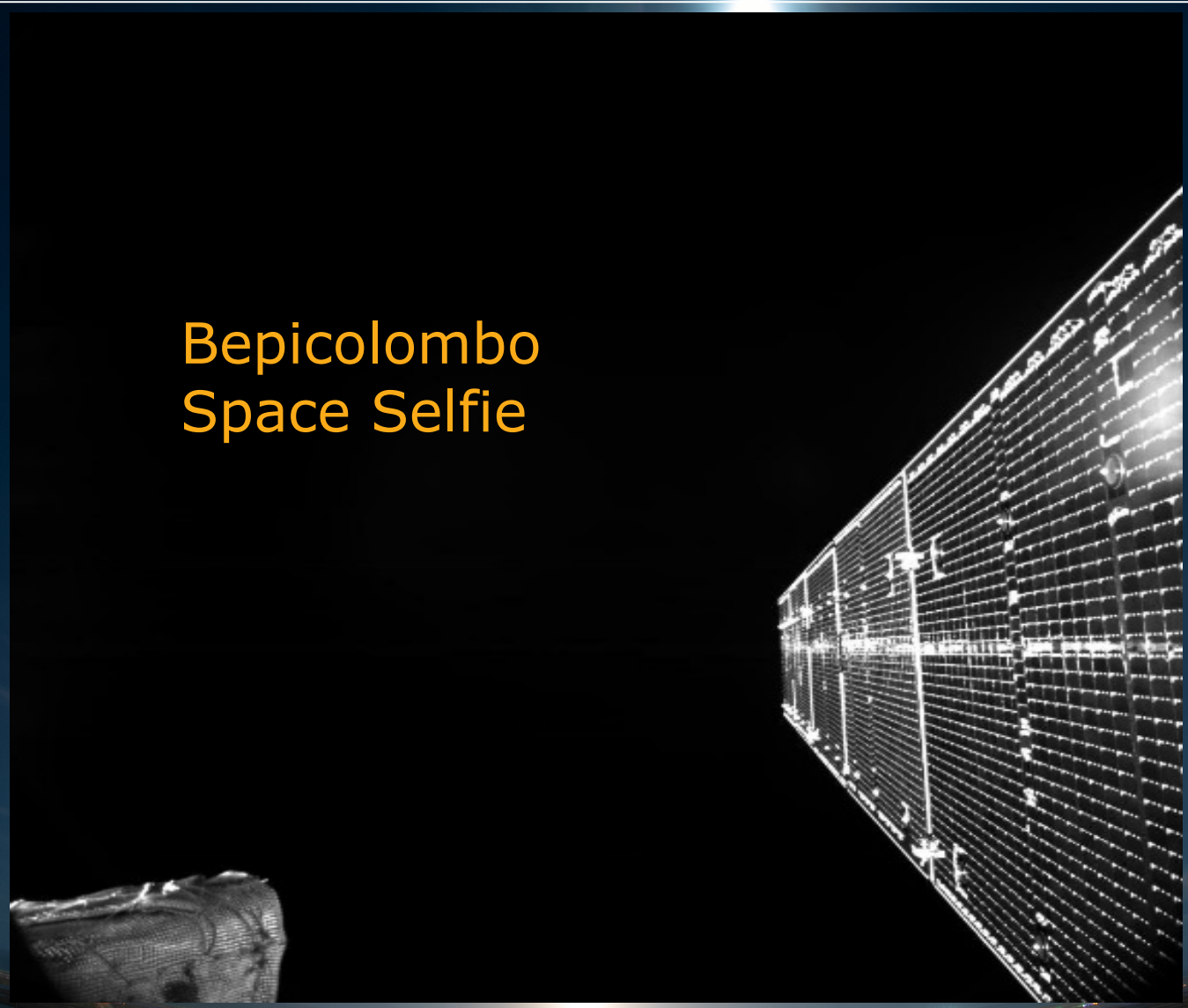
The major technical challenges were the development of a stable metallization of the die and the selection of the Schottky metal
The die attach was also optimised to minimise the thermal resistance and avoid hot spot



Bepi and Solo lots were qualified i.a.w. ESCC5000 modified for taking into account of the extended temperature range

EPPL part 2 listed:
SIC-HT-SBD01
5106/022

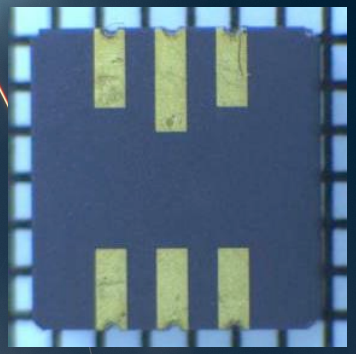
WHERE SiC HAS BEEN USED: BEPI and SOLO blocking diode

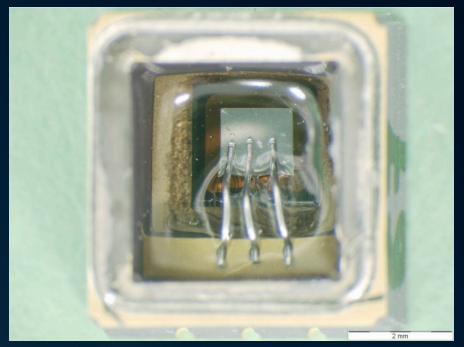


WHERE SiC HAS BEEN USED: JUICE – GALA APPLICATION

- Hermetic 1200KV SiC diode to be used in EPC for high temperature operation

SiC Diodes parameter	Target specifications
$V_{breakdown}$	1200V goal 1500V
I_f max at T_{op} max (case) ≥150°C	2A
I_r max @ V_r =1300V	≤10uA@25ºC ≤50uA@130ºC
V_f @ 0.1A	≤0.95V @ 25ºC ≤0.70V@100ºC
I_{max} non repetitive surge current	100A (t_{pulse}=10us)
I_{max} repetitive surge current	30A
C_{in} @400V, 1MHz	<30 pF
Qc @400V, 1MHz	≤20nC @ 25ºC <30nC @ T_j max
Trr (ns)	~ zero





PROTOTYPING AND CHARACTERIZATION OF
1.2KV SIC SCHOTTKY DIODES FOR TWTA APPLICATION:
THE CHALLENGE TO MEET THE USER SPECIFICATION

S. Massetti

D. Lopez, J. Moreno, E. Cordero

P. Godignon, J. Montserrat

J. Bevan

E. Maset, E. Sanchiz-Kilders

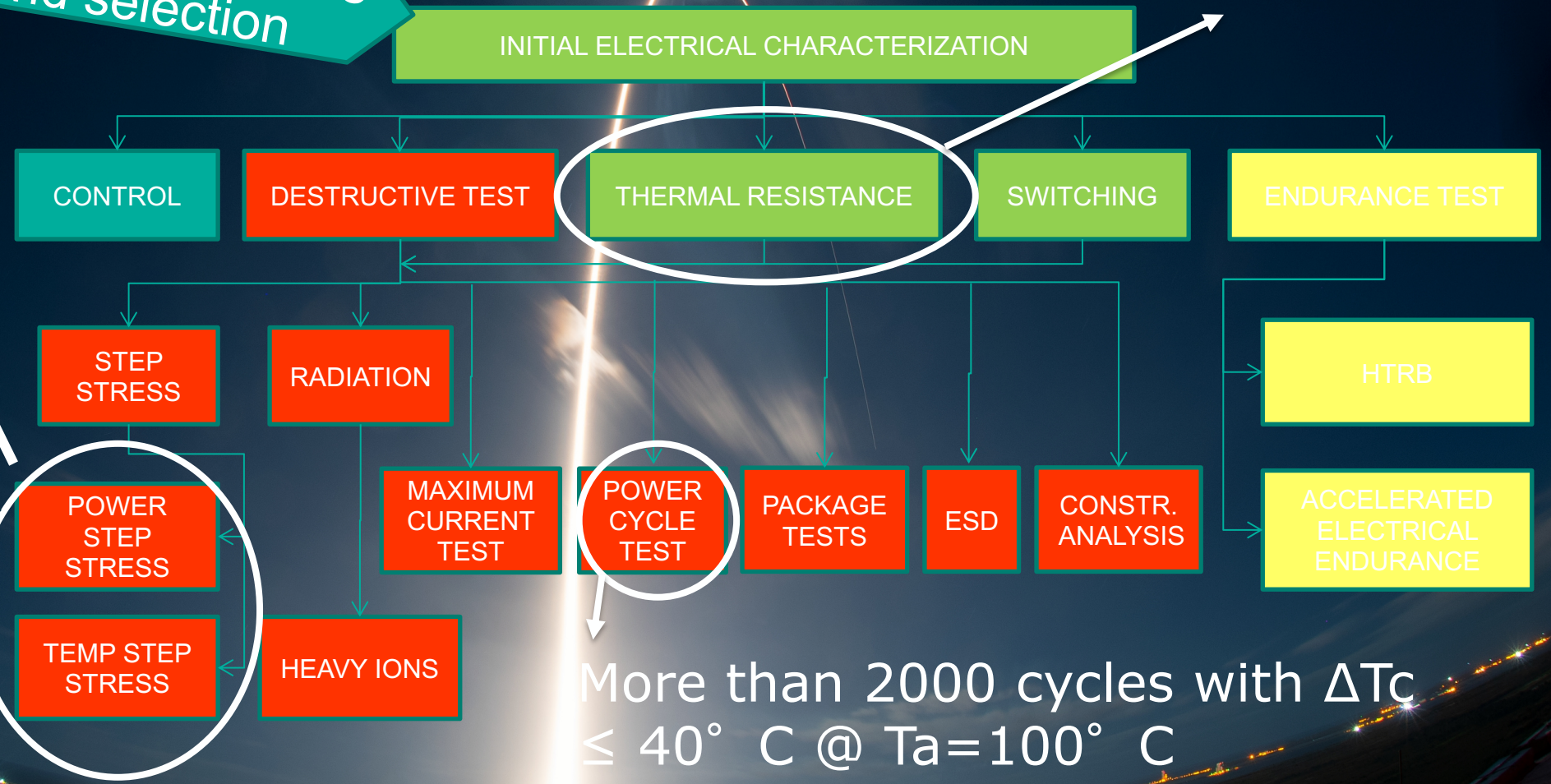
ESPC 2016 - Porto Palace , Thessaloniki 3-7 October 2016

WHERE SiC HAS BEEN USED: JUICE – GALA APPLICATION

On wafer screening and selection

To determine life test conditions

- No degradation of the devices up to 200ºC
- Degradation observed for temperatures of 215ºC and higher:
  - Increase in Vfwd
  - No changes in Irev
- To avoid thermal runaway: Pmax=4W



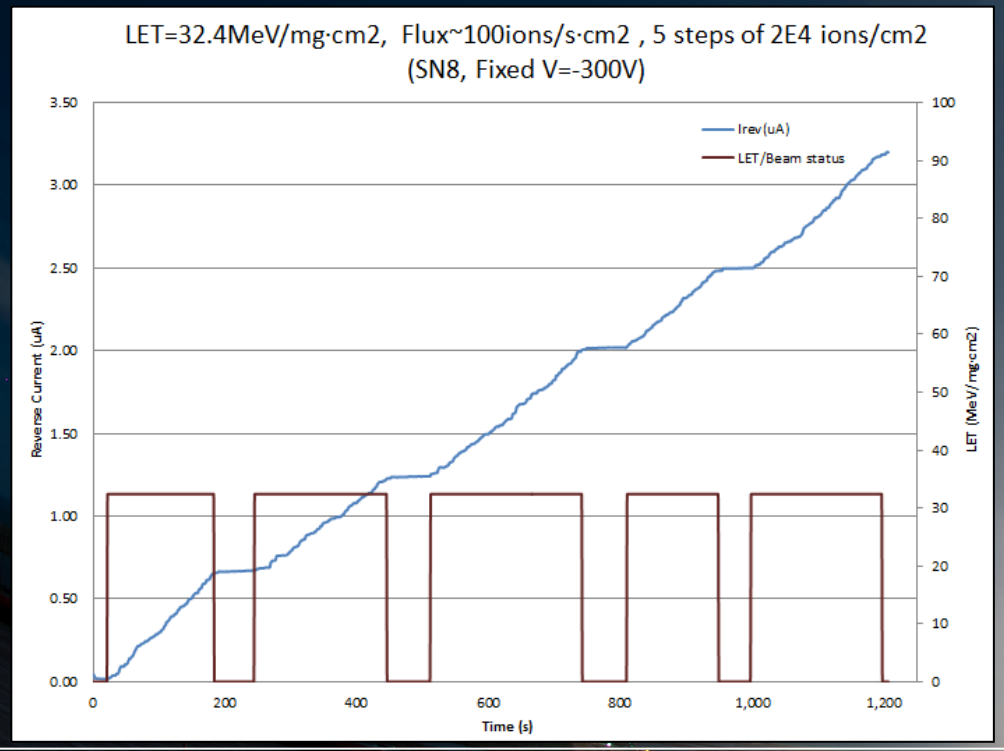
Rth(j-c) ≤85° C/W

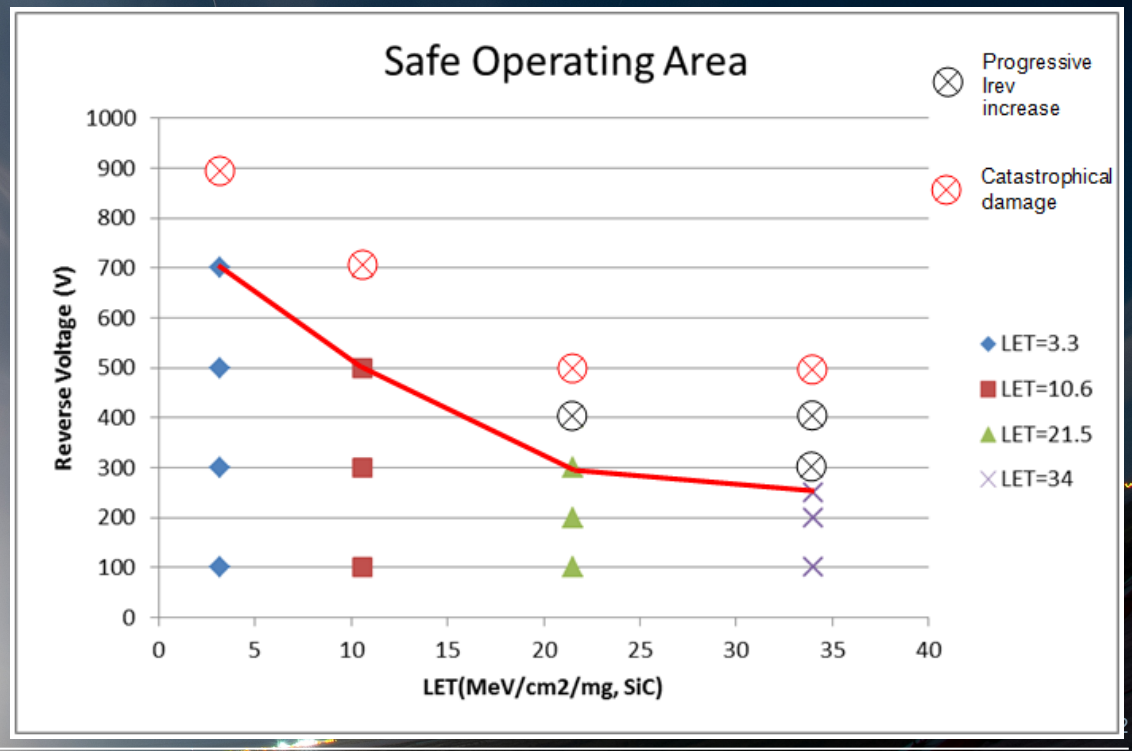
More than 2000 cycles with ΔTc ≤ 40° C @ Ta=100° C

WHERE SiC HAS BEEN USED: JUICE – GALA APPLICATION

- **Samples were sent to a potential user who confirmed that the developed diodes meet and exceed the performances they were requiring for prototyping the next generation of EPC**

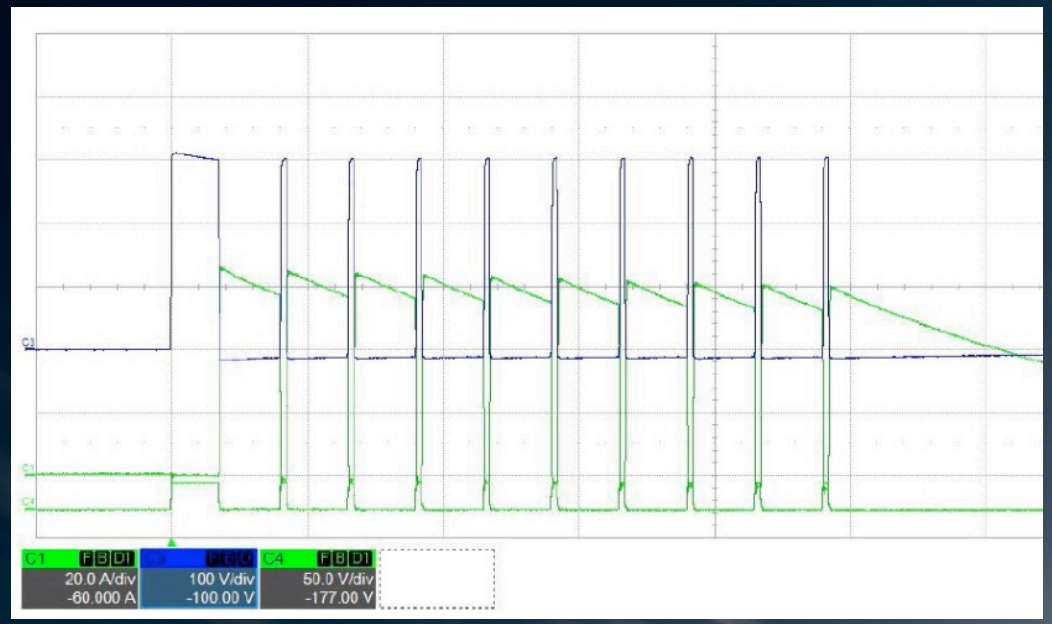
- **As expected the diodes showed heavy ions sensitivity: a general increase of Irev was observed and catastrophic failures as well at higher Vrev**



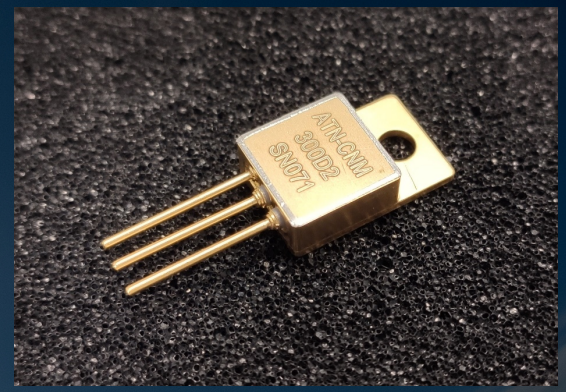


WHERE SiC HAS BEEN USED: JUICE – GALA APPLICATION

Gala instrument team contacted Alter to verify the possibility to use the TRP developed SiC diode



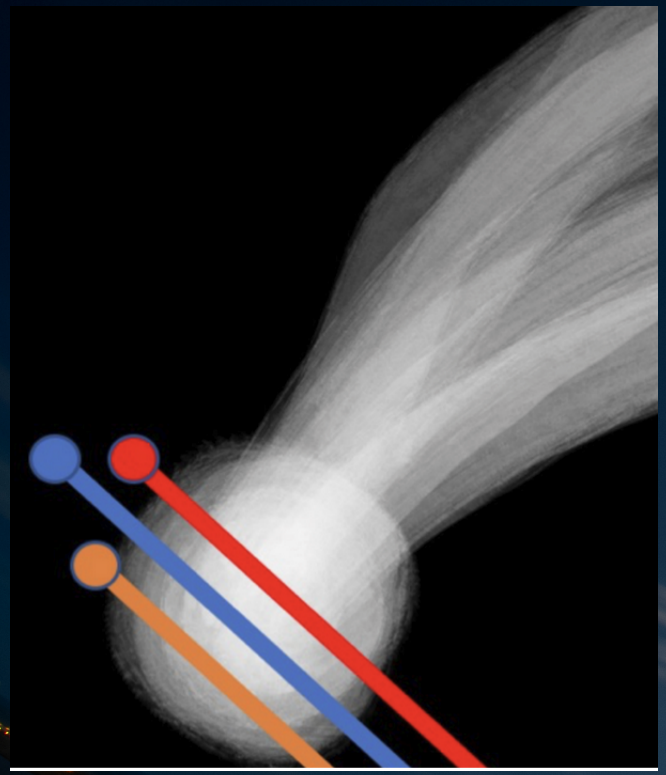
Trr<10ns
Vrev = 300V
Surge current I=64A flattens out to an Iavg=40A for 100µs every 20ms
duty cycle = 0.005



A new heavy ions test with representative GALA conditions were performed by Alter :
Vr max was increased to 360V , LET=46.1MeVcm2/mg, Fluence up to e+6 p/cm2
DUTs were submitted to HTRB after irradiation

DUTs passed the test without showing any sensible degradation.

WHERE SiC WILL BE USED: COMET I – Maniac case



SOME BACKGROUND:

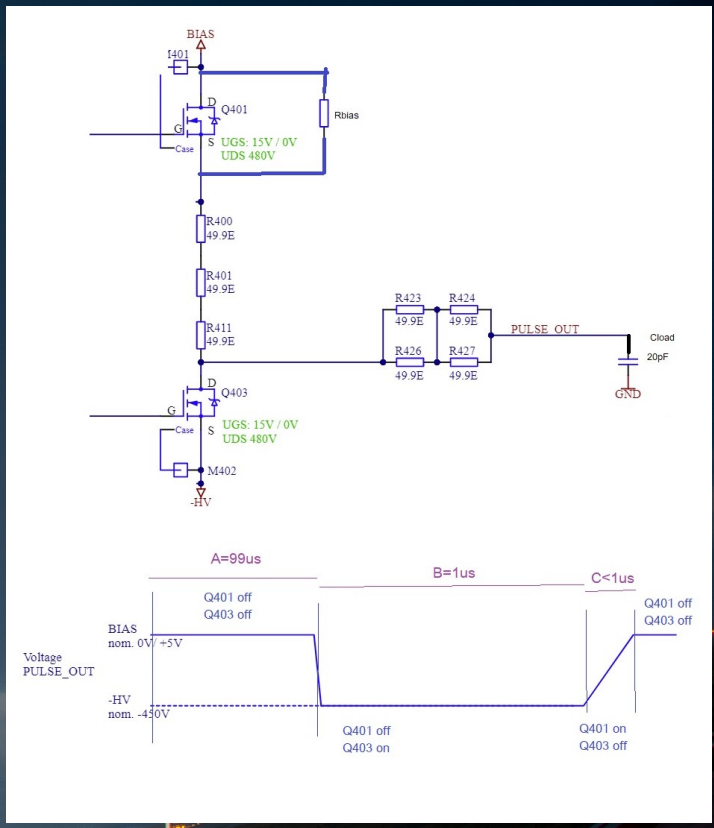
- The Comet Interceptor mission was selected by ESA in June 2019 as ESA's new fast-class mission in its Cosmic Vision Programme. Comprising three spacecraft, it will be the first to visit a Long Period Comet (LPC)
- Definition Phase (phase A/B) will end in 2022
- Comet Interceptor comprises three spacecraft. The composite spacecraft will wait at L2 for a suitable target, then travel together before the three modules separate a few weeks prior to intercepting the comet.
- Each module will be equipped with a complementary science payload
- **MANIaC**: *Mass Analyzer for Neutrals and Ions at Comets* - a mass spectrometer to sample the gases released from the comet is part of the ESA instrument suit of Spacecraft A

WHERE SiC WILL BE USED: COMET I – Maniac case

MANIAC instrument team contacted us to have some assistance on :

- Identifying a suitable high speed radiation tolerant MOSFET or
- Evaluating/radiation testing of a candidate part
- They did not find among the already space qualified Si MOSFET a candidate with the required performance

- *NMOS Breakdown voltage*
- *Vdss > 750V (before derating)*
- *Pulsed Drain current > 13A, during 10ns into capacitive load of 100pF*
- *Steady state current < 1uA*
- *Coss = < 20pF*
- *Switching speed > 100V/ns (falling transition)*
- *Pulse repetition rate 10 kHz*
- *Low Power Dissipation*
- *TID > 50 krad(Si)*
- *DSEE > 40 MeV/cm2.mg in silicon.*
- *Junction temperature range -55° C to 125° C.*
- *Footprint as small as possible*



WHERE SiC WILL BE USED: COMET I – Maniac case

- COMET I MANIAC will use the CPSA (Coordinated Parts Selection Agency) service to investigate the performance of COTS/ automotive qualified SiC MOSFET candidates

- No time /budget for a new development (both in terms of die or package design)

- For the trade off the main driver is the SOA for SEB/SEGR and in a second stage the compatibility to vacuum operation at high voltage

- The candidates will be selected based on electrical performances and voltage class from different manufacturer: both 1200V and 1700V SIC MOSFET will be tested

- The test will be mainly performed in flight operational condition (with margin) and the reliability of the survived DUT will be verified after irradiation

- **The main goal is to find a "good enough SOA"**
- **The main preference will be to rely to Automotive qualified components**

WHERE HAS BEEN USED: JUICE – GALA APPLICATION

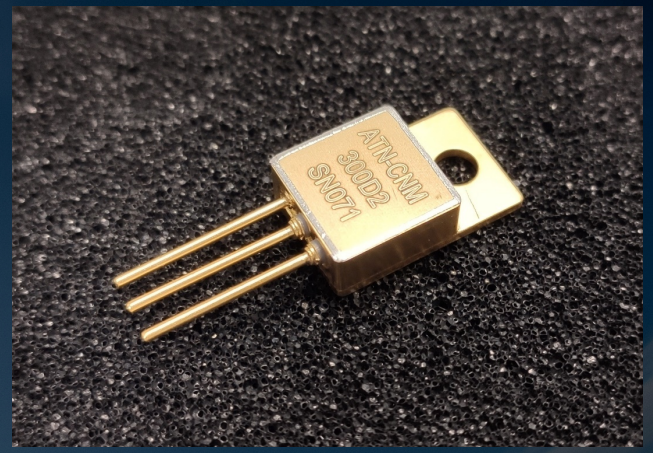
The dies were packaged in TO-257 in vacuum and without silicon gel

All dies were wire bonded with multiple wires in order to withstand the current pulses

All dies were submitted to CSAM before encapsulation to verify the quality of the die attach process

The lot was submitted to ESCC5000 qualification

All activities were coordinated/performed by Alter Technology



TRP studies main conclusions: SiC MOS structure with ST

TRP on radiation hardened SiC MOS structure with ST

GOAL: ***to study how each basic element of the MOSFET structure contributes to radiation sensitivity***

- This study shall be considered as preparatory work for the development of European radiation-hardened SiC power-MOSFETs
- TRP funded study with ST was kicked off in 2015 and concluded end of 2018
- Elementary structures have been manufactured and

have been submitted to:

- DC, AC, stability characterizations (in ST premises)
- TID test (in ESTEC TID facility)
- SEE test (in RADEF)
- FA on HI tested samples (in ST technological lab)

Paper was presented in ESPC2019

TRP studies main conclusions: SiC MOS structure with ST

MAIN OUTCOMES:

- Gate oxide on SiC is not more sensitive to SEE than Gate oxide on silicon lattice
- The PIGS and SEGR failures observed on SiC (as it has been observed on Si-Mosfet test vehicles) have to be linked with non optimized Body-Drain Junction for radiation
- High junction temperatures seems to improve the SEE response (statistics is however needed to confirm)
- The effect of epilayer and buffer layer resistivity and thickness on the SEE performances has to be deeply investigated

WAY FORWARD:

- A new study should be planned to evaluate thicker gate oxides (700Å and 800Å) and new epitaxial thicknesses in order to understand the right combination epilayer and buffer and their resistivity.
- A novel design of body-drain junction should also be investigated (similarly to what has been done in the past on Si-MOSFET).
- From testing methodology point of view, a test as you fly approach (i.e. switching) should be endorsed in parallel with the standard characterization approach.

WHERE TO MOVE FORWARD: Roadmap for introduction of SiC

The trend toward high power system and a 300V power bus shows that many applications will benefit from SiC technology already widely available on the market qualified in automotive grade and largely used in critical hybrid vehicle applications.

PRIORITY ACTION: to develop and evaluate a SIC MOSFETs power module based on automotive qualified technologies that will enable a number of high power high voltage applications in spacecraft

The envelope device should be able to operate in the following conditions:

- Power module with packaging solutions exploiting the automotive know-how
- 300 V to 500 V (free of SEB/SEGR)
- 20 A to 50 A
- 2 kHz to 100 kHz switching frequency
- Reliable and good performance at high junction temperature (175C to 200C)

WHERE TO MOVE FORWARD: CONCLUSION

RECAP OF THE MAIN CONCEPT:

FUTURE (2 to 3 years):

Design for a SEB free SiC MOSFET
- Improve the body-drain junction
- Optimize the gate thickness
- Optimize the epilayer/buffer thickness and resistivity
- Is trench design beneficial?

NOW:

Concept of good enough starting from automotive devices
- Test devices as you flight
- Derate!
- Verify stability of performance after irradiation
- SiC could be interesting even at moderate voltage for the specific performance : see e.g. blocking diode case