Small form factor Wirefree Die-On-Die WDoD™ technology used in 3D modules evaluation

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March 10th,2021
ESCCON 2021

Agenda

1. Company introduction
2. Flow 2 details
3. WDoD process description
4. WDoD evaluation for space applications
5. Conclusion

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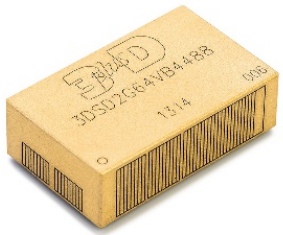
Corporate information

Space electronics solutions provider

- French Company founded in 1995
- Locations:
  - Buc, (Paris Area) France,
- People: 270 employees

Headquarters
Paris area, France

- Manufacturer of electronic products and System-in-Package for high reliability and high performance applications
- Production: 800 pcs / Week, delivery of 31 000 products in 2019
- More than 160 000 modules in space mid of 2019
- Business Regions: 35% Europe, 40% Asia, 25% North America.
- ESA and CNES approved manufacturing line for Space Applications
- ITAR Free products.
- Lines of space products: MEMORIES, INTERFACES, POINT OF LOAD, PROTECTION DEVICES, IP CORES, FPGA MODULE BASED ON NG-MEDIUM, MICRO-CAMERAS



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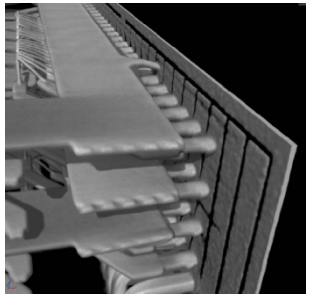
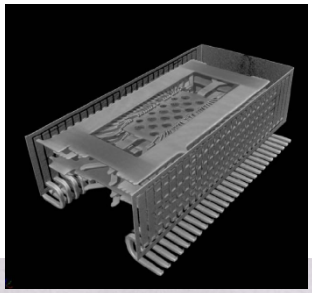
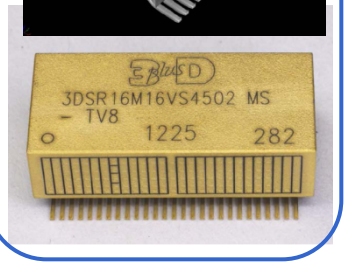
3D PLUS technologies overview

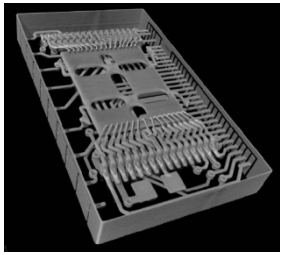
Flow 1: TSOP
→ Memory

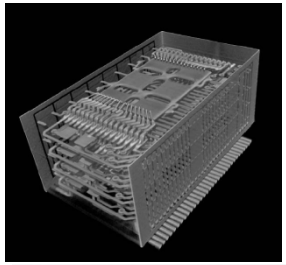


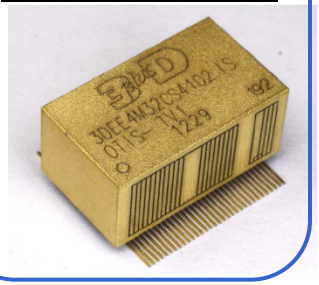




Flow 2: Packages
→ Other products & SIPs

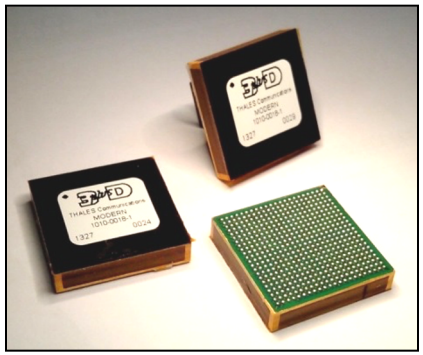




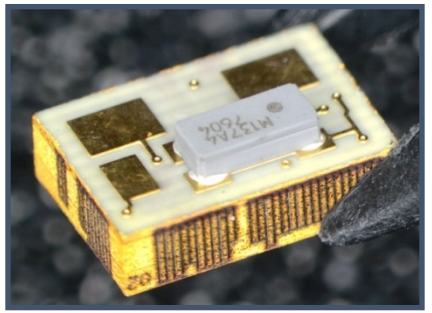


« SPACE QUALIFIED »

WDoD: New Technology



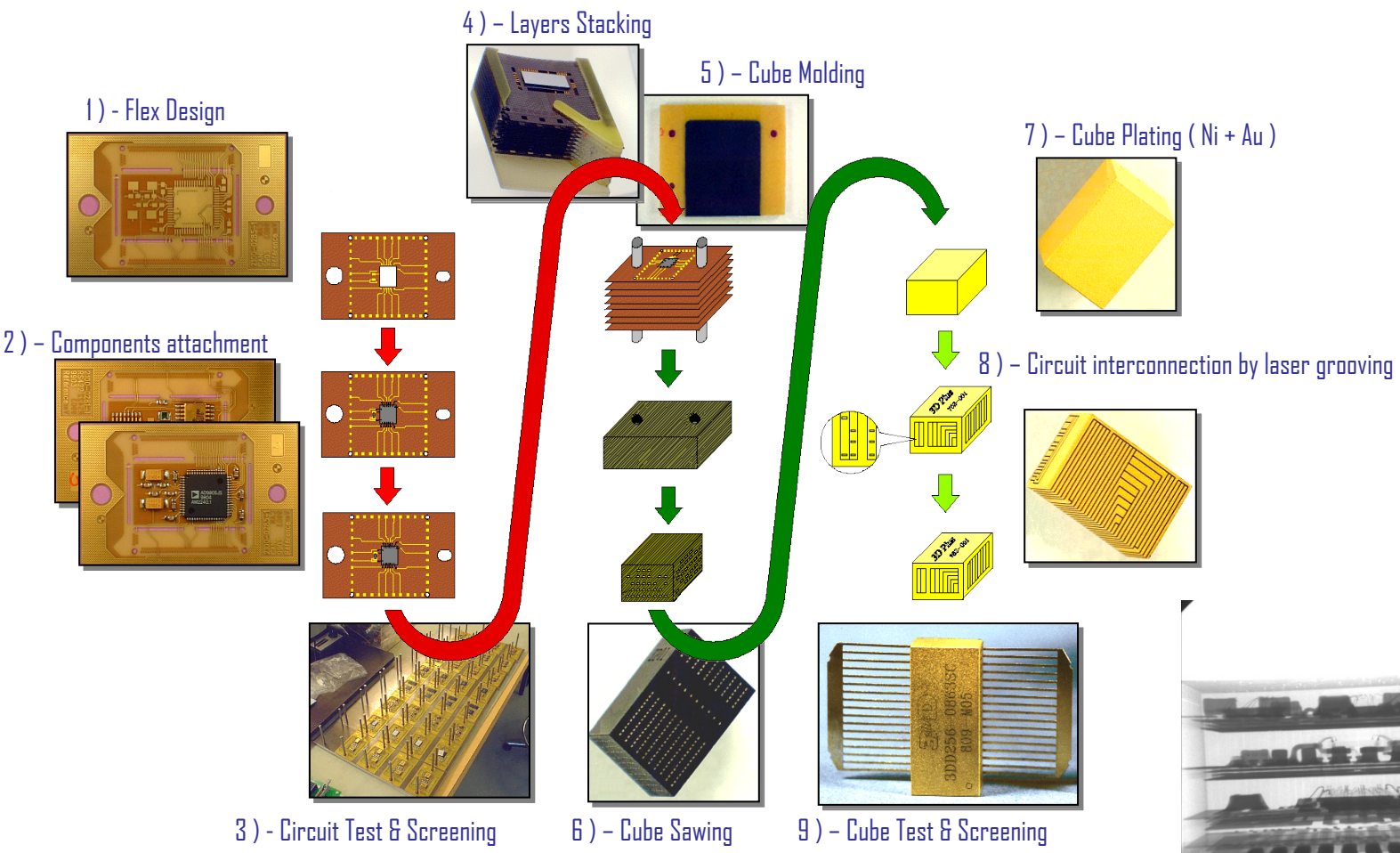
Ex 1: Computer core for THALES - July 2013 – Military applications



Ex 2: Leadless pacemaker for a European Customer – April 2013

« NON SPACE QUALIFIED »

Flow 2 Process



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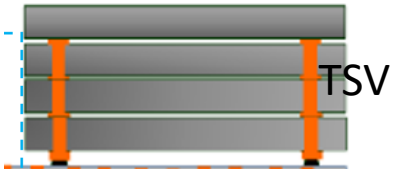
WDoD™ Technology

WDoD ™(1) initial criteria



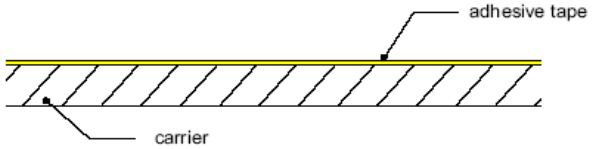
- Use of multi sourcing wafers
- Stacking of 5 to 10 levels per mm
- Size: 200µm around the larger Die
- Stacking of Known Good Rebuilt Wafer (KGRW)
- Possibility of several dice of different dimensions of the same level
- Parallel processing/Panelization from A to Z
- Possibility to stack PCB levels (flow 2) and rebuilt wafers in order to optimize performances and costs

(1) Wirefree Die on Die – Trade Mark from 3D PLUS

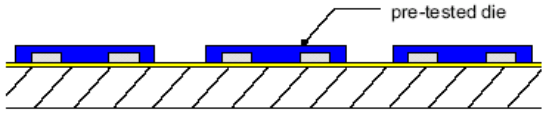
WDoD™ Technology

FLOW 3 " WDoD"

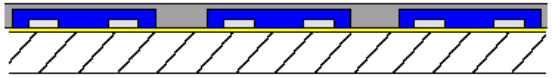
1 - Carrier lamination



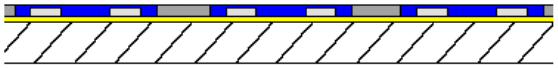
2 - Pick, Flip and place / Die on tape



3 - Compression Molding / Panel encapsulation



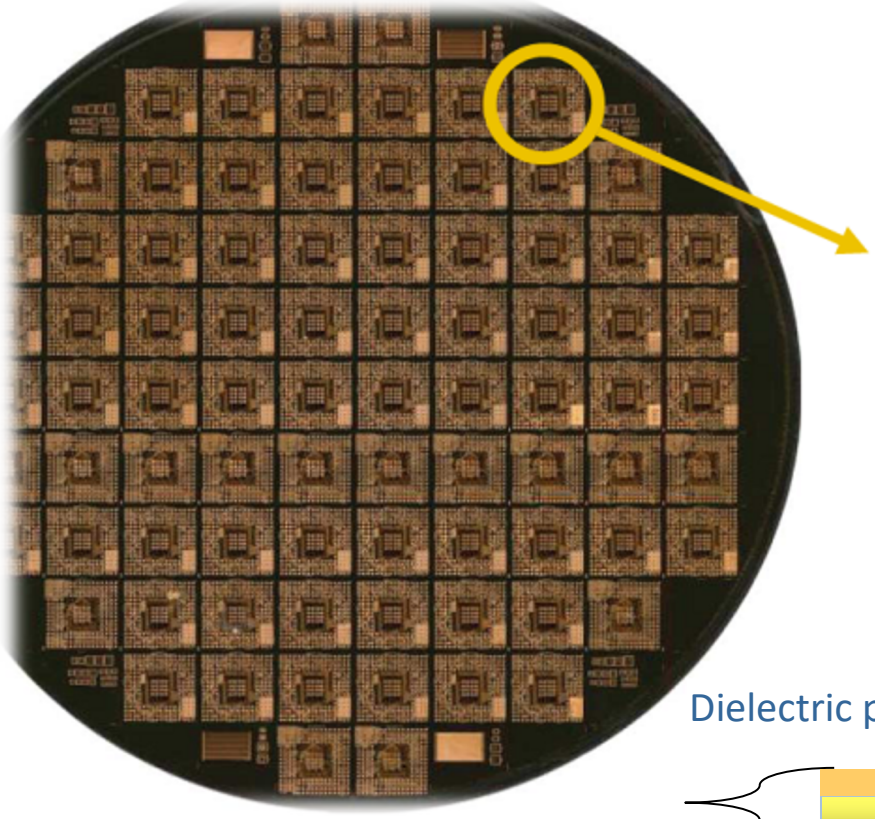
4 - Grinding (optional)

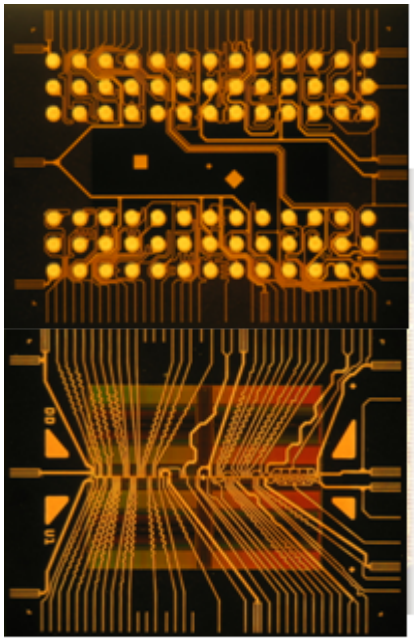


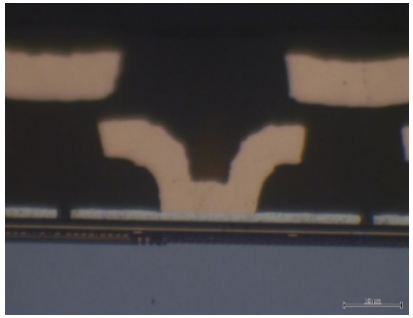
5 - De-taping

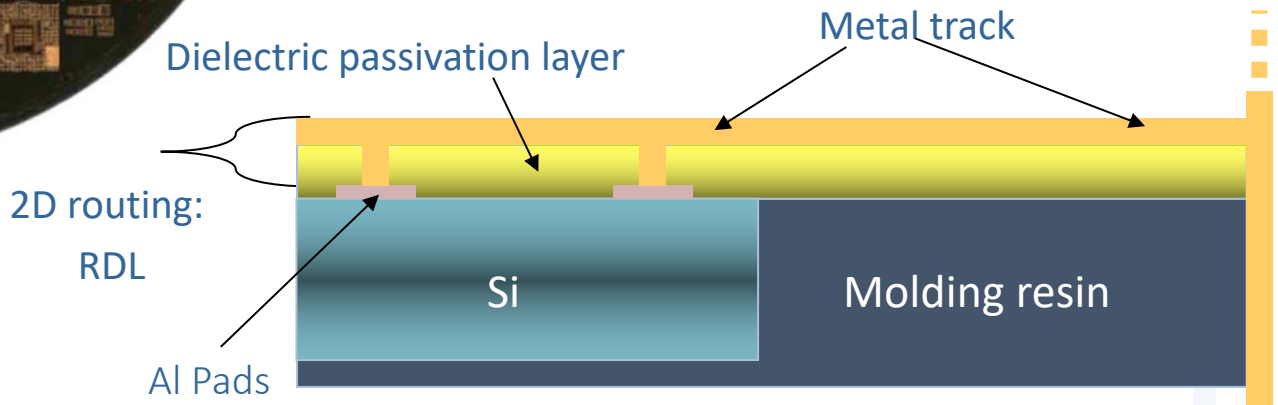
6 - Redistribution layer "RDL"

WDoD™ Technology





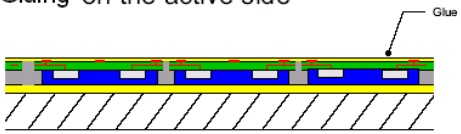




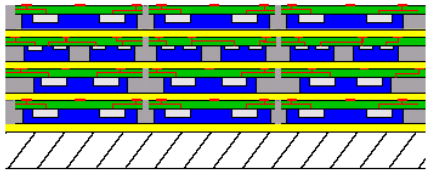
WDoD™ Technology

FLOW 3 **" WDoD"**

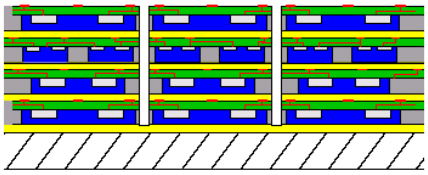
7 - Gluing on the active side



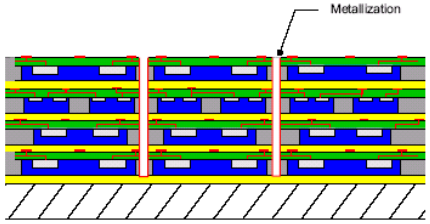
8 - Stacking of the "Known Good Rebuilt Wafer"

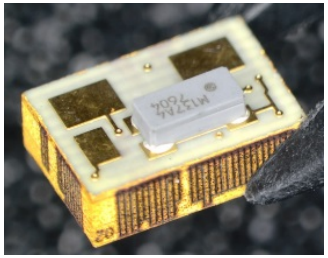


9 - Dicing of the rebuilt and stacked wafers

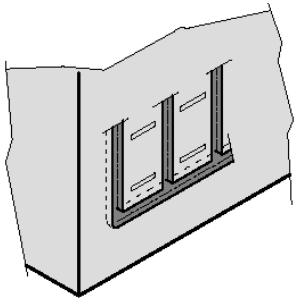


10 - Dicing street edges plating parallel process (electroless Ni + Au)





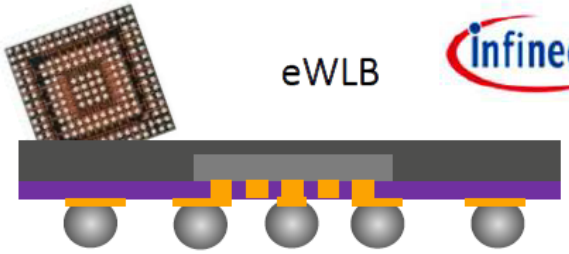
Laser patterning



Fan-Out main technologies and actors

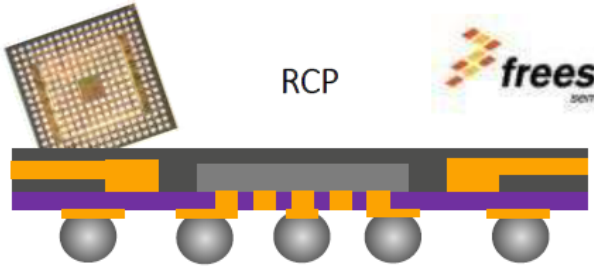
IMAPS 12th International Conference and Exhibition on Device Packaging

First Fan-out WLP Technologies



eWLB

Infineon



RCP

freescale semiconductor

STATSChipPAC

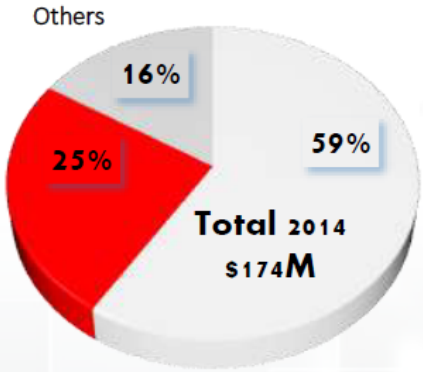
nanium

nepes

Wider adoption

nanium

Main products:
- Single Die: Mobile and Wireless
  - BB and Wireless SoC, RF, PMIC
- MCP/SiP products for Mobile (PMU), Industrial, Medical and Security applications

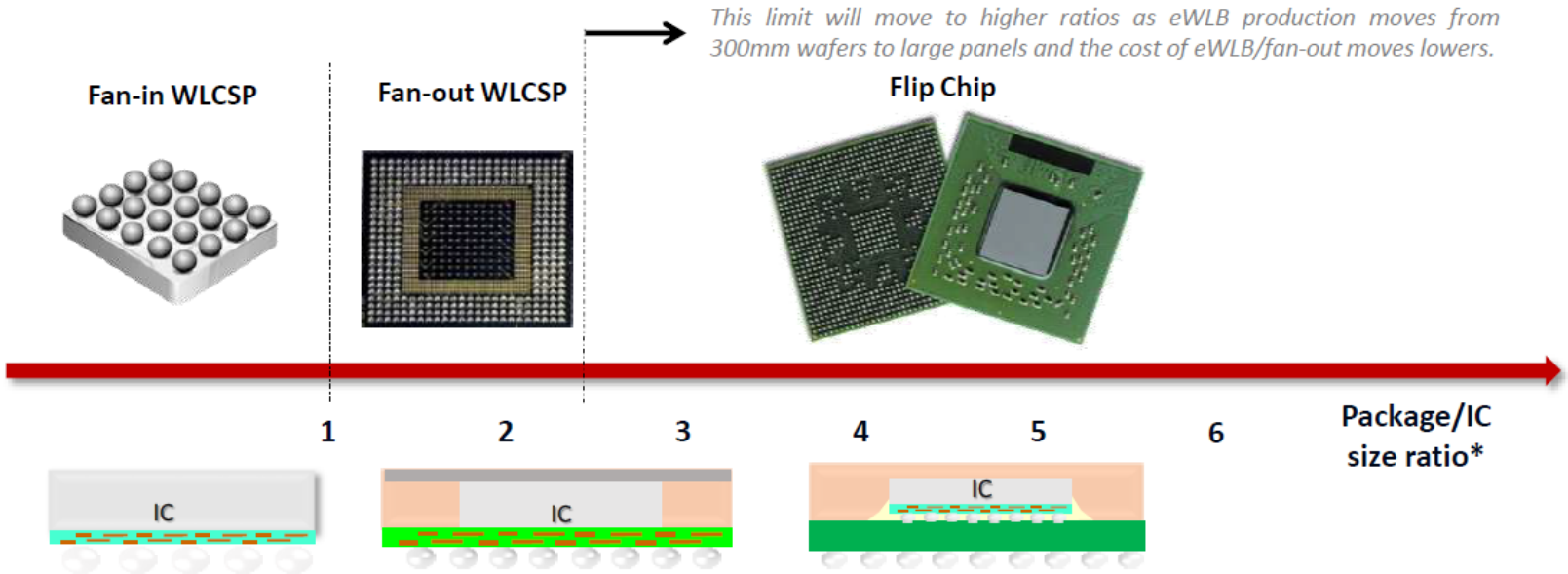


STATSChipPAC

Main products:
- Mobile and Wireless
  → BB and Wireless SoC
- RF Transceivers
- ASIC

Fan-Out position/Fan-In and Flip-Chip

Fan-Out vs. Fan-In and Flip-Chip



Advantages of Fan-Out

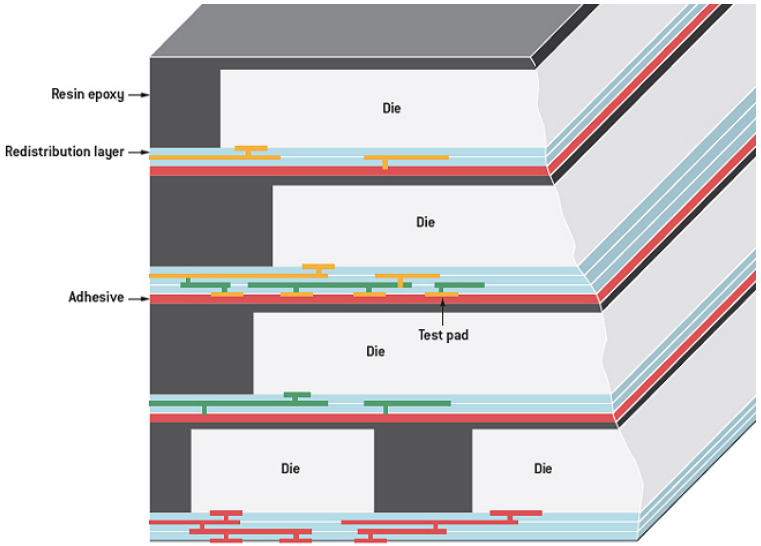
vs. Fan - In

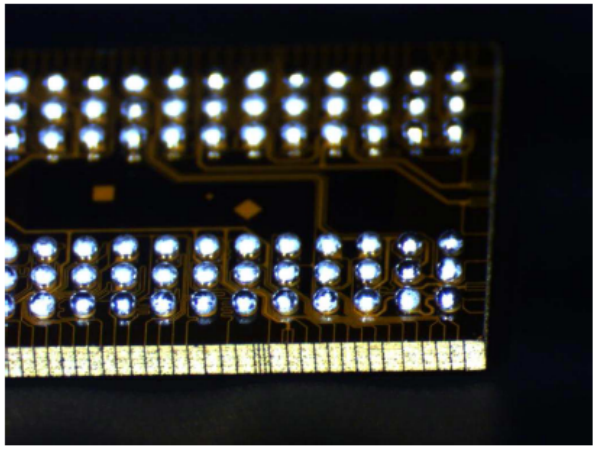
- Higher board-level reliability
- Bumping is not limited to the die size, fan-out area beyond chip area limitation
- Built-in back-side protection (protection available for WLCSP as an option only)
- Lower thermal resistance
- Higher potential for SiP integration

vs. FCBGA

- Smaller footprint
- No substrate/interposer ➔ Shorter interconnections
  - Higher electrical performance
  - lower cost
  - thinner package
- Lower thermal resistance
- Higher potential for SiP and 3D integration

WDoD™ technology

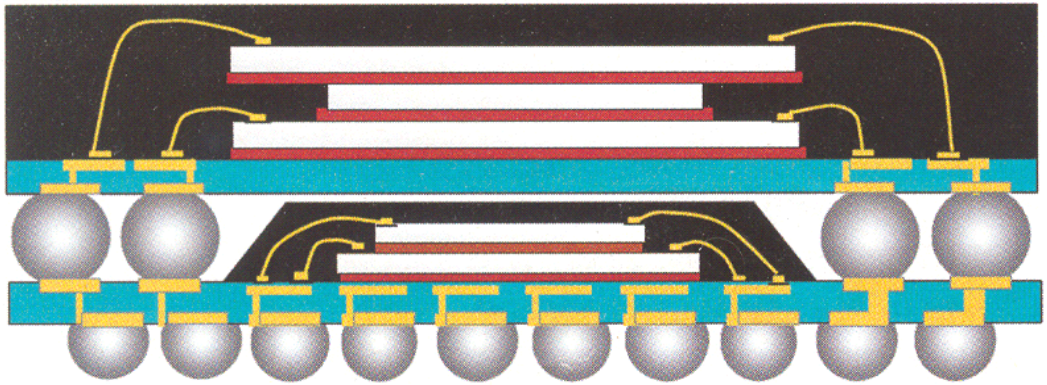


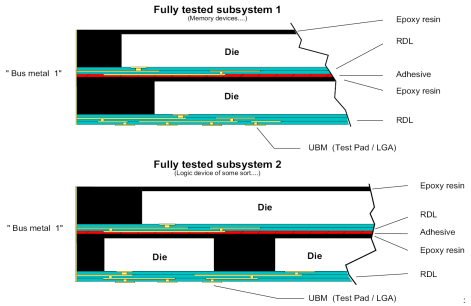


Similar technology than standard 3D PLUS technology

Huge shrinkage allowing small form factor components

WDoD™ technology





PoP and WDoD package relative sizes

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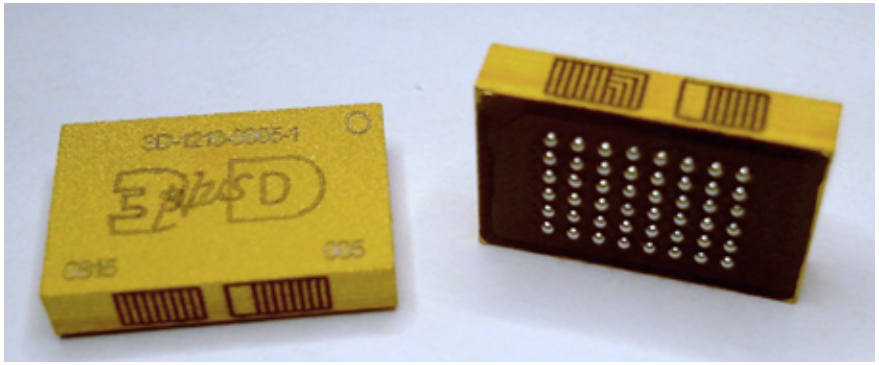
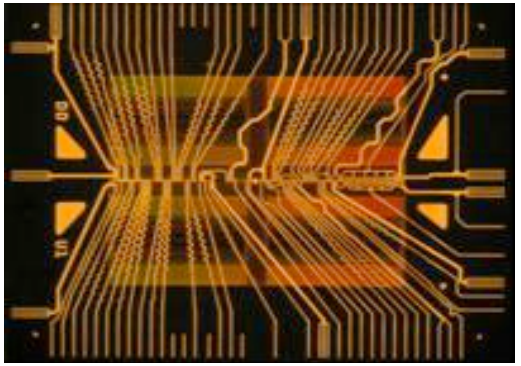
WDoD evaluation for space applications

Ojectives

3D PLUS has developed and patented for several years the WDoD™ process (Wire-Free Die on Die) for industrial applications (Quad-die DDR3 modules or modules including an FPGA, 2 mDDR). The photos below are examples :





Until now this technology has not been evaluated and qualified for a space application.

3D PLUS, with the support of CNES (French government space agency), evaluated following the ESCC2566001 specification this process in order, among other things, to identify design rules and reliability.

WDoD evaluation for space applications

Benefit

- This 3D technology allows a form-factor reduction which can be of high interest for space applications
- Main interest is the reduction of each level thickness :
- **-from 1-1.2 mm (with die on PCB) versus 0.2 -0.3 mm (WDoD™)**

- Others advantages are:
  - the connexion lengths reduction and a good alternative to flying leads PCBs.
  - No lead free packages inside the module

WDoD evaluation for space applications

Test Vehicles : SRAM Module

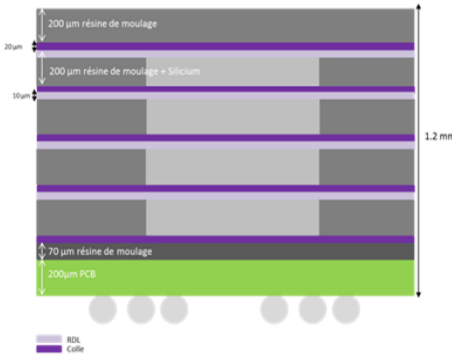
A demonstrator of 4 levels of SRAM dies has be designed and manufactured for this evaluation

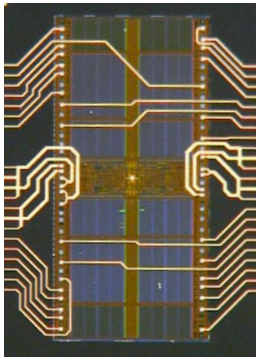
MODULE

- The SRAM module containing four chips stacked is manufactured using WDoD technology.
- There is a 200µm thick resin cover, a 200µm connection level (PCB) as well as 4 levels "reconstituted wafer" with RDL. The RDL level is common to each of the 4 levels.
- 2 providers have been tested
- Module dimensions are 6,5 x 9,5 x 1,7 mm
- Module bus metal laser pitch is 250 µm

STEPS

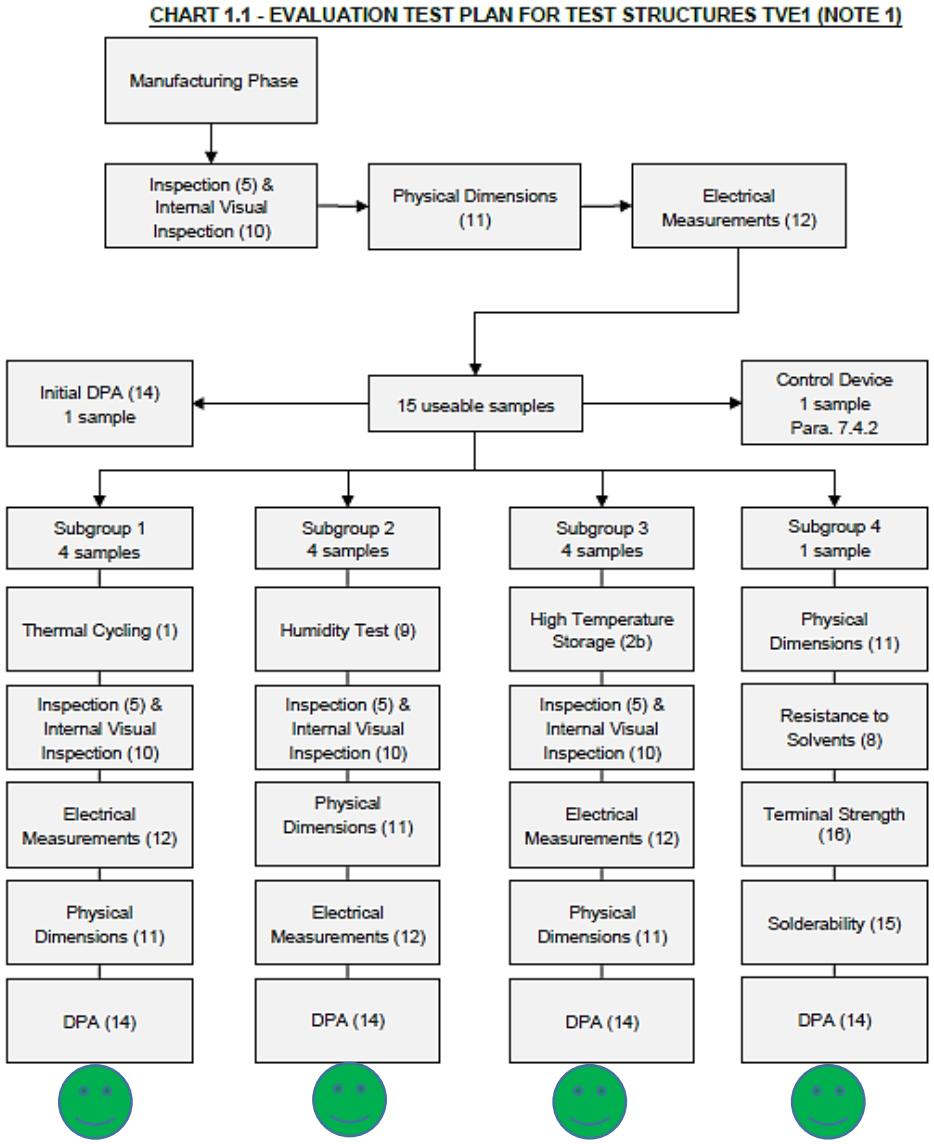
- 1 level and module demonstrators manufacturing and electrical continuity tests
- Pré -evaluation tests with failure analysis
  - MSL 5
  - Thermal cycling TCT 1500 cycles (-55;+125°C)
  - High Temperature Storage HTS 2000Hrs @125°C
  - THB 1000 hrs 85°C;85 %HR





WDoD evaluation for space applications

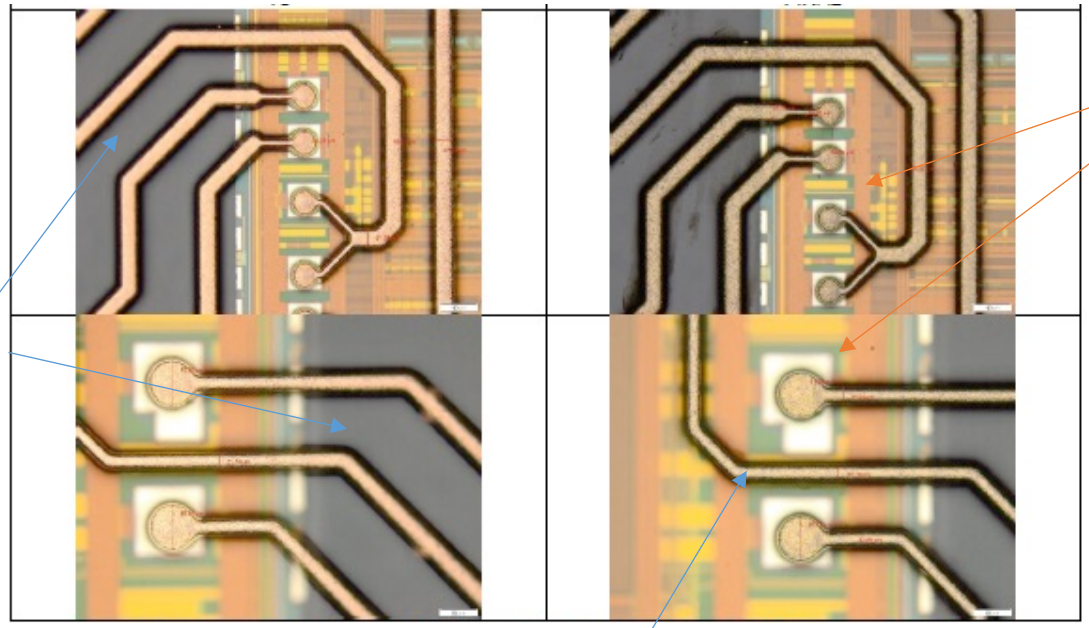
Component level Tests : 1 level 2D panel with RDL



2D panels evaluation was successfull

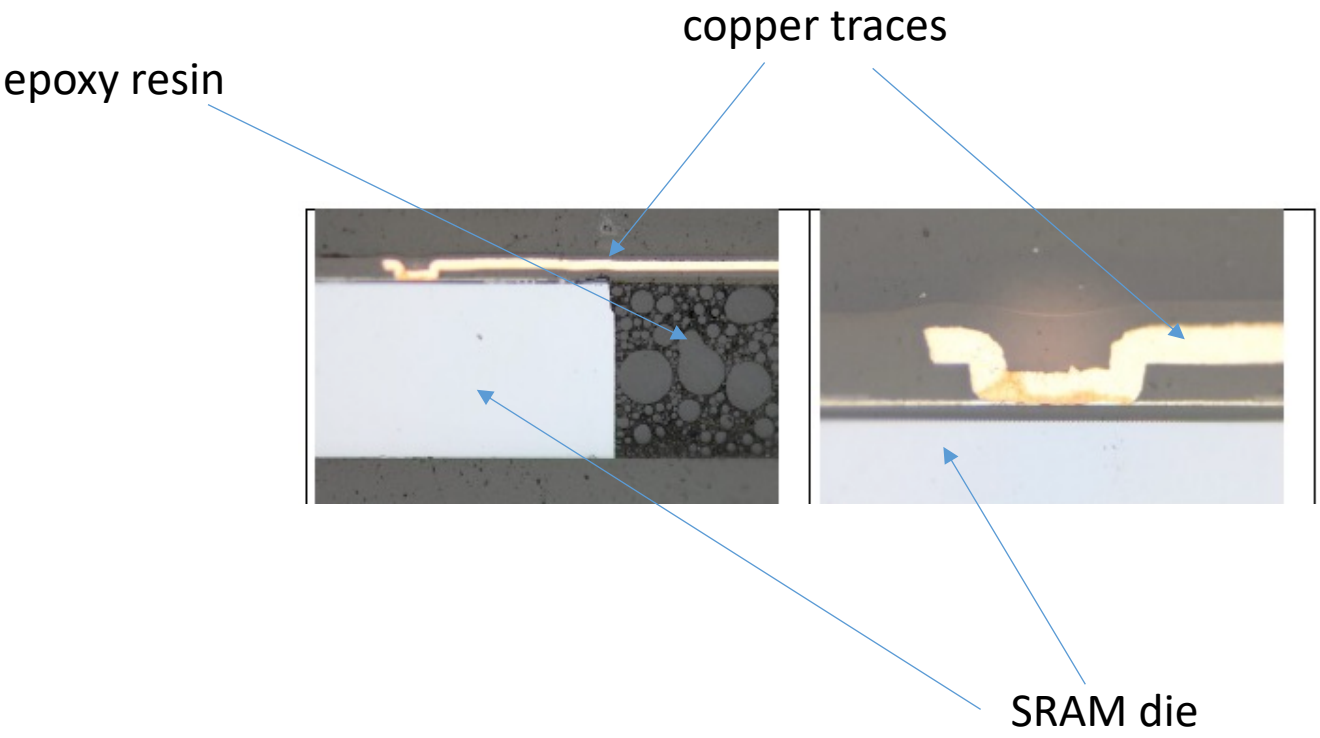
WDoD evaluation for space applications

2D level top view



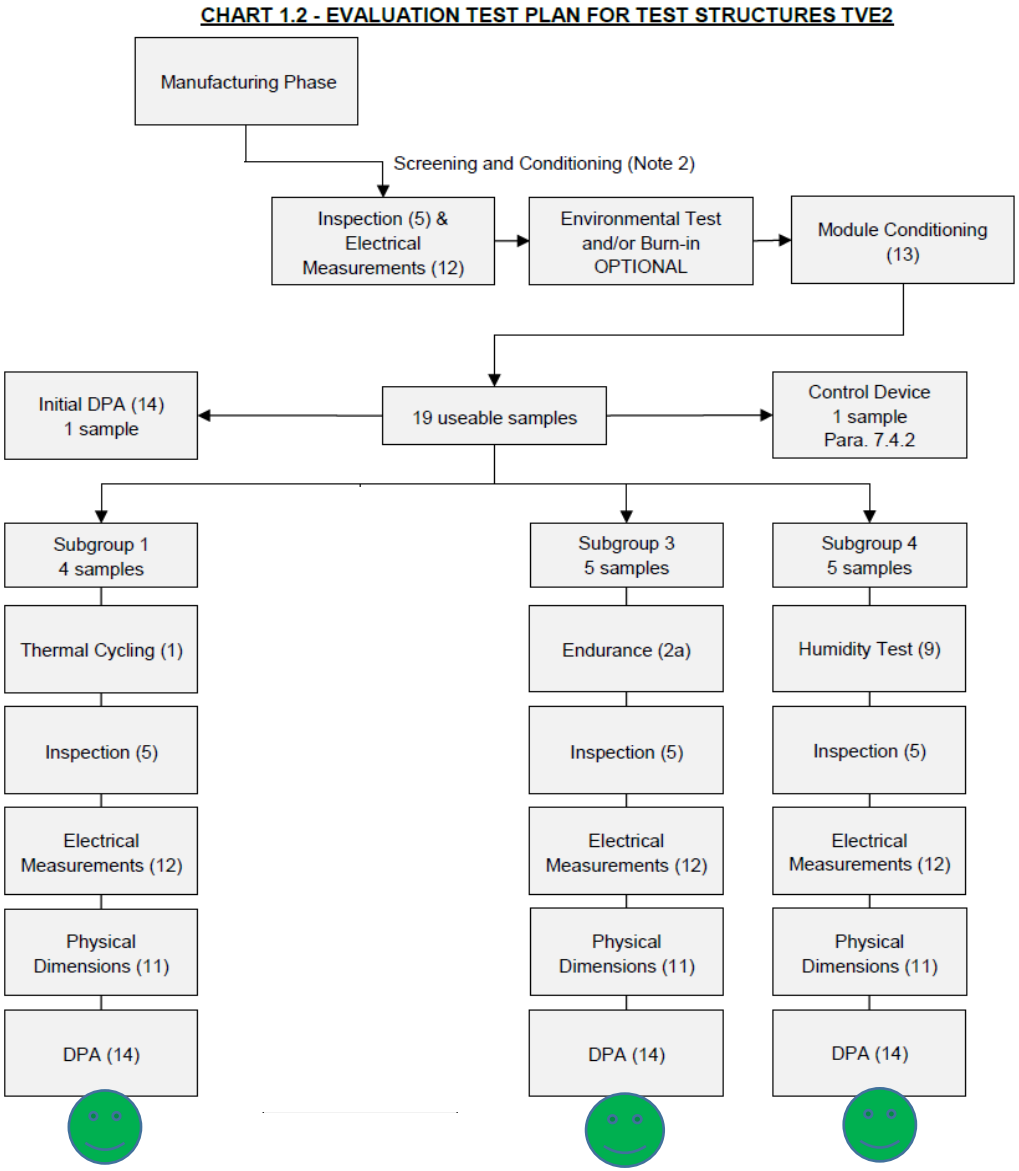
WDoD evaluation for space applications

2D level cross section



WDoD evaluation for space applications

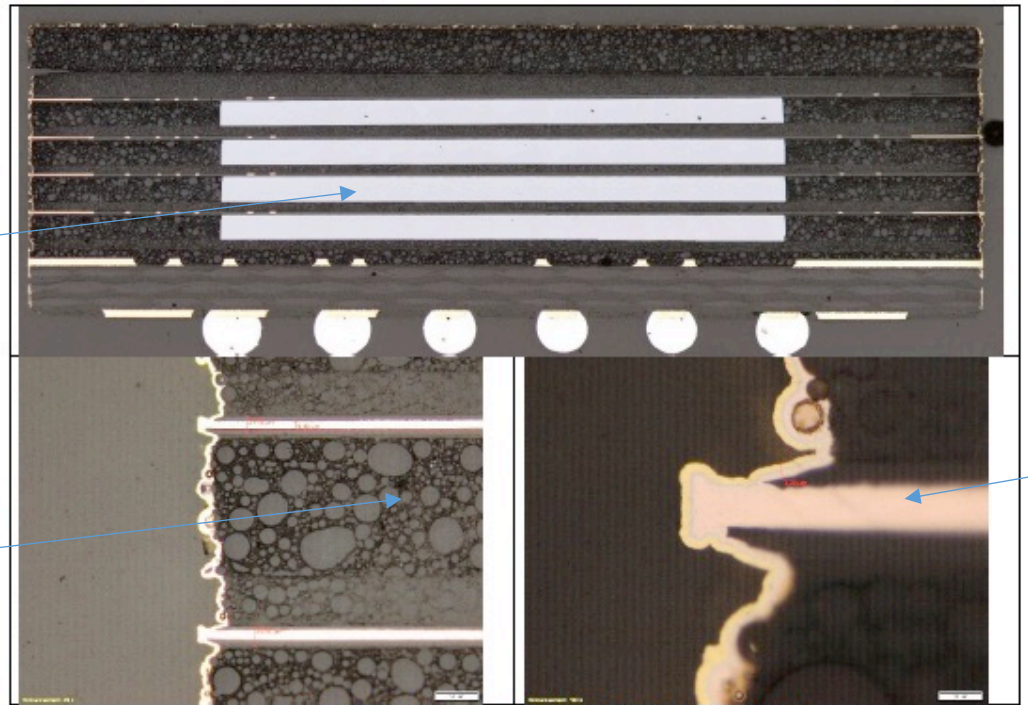
Module level Tests



3D modules evaluation was successfull

WDoD evaluation for space applications

3D module cross section



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Conclusion- Next steps

- A 3D demonstrator consisting of 4 levels of SRAM dies was designed. Two sub-contractors in charge of manufacturing the RDL (Redistribution Layer) have been selected.

- A batch of demonstrators was manufactured and submitted with success to evaluation testing plans based on the ESCC 2566001 specification

- Next steps scheduled through a new RT funded by CNES :
  - Process and materials modification for more heterogeneous module including Fan-Out levels with 2 copper layers and PCB levels

- 3D PLUS acknowledges CNES for his support in this RT