



GR740 Plastic BGA Development

Overview Presentation

Date: 2021-03-11

PUBLIC



Abstract

- Strong demand to reduce cost for space electronics including EEE components, especially for telecom constellation programs
- Done by employing methods, materials and techniques used for commercial and automotive industry, e.g. organic packages
- Development objective:
 - Assemble existing GR740 die in suitable organic package
 - Process it through an adapted test flow
 - Perform an evaluation demonstrating the capability to reach required standards for telecom constellation programs.

PUBLIC



Agenda

- About Cobham Gaisler (CG)
- Introduction to GR740
- Scope
- Project organization
- Milestones
- Evaluation activities
- Conclusion





A world leader in embedded computer systems for harsh environments



Experts in fault-tolerant computing



We provide a full ecosystem to support hardware and software design for:

- Standard components
- Semi-custom FPGA
- Full custom ASIC



Based on SPARC and RISC-V architectures







Components

High-reliability

Radiation hardened

Space qualified

Fault-tolerant

NOEL Processor Family

• GR7xv, NOEL-V, 16-Core, in development

LEON Processor Family

- GR765, LEON5FT, in development
- GR740, LEON4FT, quad-core, 250 MHz, QML-V approval exp. Q2 2021
- GR740 PBGA, LEON4FT, quad-core, 250 MHz, prototypes Q2 2021
- GR716A, LEON3FT, single-core, 50 MHz, ESCC 9000 screening exp. Q2 2021
- GR716B, LEON3FT, single core 100 MHz, in development
- GR712RC, LEON3FT, dual-core, 100 MHz, Vendor class S
- UT700, LEON3FT, single-core, 166 MHz, QML-Q, QML-V
- UT699E, LEON3FT, single-core, 100 MHz, QML-Q, QML-V
- UT699, LEON3FT, single-core, 66 MHz, QML-Q, QML-V

Interconnect

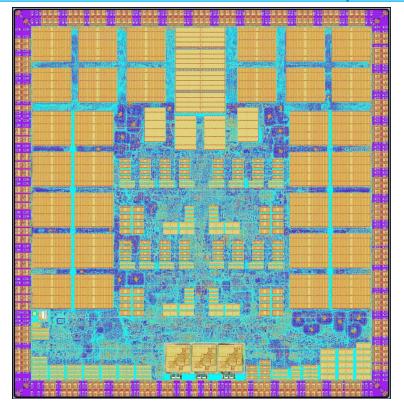
• GR718B, Vendor class S

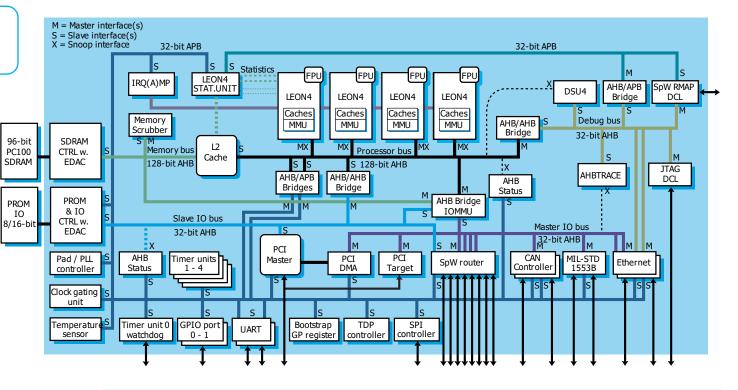


Introduction to GR740



Radiation-hard system-on-chip quad-core fault-tolerant LEON4 SPARC V8 processor





Cobham Gaisler digital IP: LEON4FT and IO peripherals
STMicroelectronics C65SPACE technology platform
Complete software toolchain and debuggers are available





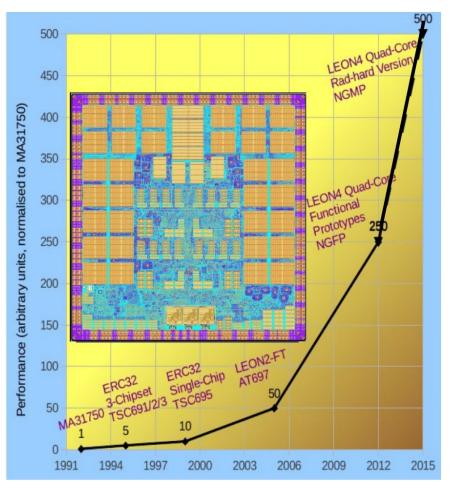


https://www.gaisler.com/

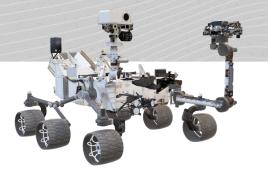
Introduction to GR740



Power <2.0W, Performance >1700 DMIPS



Ref: Roland Weigand. GR740 User day presentation: "from concept to product NGMP to GR740"







GR740 - IPAC Computer for the Platino mission



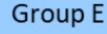
GR740 - WFIRST Processor Board



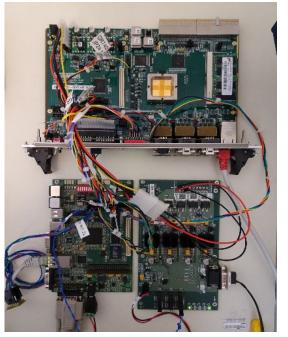


Introduction to GR740. Radiation results











- TID tolerance of 300 krad(Si)
- Overall SEE rate below 1x10⁻⁵ events/device/day (GEO)
- SEL > 125 MeV.cm²/mg (T>85°C & max supply)





Introduction to GR740







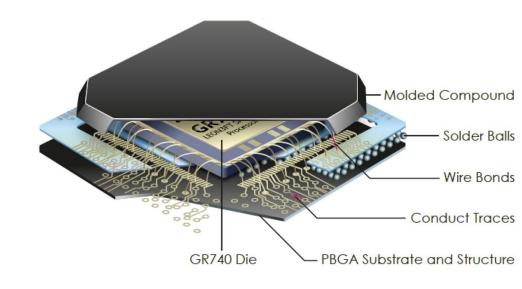
ESA's next generation Microprocessor (NGMP) development time-line:

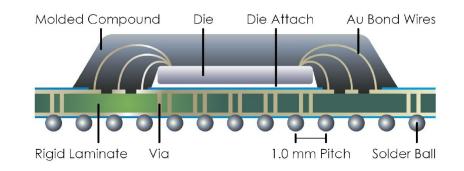
- Ceramic
 - 2009, Start of the development under a TRP contract with ESA (VHDL design and verification by simulation on FPGA).
 - 2014, Implementation of NGMP into a space chip technology (C65Space).
 - 2016, Engineering models of the GR740 were evaluated.
 - 2018, Flight Silicon manufactured and validated (including radiation).
 - 2020, All QML-V related qualification tests successfully completed.
 - 2021-Q2, QML-V and QML-Q certification by the DLA expected
- Organic (GR740PBGA)
 - 2020-Q1, Start of the development under an ESA ARTES Competitiveness & Growth contract
 - 2021-Q1, First electrical samples being validated

Scope of ARTES program



- Cobham Gaisler to develop the quad-core LEON-4 GR740 in plastic package
- Same wafer material used as for the ceramic package product i.e. full traceability
- Re-use lessons learnt and heritage from the ceramic package project
- Perform an evaluation demonstrating the capability to reach required standards for telecom constellation programs.





Project organisation



Prime contractor

- Cobham Gaisler AB, Sweden
 - Product owner



- Synergie CAD PSC, France
 - Overall responsibility for electrical testing, mechanical screening and evaluation activities
 - Design and fabricate;
 - The test load board
 - The HTOL system
 - The THB board
 - Adapt the production test program
 - Interface towards ST Microelectronics
- ST Microelectronics, France
 - Responsibility for supply of dice, substrate and package design and assembly





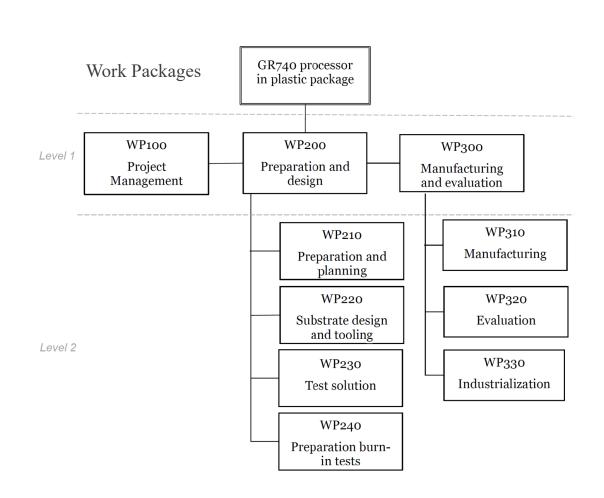




Achieved Milestones

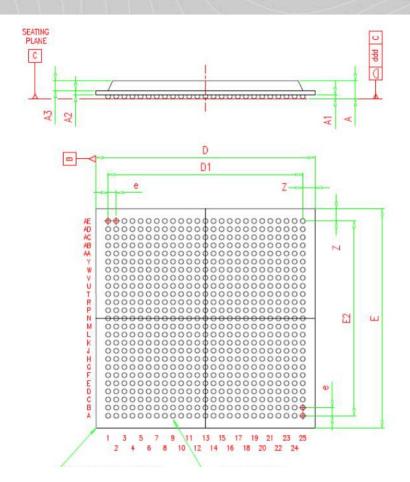


- Package drawing
 - Body size: 27*27mm, 625 balls
 - Solder ball pitch; 1 mm
 - Same footprint as ceramic package and pin-compatible
- BOM
- Electrical & thermal simulations
- Load board, THB and HTOL boards developed
- First samples have been manufactured and electrically tested



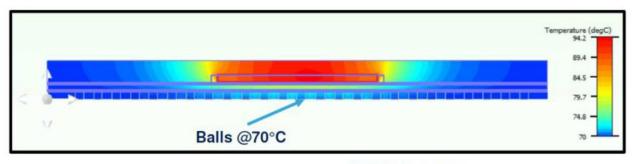
GR740PBGA package

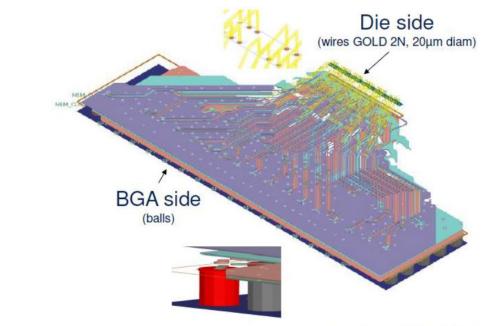




- Same footprint as ceramic package and pincompatible
- 4-layers substrate
- SACN306 balls

 Thermal and electrical simulations of the package performed by ST

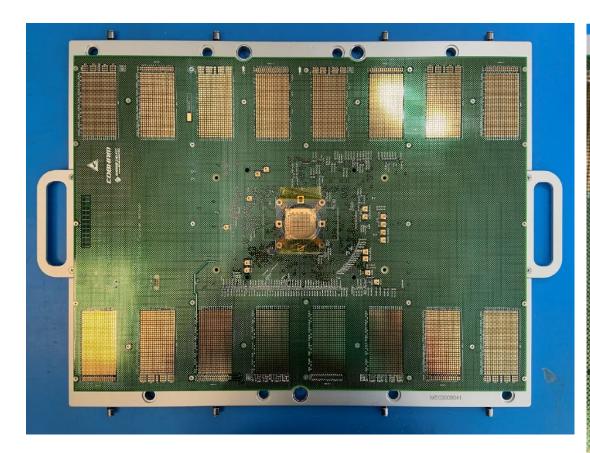






GR740PBGA Load board





- Load board verified and operational
- Temperature range selected for GR740PBGA:
 - -40°C to +105°C







Images courtesy of Synergie CAD

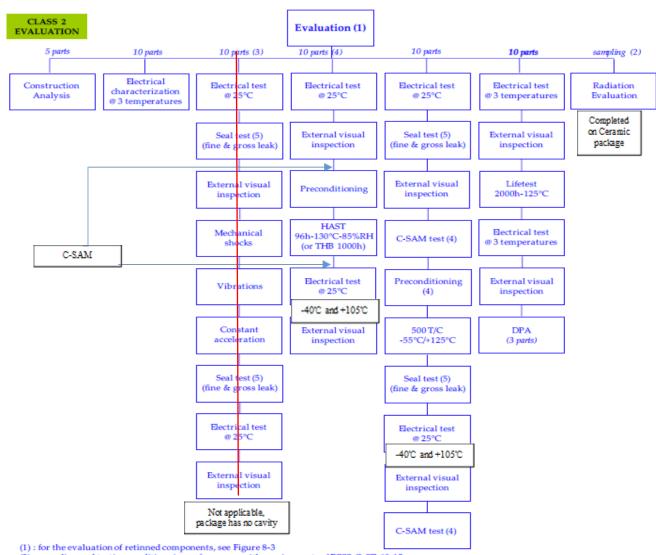
Evaluation activities



- ECSS-Q-ST-60-13C, class 2
 - Constructional Analysis
 - Electrical characterisation
 - THB, 1000 hours
 - 500 TC
 - HTOL, 2000 hours
- ESD CDM
- Outgassing characterisation







- (2): sampling and testing conditions in conformance with requirements of ECSS-Q-ST-60-15
- (3): applicable in case of cavity package
- (4): applicable to plastic package only
- (5): applicable to hermetic & cavity package

Conclusion



- About to supply the telecom constellation market with
 - a high-rel rad-hard die developed for QML-V
 - that will be able to support telecom constellation programs with a cost-effective package technology
- Great market interest for the GR740PBGA

Thank you for your attention!

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