The Design and Simulation of Lateral SiC Power Devices for Satellite Power Supply Applications

A presentation to ESCCON 2021

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Introduction

The UK's Engineering and Physical Sciences Research Council (EPSRC) have funded the University of Warwick's project entitled *Silicon Carbide Power Conversion for Telecommunications Satellite Applications.*

- The project runs from April 2021 to September 2024
- The project will be supported by Thales Alenia Space, Clas-SiC Wafer Fab, Micross and the Compound Semiconductor Applications Catapult.

The project will focus on the development of radiation-hard SiC power devices for satellite applications.

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Motivation for SiC Power Devices in Telecommunications Satellites

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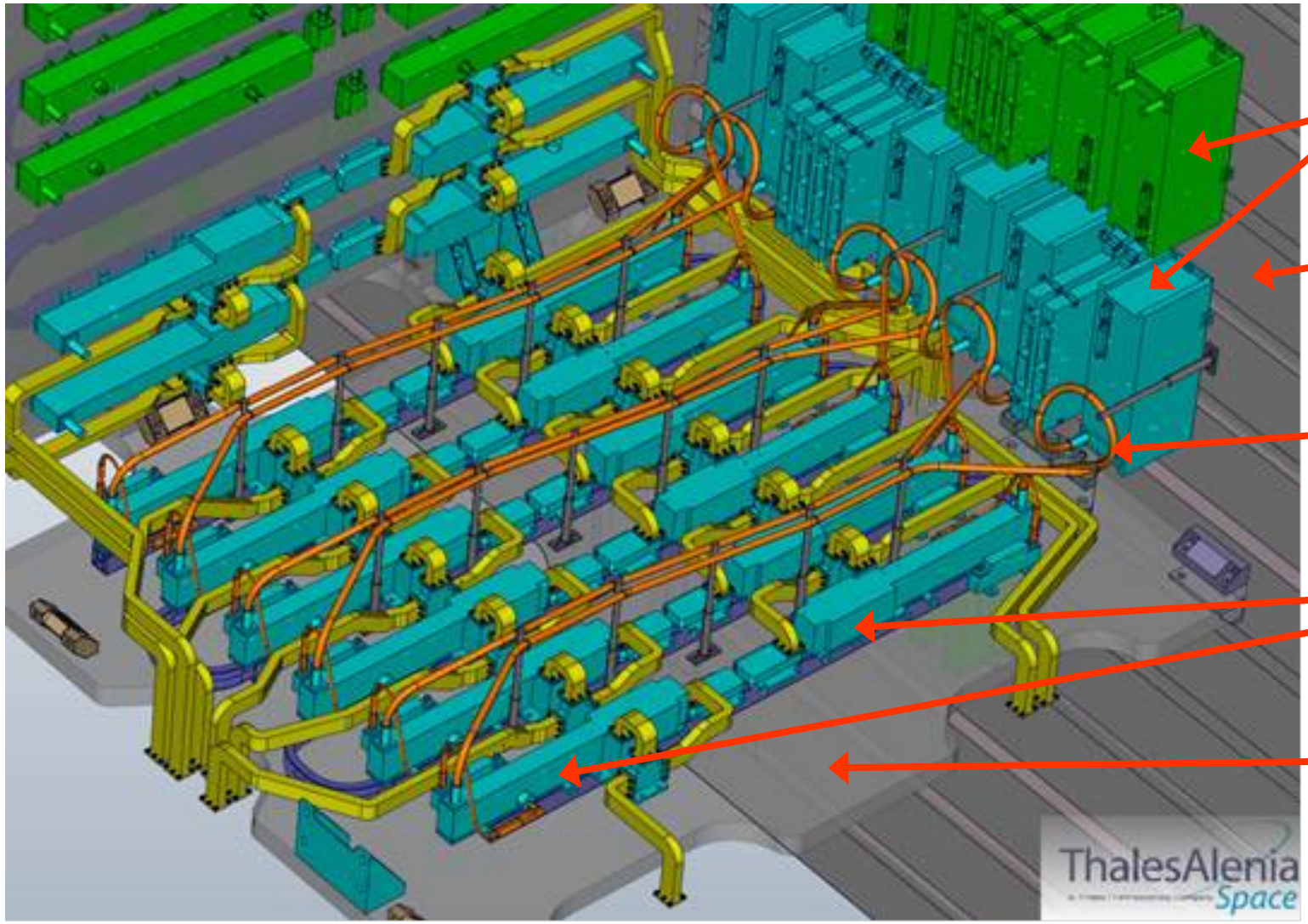


Electronic Power Conditioners (EPCs)

EPC Base Plate at **60°C**

High Voltage Cables

Travelling Wave Tubes (TWTs)

TWT Base Plate at **85°C**

A Typical Telecom Satellite Payload

Image courtesy of project partners Thales Alenia Space

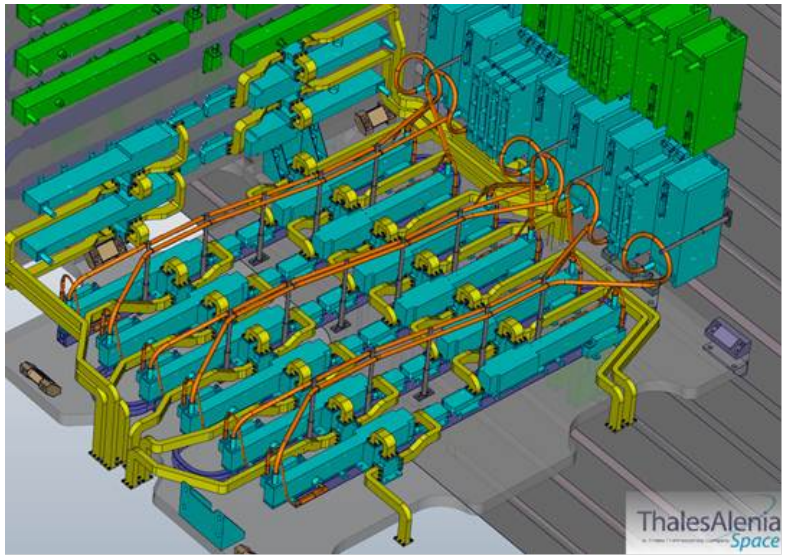
Motivation for SiC Power Devices in Telecommunications Satellites

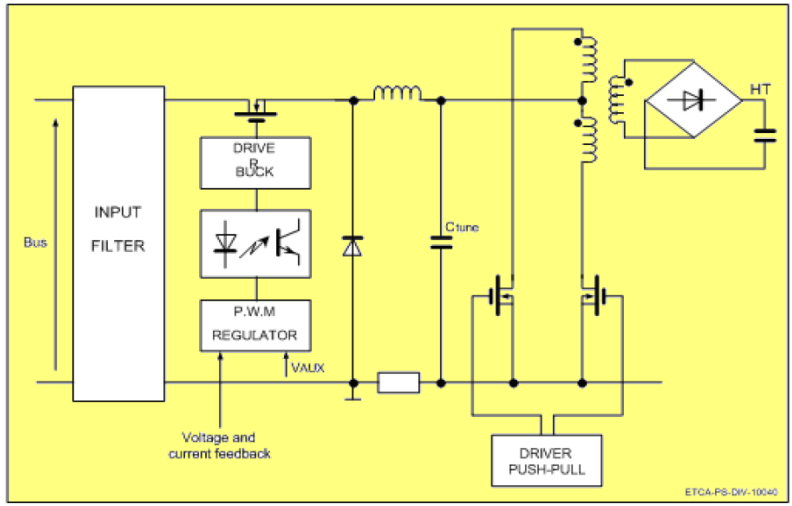
Existing Si power devices are limited to 110°C junction temperature after derating. This requires an EPC base plate rating of up to **60°C**.

The low efficiency of the TWT heats its base plate up to **85°C**.

This discrepancy in temperature:

- Prevents **co-mounting** of the TWT and EPC
- Requires 1.5m of **heavy cabling** between the TWT and EPC.





Smart Topology of an EPC

Images courtesy of project partners Thales Alenia Space

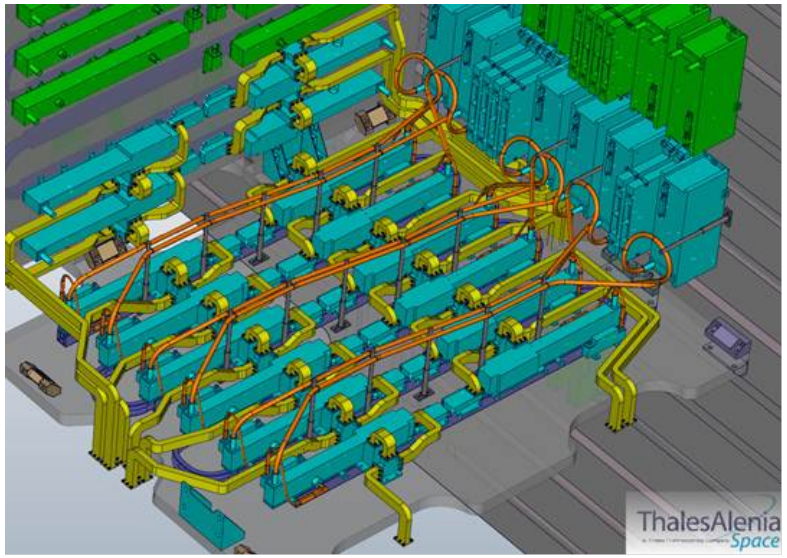
Motivation for SiC Power Devices in Telecommunications Satellites

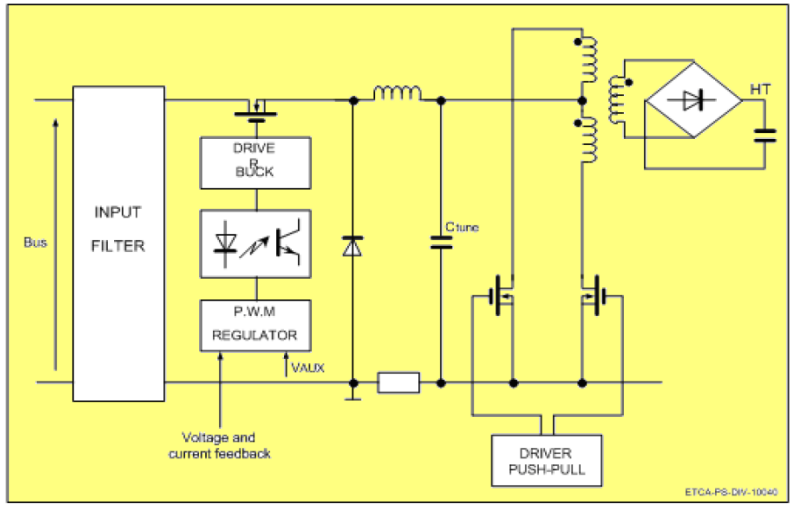
The aim of this project is to replace all Si parts in the EPC with 1200 V SiC MOSFETs and Schottky diodes rated to 225°C.

The **primary motivation** for this is to enable an increase of the EPC baseplate to at least 85°C and hence the co-mounting of the EPC and TWT.

This will enable:

- Heavy cables to be shortened to ~20 cm.
- A lower cost and faster final payload integration
- Up to 33% more EPC dissipation capability due to better thermal radiation (T^4) outside the satellite





Smart Topology of an EPC

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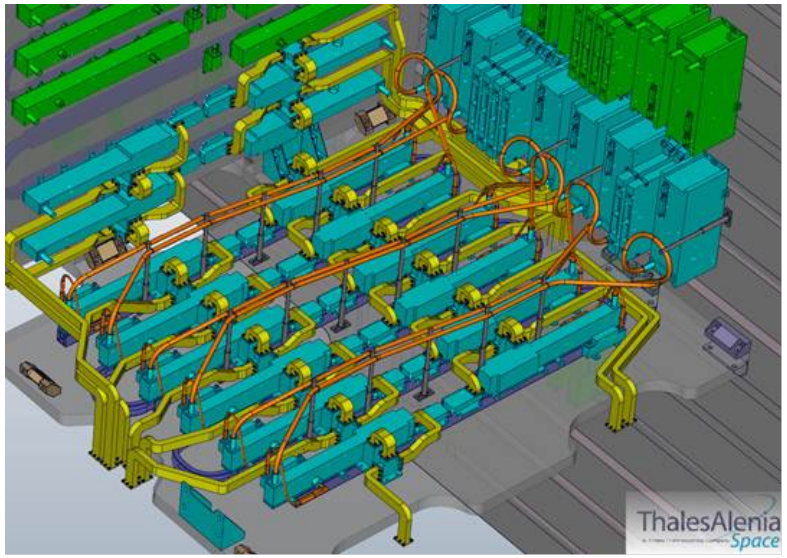
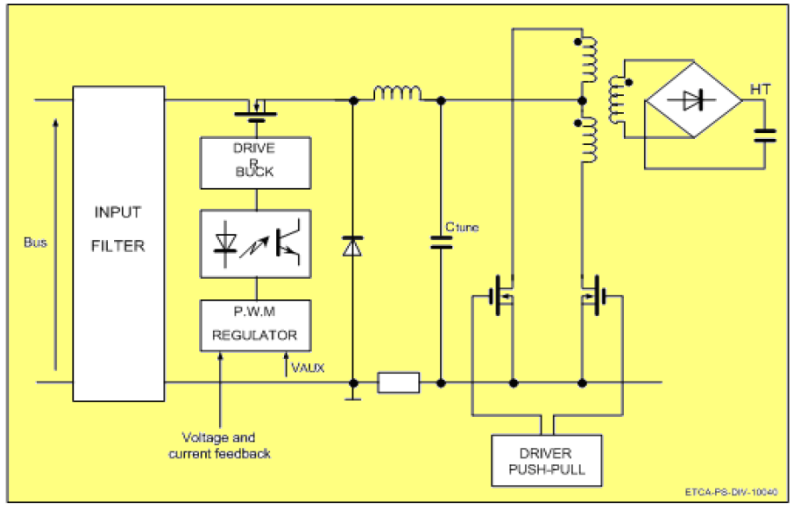
Motivation for SiC Power Devices in Telecommunications Satellites

The aim of this project is to replace all Si parts in the EPC with 1200 V SiC MOSFETs and Schottky diodes rated to 225°C.

The **secondary motivation** for this is to produce a lighter, smaller and/or more efficient EPC, achieved through enabling faster switching speeds, and hence smaller passive components.

Combined, these benefits could enable increase TWT/EPC capacity, potentially adding 16 more RF channels.





Smart Topology of an EPC

Images courtesy of project partners Thales Alenia Space

SEE testing on COTS SiC Power Devices

The electrical requirements to meet the brief for a TAS EPC are simple enough to obtain in SiC. Focussing on just the diode:

- 1200 V Breakdown Voltage (V_{BD})
- Notional 2 A forward current (I_F) rating
- Minimal leakage (I_R) and forward voltage drop (V_F) requirements.
- 225°C Temperature rating (T_{max})

These *could* be obtained with a standard (e.g. automotive focussed) SiC diode chip, repackaged to achieve the T_{max}.

SEE testing on COTS SiC Power Devices

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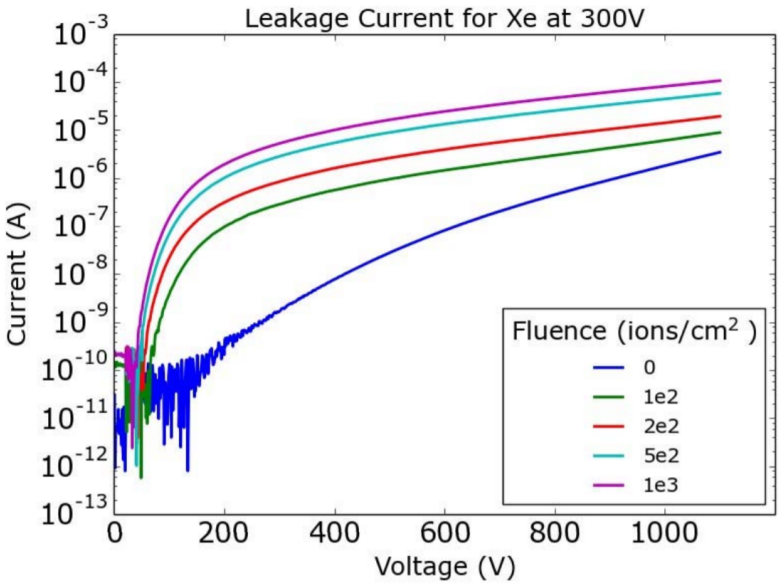
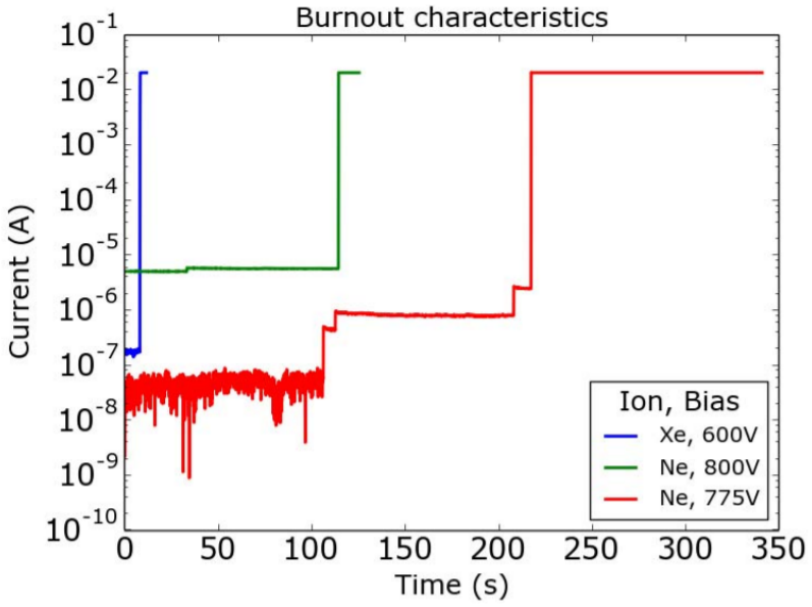
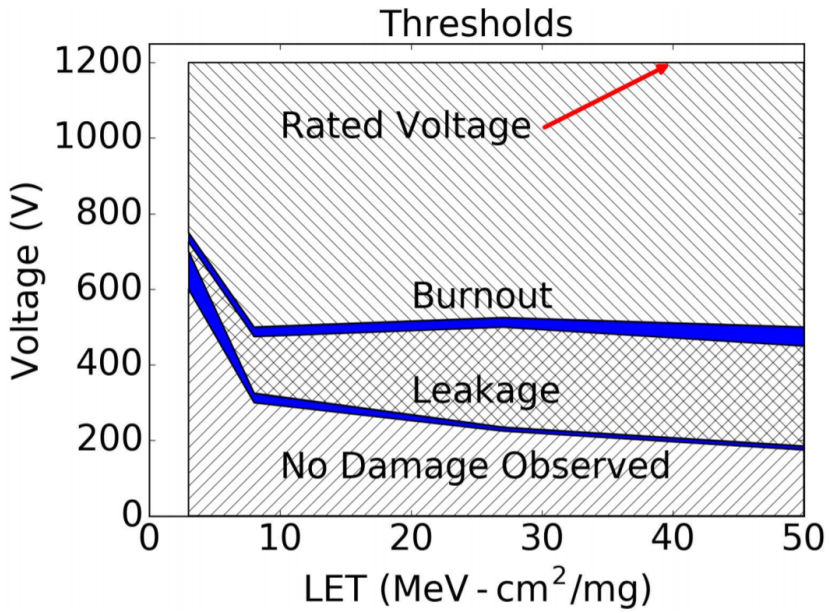
However, the standard ESA radiation requirements, in particular the SEE immunity level (> 60 MeV.cm^2/mg), are a more challenging prospect for SiC discretes.

Presented here are experimental results published[1] on a Wolfspeed 1200 V 20A (C4D020120A) diode in an open package.





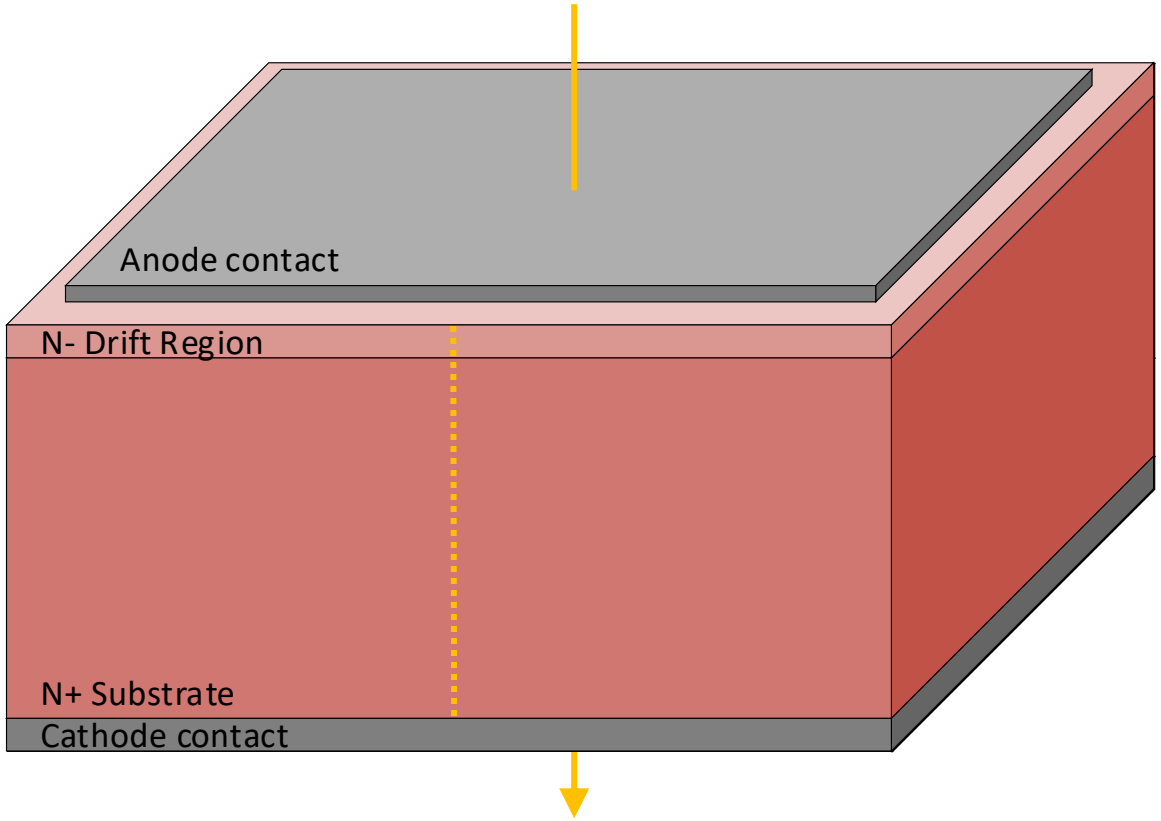
Xe @ 49 MeV.cm^2/mg; Ne@2.8 MeV.cm^2/mg



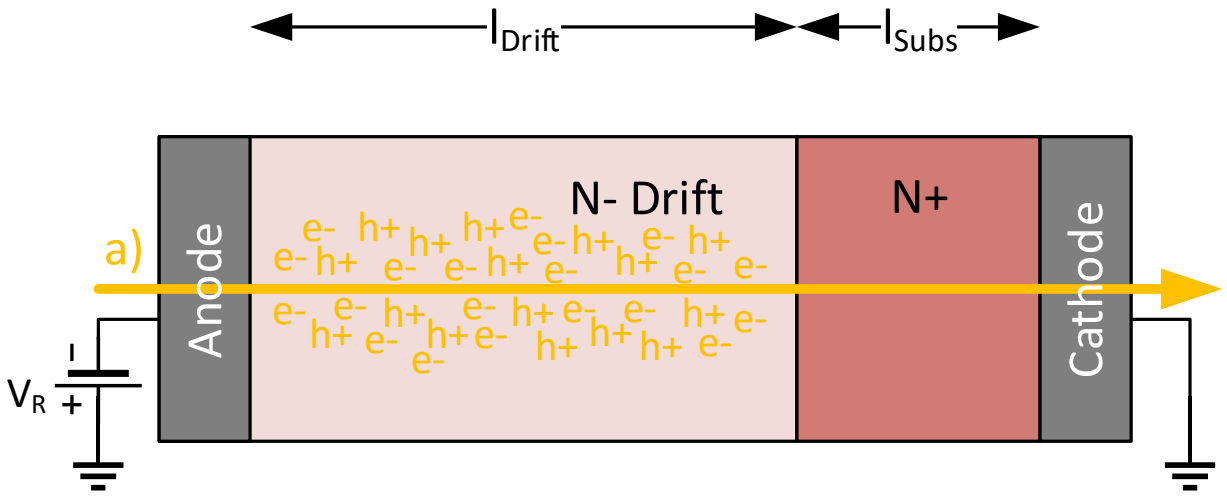
[1] Witulski et al. "Single-event burnout of SiC junction barrier Schottky diode high-voltage power devices." *IEEE Transactions on Nuclear Science* 65.1 (2017): 256-261.

SEE Simulation of Vertical SiC Power Devices

In a terrestrial COTS SiC device, there is every motivation to use a vertical designed power device structure. This is the most efficient layout to achieve a V_{BD}, while minimising the area required to attain the required I_F.



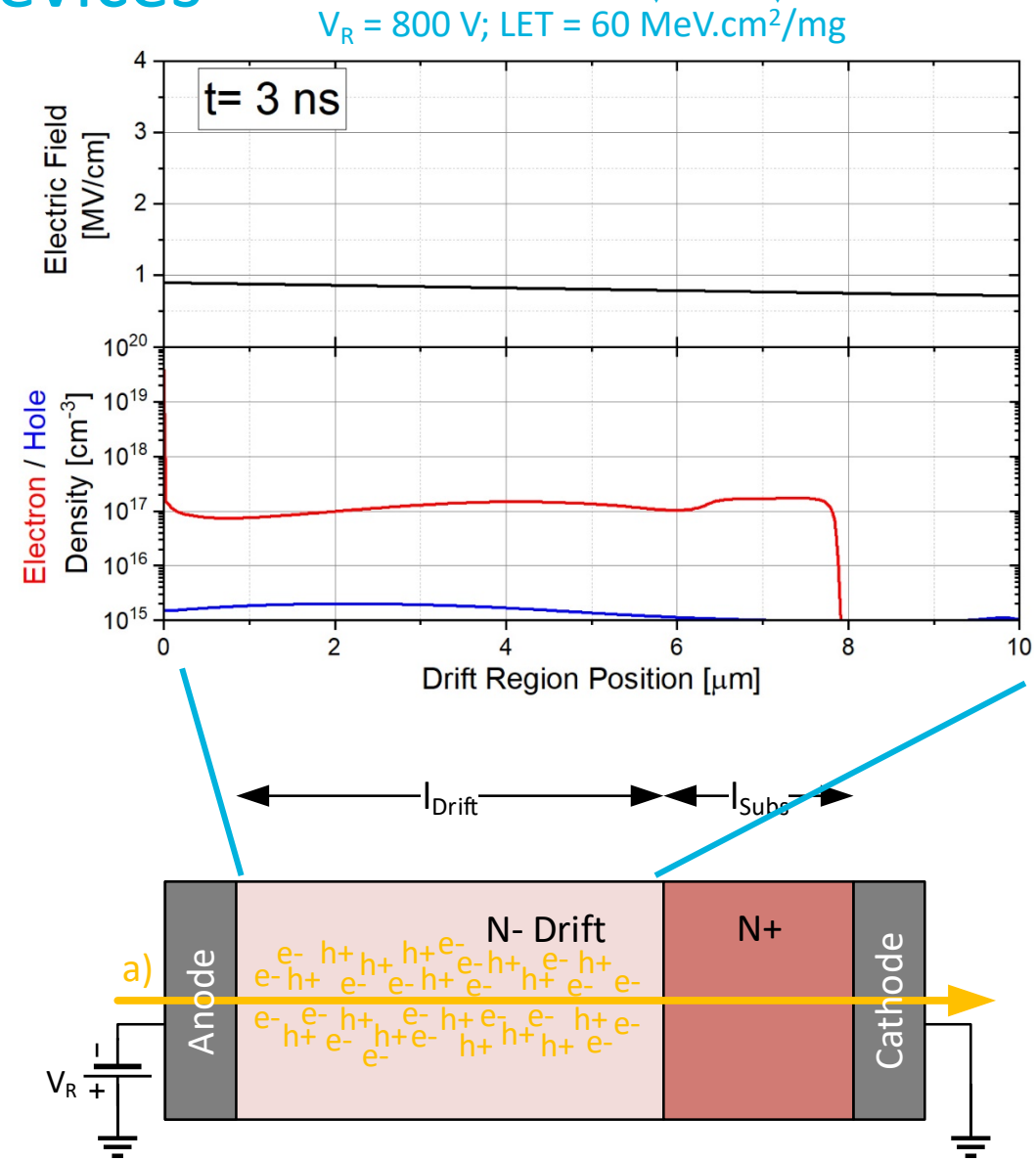
Yet, the geometries of a vertical device mean that a heavy ion will always traverse the drift region, creating electron-hole pairs as it goes.



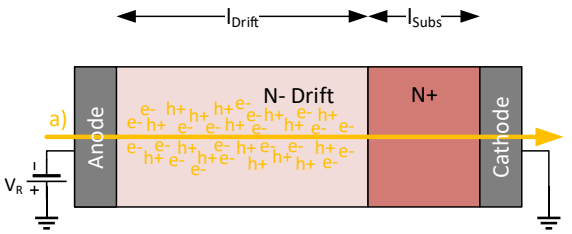
SEE Simulation of Vertical SiC Power Devices

Our simulations have revealed the extent of the SEE problem in vertical SiC power devices:

- As the device is in its off state pre-strike, it is blocking a large voltage when the device is off, with a large peak electric field.
- The heavy ion tears through the drift creating electron-hole pairs.
- Their presence prevents e-field being supported locally, squeezing the e-field into ever smaller regions at the end, creating large e-field spikes
- The reverse bias initiates carrier sweep out but the movement of charge + large voltage creates power, and hence very high temperature.
- The extreme local temperatures cause permanent damage.

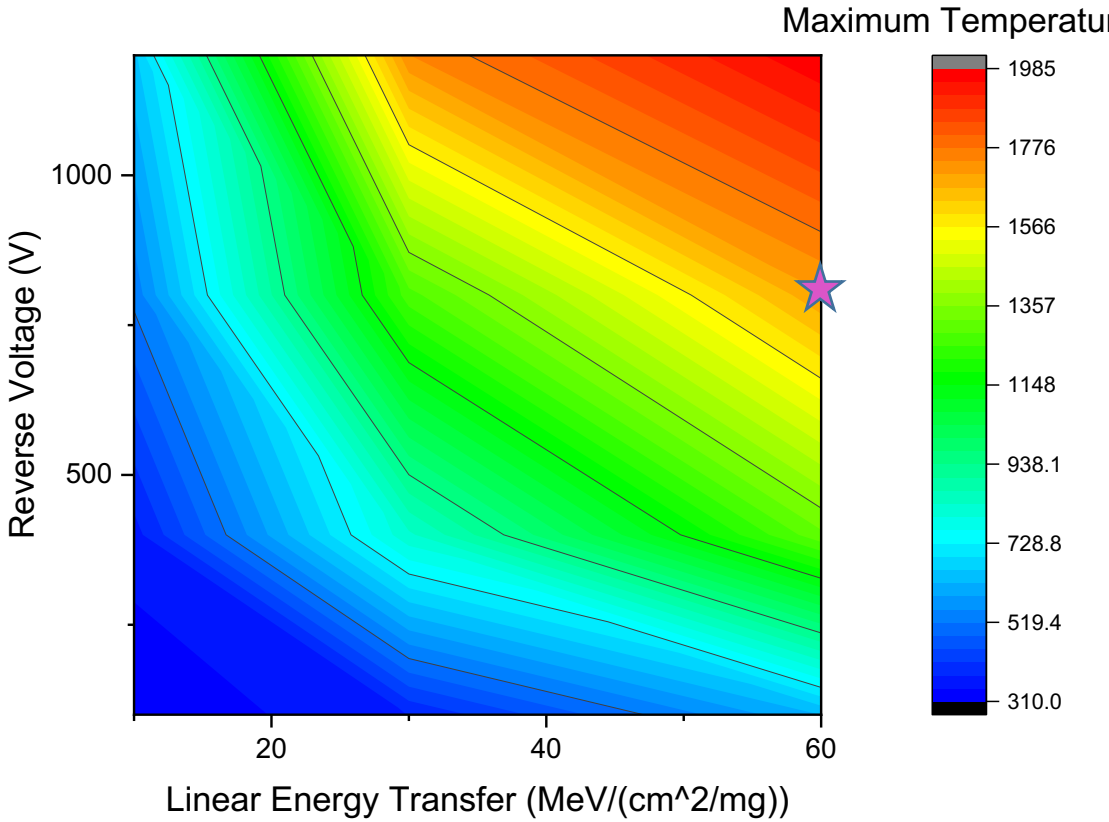


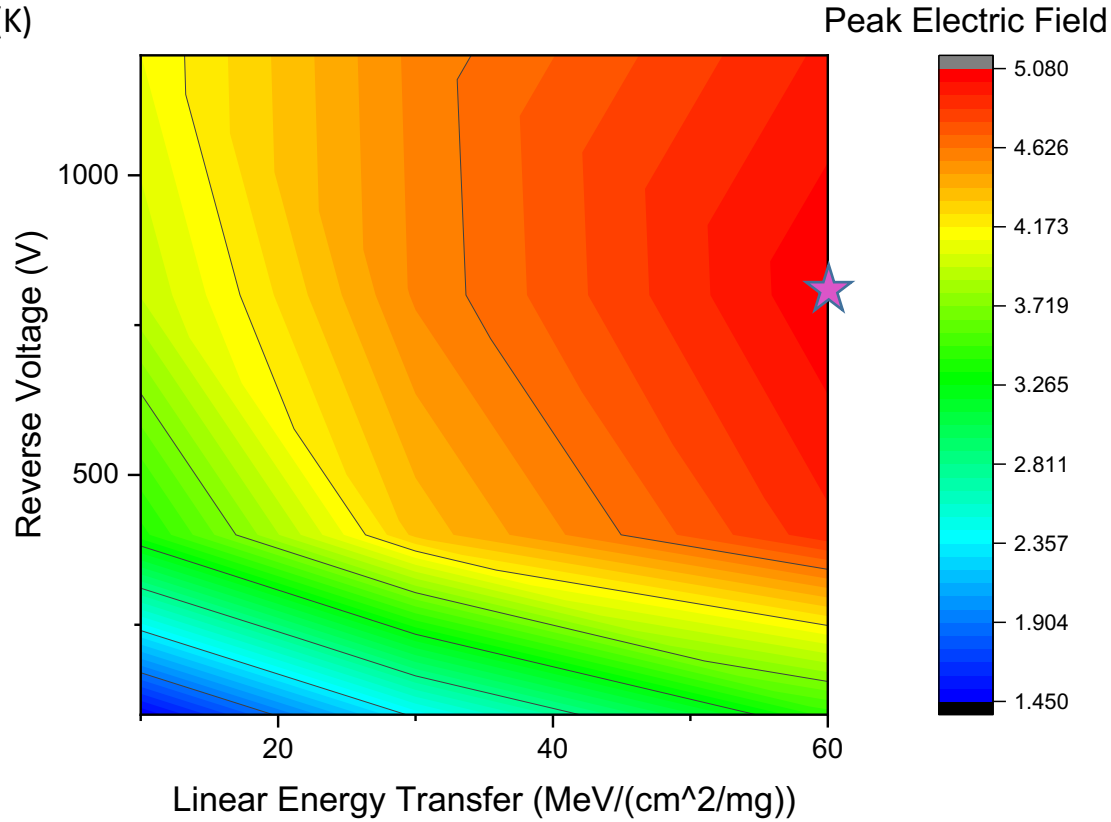
SEE Simulation of Vertical SiC Power Devices



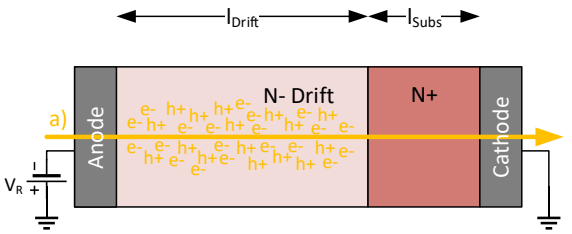
Our simulations have revealed the extent of the SEE problem in vertical SiC power devices:

The plots below show the maximum localised e-field spikes and temperatures simulated in the drift region at various LETs/voltages for a 1200 V rated device:





SEE Simulation of Vertical SiC Power Devices



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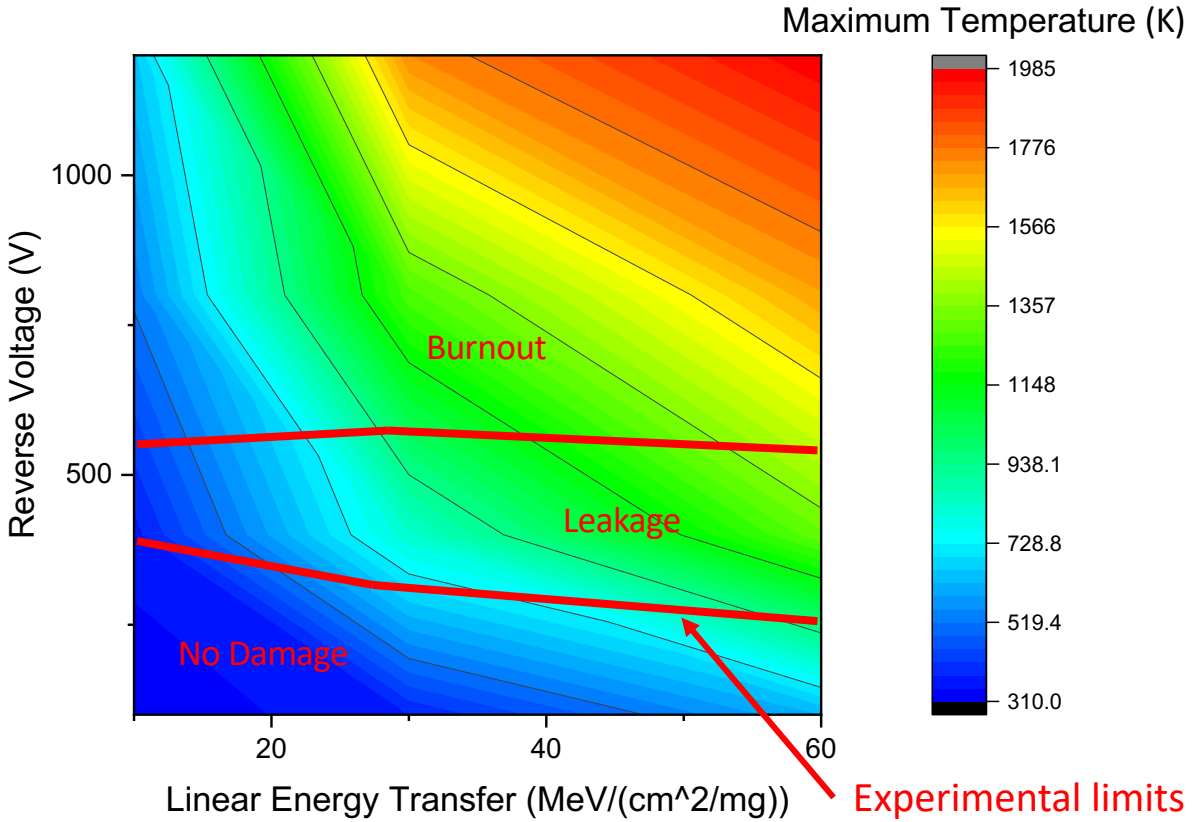
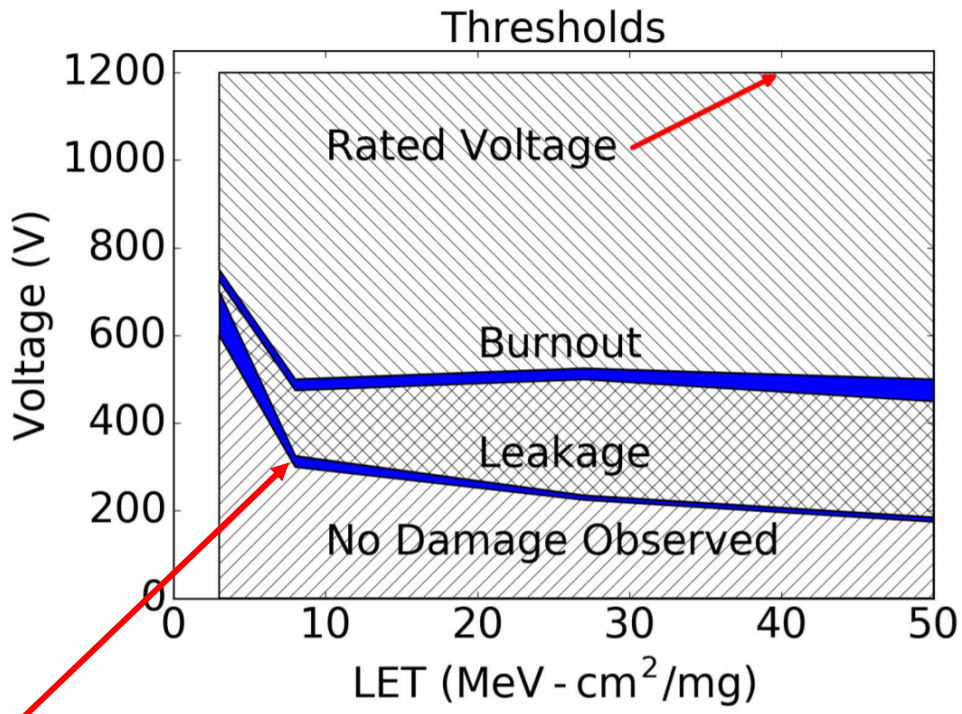




Experimental limits

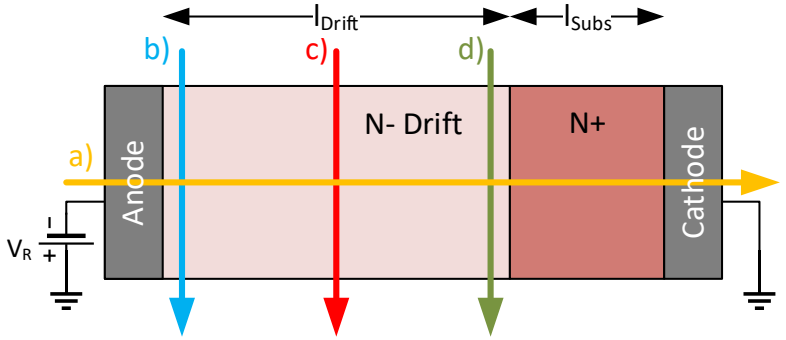
Practical SiC diode results

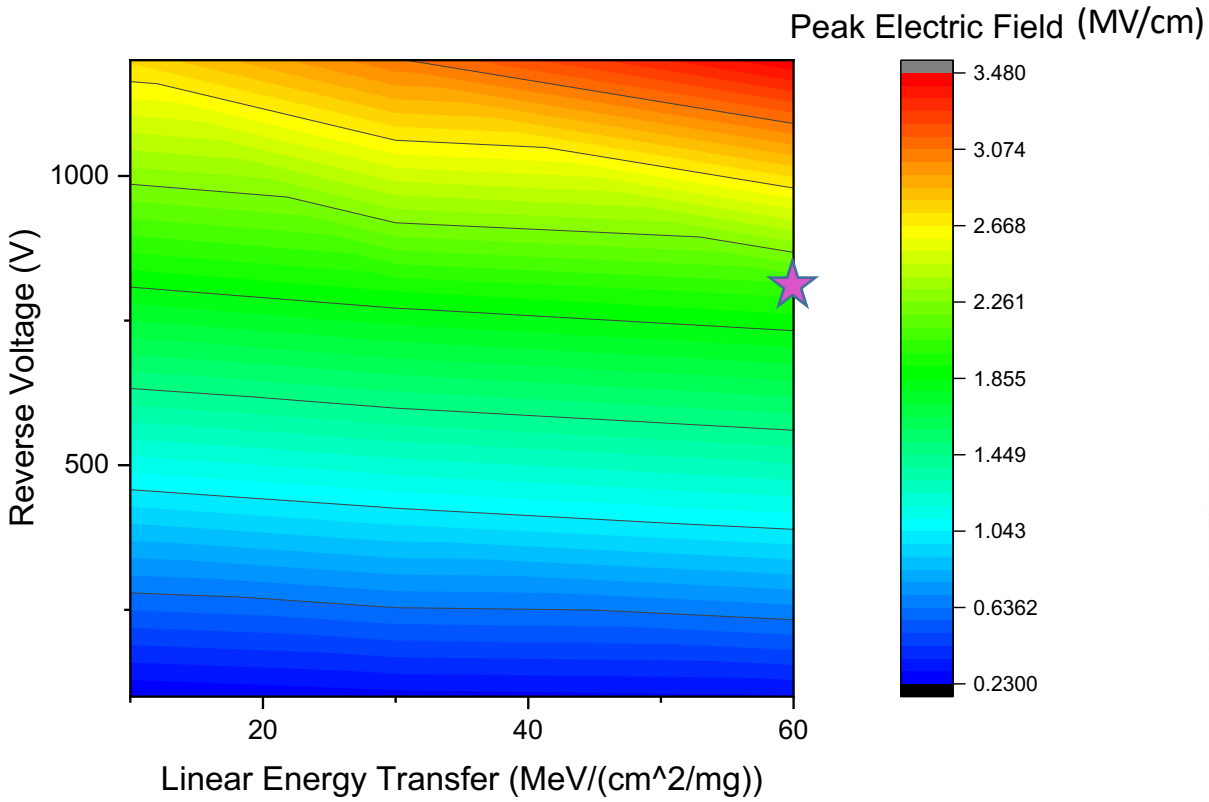
From: [1] Witulski et al. *IEEE Transactions on Nuclear Science* 65.1 (2017): 256-261.

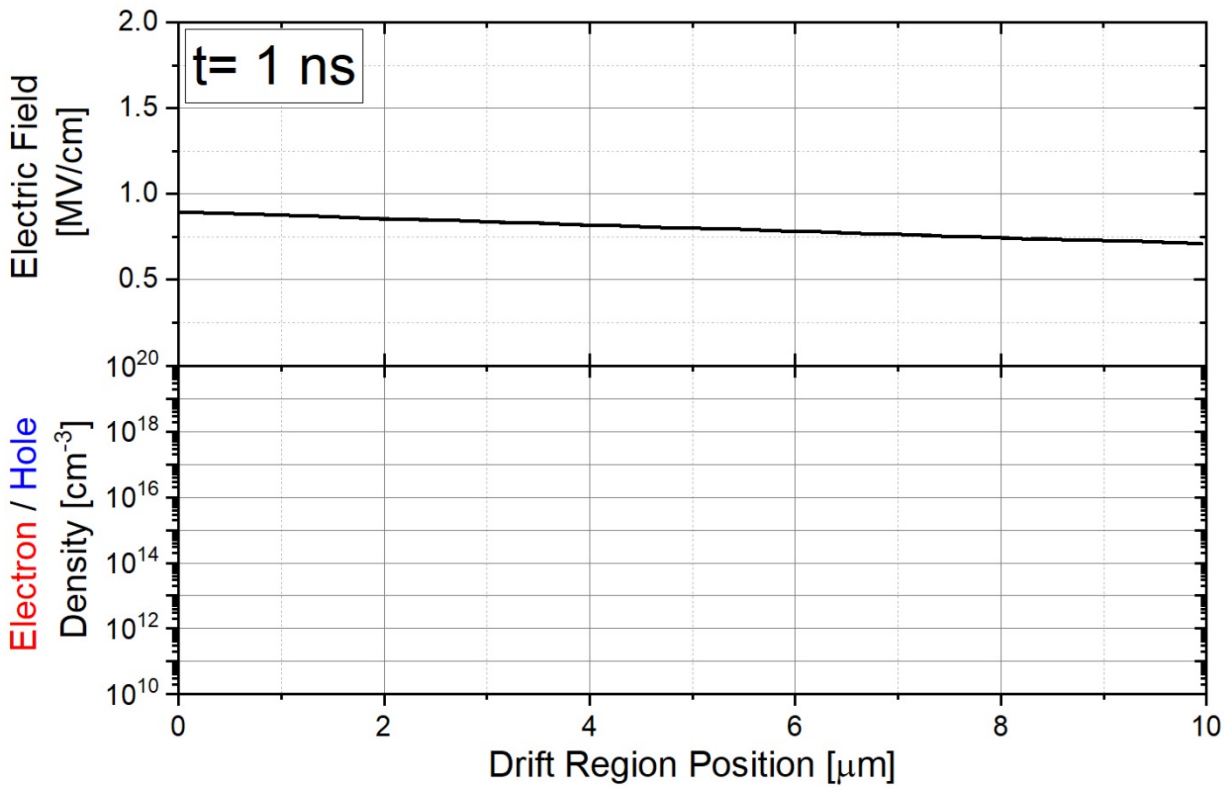
SEE Simulation of Lateral SiC Power Devices

Issues with vertical SiC devices parallel Si, SOI and GaN. Like these, a rad-hard SiC device should be lateral.

To show this, heavy ions were fired laterally, across the drift region in 3 positions. Here are the e-field results in (b) 1 µm from surface.



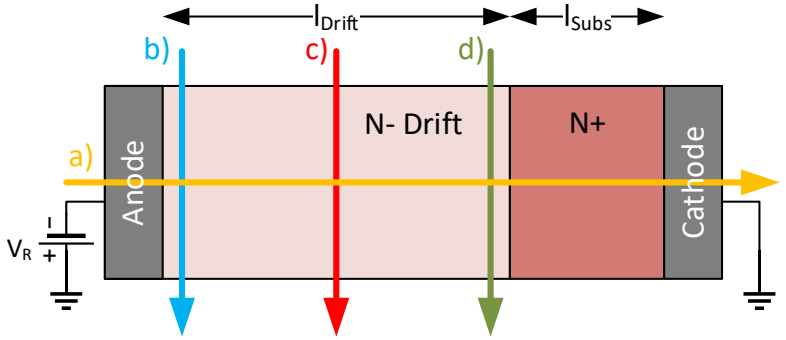


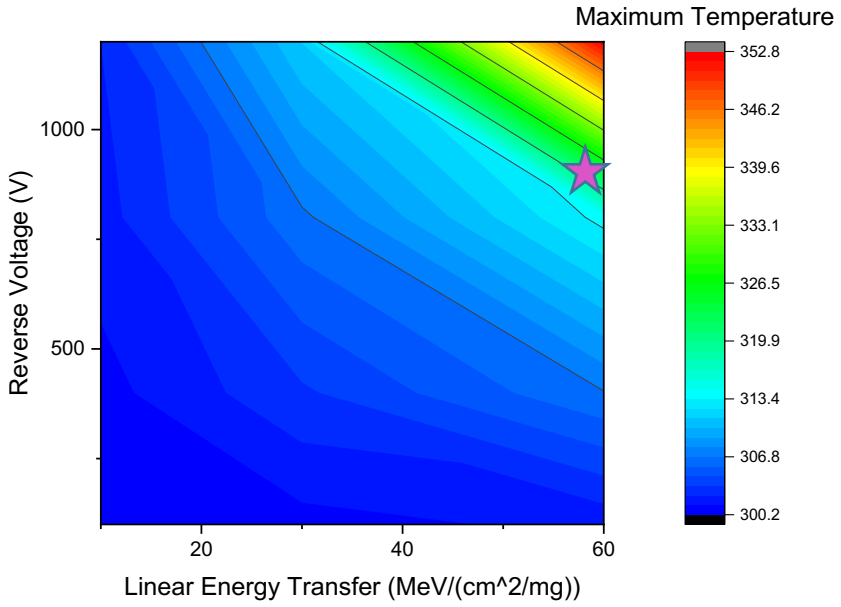


SEE Simulation of Lateral SiC Power Devices

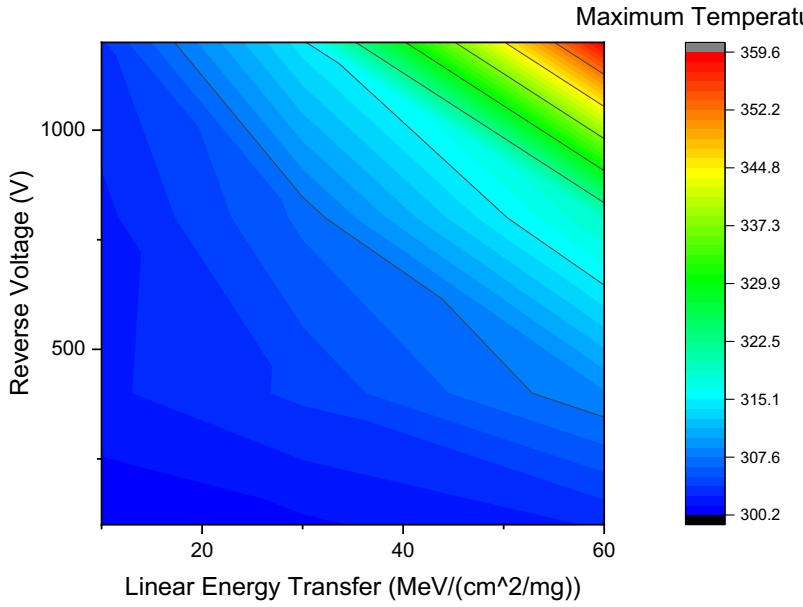
Issues with vertical SiC devices parallel Si, SOI and GaN. Like these, a rad-hard SiC device should be lateral.

The temperature plots form the three locations show temp rise of <60 K and 15 K variation in the 3 locations

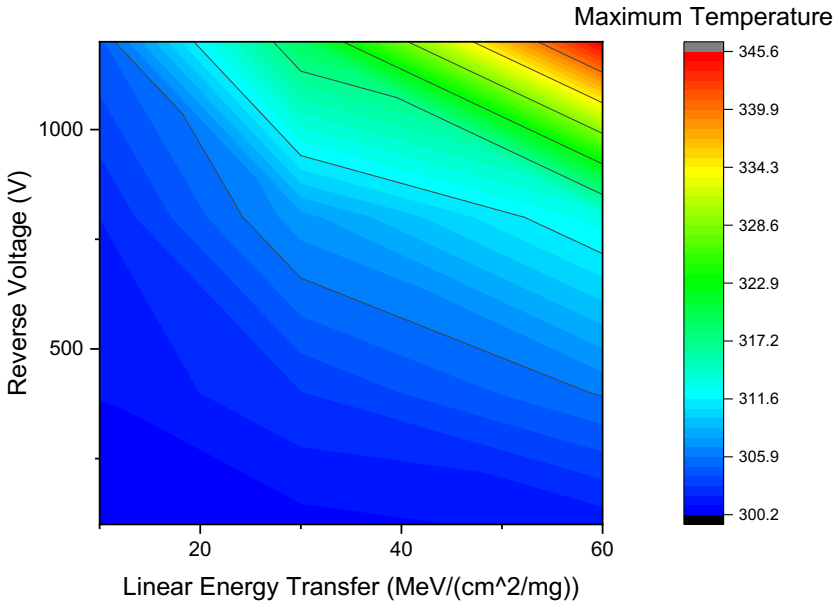




Position (b) – 1 µm from surface



Position (c) – 5 µm from surface



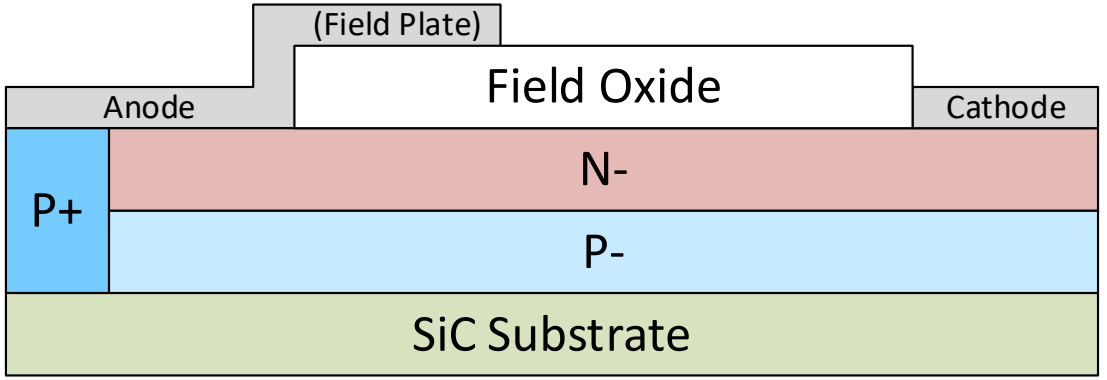
Position (d) – 9 µm from surface

SEE-Tolerant SiC RESURF Devices

Like Si, SOI and GaN before, it is clear that SiC can be made rad-hard if it is properly designed for. Our first fully-optimised SiC lateral RESURF design is depicted below.

SEE/Radiation Tolerance

- The lateral design means there is little chance of a heavy ion traversing the full drift region, minimising the e-field peak.
- Incorporating the P-/P+ regions act as a sink for holes, making their extraction much easier, and minimising temperature rises.
- In our aggressive design, local temperature is limited to **78 K** at 60 MeV.cm^2/mg and V_R=1200 V. More conservative designs can limit this to <50 K.

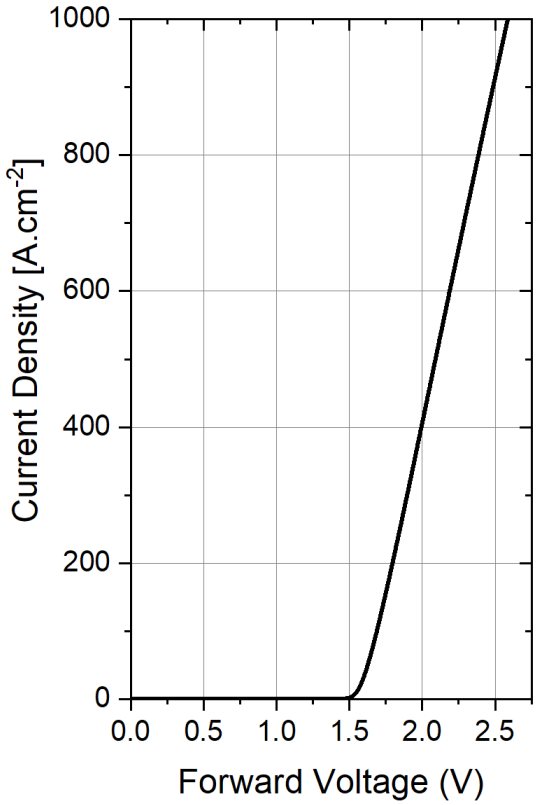


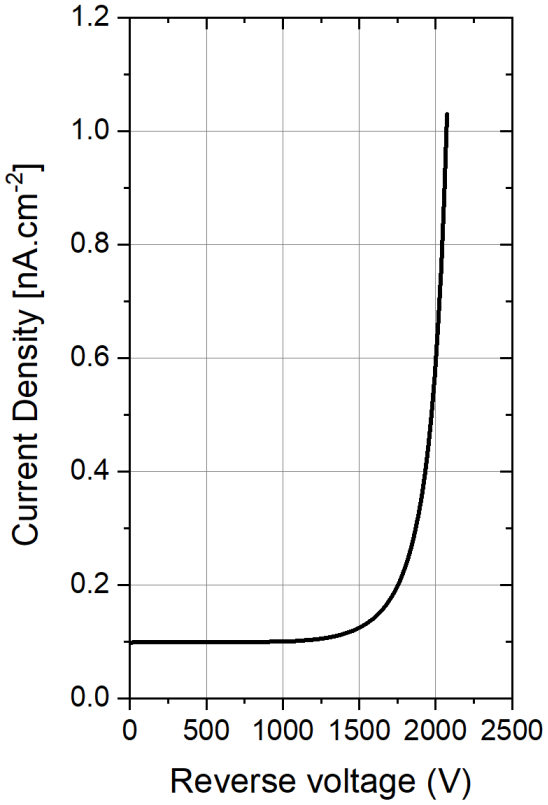
SEE-Tolerant SiC RESURF Devices

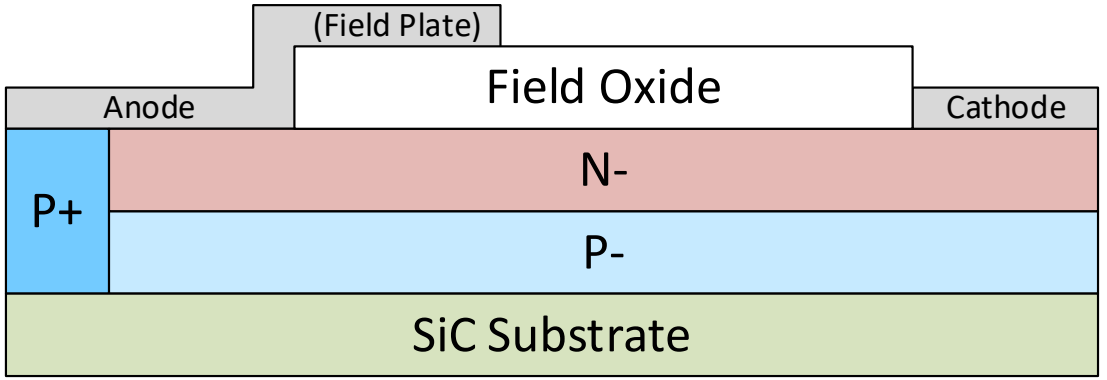
Use of field plates and fine control of the doping/width of the N- layer allows V_{BD} to be maximised and R_{ON} minimised

Electrical Properties

- The RESURF/charge balance effect means the 10 µm drift region supports a V_{BD} of 1800 V.
- The current rating will depend on the length and number of the anode/cathode stripes.
- The p- and n- layers can be grown and their doping finely controlled via CVD epitaxy.
- Various ideas are being considered to isolate the device area from the substrate – either a P+ interlayer, or even a semi-insulating layer.
- Design is easily adapted for a MOSFET layout once diode is proven.







Conclusions

The EPSRC project *Silicon Carbide Power Conversion for Telecommunications Satellite Applications* begins in April 2021

- Replacing Si technology with high temp SiC devices in a Thales Alenia Space EPC will improve payload integration, potentially freeing up space for 16 more RF channels.
- Radiation hardening SiC power devices remains the biggest challenge, one that requires a shift away from conventional (e.g. automotive) vertical device architectures
- Preparatory simulations dispel the myth that SiC cannot be radiation hardened without considerable derating. Lateral RESURF architectures, similar to those used in Si and SOI, show great promise.
- Over the 3.5 year project, device designs will be fabricated in-house at Warwick, packaged at Micross, radiation tested at UC Louvain, and delivered for testing/integration at TAS.

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