APPLICATION FOR ESCC QUALIFICATION APPROVAL

Page 1

Component Title: **Integrated Circuits, Silicon, Monolithic, Radiation-Hardened 32-bit ARM Cortex-M7 Microcontroller**

Appl. No. 372

Executive Member: CNES Date: 12/03/2021

1 Components (including series and families) submitted for Qualification Approval

ESCC COMPONENT. NO.	VARIANTS	RANGE OF COMPONENTS	BASED ON	TEST VEHICLE / S	COMPONENT SIMILAR
9512/006	01	Integrated Circuits, Silicon Monolithic, Radiation-Hardened 32-bit ARM Cortex-M7 Microcontroller	SAMRH71 - ATMX150RHA technology	SAMRH71 CQFP-256	

2 Component Manufacturer

MICROCHIP TECHNOLOGY NANTES

3 Location of Manufacturing Plant

MCHP Nantes (design & test)
UMC Taïwan (wafer fab 8C)
MMT Thailand (assembly)

4 ESCC Specification used for Qualification

Generic: ESCC 9000 issue 10
Issue

Detail/s: ESCC 9512/006 issue 1
Issue

5 Qualification Report Reference and date:

SoC ARM Development SAMV71RHBD - PUMA - ESCC Evaluation Report Rev2

Date: 09/02/2021

6 **PID** used for manufacturing Qualification Lot

Ref No: SAMRH71 PID 0040 rev. 0
Issue: Rev 0
Date: 12/03/2021

7 **PID** changes since start of qualification

None ☒
Minor* ☐
Major* ☐

8 Current **PID** Verified by CNES

Name of Executive Representative Agency

Ref No: SAMRH71 PID 0040 rev. 0 – 12/03/2021

MMT PID FOR MCHP NANTES – 1G-QM-0105 – 04/02/2019

9 Current Manufacturing facilities surveyed by:

CNES (D. Dangla, F. Malou) & ESA (F. Martinez) 10/07/2019

(Name of Executive Responsible) (Date)

Report Reference - ESCC Audit of MMT Assembly for ATC18RHA and ATMX150RHA ASICs - DSO/AQ/EC-2019.0013984, 30/08/2019

Satisfactory: Yes ☒ No ☐ Explain

10 Quality and Reliability Data

Evaluation testing performed Yes ☒ No ☐

Report Ref. No.: ESCC Evaluation Report 2020-EC-731 Rev2 Date: 01/12/2020

Equivalent Data: Single Phase Qualification applies

Certification:

Failure analysis, DPA, NCCS available Yes ☒ No ☐

(supply data)

Ref Nos. and purpose:

Construction analysis report MCHP/SERMA Report 20-1705-100 06/2020

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The undersigned hereby certifies on behalf of the ESCC Executive, that the above information is correct; that the appropriate documentation has been evaluated; that full compliance to all ESCC requirements is evidence except as stated in box 13; that the reports and data are available at the ESCC Executive and therefore applies for ESCC qualification status to be given to the component(s) listed herein.

Date: 12/03/2021

JP. BUSSENOT

(Signature of the Executive Coordinator)

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Continuation of Boxes above: (Only non-confidential comments)

[5] SoC ARM Development SAMV71RHBD - PUMA - ESCC Evaluation Report - CNES contract 180954 DL6.8.3 rev2 and associated reports:

- ATMX150RHA Qualification Test Report - QTR 2018-IC-384 rev1
- ATMX150RHA Process Identification Document - PID0037 revD
- MMT - Assembly of multi-decks & Flat-substrate packages - Qualification Test Report - QTR 2017-EC-212 rev2
- SAMRH71 ESCC Evaluation Plan - CNES contract 180954 DL6.8.1 rev1.0
- SAMRH71 Process Identification Document - CNES contract 180954 DL6.8.5 - PID0040 rev0
- SAMRH71 ESCC Detail Specification - CNES contract 180954 DL6.8.4 draft C
- SAMRH71 Electrical characterization report - CNES contract 180954 DL4.6.4 rev1.1
- Rapport de test ions lourds - CNES contract 180954 DL5.7.2 rev1
- Rapport de test en dose cumulée - CNES contract 180954 DL5.7.4 rev1
- SAMRH71F20C Radiation Test Report - rev 5.0 - December 2020
- Construction Analysis on a SAMRH71F20C-7GB-SV Microcontroller from Microchip, Report 20-1705-100 - June 10th, 2020

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Non compliance to ESCC requirements:

No.:	Specification	Paragraph	Non compliance

14

Additional tasks required to achieve full compliance for ESCC qualification or rationale for acceptability of noncompliance:

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Executive Manager Disposition

Application Approval: Yes ☒ No ☐

Action / Remarks:

Digitally signed by Britta Schade
Date: 2021.05.28 10:54:16 +02'00'

Date:

B. Schade: Head of the Product Assurance and Safety Department

ANNEX 1: LIST OF TESTS DONE TO SUPPORT QUALIFICATION

Tests conducted in compliance with: ESCC 9000

- ESCC 9000 generic specification; Chart F4 (for ESCC/QPL parts);
- Or PID-TFD [redacted] (for ESCC/QML parts)

Tests vehicle identification/description:

SAMRH71 CQFP-256	SAMRH71 has been designed in compliance with ATMX150RHA design rules. Nevertheless, SAMRH71 embarks 2 specific entities not covered by the ATMX150RHA Standard Evaluation Circuit 002OP used for ATMX150RHA ESCC qualification (ESCC certificate 359 valid until 25 April 2021): a NVM block and programmable I/O's. These features not mandatory for ASICs are necessary to meet customer needs for microprocessors. SAMRH71 also embarks more transistors than the maximum number covered by the ATMX150RHA SEC 002OP (97M Xtors compared to a maximum coverage of 90M Xtors). The qualification has been performed with flight models randomly chosen from 3 diffusion/inspection lots. The flight models screening is compliant with -SV requirements as described in AEQA0242 (http://ww1.microchip.com/downloads/en/Quality_ReliabilityDocs/AEQA0242_DS60001546B.pdf), with static burn-in (Mil-STD-883 TM1015A). See DL6.8.3 ESCC Evaluation Report, ref. 2020-EC-731 Rev2 (QP-SAMRH71, December 2020)

Detail Specification reference: 9512/006

Subgroup	Test	Tick when done	Conditions	Date Code Diffusion Lot	Tested Qty	No. of Rejects	Comments if not performed. Comments on Rejection
Environmental/Mechanical Subgroup	Mechanical Shock	☒	MIL-STD-883, Test Method 2002B	A68AN00000 DC1952 (15 parts)	15	0	5+45 pulses
	Vibration	☒	MIL-STD-883, Test Method 2007A		15	0	12+108 sweeps
	Constant Acceleration	☒	MIL-STD-883, Test Method 2001E		15	0	Y1
	Seal Test	☒	MIL-STD-883, Test Method 1014		15	0	
	3 Temperature Electrical Test	☒	3 Temperature Electrical Test	A68ARA25UH DC2005 (15 parts)	15	0	
	External Visual Inspection	☒	MIL-STD-883, Test Method 2007		15	0	
	Thermal Shock	☒	MIL-STD-883. Test Method 1011C		15	0	15+85 cycles
	Temperature Cycling	☒	MIL-STD-883. Test Method 1010C		15	0	100 cycles
	Moisture Resistance	☒	MIL-STD-883, Test Method 1004	A68AQ00000 DC2004 (15 parts)	15	0	
	Seal Test	☒	MIL-STD-883, Test Method 1014		15	0	
	3 Temperature Electrical Test	☒	3 Temperature Electrical Test		15	0	
	External Visual Inspection	☒	MIL-STD-883, Test Method 1010		15	0	

Subgroup	Test	Tick when done	Conditions	Date Code Diffusion Lot	Tested Qty	No. of Rejects	Comments if not performed. Comments on Rejection
Endurance Subgroup	Operating Life	☒	MIL-STD-883, Test Method 1005	4000h, Tamb=125°C, Vccmax			
	Intermediate and End-Point Electrical Measurements	☒	Intermediate and End-Point Electrical Measurements in the Detail Specification	A68AQ00000 DC2004 Si-lot DGR3N.1 (15 parts)	45	0	
				A68AN00000 DC1952 Si-lot DGR3P.1 (16 parts)	45	0	
				A68ARA25UH DC2005 Si-lot DGR3Q.1 (14 parts)	45	0	
	Seal (Fine and Gross Leak)	☐	MIL-STD-883, Test Method 1014				
	External Visual Inspection	☐	ESCC Basic Specification No. 20500				
Assembly Capability Subgroup	Permanence of Marking	☐	ESCC Basic Specification No. 24800				Covered by ATMX150RHA ESCC qualification tests ESCC certificate 359 valid until April 2021
	Terminal Strength	☐	MIL-STD-883, Test Method 2004				
	Internal Visual Inspection	☐	ESCC Basic Specification No. 20400				
	Bond Strength	☐	MIL-STD-883 Test Method 2011				
	Die Shear or Substrate Attach Strength	☐	MIL-STD-883 Test Method 2019 or 2027				
Additional Tests	Flash memory write/erase endurance cycling	☒	MIL-STD-883 Test Method 1033	A68AQ00000 DC2004 Si-lot DGR3N.1 (15 parts)	15	0	Write/Erase endurance cycling has been performed over the temperature range [0°C, 85°C]. Post- endurance electrical tests have been done over the military temperature range [-55/25/125°C]. Endurance 1 kcycle, 85°C, Vccmax, page mode Electrical test 3-temperature

	Flash memory write/erase endurance cycling	☒	MIL-STD-883 Test Method 1033	A68AN00000 DC1952 Si-lot DGR3P.1 (16 parts)	16	0	Write/Erase endurance cycling has been performed over the temperature range [0°C, 85°C]. Post- endurance electrical tests have been done over the military temperature range [-55/25/125°C]. Endurance 10 kcycle, 25°C, Vccmax, page mode Electrical test 3-temperature
	Flash memory write/erase endurance cycling	☒	MIL-STD-883 Test Method 1033	A68ARA25UH DC2005 Si-lot DGR3Q.1 (14 parts)	14	0	Write/Erase endurance cycling has been performed over the temperature range [0°C, 85°C]. Post- endurance electrical tests have been done over the military temperature range [-55/25/125°C]. Endurance 1 kcycle, 0°C, Vccmax, page mode Electrical test 3-temperature
	Data Retention	☒	JESD22A117	A68AQ00000 DC2004 Si-lot DGR3N.1 (15 parts) A68AN00000 DC1952 Si-lot DGR3P.1 (15 parts) A68ARA25UH DC2005 Si-lot DGR3Q.1 (15 parts)	45	0	Data retention has been performed up to 1000h at 250°C. Electrical tests have been done over the military temperature range [-55/25/125°C]. 700 hours, 250°C, Elect. test 3-temperature 1000 hours 250°C, Elect. test 3-temperature
	Electrical Latch-Up	☒	JEDEC78	DFNPJA25SV DC1947 Si-lot CQFP-256	6	0	Current injection 100mA, Overvoltage 1.5*Vccmax, Class I: 25°C ambient Class II: 125°C ambient
	ESD (HBM & CDM)	☒	MIL-STD-883 Test Method 3015 ANSI/ESDA/JEDEC JS-002	A68AN00000 DC1952 Si-lot CQFP-256	3 3	3 0	ESD HBM level is class 0 (<250V). The low level shall be improved in the coming revision E of the die 77906. ESD CDM levels is class C0a (<125V) The revision E of the die 77906 will also improve the CDM level.
	Construction Analysis	☒		Die analysis DGR3P.1 Si-lot Assembly analysis A68ARA25UH DC2005	X	X	OK

	Radiation Tests	☒	TID ESA/SCC 22900 MIL-STD-883 Test Method 1019	DGR3N.1 (9 parts) DGR3P.1 (10 parts) DGR3Q.1 (8 parts)	27 27	0 0	Tested up to 150 krad(Si) without NVM (22biased & 5unbiased) 15 krad(Si) with NVM (22biased & 5unbiased)
			Heavy Ions Single Event Latch-Up Single Event Upset ESA/SCC 25100 EIA/JESD57	DFNPH.1	3 3	0 0	SEL: No SEL events have been observed up to a LET of 62.2 MeV.cm²/mg @Vccmax @125°C. SEU: See report

NOTES ON THE COMPLETION OF THE APPLICATION FORM FOR ESCC QUALIFICATION APPROVAL

ENTRIES

Form Heading	shall indicate:— the title of the component as given in its detail specification or the name of the series or family; — the entering date; — the serial number and the suffix of the form.
Box 1	shall provide details given in table; in particular there shall be listed - the variants or range of variants; the range of components by using the ESCC code for values tolerances, etc.; the designation given in detail specification as 'based on'; ---under Test Vehicle enter either a cross or the specific characteristic capable to identify the component tested; — under component similar enter a cross.
Box 2 and 3	Manufacturer's name and location of plant where the components were manufactured and tested.
Box 4	Generic and detail specifications used during qualification program.
Box 5	Reference to test report(s) submitted in support of application.
Box 6	Enter details to identify the PID that was applicable at the time the qualification lot was manufactured.
Box 7	If the PID was evolved after qualification lot manufacture, adequate details of such evolution shall be provided together with reasons for changes. Major changes shall be clearly marked.
Box 8	The box serves to identify the current PID and the Executive Representative that has verified it together with the date of this occurrence.
Box 9	This box can be completed only after a physical visit to the plant to confirm that the practices, procedures, materials, etc. used in manufacturing the components are as described in the PID. This survey shall be carried out in accordance with the requirements of ESCC Basic Specification No. 20200 and its findings shall be recorded.
Box 10	Details entered shall be sufficient to evidence that an evaluation program according to ESCC Basic Specification No. 22600 has been performed and that the results thereof are summarized in the survey and test reports. If the evaluation program has not been carried out according to established ESCC documents, the applicant Executive Representative shall provide alternative data and declare its assessed degree of satisfactory compliance with the ESCC basic requirements. Reference shall be made to the reports on Destructive Physical Analysis (DPA), Failure Analysis and Non conformance (NCCS) issued during the Evaluation and/or Qualification Phase.
Box 11	Enter the name of the Executive Coordinator and the signature.
Box 12	To be used when there is a need to expand any of the boxes from 1 through 10. Identify box affected and reference the Box 12 in the relevant Box. Box 12 can be broken into 12a, 12b, etc. if several Boxes have to be expanded.
Box 13	Fill table as requested.
Box 14	Fill in any additional tasks required to achieve full compliance.
Box 15	All Executive recommendations on the application itself, special conditions or restrictions, modifications of the QPL or ESCC QML entry, letters to the manufacturer, etc. shall be entered clearly in Box 15, signed by the ESA Representative.
Box 16	Fill in Table as requested.
Box 17	Confidential details of PID changes shall be provided.
Box 18	State noncompliance with reference to specification(s) and paragraph(s). To simplify reference in Box 18 each nonconformance shall be sequentially numbered. If relevant state 'None'
Box 19	Any additional action deemed necessary by the Executive Representative to bring the submitted data to a standard likely to be accepted by the ESCC Executive should be listed herein or the reason(s) to accept the nonconformance.
Box 20	Additional Comments