ESCC QUALIFIED, RESIN-ENCAPSULATED MEMORY MODULE, NON-HERMETICALLY SEALED, CONSTRUCTED AS A 3D STACK OF PLASTIC PACKAGED, INDIVIDUAL ADD-ON COMPONENTS

ESCC Generic Specification No. 6001

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DCR No.	CHANGE DESCRIPTION

TABLE OF CONTENTS

1 INTRODUCTION

1.1 SCOPE

This specification defines the general requirements for the qualification, qualification maintenance, procurement, and delivery of ESCC Qualified, resin-encapsulated memory modules, non-hermetically sealed, constructed as a 3D stack of plastic packaged active memory add-on components, for space applications.

This specification contains the appropriate inspection and test schedules and also specifies the data documentation requirements.

1.2 APPLICABILITY

This specification is applicable to the granting of qualification approval to memory modules qualified in accordance with the following ESCC method:

- Qualification of Standard Components per this ESCC Generic Specification and ESCC Basic Specification No. 20100.

It is also only applicable to the procurement of memory modules so qualified. Such memory modules shall be produced in a manufacturing line which holds a valid Process Capability Approval (PCA) in accordance with ESCC Basic Specification No. 2566001.

NOTE:
The procurement and qualification of non-hermetic microelectronic modules which include internal interconnection means, such as Printed Circuit Boards other than at termination level, are not included within the scope of this specification.

2 APPLICABLE DOCUMENTS

The following documents form part of, and shall be read in conjunction with, this specification. The relevant issues shall be those in effect on the date of starting qualification or placing the Purchase Order.

2.1 ESCC SPECIFICATIONS

- No. 20100, Requirements for the Qualification of Standard Electronic Components for Space Application.
- No. 20200, Component Manufacturer Evaluation.
- No. 2026000, Checklist for Hybrid Microcircuit Manufacturer and Line Survey
- No. 20600, Preservation, Packaging and Dispatch of ESCC Components.
- No. 21001, Destructive Physical Analysis of EEE Components.
- No. 21300, Terms, Definitions, Abbreviations, Symbols and Units.
- No. 21700, General Requirements for the Marking of ESCC Components.
- No. 22600, Requirements for the Evaluation of Standard Electronic Components for Space Application.
- No. 2269000, Evaluation Test Programme for Integrated Circuits: Monolithic and Multichip Microcircuits, Wire-Bonded, Hermetically Sealed and Flip-Chip Monolithic Microcircuits, Solder Ball Bonded, Hermetically and Non-Hermetically Sealed.
- No. 22800, ESCC Non-Conformance Control System.
- No. 22900, Total Dose Steady-State Irradiation Test Method.
- No. 23500, Lead Materials and Finishes for Components for Space Application.

- No. 23800, Electrostatic Discharge Sensitivity Test Method.
- No. 24600, Minimum Quality System Requirements.
- No. 24800, Resistance to Solvents of Marking, Materials and Finishes.
- No. 25100, Single Event Effects Test Method and Guidelines.
- No. 25600, Requirements for Process Capability Approval.
- No. 2566001, Requirements for the Process Capability Approval for Manufacturing Lines of Non-Hermetic Microelectronic Modules.

For qualification and qualification maintenance or procurement of memory modules, with the exception of ESCC Basic Specifications Nos. 20100, 21700, 22800 and 24600, where Manufacturers' specifications are equivalent to, or more stringent than, the ESCC Basic Specifications listed above, they may be used in place of the latter, subject to the approval of the ESCC Executive.

Such replacements shall be clearly identified in the applicable Process Identification Document (PID). Such replacements may be listed in an appendix to the appropriate Detail Specification at the request of the Manufacturer, subject to the approval of the ESCC Executive.

Unless otherwise stated herein, references within the text of this specification to "the Detail Specification" shall mean the relevant ESCC Detail Specification.

2.2 OTHER (REFERENCE) DOCUMENTS

- ECSS-Q-ST-60-05, Space Product Assurance: Generic Procurement Requirements for Hybrid Microcircuits.
- ECSS-Q-ST-60-13, Space Product Assurance: Commercial Electrical, Electronic and Electromechanical (EEE) Components.
- ECSS-Q-ST-60-14, Space Product Assurance: Relifing Procedure - EEE Components.
- ECSS-Q-ST-70, Space Product Assurance: Materials, mechanical Parts and Processes.
- ECSS-Q-ST-70-08, Space Product Assurance: Manual Soldering of High-Reliability Electrical Connections.
- ECSS-Q-ST-70-38, Space Product Assurance: High-Reliability Soldering for Surface-Mount and Mixed Technology.
- JEP001, JEDEC Foundry Process Qualification Guidelines - Backend of Line (Wafer Fabrication Manufacturing Sites).
- JESD22-A101, JEDEC Standard Test Method: Steady-State Temperature-Humidity Bias Life Test.
- JESD22-A110, JEDEC Standard Test Method: Highly-Accelerated Temperature and Humidity Stress Test (HAST).
- JESD22-A113, JEDEC Standard Test Method: Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing.
- JESD22-B106, JEDEC Standard Test Method: Resistance to Solder Shock for Through-Hole Mounted Devices.
- MIL-STD-883, Test Methods and Procedures for Micro-electronics.

2.3 ORDER OF PRECEDENCE

For the purpose of interpretation and in case of conflict with regard to documentation, the following order of precedence shall apply:

(a) ESCC Detail Specification.
(b) ESCC Generic Specification.
(c) ESCC Basic Specification.
(d) Other documents, if referenced herein.

3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

The terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following shall apply:

Memory Module	A module assembled using individually packaged, active memory add-on components, with an interconnection substrate, all interconnected to perform a specified electronic function. The resulting 3D construction is protected using a polymeric curing material which provides the ultimate encapsulation level. **NOTES:** The active add-on components are monolithic, plastic packaged, memory components. The electronic functions of memory modules covered by this specification include SRAM, SDRAM, DDR, MRAM, EEPROM, NAND-FLASH, NOR-FLASH. These modules are not intended to be hermetic.
Memory Module Lot	A production lot, as defined in ECSS-Q-ST-60-05, of memory modules constructed using active memory add-on components that all originate from a single homogenous lot. All manufacturing steps, and the subsequent Screening Tests for the memory module lot shall each be performed at the same time or within an uninterrupted period of time.
Repair	Action to correct a defect of a memory module that leads to a configuration item change. **NOTES:** Unlike rework, repair does affect or modify parts of the defective memory module. An NCR needs to be raised in relation to any repair activity in accordance with ESCC Basic Specification No. 22800.
Rework	Action to correct a defect of a memory module that does not lead to a configuration item change. **NOTES:** Unlike repair, rework does not affect or modify parts of the defective memory module. Unlike repair, an NCR does not need to be raised in relation to repair activity.
Homogeneous Lot (as relates to active memory add-on components)	A unique lot with respect to diffusion, metallization, passivation and assembly, with a single date and trace code (ref. ECSS-Q-ST-60-13).

4 REQUIREMENTS

4.1 GENERAL

Unless otherwise specified, the requirements for the qualification of a memory module shall be in accordance with ESCC Basic Specification No. 20100 and this Specification.

The test requirements for procurement of qualified memory modules (see Chart F1) shall comprise:

- Production Control: including element evaluation, add-on component procurement and other Special In-Process Controls
- Screening Tests
- Periodic Testing
- Lot Validation Testing if stipulated in the Purchase Order.

4.1.1 Specifications

For qualification, qualification maintenance, procurement and delivery of memory modules in conformity with this specification, the applicable specifications listed in Section 2 of this document shall apply in total unless otherwise specified herein or in the Detail Specification.

4.1.2 Conditions and Methods of Test

The conditions and methods of test shall be in accordance with this specification, the ESCC Basic Specifications referenced herein and the Detail Specification.

4.1.3 Manufacturer's Responsibility for Performance of Tests and Inspections

The Manufacturer shall be responsible for the performance of tests and inspections required by the applicable specifications. These tests and inspections shall be performed at the plant of the Manufacturer of the memory modules unless it is agreed by the ESCC Executive to use an approved external facility.

4.1.4 Inspection Rights

The ESCC Executive reserves the right to monitor any of the tests and inspections scheduled in the applicable specifications.

4.1.5 Customer Source Inspections

4.1.5.1 Pre-Assembly Customer Source Inspection

If stipulated in the Purchase Order, the Orderer may perform a source inspection at the Manufacturer's facility prior to assembly of the memory modules. Details of the inspections to be performed or witnessed and the required period of notification shall be as stipulated in the Purchase Order.

4.1.5.2 Final Customer Source Inspection

If stipulated in the Purchase Order, the Orderer may perform a source inspection at the Manufacturer's facility at an appropriate point(s) during or at the end of Screening, and/or during or at the end of Lot Validation Testing testing (if applicable), that has been agreed with the Manufacturer (e.g. witness of final Room Temperature Electrical Measurements; performance of External Visual Inspection and Dimension Check; review of the data documentation package). Details of the inspections to be performed or witnessed and the required period of notification shall be as stipulated in the Purchase Order.

4.2 QUALIFICATION AND QUALIFICATION MAINTENANCE REQUIREMENTS ON A MANUFACTURER

To obtain and maintain the qualification of a memory module, or family of memory modules, a Manufacturer shall satisfy the requirements of ESCC Basic Specification No. 20100, except as amended in Para. 4.2.1.

4.2.1 Single Phase Qualification (SPQ)

The detailed evaluation phase of ESCC Basic Specification No. 20100 shall not be performed. Instead, additional assessment activities, to be performed by the Manufacturer, and supervised by and agreed with the ESCC Executive, shall be included as an initial stage in the process of achieving qualification. This approach is outlined in Chart F0 and detailed below.

Under the supervision and agreement of the ESCC Executive, the Evaluation of a Component requirements, as specified in ESCC Basic Specification No. 20100 Para. 5.3.2, may be implemented through dedicated test plans and inspections or, alternatively, through the initial assessment of existing data as detailed in this paragraph. This initial assessment shall conclude with an extended data review. Such data review may be combined with the Evaluation of a Manufacturer requirements, as specified in ESCC Basic Specification No. 20100 Para. 5.3.1 and ESCC Basic Specification No. 20200, in the form of an extended initial audit.

(a) Manufacturer Assessment

The Manufacturer shall provide the following information for the memory module(s) being qualified, to the ESCC Executive for review:

- A detailed conformance matrix to the general requirements for qualification included in ESCC Basic Specification No. 20100.
- Information explicitly indicating full details on the compliance, or otherwise, of the Manufacturer's quality management system to the requirements of ESCC Basic Specification No. 24600.
- A completed ESCC Manufacturer Checklist in accordance with ESCC Basic Specification Nos. 20200 and 2026000
- The draft Process Identification Document (PID).
- A draft ESCC Detail Specification

(b) Memory Module Assessment

The Manufacturer shall provide to the ESCC Executive sufficient information to enable the full assessment of the suitability of the memory module(s) being qualified under the following criteria:

- design margins
- constituent materials and active memory add-on components
- construction
- characterisation and performance over the full operating and storage temperature ranges
- radiation performance
- intrinsic reliability

Specific requirements, to be addressed for the memory module(s) being qualified, shall include the following (the relevant requirements specified in ESCC Basic Specification Nos. 22600 and 2269000 may be used for guidance):

i. Active Memory Add-on Component Traceabiity
Evidence of available traceability information for the selected active memory add-on components shall be assessed in order to verify compliance with this specification's requirements on memory module lots and to ensure the representativeness of assessments and evaluations performed with regards to reliability and radiation hardness.

ii. Component Reliability Assessment
This assessment shall address potential failure mechanisms and mitigation strategies, at both the active memory add-on component level and the memory module level, including, for example, calculation/evaluation of activation energy and acceleration factors for voltage and temperature, and the establishment of long term reliability failure rates.

The information gained during the determination of failure mechanisms and activation energy shall be used to determine appropriate life test conditions that would verify the goal of 18 years satisfactory operating life at Tj ≤ +110°C (see MIL-STD-883, Test Method 1016 for guidance). The Manufacturer shall determine worst case characteristics for the memory module (JEP001 may be used as a guideline). Suitable information shall be provided to demonstrate that the goal of 18 years satisfactory operating life at Tj ≤ +110°C is also met at the active memory add-on component level.

If no suitable data are available, the 4000 hours Operating Life test, to be performed during qualification testing in accordance with Chart F4, shall be extended, as suitable, for evaluation purposes.

iii. Construction Analysis
Construction analysis shall be performed on a minimum of 3 sample Memory Modules. The content and extent of the construction analysis shall be agreed with the ESCC Executive. ESCC Basic Specification No. 21001 may be used as a guideline.

The combination of materials and processes used to produce the memory modules shall be evaluated and validated in accordance with ESCC Basic Specification No. 2566001.

iv. Electrical Characterisation
Suitable information on the specific electrical performance details for the memory module(s), including the verification of their functionality over the full operating temperature range, shall be provided (as applicable).

v. Radiation Assessment
Suitable information on the ability of the memory module(s) to withstand the space radiation environment in line with the requirements of ESCC Basic Specification Nos. 22900 and 25100 (as applicable) shall be provided.

vi. Package Assessment

Suitable information on the following specific package assessment details for the memory module(s) shall be provided (as applicable):

- Assessment of the memory module(s) capability to withstand typical mounting in accordance with ECSS-Q-ST-70-08 and/or ECSS-Q-ST-70-38.
- Resistance to Soldering Heat.
- Pin-to-Pin Isolation.
- Thermal Resistance Characterisation.
- The ability to withstand thermal cycling and thermal shock.
- The ability to withstand environmental loads as vibration and mechanical shock.
- Aspects specific to the non-hermetic nature of the memory modules: HAST or other PCA testing as suitable, as defined in ESCC Basic Specification No. 2566001.

NOTE:

For SPQ, the number of memory modules selected for component assessment testing will depend on whether a single memory module type or a family of memory modules is being assessed, the number of memory modules types chosen to represent the family, and the availability of appropriate, suitable information. The memory module types chosen to represent a family shall cover the range of memory modules to be qualified and shall be representative of the different package and pin configurations. They shall also be the most suitable for highlighting those characteristics and parameters that are pertinent to an investigation into failure modes and weaknesses. These test samples shall be as specified by or agreed with the ESCC Executive.

The verification of the completeness and adequacy of data related to the preliminary additional assessment, will be performed by the ESCC Executive as part of a Manufacturer Data Review, to be conducted in accordance with ESCC Basic Specification Nos. 20200 and 2026000, and this specification.

Subject to the ESCC Executive verifying the adequacy and completeness of the additional assessment information in (a) and (b) above, as presented by the Manufacturer during the Manufacturer Data Review, this initial stage of SPQ will be considered completed. The draft ESCC Detail Specification and PID shall be revised as necessary, and frozen pending completion of qualification testing. SPQ shall continue in line with the requirements of the Qualification Testing Phase as detailed in ESCC Basic Specification No. 20100 and Chart F4 of this specification.

4.3 DELIVERABLE COMPONENTS

Memory modules delivered to this specification shall be processed and inspected in accordance with the relevant Process Identification Document (PID).

Each memory module identified with an ESCC component number and delivered to this specification shall:

- be traceable to its memory module lot.
- have satisfactorily completed all the tests required by the relevant issues of the applicable specifications.
- be produced from lots that are considered by the Manufacturer to be capable of passing all applicable tests, and sequences of tests, that are defined in Chart F4. The Manufacturer shall not knowingly supply memory modules that cannot meet this requirement. In the event that, subsequent to delivery and prior to operational use, a memory module is found to be in a condition such that, demonstrably, it could not have passed these tests at the time of manufacture, this shall be grounds for rejection of the delivered lot.

4.3.1 Lot Failure

Lot failure may occur during Screening Tests (Chart F3) or Qualification, Periodic Testing and Lot Validation Testing (Chart F4).

Should such failure occur during qualification, qualification maintenance or procurement, the Manufacturer shall initiate the non-conformance procedure in accordance with ESCC Basic Specification No. 22800. The Manufacturer shall notify the Orderer and the ESCC Executive by any appropriate written means, within 5 working days, giving details of the number and mode of failure and the suspected cause. No further testing or analysis shall be performed on the failed memory modules until so instructed by the ESCC Executive.

4.4 MARKING

All memory modules procured and delivered to this specification shall be marked in accordance with ESCC Basic Specification No. 21700.

4.5 MATERIALS AND FINISHES

Specific requirements for materials and finishes are specified in the Detail Specification. Where a definite material or finish is not specified a material or finish shall be used so as to ensure that the memory module meets the performance requirements of this specification and the Detail Specification. Acceptance or approval of any constituent material or finish does not guarantee acceptance of the finished product.

The manufacturer shall implement a system for the selection and control of materials and active memory add-on components in conformance with ECSS-Q-ST-70.

All materials and finishes of the memory modules specified in the Detail Specification shall comply with the restrictions on materials specified in ESCC Basic Specification No. 22600.

4.6 DESIGN ASSURANCE

4.6.1 General

The design activities undertaken by a manufacturer in order to implement specific electrical functions, derived from a circuit diagram, in a finished memory module shall include:

- the selection of a technology (a combination of materials, processes and active memory add on components)
- the definition of the physical layout of the interconnections necessary to enable the electrical function
- the application of derating requirements, as applicable
- the implementation of radiation hardness assurance provisions, for the active memory add-on components and for the whole memory module circuit
- the analysis of the design with regard to its reliability

The ESCC Executive shall verify, as applicable for each memory module design within the qualification domain, the conformance to the requirements of Para. 4.6 prior to commencing the Qualification test campaign as specified in Para. 7.1.

4.6.2 The Selection of a Technology

The materials, processes and active memory add-on parts assembled to produce ESCC qualified memory modules delivered in accordance with this specification shall be as described in the relevant Module Technology Identification Form (MTIF; based on the HTIF in ESCC-Q-ST-60-05 Annex A) provided by the memory module Manufacturer and approved by the ESCC Executive for the memory module in question.

The requirements applicable to add-on components, materials and processes so selected are specified in Para. 5.2.

Such memory modules shall be produced in a manufacturing line which holds a valid Process Capability Approval (PCA) in accordance with ESCC Basic Specification No. 2566001.

The performance requirements of a memory module qualified in accordance with this specification shall be as specified in the Detail Specification.

4.6.3 Radiation Hardness Assurance

The design of memory modules to be ESCC qualified in accordance with this specification shall conform to Radiation Hardness Assurance (RHA) requirements as specified herein.

The RHA methodology implemented by a Manufacturer seeking ESCC qualification of a memory module shall:

- Be able to guarantee the conformance of delivered modules to performance requirements which include radiation effects. Such requirements shall be specified in the applicable Detail specification and, for procurement, be stipulated in the Purchase Order, if required by the Customer.
- Be able to implement radiation hardness assurance at active memory add-on component level.
- Analyse memory module performance degradations in consideration of the active memory add-on component's sensitivity.
- Take into account the following radiation-induced effects: Total Ionizing Dose (TID), Displacement Damage (or Total Non-Ionizing Dose, TNID) and Single Event Effects (SEE).

  NOTE: Spacecraft charging effects are out of the scope of this specification.

4.7 RADIATION TESTING

For qualification or qualification maintenance, total dose radiation testing shall be performed, at the active memory add-on component level, when specified in the Detail Specification to the specified total dose level (see Para. 5.2.1.1)

For procurement, as stipulated in the Purchase Order, total dose radiation testing shall be performed, at the active memory add-on component level, to the total dose level specified in the Detail Specification or to an alternate level if so stipulated in the Purchase Order (see Para. 5.2.1.1).

The qualification status of the procured memory modules shall not be impacted by any change to the total dose level applied to the active memory add-on components.

For procurement, any lot of active memory add-on components that fails the specified total dose radiation test level may be accepted to a lower level of radiation subject to satisfactory test results at the lower level. In this case the total dose radiation level letter for the associated memory module lot(s) shall be modified accordingly.

4.8 ADD-ON COMPONENTS, MATERIALS AND PROCESSES REQUIREMENTS

Add-on components, materials and processes used in memory modules supplied to this specification shall meet the requirements of Para. 5.2. The requirements for add-on components, materials and processes shall be listed in the ESCC Executive approved PID.

5 PRODUCTION CONTROL

5.1 GENERAL

Unless otherwise specified herein or in the Detail Specification, all memory modules as well as all active memory add-on component lots and materials incorporated into memory module lots, used for qualification and qualification maintenance, Lot Validation Testing and for delivery shall be subject to tests and inspections in accordance with Chart F2 in the sequence shown. The applicable test requirements are detailed in the paragraphs referenced in Chart F2.

In particular, the requirements applicable to active memory add-on components are specified in Paras. 5.2 and 5.2.1.

Any active memory add-on component lot, material lot or individual memory module which does not meet these requirements shall be removed and at no future time be resubmitted to the requirements of this specification.

The full production control provisions are defined in the PID.

5.1.1 Rework and Repair

The scope of a manufacturer’s activities with regards to both rework and repair allowed during the manufacturing of a memory module shall be sufficiently documented in the ESCC Executive approved PID of the manufacturing line concerned.

With regard to repair, as long as the manufacturing operations performed on a memory module are within the approved PID for the manufacturing line, the repair of a defective memory module during the manufacturing stage may take place in the context of activities derived from a minor NCR, addressed by a local (Level 1) Materials Review Board as specified in ESCC Basic Specification No. 22800.

5.2 REQUIREMENTS FOR ADD-ON COMPONENTS, MATERIALS AND PROCESSES

All add-on components, materials and processes used in deliverable memory modules in conformity with this specification shall each be compliant with the requirements and the approved domain of a valid Process Capability Approval (PCA) for the memory module manufacturing line, in accordance with ESCC Basic Specification No. 2566001.

This includes the following elements (as applicable):

- Individual, plastic packaged, active memory add-on components.
- Interconnection substrate and electrical connections within the memory module
- Encapsulating resin
- Other materials (such as attachment mediums, carriers, mechanical parts)
- Manufacturing processes

Each of these elements shall, as a minimum, be validated through assessment, inspection and test as specified in Paras. 5.2.1 and 5.2.2 prior to their use within the assembly of the memory modules to be qualified in accordance with this specification.

For the purposes of qualification in accordance with this specification, the actual verification of the memory module's conformance to the requirements of this specification shall be achieved by inspection (review of the PID and element evaluation test reports provided by the Manufacturer), and audit of the Manufacturer's facilities, both performed by the ESCC Executive.

The element evaluation test plan(s) may be based on the incremental evaluation approach specified in ESCC Basic Specification No. 2566001.

The PID shall include a list of add-on components, materials and processes which have been successfully tested in accordance with the requirements of this specification and approved for their inclusion in the PID by the ESCC Executive.

5.2.1 Element Evaluation: Validation of Active Memory Add-on Components

All active memory add-on components used in deliverable memory modules in conformity with this specification shall each be procured as traceable, homogeneous lots in accordance with the relevant procurement documentation listed in the ESCC Executive approved PID.

The selection and use of active memory add-on components shall include an initial assessment by the memory module Manufacturer, followed by inspections and tests at the time of their procurement.

A single memory module lot shall contain only a single homogeneous lot of active memory add-on components. Active memory add-on components shall be traceable to their memory module lot and their individual date and trace codes (ref. ECSS-Q-ST-60-13 Para. 4.3).

Active memory add-on components, prior to their use in the construction of memory modules in conformity with this specification, shall be compliant with the Class 1 component evaluation, component procurement, procurement specification, screening, lot acceptance, and handling and storage requirements of Paras. 4.2.3, 4.3, 4.3.1, 4.3.2, 4.3.3, 4.3.5 and 4.4, respectively, of ECSS-Q-ST-60-13.

Active memory add-on components shall be assembled into the memory modules within the time restrictions specified by the active memory add-on component manufacturer, if any. ECSS-ST-Q-60-14 Class 1 requirements for relifing may be applied by the memory module Manufacturer to active memory add-on components so long as they do not contravene any relevant restrictions as (or if) specified by the active memory add-on component Manufacturer.

Test optimisation during the 100% screening of active memory add-on components prior to their use in memory modules, may be implemented in order to avoid repetition of tests or stress accumulation during successive testing at add-on component and memory module level. Such test optimisation shall be described in the PID and approved by the ESCC Executive. In this case, the agreed deviations shall be described in the memory module Detail Specification.

5.2.1.1 Total Dose Radiation Testing

For qualification or qualification maintenance of memory modules:

- Each single homogeneous lot of active memory add-on components incorporated into memory modules being subjected to testing shall have been subjected to and successfully completed Total Dose Radiation Testing in accordance with Para. 8.1 to the total dose level specified in the Detail Specification.

During procurement of memory modules:

- If stipulated in the Purchase Order, each single homogeneous lot of active memory add-on components incorporated into memory modules being procured shall have been subjected to and successfully completed Total Dose Radiation Testing in accordance with Para. 8.1 to the stipulated total dose level.

5.2.2 Element Evaluation: Validation of Materials and Processes

All materials and processes used in memory modules in conformity with this specification, including interconnection substrate, electrical connections and encapsulating resin, shall be in conformance with the requirements of the ESCC Executive approved PID and the valid Process Capability Approval (PCA) for the memory module manufacturing line in accordance with ESCC Basic Specification No. 2566001.

5.2.3 Documentation

Documentation applicable specifically to active memory add-on components shall be in accordance with Para. 9.5.

5.3 SPECIAL IN-PROCESS CONTROLS

5.3.1 Pre-Assembly Visual Inspection

Pre-Assembly Visual Inspection shall consist of external visual inspection of all the different elements used in construction of the memory modules prior to encapsulation, including active memory add-on components, in accordance with Para. 8.2.

5.3.2 Dimension Check

Dimension Check shall be performed after assembly of the memory modules in accordance with Para. 8.3 on 3 samples only. In the event of any failure a 100% Dimension Check shall be performed.

5.3.3 Weight

The maximum weight of the memory module specified in the Detail Specification shall be guaranteed but not tested.

5.3.4 Documentation
Documentation of Special In-Process Controls shall be in accordance with Para. 9.6.

6 SCREENING TESTS

6.1 GENERAL
Unless otherwise specified herein or in the Detail Specification, all lots of memory modules used for qualification and qualification maintenance, Lot Validation Testing, and for delivery, shall be subjected to tests and inspections in accordance with Chart F3 in the sequence shown.

All memory modules shall be serialised prior to the tests and inspections.

Any memory modules which do not meet these requirements shall be removed from the lot and at no future time be resubmitted to the requirements of this specification.

The applicable test methods and conditions are specified in the paragraphs referenced in Chart F3.

6.2 FAILURE CRITERIA

6.2.1 Environmental and Mechanical Test Failure
The following shall be counted as memory module failures:

- Memory modules which fail during tests for which the pass/fail criteria are inherent in the test method, i.e. External Visual Inspection.

6.2.2 Parameter Drift Failure
The acceptable change limits are shown in Parameter Drift Values in the Detail Specification. A memory module shall be counted as a parameter drift failure if the changes during Power Burn-in are larger than the drift values (Δ) specified.

6.2.3 Parameter Limit Failure
A memory module shall be counted as a limit failure if one or more parameters exceed the limits shown in Room Temperature Electrical Measurements or High and Low Temperatures Electrical Measurements in the Detail Specification.

Any memory module which exhibits a limit failure prior to the submission to Power Burn-in shall be rejected and not counted when determining lot rejection.

6.2.4 Other Failures
A memory module shall be counted as a failure in any of the following cases:

- Visual failure.
- Mechanical failure.
- Handling failure.
- Lost component.

6.3 FAILED COMPONENTS
A memory module shall be considered as failed if it exhibits one or more of the failure modes described in Para. 6.2.

6.4 LOT FAILURE

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.1.

6.4.1 Lot Failure during 100% Testing

If the number of components failed on the basis of the failure criteria specified in Paras. 6.2.2 and 6.2.3 exceeds either 10% (rounded upwards to the nearest whole number) of the memory modules submitted to Power Burn-in of Chart F3, or 5% (rounded upwards to the nearest whole number) of the total quantity of active memory add-on components that make up those memory modules, the memory module lot shall be considered as failed.

If a lot is composed of groups of memory modules of one family defined in one ESCC Detail Specification, but separately identifiable for any reason, then the lot failure criteria shall apply separately to each identifiable group.

6.4.2 Lot Failure during Sample Testing

A memory module lot shall be considered as failed if the number of allowable failures during sample testing as specified herein or in the Detail Specification, is exceeded.

Unless otherwise specified, if a lot failure occurs, a 100% testing may be performed but the cumulative percent defective shall not exceed that specified in Para. 6.4.1.

6.5 DOCUMENTATION

Documentation of Screening Tests shall be in accordance with Para. 9.7.

7 QUALIFICATION, QUALIFICATION MAINTENANCE AND LOT VALIDATION TESTING

The requirements of this paragraph are applicable to the tests performed on memory modules or test structures as part of qualification or qualification maintenance in accordance with ESCC Basic Specification No. 20100. They are also applicable to Lot Validation Testing as part of procurement.

7.1 QUALIFICATION TESTING

7.1.1 General

Qualification testing shall be in accordance with the requirements specified in Chart F4. The tests of Chart F4 shall be performed on the specified sample, chosen at random from the memory modules which have successfully passed the tests in Chart F3. This sample constitutes the Qualification Test Lot.

The Qualification Test Lot is divided into subgroups of tests and, unless otherwise specified, all memory modules assigned to a subgroup shall be subjected to all of the tests in that subgroup, in the sequence shown. The applicable test requirements are detailed in the paragraphs referenced in Chart F4.

The conditions governing qualification testing are specified in ESCC Basic Specification No. 20100.

7.1.2 Distribution within the Qualification Test Lot

The Qualification Test Lot shall be comprised in accordance with the following provisions, depending on whether it is required to obtain qualification for a single memory module type or for a family of memory module types.

7.1.2.1 Single Component Type

When it is proposed to submit a single memory module type for qualification testing, the sample quantity shall be as specified in Chart F4.

However, when such a single memory module type is to be qualified in more than one type of package, each package variation must be equally represented in, the Environmental, Endurance and Assembly Capability Subgroups of Chart F4. For this purpose, the applicable sample distribution shall be the same as for the qualification of a family of memory module types as specified in Para. 7.1.2.2.

7.1.2.2 Family of Component Types

A family of memory module types is a series of components produced by the same manufacturing techniques, using the same types of machines and apparatus. Such memory modules will be designed for the same supply, bias and signal voltages and for an input/output compatibility with each other under an established set of loading rules. They shall be produced using the same technology (e.g. the same diffusion schedules, method of metallisation, potting materials, and assembly schedules, etc.) and identical design rules.

Qualification may be granted to a family of memory modules subject to the successful outcome of the qualification testing of certain specified memory module types to represent the family.

Structurally similar memory modules from such a family may be grouped together for the purpose of selecting samples for qualification testing. The memory module types selected must adequately represent all of the various mechanical, structural and electrical elements encountered within the family.

The memory module types chosen must be those that employ the extremes of design rules and tolerances and contain the maximum of internal sub-circuitry complexity, i.e. usually those that give the greatest risk of rejection.

When qualification is required for memory module types in more than one type of package, each package must be adequately represented in the Environmental, Endurance and Assembly Capability subgroups.

The memory module types may be specified by, but in any case shall be agreed with the ESCC Executive prior to the commencement of qualification testing and the justification for the selection shall be declared in the qualification test report.

The number of memory module types selected as representative of the family will therefore determine the total number of memory modules comprising the qualification test lot. The sample sizes shall be agreed with the ESCC Executive prior to the commencement of Qualification Testing

7.2 QUALIFICATION MAINTENANCE (PERIODIC TESTING)

Qualification is maintained through periodic testing and the test requirements of Para. 7.1 shall apply. For each subgroup, the sample size, the test requirements and the period between successive subgroup testing shall be as specified in Chart F4.

The conditions governing qualification maintenance are specified in ESCC Basic Specification No. 20100.

7.3 LOT VALIDATION TESTING

For procurement of each memory module lot, Lot Validation Testing is not required and shall only be performed if specifically stipulated in the Purchase Order.

When Lot Validation Testing is required, it shall consist of the performance of one or more of the tests or subgroup test sequences of Chart F4. The testing to be performed and the sample size shall be as stipulated in the Purchase Order.

When procurement of more than one memory module type is involved from a family, range or series, the selection of representative samples shall also be stipulated in the Purchase Order.

7.4 FAILURE CRITERIA

The following criteria shall apply to qualification, qualification maintenance and Lot Validation Testing.

7.4.1 Environmental and Mechanical Test Failure

The following shall be counted as memory module failures:

- memory modules which fail during tests for which the pass/fail criteria are inherent in the test method, e.g. Terminal Strength, etc.

7.4.2 Electrical Failure

The following shall be counted as memory module failures:

- memory modules which fail one or more of the applicable limits at each of the relevant data points specified for environmental and endurance testing in Intermediate and End-Point Electrical Measurements in the Detail Specification.

7.4.3 Other Failures

A memory module shall be counted as a failure in any of the following cases:

- Visual failure
- Mechanical failure
- Handling failure
- Lost component

7.5 FAILED COMPONENTS

A memory module shall be considered as failed if it exhibits one or more of the failure modes detailed in Para. 7.4.

When requested by the ESCC Executive, failure analysis of failed memory modules shall be performed under the responsibility of the Manufacturer and the results provided.

Failed memory modules shall be retained at the Manufacturer’s plant until the final disposition has been agreed and certified.

7.6 LOT FAILURE

For qualification and qualification maintenance, the lot shall be considered as failed if one memory module in any subgroup of Chart F4 is a failed component based on the criteria specified in Para. 7.4.

For procurement, the lot shall be considered as failed if one memory module in any test specified for Lot Validation Testing is a failed component based on the criteria specified in Para. 7.4.

In the case of lot failure, the Manufacturer shall act in accordance with Para. 4.3.1.

7.7 QUALIFICATION, PERIODIC TESTING AND LOT VALIDATION TESTING SAMPLES

All tests of Chart F4 are considered to be destructive and therefore memory modules so tested shall not form part of the delivery lot.

7.8 DOCUMENTATION

Documentation of Qualification, Periodic Testing, and Lot Validation Testing shall be in accordance with Para. 9.8.

8 TEST METHODS AND PROCEDURES

If a Manufacturer elects to eliminate or modify a test method or procedure, the Manufacturer is still responsible for delivering memory modules that meet all of the performance, quality and reliability requirements defined in this specification and the Detail Specification.

Documentation supporting the change shall be approved by the ESCC Executive and retained by the Manufacturer. It shall be copied, when requested, to the ESCC Executive. The change shall be specified in an appendix to the Detail Specification and in the PID.

8.1 TOTAL DOSE RADIATION TESTING

ESCC Basic Specification No. 22900 to the total dose level specified in the Detail Specification or as stipulated in the Purchase Order, performed at active memory add-on component level.

8.2 PRE-ASSEMBLY VISUAL INSPECTION

All active memory add-on components shall be visually inspected prior to assembly within the memory module in accordance with MIL-STD-883, Test Methods 2009 and 2017 Class K as well as any technology specified additional requirements as specified in the ESCC Executive approved PID.

In addition to the test methods specified above, this inspection shall verify that no damage has occurred to, and no contamination is present on, the any of the various elements and substrate.

8.3 DIMENSION CHECK

Dimension Check shall be performed on a sample of 3 memory modules in accordance with MIL-STD-883, Test Method 2016 and the Detail Specification. In the event of any failure a 100% Dimension Check shall be performed.

8.4 TEMPERATURE CYCLING

8.4.1 Screening Tests (Chart F3)

MIL-STD-883, Test Method 1010. Test Condition B (10 cycles; -55 (+0 -10)°C to +125 (+15 -0)°C).

8.4.2 Qualification and Periodic Testing (Chart F4)

MIL-STD-883, Test Method 1010. Test Condition B (-55 (+0 -10)°C to +125 (+15 -0)°C), except the number of cycles shall be 500 minimum. The following details shall also apply:

(a) Preconditioning shall be performed prior to Temperature Cycling as follows:
- For though-hole memory modules: in accordance with JESD22-B106.
- For SMD memory modules: in accordance with JESD22-A113.

8.5 ELECTRICAL MEASUREMENTS

8.5.1 Parameter Drift Values

At each of the relevant data points during Screening Tests (Chart F3), Parameter Drift Values shall be measured as specified in the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated.

8.5.2 High and Low Temperatures Electrical Measurements

High and Low Temperatures Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers.

8.5.3 Room Temperature Electrical Measurements

Room Temperature Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers.

8.5.4 Intermediate and End-Point Electrical Measurements

At each of the relevant data points during Qualification, Periodic Testing and Lot Validation Testing (Chart F4), Intermediate and End-Point Electrical Measurements shall be performed as specified in the Detail Specification. All values obtained shall be recorded against serial numbers and the parameter drift calculated, if specified.

8.6 POWER BURN-IN

MIL-STD-883, Test Method 1015, Test Condition D with the following conditions:

- Duration: Unless otherwise specified in the Detail Specification, memory modules shall be subjected to a total Power Burn-in period of 240 (+24 -0) hours.
- Test Temperature: Unless otherwise specified in the Detail Specification, ambient or case temperature to achieve Tj (+0 -10)°C as specified in the Detail Specification.
- Other Test Conditions: As specified in Power Burn-in in the Detail Specification.
- Data Points:
  As specified in Parameter Drift Values in the Detail Specification at 0 and T (+24 -0) hours (where T is the specified duration).

  Drift shall be related to the initial measurement for Power Burn-in.

8.7 EXTERNAL VISUAL INSPECTION

External Visual Inspection shall be performed in accordance with MIL-STD-883, Test Method 2009.

8.8 MICROSECTIONING

The Memory Module shall be microsectioned in a suitable plane to enable clear inspection of its internal structure including platings, external leads and the internal stack of add-on components. The exposed internal face of the module shall be polished to a surface finish that enables accurate measurements of all module plating thicknesses. As a minimum, the inspection shall address the following aspects to ensure that they meet the requirements of the PID:

- Plating requirements of the module and external leads, as specified in the Detail Specification including adhesion of plating to the leads.
- alignment of the internal stack within the module.
- adhesion of the module encapsulation resin to the surfaces of the internal add-on components.
- connection of internal add-on component terminals to the outer module plating.

Photographs of all aspects of the microsectioned module shall be taken, each recorded against serial number.

8.9 HUMIDITY (THB OR HAST)

Either Temperature Humidity Bias (THB) in accordance with JESD22 Test Method A101 (+85 ±2°C, 85 ±5%, 1000 hours), or Highly Accelerated Stress Test (HAST) in accordance with JESD22 Test Method A110 (+130 ±2°C, 85 ±5%, 96 hours, or +110 ±2°C, 85 ±5%, 264 hours) shall be performed with the following conditions:

- Test Method: As specified in Humidity Test Conditions in the Detail Specification.
- Preconditioning shall be performed prior to THB and HAST as follows:
  - For though-hole memory modules: in accordance with JESD22-B106.
  - For SMD memory modules: in accordance with JESD22-A113.
- Bias Conditions: Continuous bias as specified in Humidity Test Conditions in the Detail Specification.
- Data Points:
  As specified in Intermediate and End-Point Electrical Measurements in the Detail Specification at prior to and on completion of testing. If drift values are specified, the drift shall always be related to the initial measurement.

8.10 OPERATING LIFE

MIL-STD-883, Test Method 1005.

- Duration:
  - 4000 hours for initial Qualification Testing, and for Periodic Testing for renewal of qualification after lapse (Chart F4)
  - 2000 hours for Periodic Testing for extension of qualification (Chart F4)
- Test Temperature: Ambient or case temperature to achieve Tj (+0 -10)°C as specified in the Detail Specification.
- Other Test Conditions: As specified in Operating Life in the Detail Specification.
- Data Points:
  As specified in Intermediate and End-Point Electrical Measurements in the Detail Specification at 0 hour, 1000 ±48 hours and 2000 ±48 hours (and 4000 ±48 hours if applicable). If drift values are specified, the drift shall always be related to the 0 hour measurement.

8.11 SOLDERABILITY

MIL-STD-883, Test Method 2003, to be performed on all leads.

8.12 PERMANENCE OF MARKING

ESCC Basic Specification No. 24800 or MIL-STD-883, Test Method 2015

8.13 TERMINAL STRENGTH

Unless otherwise specified in the Detail Specification, MIL-STD-883, Test Method 2004, Test Condition B2 performed on 3 leads (excluding corner leads) or 10% of the leads (whichever is greater) randomly selected on each memory module.

9 DATA DOCUMENTATION

9.1 GENERAL

For the qualification, qualification maintenance and procurement for each memory module lot a data documentation package shall exist in a printed or electronic form.

This package shall be compiled from:

(a) Cover sheet (or sheets).
(b) List of equipment (testing and measuring).
(c) List of test references.
(d) Add-on components procurement and element evaluation data (Chart F2).
(e) Special In-Process Controls data (Chart F2).
(f) Screening Tests data (Chart F3).
(g) Qualification, Periodic Testing and Lot Validation Testing (when applicable) data (Chart F4).
(h) Failed components list and failure analysis report (when applicable).
(i) Certificate of Conformity.

Items (a) to (i) inclusive shall be grouped, preferably as subpackages and, for identification purposes, each page shall include the following information:

- ESCC Component Number.
- Manufacturer's name.
- Memory Module Lot identification.
- Date of establishment of the document.
- Page number.

Whenever possible, documentation should preferably be available in electronic format suitable for reading using a compatible PC. The format supplied shall be legible, durable and indexed. The preferred storage medium is CD-ROM and the preferred file format is PDF.

9.1.1 Qualification and Qualification Maintenance

In the case of qualification or qualification maintenance, the items listed in Para. 9.1(a) to (j) are required.

9.1.2 Memory Module Procurement and Delivery

For all deliveries of memory modules procured to this specification, the following documentation shall be supplied:

(a) Cover sheet (if all of the information is not included on the Certificate of Conformity).
(b) Certificate of Conformity (including range of delivered serial numbers).
(c) Information related to packaging, transportation and storage of the memory modules (see Para. 11).

9.1.3 Additional Documentation

The Manufacturer shall deliver additional documentation containing data and reports to the Orderer, if stipulated in the Purchase Order.

9.1.4 Data Retention/Data Access

If not delivered, all data shall be retained by the Manufacturer for a minimum of 20 years during which time it shall be available for review, if requested, by the Orderer or the ESCC Executive.

9.2 COVER SHEET(S)

The cover sheet(s) of the data documentation package shall include as a minimum:

(a) Reference to the Detail Specification, including issue and date.
(b) Reference to the applicable ESCC Generic Specification, including issue and date.
(c) ESCC Component Number and the Manufacturer's part type number.
(d) Memory Module Lot identification.
(e) Range of delivered serial numbers.
(f) Number of the Purchase Order.
(g) Total dose radiation test level (if applicable).
(h) Information relative to any additions to this specification and/or the Detail Specification.
(i) Manufacturer's name and address.
(j) Location of the manufacturing plant (specify place of assembly and test).
(k) Signature on behalf of Manufacturer.
(l) Total number of pages of the data package.

9.3 LIST OF EQUIPMENT USED

A list of equipment used for tests and measurements shall be prepared. Where applicable, this list shall contain inventory number, Manufacturer's type number, serial number, etc. This list shall indicate for which tests such equipment was used.

9.4 LIST OF TEST REFERENCES

This list shall include all Manufacturer's references or codes which are necessary to correlate the test data provided with the applicable tests specified in the tables of the Detail Specification.

9.5 ADD-ON COMPONENTS PROCUREMENT AND ELEMENT EVALUATION TESTING DATA (PARA. 5.2.1 AND CHART F2)

For each memory module lot, a summary of the procurement details applicable to all active memory add-on components contained therein shall be complied including:

- Procurement documentation
- Add-on component Manufacturer's name and location
- Lot identification
- Certificate of Conformity
- Traceability information against memory module serial number.

For active memory add-on component element evaluation testing in accordance with Para. 5.2.1, documented evidence of its satisfactory completion (analyses, test reports, technical notes, etc) shall be compiled and retained by the Manufacturer. It shall remain available for review by the ESCC Executive on request.

A total dose radiation test report shall be prepared in accordance with the requirements of ESCC Basic Specification No. 22900 (if specified).

9.6 SPECIAL IN-PROCESS CONTROLS DATA (CHART F2)

A test result summary shall be compiled showing the total number of memory modules submitted to, and the total number rejected after each of the tests.

9.7 SCREENING TESTS DATA (CHART F3)

A test result summary shall be compiled showing the total number of memory modules submitted to and the total number rejected after each of the tests. For each test requiring electrical measurements, the results shall be recorded against memory module serial number. Drift calculations shall be recorded for each specified test against memory module serial number.

9.8 QUALIFICATION, PERIODIC TESTING AND LOT VALIDATION TESTING DATA (CHART F4)

9.8.1 Qualification Testing

A test result summary shall be compiled showing the memory modules submitted to, and the number rejected after each test in each subgroup. Memory module serial numbers for each subgroup shall be identified. For each test requiring electrical measurements, the results shall be recorded against memory module serial number. Where a drift value is specified during a test, the drift calculation shall be recorded against memory module serial number.

9.8.2 Periodic Testing for Qualification Maintenance

A test result summary shall be compiled showing the memory modules submitted to and the number rejected after each test in each subgroup. Memory module serial numbers for each subgroup shall be identified. For each test requiring electrical measurements, the results shall be recorded against memory module serial number. Where a drift value is specified during a test, the drift calculation shall be recorded against memory module serial number.

In addition to the full test data a report shall be compiled for each subgroup of Chart F4 to act as the most recent Periodic Testing summary. These reports shall include a list of all tests performed in each subgroup, the ESCC Component Numbers and quantities of memory modules tested, a statement confirming all the results were satisfactory, the date the tests were performed and a reference to the full test data.

9.8.3 Lot Validation Testing

A test result summary shall be compiled showing the memory modules submitted to and the number rejected after each test. Memory module serial numbers shall be identified. For each test requiring electrical measurements, the results shall be recorded against memory module serial number. Where a drift value is specified during a test, the drift calculation shall be recorded against memory module serial number.

9.9 FAILED COMPONENTS LIST AND FAILURE ANALYSIS REPORT

The failed components list and failure analysis report shall provide full details of:

(a) The reference and description of the test or measurement performed as defined in this specification and/or the Detail Specification during Production Control, Screening Tests, Qualification, Periodic Testing and Lot Validation Testing.
(b) Traceability information including memory module lot and memory module serial number (if applicable) of the failed memory module.
(c) The failed parameter and the failure mode of the memory module.
(d) Detailed failure analysis (if requested by the ESCC Executive or Orderer).

9.10 CERTIFICATE OF CONFORMITY

A Certificate of Conformity shall be established in accordance with the requirements of ESCC Basic Specification No. 20100.

10 DELIVERY

For procurement, for each order, the items forming the delivery are:

(a) The delivery lot.
(b) The memory modules used for Lot Validation Testing (as applicable), but not forming part of the delivery lot.
(c) The relevant documentation in accordance with the requirements of Paras. 9.1.2 and 9.1.3.

All data of all memory modules submitted to Lot Validation Testing shall also be copied, when requested, to the ESCC Executive.

For qualification or qualification maintenance, the disposition of the Qualification Test Lot and its related documentation shall be as specified in ESCC Basic Specification Nos. 20100 and the relevant paragraphs of Section 9 of this specification.

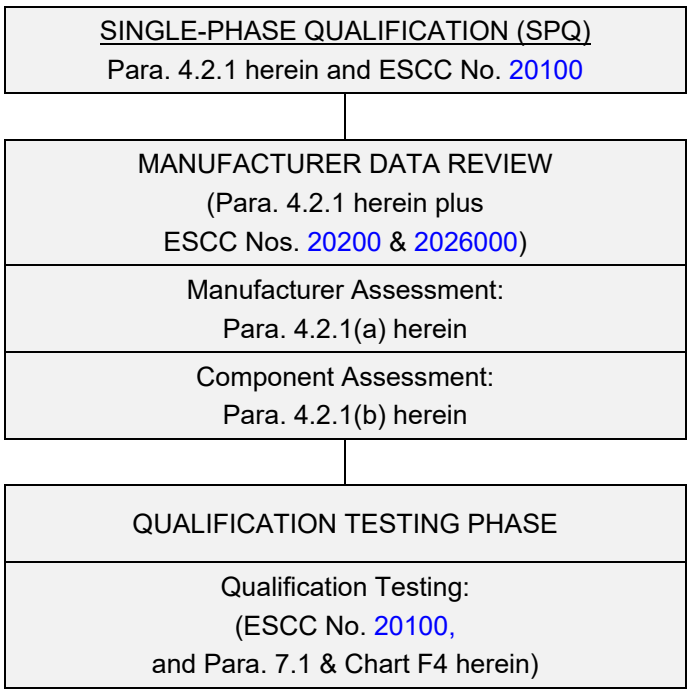
11 PACKAGING AND DISPATCH

The packaging and dispatch of memory modules to this specification shall be in accordance with the requirements of ESCC Basic Specification No. 20600.

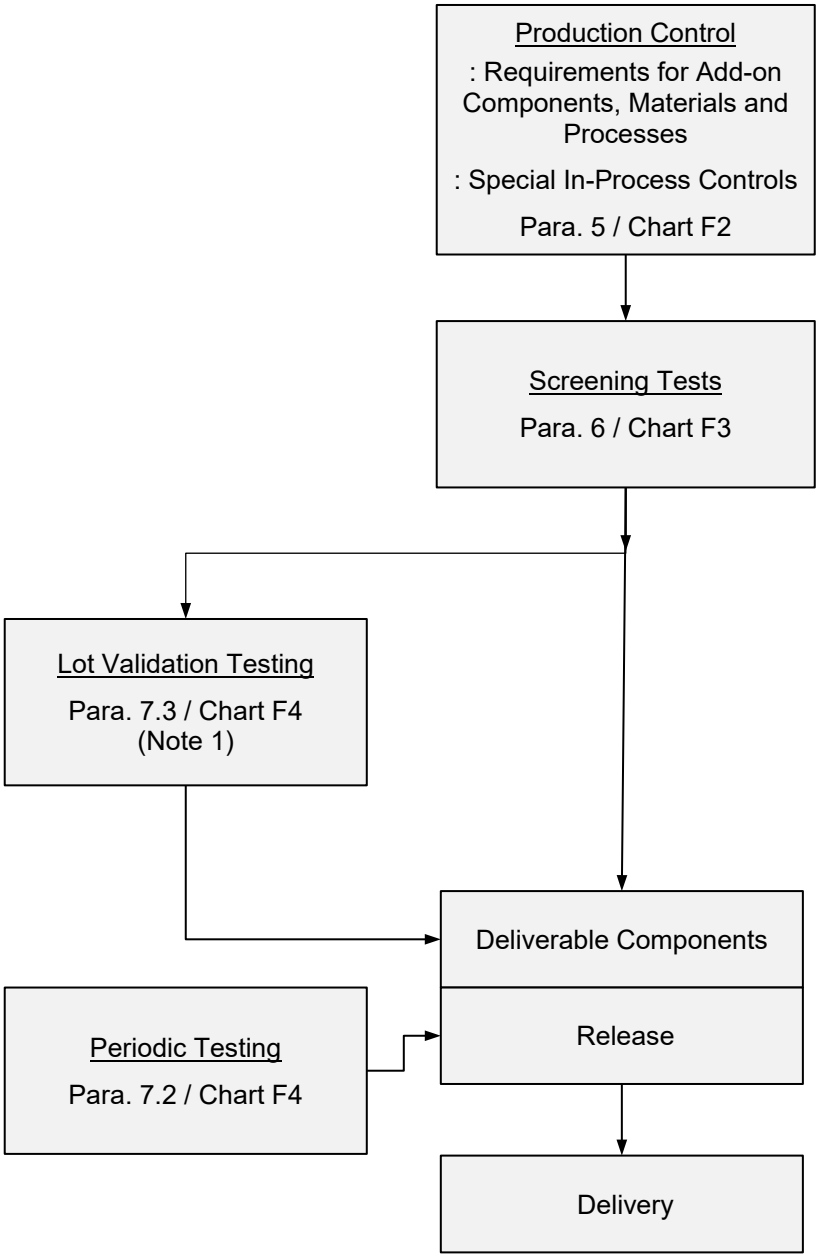
In addition, the Manufacturer shall define adequate provisions for packaging, transportation and storage of the memory modules, with special consideration to their non-hermetic nature. These provisions shall be as referenced in the PID. The Manufacturer shall provide the Orderer with this information prior to delivery.

12 CHARTS

12.1 CHART F0 (INFORMATIVE) - INITIAL (PRODUCT) QUALIFICATION



12.2 CHART F1 - GENERAL FLOW FOR PROCUREMENT



NOTES:

1. Lot Validation Testing is not required unless specifically stipulated in the Purchase Order.

12.3 CHART F2 - PRODUCTION CONTROL

MEMORY MODULE LOT MANUFACTURING (including Para. 4.6 Design Assurance)	
REQUIREMENTS FOR ADD-ON COMPONENTS, MATERIALS AND PROCESSES (see Para. 5.2)	
Para. 5.2.1	Element Evaluation: Validation of Active Memory Add-on Components (including: evaluation; procurement; screening, lot acceptance) (1)
Para. 5.2.1.1	Total Dose Radiation Testing of Active Memory Add-on Components (1) (2)
Para. 5.2.2	Element Evaluation: Validation of Materials and Processes (including substrate, electrical connections, encapsulation resin) (1)
SPECIAL IN-PROCESS CONTROLS	
Para. 5.3.1	Pre-Assembly Visual Inspection
-	Assembly & Encapsulation (in accordance with the PID)
Para. 5.3.2	Dimension Check (1)
Para. 5.3.3	Weight (3)
TO CHART F3 – SCREENING TESTS	

NOTES:
1. Performed on a sample basis.
2. For procurement, only required if stipulated in the Purchase Order.
3. Guaranteed but not tested.

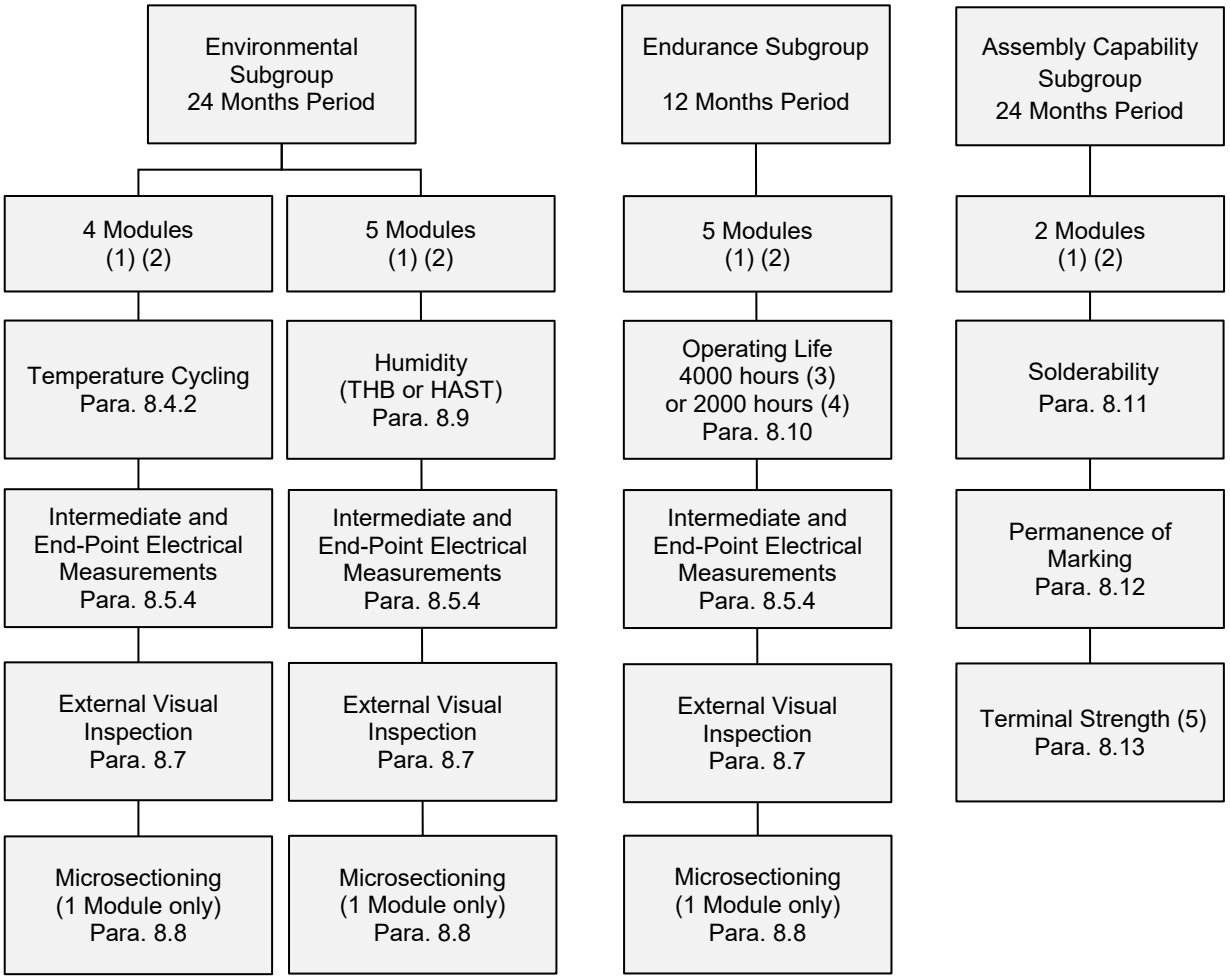
12.4 CHART F3 – SCREENING TESTS

MEMORY MODULES FROM PRODUCTION CONTROL	
Para. 6.1	Serialisation
Para. 8.4.1	Temperature Cycling
Para. 8.5.1	Parameter Drift Values (Initial Measurements)
Para. 8.6	Power Burn-in
Para. 8.5.1	Parameter Drift Values (Final Measurements) (1)
Para. 8.5.2	High and Low Temperatures Electrical Measurements (1)
Para. 8.5.2	Room Temperature Electrical Measurements (1) (2)
Para. 6.4	Check for Lot Failure (3)
Para. 8.7	External Visual Inspection
TO CHART F4 WHEN APPLICABLE	

NOTES:

1. The lot failure criteria of Para. 6.4 apply to this test.
2. Measurements of Parameter Drift Values need not be repeated in Room Temperature Electrical Measurements.
3. Check for Lot Failure shall take into account all electrical parameter failures that may occur during Screening Tests in accordance with Paras. 8.5.1, 8.5.2 and 8.5.3 subsequent to Power Burn-in.

12.5 CHART F4 – QUALIFICATION, PERIODIC TESTING AND LOT VALIDATION TESTING



NOTES:

1. Only applicable to qualification and qualification maintenance for a single-phase qualification of a single type of memory module. For qualification and qualification maintenance of a family of such memory modules or modules with different packages, the sample sizes shall be agreed with the ESCC Executive prior to the commencement of Qualification Testing. For Lot Validation Testing sample sizes, see Para. 7.3.
2. No failures are permitted.
3. Applicable to Qualification Testing, and to Periodic Testing for renewal of qualification after lapse.
4. Applicable to Periodic Testing for extension of qualification.
5. Terminal Strength may be performed at any point during the Assembly Capability Subgroup, depending on package configuration.