5.2.3 ST Microelectronics, France: ASIC platform C65Space

5.2.3.1 Contact Information

Address	ESCC Chief Inspector
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5.2.3.2 Qualification

Current Qualification Certificate No.	In QML since:	Type Designation
381	Aug 2022	Integrated Circuits, Silicon, Monolithic, CMOS Radiation Hardened 65nm ASIC Platform, based on type C65Space

Applicable documents:

ESCC Generic Specification No. 9000; ESCC Detail Specification No. 9202/086

STMicroelectronics Process Identification Documents:

- 8097046: GENERIC PID Ref. ST.01.2008

- DM00508779: PID FOR ASICs C65S WB and FC

- DM00508782: PID ASICs C65Space WB and FC Die Layout

5.2.3.3 List of Qualified Components

Detail Specification	Generic part number	Circuit function
9304/010	NX1H35AS-CQ352	3M System gate field programmable gate array
9304/010	NX1H35AS-LGA625	3M System gate field programmable gate array

5.2.3.4 Technology Flow Abstract

GENERAL FEATURES

The CMOS 65nm SPACE is a silicon technology node, 8 metal layers. It provides a logic capacity with additional DSPs, a 400 Mbs SpaceWire physical interface and also a DDR 2/3 physical interface. Benefiting from an advanced underlying technology, the NG-Medium provides high performances in terms of frequency and consumption. It is also reprogrammable without any limits.

- Power supply:
  - Core: 1.2V±10%.
  - IOS: 1.5V±10% or 1.8V±10% or 2.5V±10% or 3.3V±10%.
- Performance:
  - 250MHz Logic.
  - 333MHz DSP.
  - 800Mbps I/O.
- Temperature :
  - -55°C to +125°C.

BASIC INFORMATION

Main features

– 65 nm ST-SPACE process technology.
– 4-Input Look-up tables.
– Lut expender to support up to 16 bits boolean functions.
– High performance carry chains.
– Advanced interconnect network to support random logic and coarse grain block functions.
– DSP Blocks for complex arithmetic operations.
– User memories with variable width and depth.
– Configuration modes: JTAG, Parallel 8 bits, Parallel 16 bits, Serial dump bus, Space Wire
– Integrated Space Wire interface available for user applications.
– Dedicated lowskew distribution network for clock, reset and load enable signals.
– On-chip thermal monitoring capability.

Input/Output features

– Multiple I/O powering support from 1.5V to 3.3V
– Cold sparing support.
– Programmable output drive to support multiple industry standards.
– Embedded logic to support DDR2 and DDR3.
– 800 Mbps I/O support.
– LVDS compatible mode.
– All pins support 2000V of ESD-HBM.
– Embedded logic to support Space Wire Data Strobe encoding.
– Programmable delay lines on all pins.
– Programmable resistive termination.

COMPONENT TYPES

Part number	FPGA Matrix	Detail Specification	Package	Temperature range
920208601A35AS	NX1H35AS	9304/010	CQFP-352	-55°C to +125°C
920208601A35AS	NX1H35AS	9304/010	CLGA-625	-55°C to +125°C

5.2.3.5 Technology Flow Definition

The Technology Flow Definition domain covers the design, fabrication, assembly and testing of packaged products using ST C65Space silicon technology node and ST assembly line technology capabilities in CQFP352 and CLGA625 packages family.

1. Design

The following features are based on ST ESCC evaluated libraries from C65SPACE Design Environment:
- DSPs,
- DPRAMs & SPREGs memories,
- Input / Output in I/O Banks (except for the pas itself, which keeps original pad structure but receives Custom Design Add On featuring)
- Bitstream manager,
- PLLs (1201),
- Waveform generators,
- SapceWire Interface (including LVDS pads).

Other features designed by NanoXplore are full in compliant with ST C65Space design rules.

The NG-MEDIUM FPGA is based on NanoXplore patented interconnect architecture offering the highest logic density as well as high efficiency mapping. Application mapping is supported by NanoXplore tools based on proprietary algorithms tailored to the interconnect topology.

The device is composed of a central fabric embedding the programmable logic, RAM and DSP blocks, and peripheral I/O buffers. The fabric is covered with a grid of high level functional blocks interleaved with interconnect structures providing routing resources to realize the connections within the fabric and to the peripheral I/O buffers. The programmable logic resources are arranged in a hierarchical structure called a TILE with a specific local interconnect network. The I/O buffers are arranged into multiple banks. Each bank has its own I/O buffer supply voltage.

2. Fabrication

The wafer manufacturing is performed in ST Crolles 300mm fab using the new C65SPACE technology silicon node developed in ST Crolles 300mm and successfully qualified by ST in September 2014.

The main characteristics of the silicon die are described below:

Mask Levels: 41.
Masks Levels of Metallization: 8 (7 Layers in Cu + 1 Layer Ta/TaN/AlCu).

Die size: 15.3*10.96 mm².
Die Pad Pitch: 70µm min.
Die Pad Opening: 44*108 µm².
Die Pads Numbers: 374 non-staggered.
Die Finish Front Side (passivation): PSG + Nitride.
Die Finish Back Side: Raw Silicon.
An additional step of OPM (Over Pad Metallization) deposition is performed at a third party subcontractor ChipBond (TW), under ST quality control.
OPM : TiW/Au (Au= 3.5µm±1µm)
OPM Pad size : 54*165 µm²

3. Assembly

Process

The assembly process of the C65 Space devices is set-up in the historical ST Space certified plant in Rennes, France using the main following process capabilities:

Die Attach Medium: “Cyanate Ester” JM7000
Wire Bonding technology: Ultrasonic Gold Ball-Bonding.
Wire: 0.8 mils (20µm) Gold 4N
Bonding Decks & Bonding wire number:

	CQFP352	CLGA625
Bonding decks N#	2	2
Bonding wires N#	448	630
Bond Wires on Deck #1	223	323
Bond Wires on Deck #2	225	307

Package 1

Ceramic Quad Flat Package with 352 leads (CQFP352) with Ceramic Tie Bar
Dimensions: 75*75*3.51 mm3.
Cavity Size: 17*12.66 mm²
Cavity Volume: 320 mm3.
Lid Material: Kovar with Plating Layers (Ni/Au)
Lid Size: 23.62*19.30 mm²
Lead finishing: Au Plated

Package 2

Ceramic Land Grid Array with 625 leads (CLGA625)
Dimensions: 29*29*4.02 mm3.
Cavity Size: 17.00*12.66 mm²
Lead sealing: Eutectic brazing with Au/Sn alloy preform
Cavity Volume: 252.9 mm3.
Lid Material: Kovar with Plating Layers (Ni/Au)
Lid Size: 20.47*20.47 mm²
Lead finishing: Au Plated

4. Control and Test

The control & test of C65 Space devices are performed in both ST Grenoble plant, France for electrical testing and accelerated ageing (reliability screening) and Rennes, France for all other space related tests or at subcontracted third parties under Rennes Quality monitoring and control.

All these space related manufacturing operations are performed under the supervision and control of the ST ESCC Chief Inspector, located in our basic space plant, Rennes.

5. TCVs and SEC

TCV program has been carried out to address intrinsic failure mechanisms of the C65Space technology. NG-Medium encapsulated in CQFP352 and CLGA625 are used as SECs to conduct all the requested evaluation and qualification tests.

6. Radiation Characteristics

The ST C65SPACE technology has been developed to fulfil the following characteristics:

- SEL immune up to LET > 60MeV.cm2/mg.
- TID tolerance = 300 krad(Si).

5.2.3.6 Manufacturing sites

DESIGN:
NanoXplore
1 avenue de la Cristallerie, 92310 Sèvres, France

WAFER FABRICATION:
ST Crolles 300 - 850 rue Jean Monnet 38926 Crolles, France

ASSEMBLY:
ST Rennes – 3 rue de Suisse 35200 Rennes, France. Basic Plant

CONTROL AND TEST:
ST Grenoble - 12 rue Jules Horowitz, B.P. 217 38019 Grenoble, France
ST Rennes – 3 rue de Suisse 35200 Rennes, France. Basic Plant