SiCRET

Silicon Carbide Reliability Evaluation for Transport

An end user driven project

Contribution to study of dynamic effect on SiC MOSFETs

Presentation for ESCCON 2023 – Olivier Perrotin

March 8th, 2023

Agenda.

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- **SiCRET Project – presentation & Objective**
- **GSS Investigation – Screening DoE**
- **GSS Investigation – Results**
- **GSS Investigation – Conclusion + Next Steps**

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SiCRET Project

Presentation and Objective

SiCRET *An end user driven project*

Silicon Carbide (MOSFET) Reliability Evaluation for Transport

~ 5.3 M€ (ANR*)

*ANR: French National Research Agency

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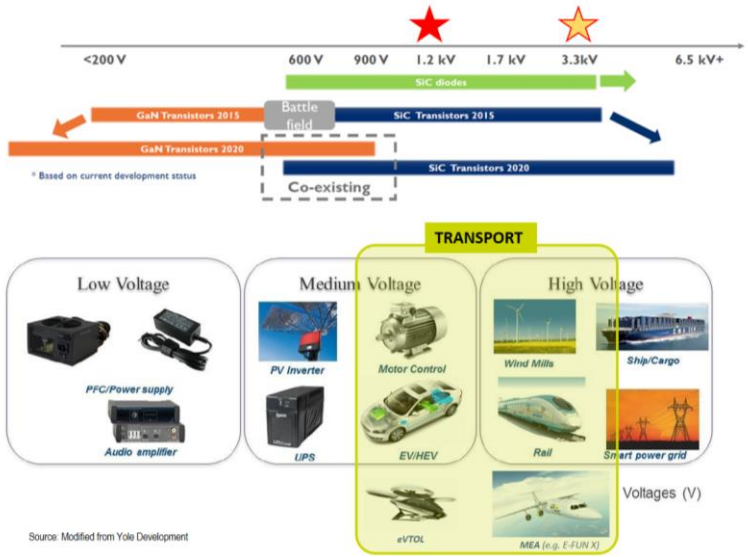
36 months (May 2020 to Apr 2023)

End-user oriented project focused on

- **Test for SiC :** Definition of test procedures and methodologies adapted to user mission profiles (**dedicated SiC technology qualification**)
- **Design for SiC :** Establishment of mitigation solution (with respect to end-user MP) such as design recommendation (e.g.Derating rules for safety margins, etc.)

Context



- Future electrification technologies require drastic improvements of power electronics. SiC MOSFET are key enablers.
- Reliability/ lifetime are mandatory for SiC adoption
- Convergence of applications / high reliability requirements
- Strong investment of industry is necessary to adapt qualification approach and design rules

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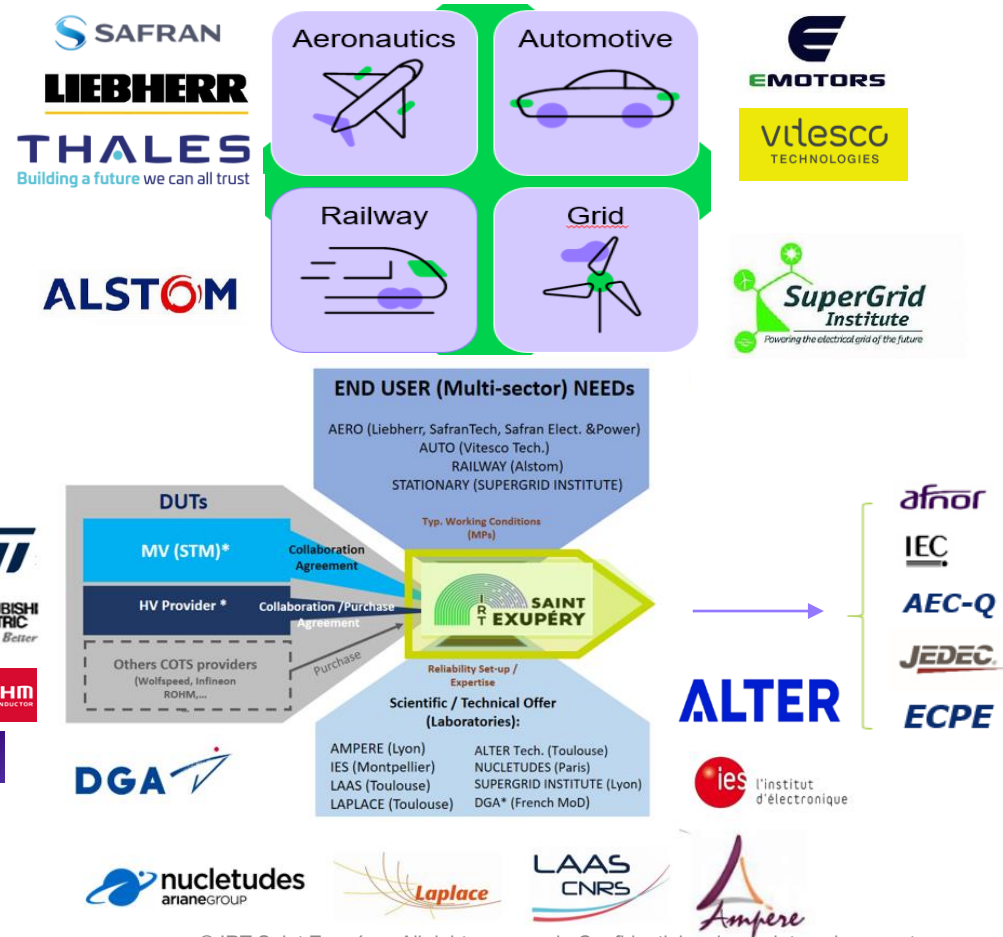
Project members and partners



Reliability Test Plan: Synopsis

Optimization Methodological Approach (costs-effectiveness)

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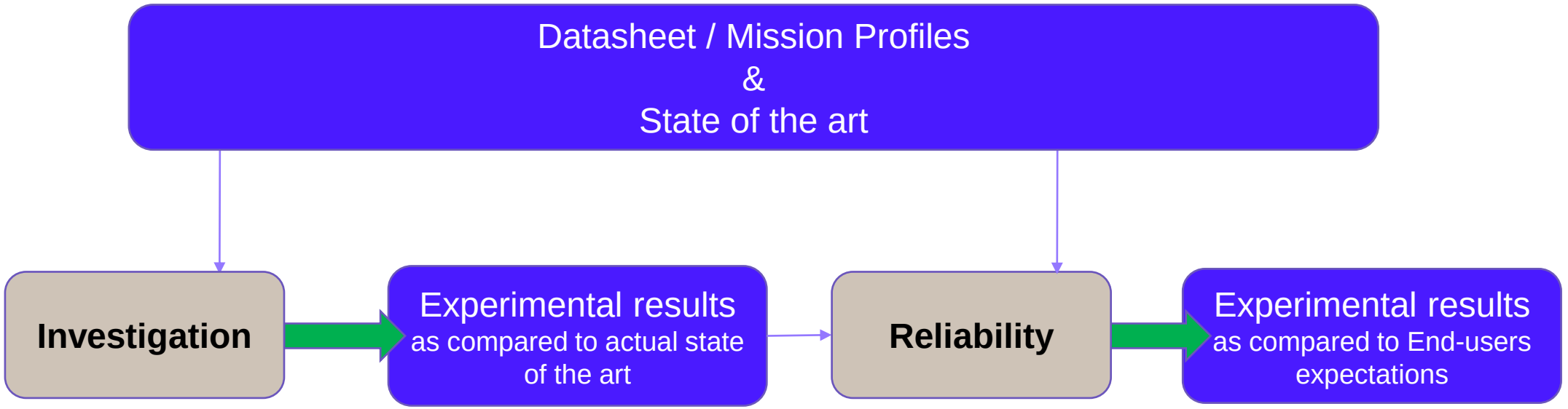

#Nr DUT*: small (No statistics)
Short test Time (Higher intensity level of stressors)

Objectives

- Identify key stressors
- Identify failure mechanisms
- Define failure indicators and criteria
- Define conditions of reliability test phase
- Define test procedure of reliability phase

#Nr DUT*: large (statistics)
Long enough test Time to detect failure – Degradation monitoring

Objective

- Build lifetime models

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**DUT: Device Under Test*

Medium Voltage Reliability Test Plan

Optimization Methodological Approach (costs-effectiveness)

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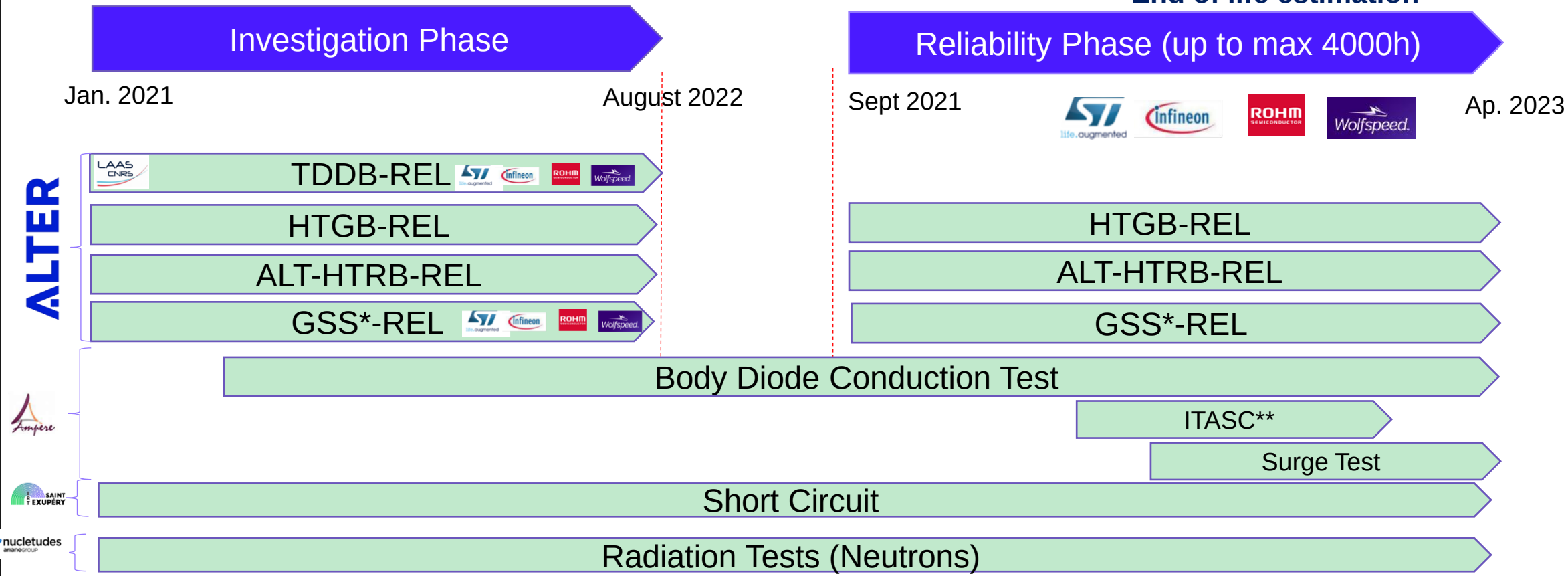
Investigation phase: Main Stressor definition

Reliability phase: Aging models
End of life estimation



* Gate Switching Stress (See JEP195)
**Inverter Test with Accelerate Switching Condition

« REL » → above usual qualification time, up to EoL or degradation to derive ageing law

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GSS Investigation

A single Screening DoE

GSS test conditions – Screening DOE

Same DoE for each Manufacturer

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Device Selection:

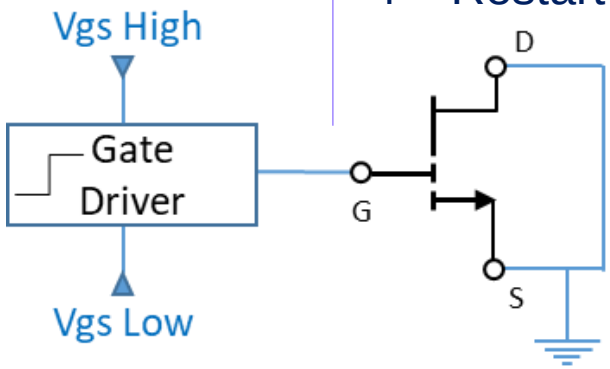
- Trench and Planar technologies
  - DUT A: Trench
  - DUT B: Planar
  - DUT C: Trench
  - DUT D: Planar
- Last SiC Mosfet generation available in 2020/2022
- TO-247-3L package
- Automotive Grade version
- Range caliber: 1200V, ~30 A, ~75 mΩ

Investigation Test duration: 85h (1.53E+11 cycles@500 KHz)

Remote interim Readouts: 4h, 23h, 45h, 65h

Process Control:

1 – **Power ON**:
   a: Start Power and signals
   b: Increase temperature (individual heaters)
2 – **Power OFF**:
   a: Decrease temperature
   b: Power Off after 15 minutes (T°<55°C)
3 – Perform electrical measurements after 1 h
4 – Restart Power ON before 4 h.



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GSS ALTER test bench

Programmable GSS test bench

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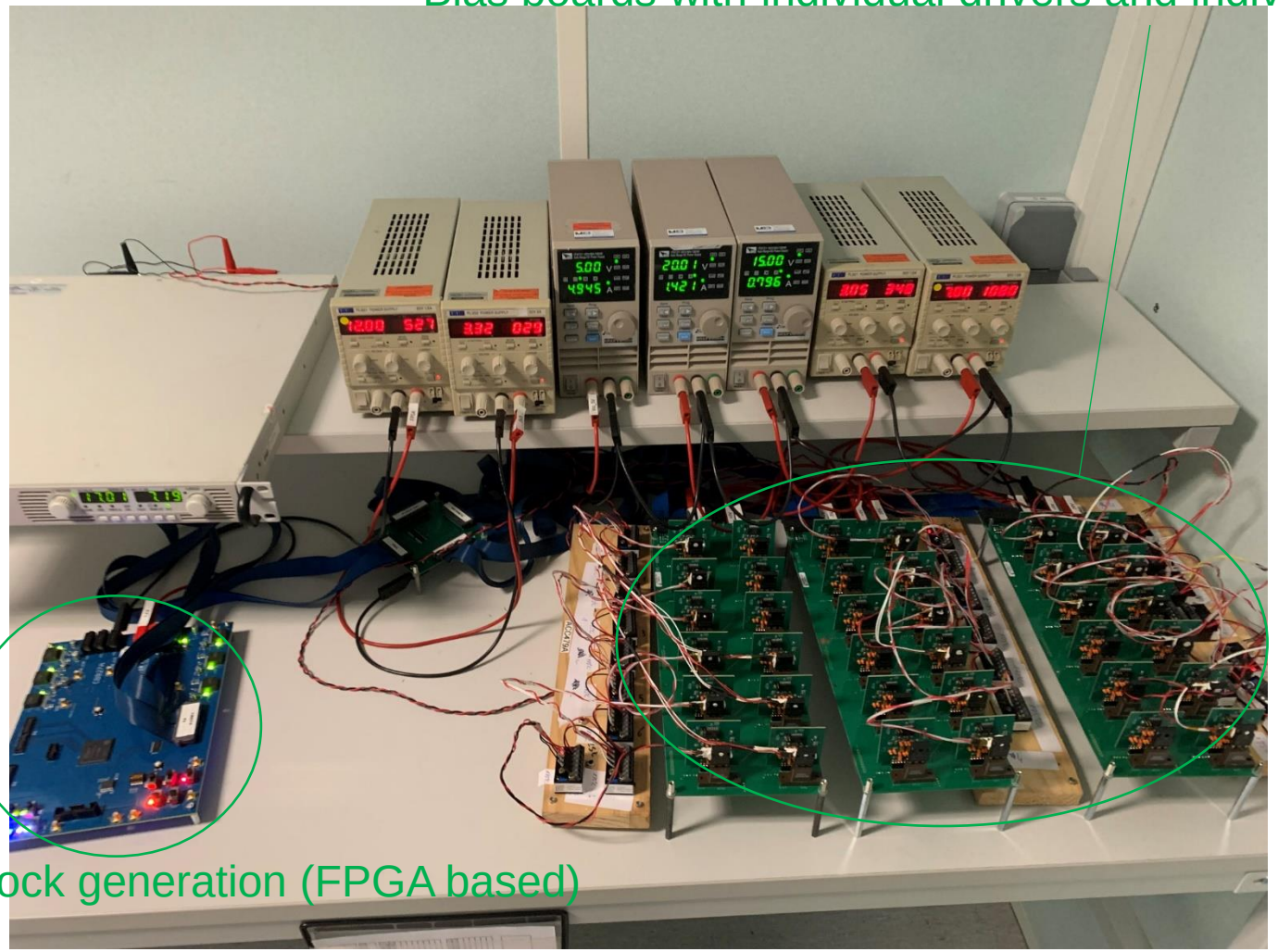
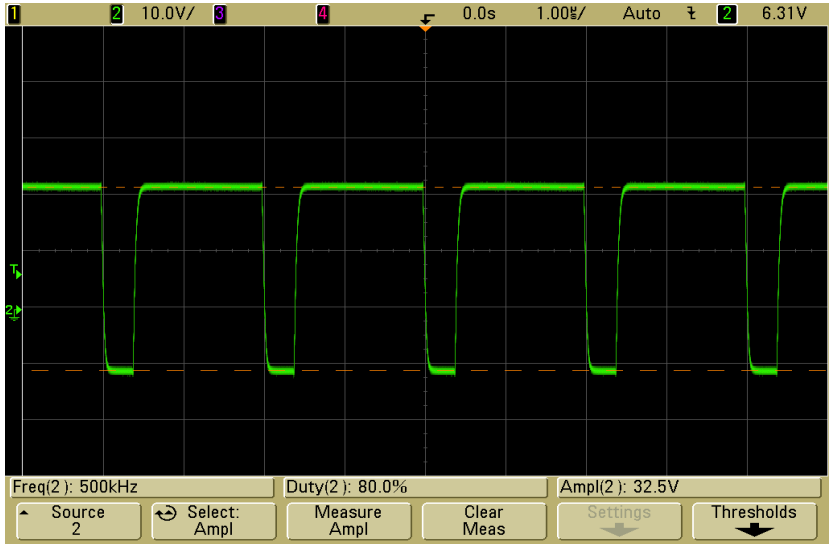
Bias boards with individual drivers and individual heaters



Clock generation (FPGA based)

Example Signal on 1 position
(-10V/+22V ; 500kHz ; 80%)



6x 12 positions.
Individual programable signals:
- Frequency from 1 KHz to 2 MHz
- Duty cycle from 20% to 80%
- OFF time selection

Temperature from Room to +200°C

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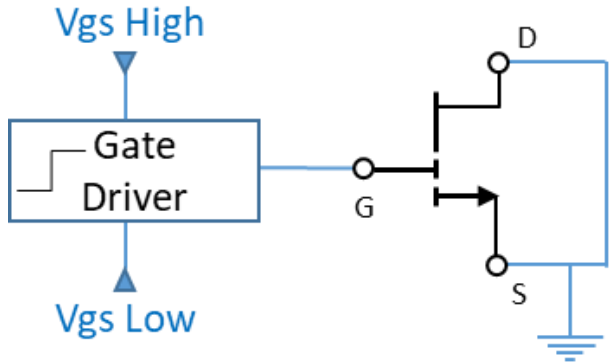
GSS test conditions - DOE

Same DoE for each Manufacturer

Glossary (from datasheet):

- Vgs,on: Recommended turn-on gate voltage
- Vgs,off: Recommended turn-off gate voltage
- VgMax: Max positive transient voltage
- VgMin: Min negative transient voltage
- VgsAv: Average value between VgsMin and Vgs,OFF



HTGS DoE	Gate voltage	Temperature	Frequency	Duty cycle	Qty
Condition 1	Vgs,off / Vgs,on	25°C	500 kHz	20%	3
Condition 2	VgsMin /Vgs,on	25°C	500 kHz	20%	3
Condition 3	VgsMin / VgsMax	25°C	500 kHz	20%	3
Condition 4	Vgs,off / Vgs,on	25°C	500 kHz	80% (*)	3
Condition 5	VgsMin / Vgs,on	25°C	500 kHz	80% (*)	3
Condition 6	Vgs,off / Vgs,on	125°C	500 kHz	20%	3
Condition 7	VgsMin / VgsMax	125°C	500 kHz	20%	3
Condition 8	Vgs,off / Vgs,on	175°C	500 kHz	20%	3
Condition 9	VgsMin / Vgs,on	175°C	500 kHz	20%	3
Condition 10	VgsMin / VgsMax	175°C	500 kHz	20%	3
Condition 11	Vgs,off / VgsMax	175°C	500 kHz	20%	3
Condition 12	VgsAv / Vgs,on	175°C	500 kHz	20%	3

Note (*): DC = 80% means 80% ON, 20% OFF

Vth Characterization

Preconditioning protocol definitions

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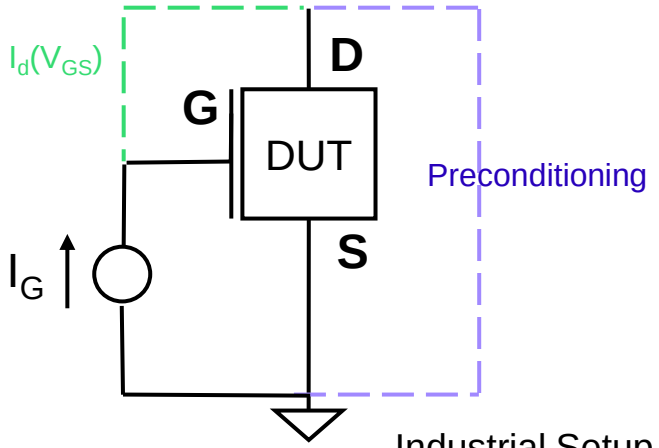
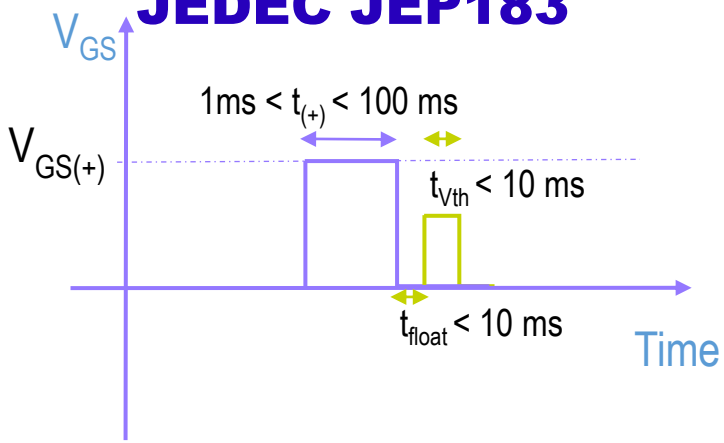
Main DC parameters used as indicator: $V_{GS(th)}$, $R_{DS(ON)}$, VHyst, BVDSS, Vsd, Idss, Igss, Cgs

V_{th} measurement @ Id = 1 mA



Unipolar

JEDEC JEP183



Bipolar

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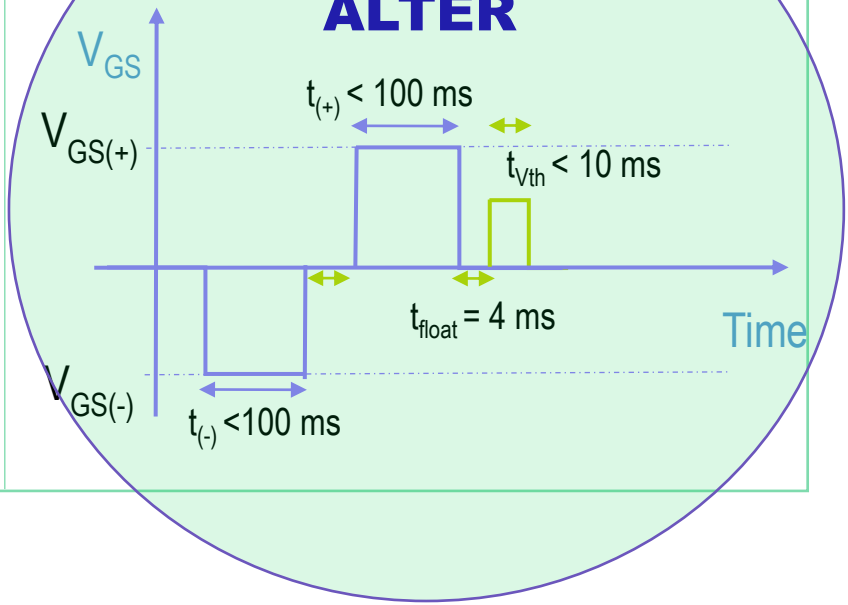

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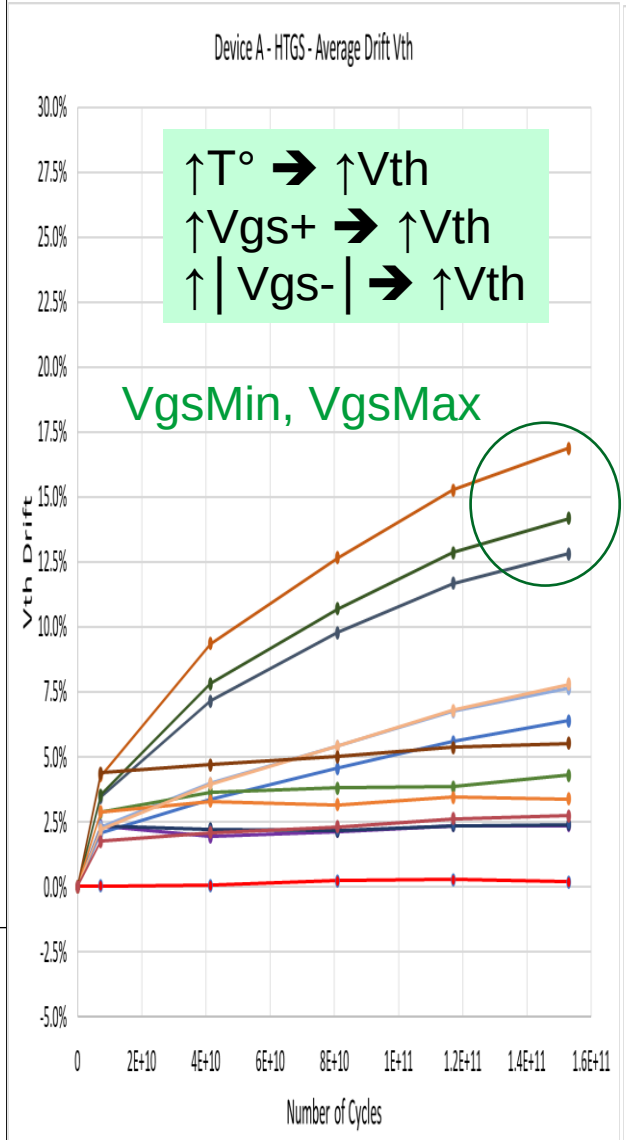
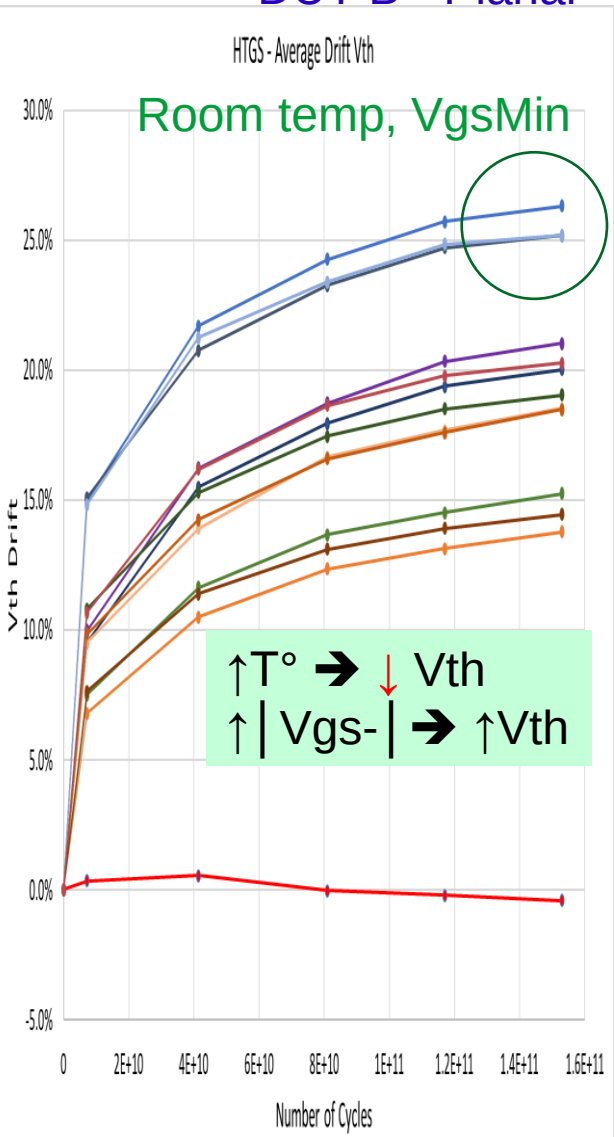
GSS Investigation Results

GSS : Vth (1mA) drift

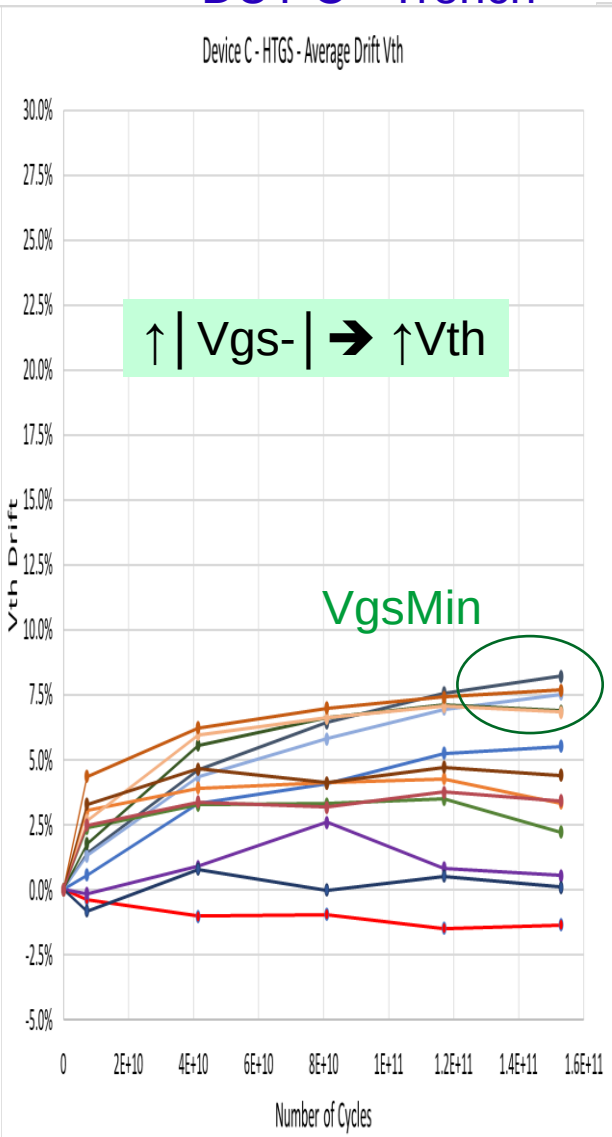
DUT A – Trench



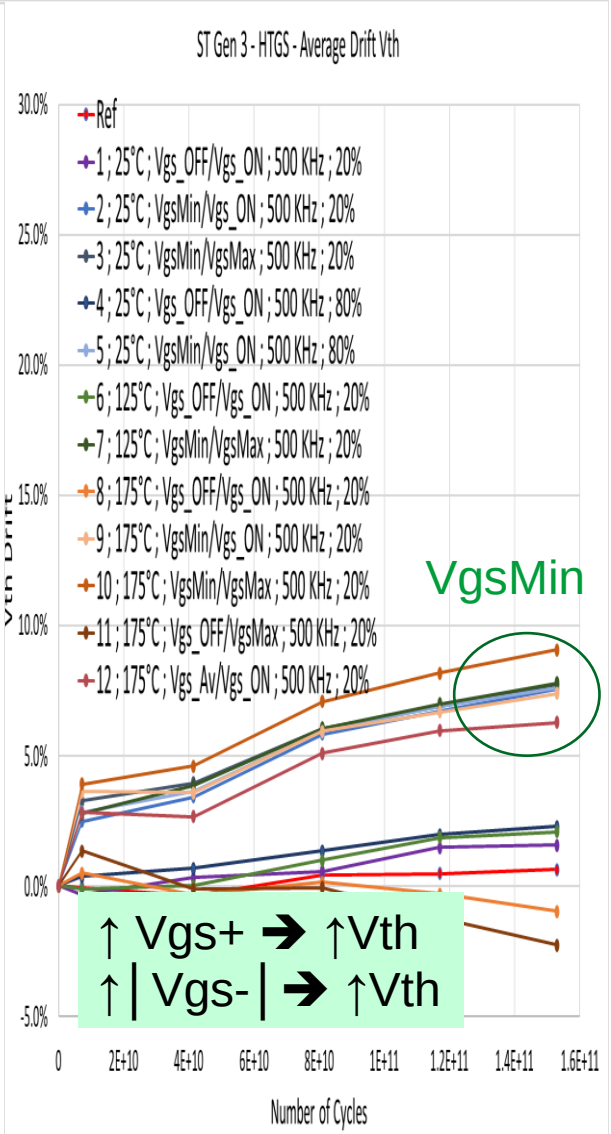
DUT B - Planar



DUT C - Trench



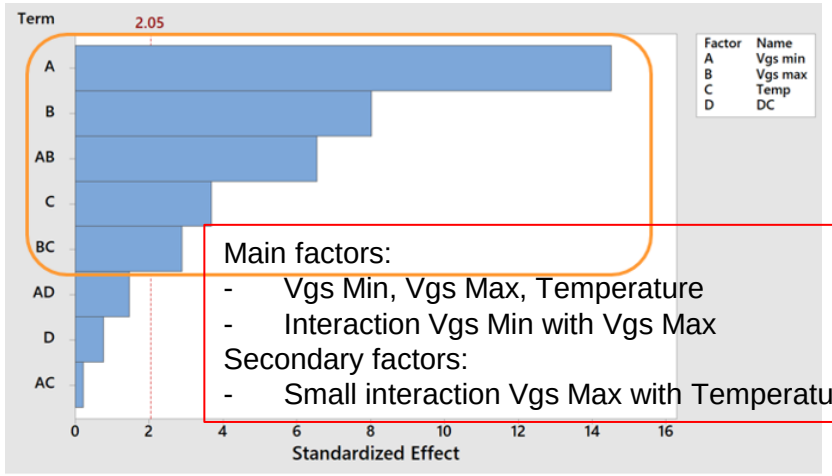
DUT D - Planar



Main stressors are technology dependent

GSS : VthSicret (1mA) drift

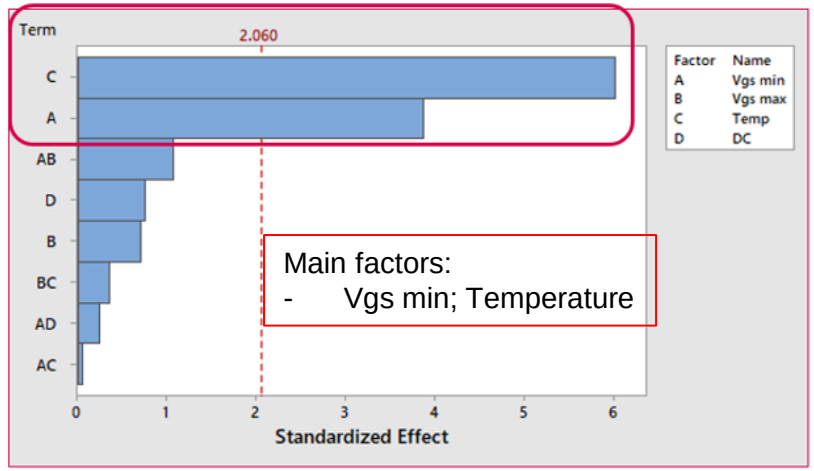
DUT A – Trench



Main factors:
- Vgs Min, Vgs Max, Temperature
- Interaction Vgs Min with Vgs Max

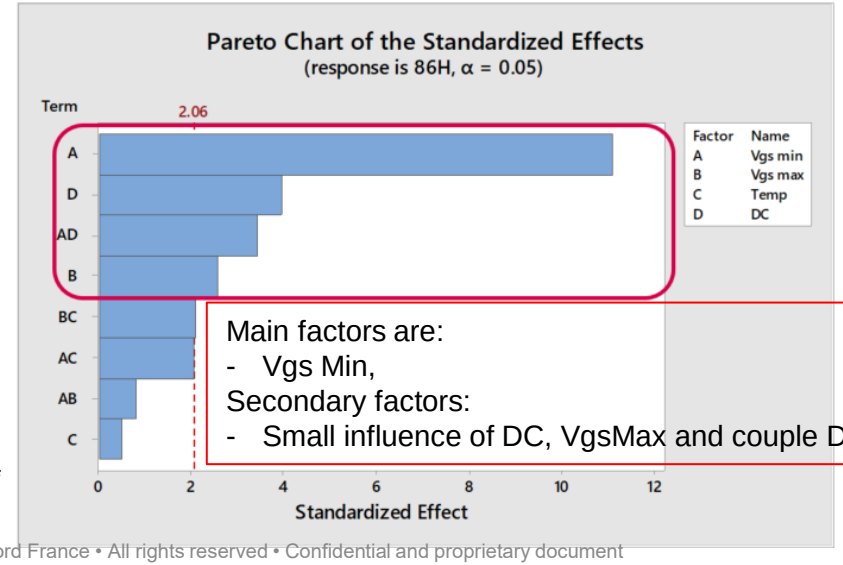
Secondary factors:
- Small interaction Vgs Max with Temperature

DUT B - Planar



Main factors:
- Vgs min; Temperature

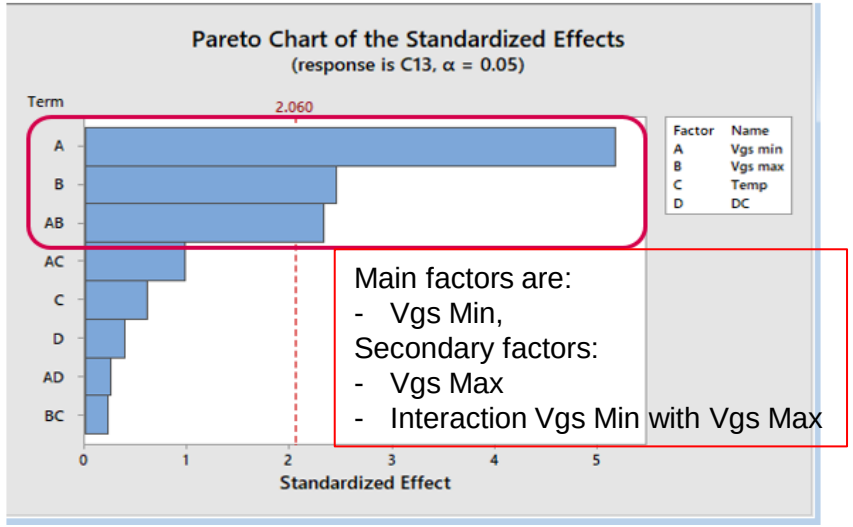
DUT C - Trench



Main factors are:
- Vgs Min,

Secondary factors:
- Small influence of DC, VgsMax and couple DC x VgsMin

DUT D - Planar



Main factors are:
- Vgs Min,

Secondary factors:
- Vgs Max
- Interaction Vgs Min with Vgs Max

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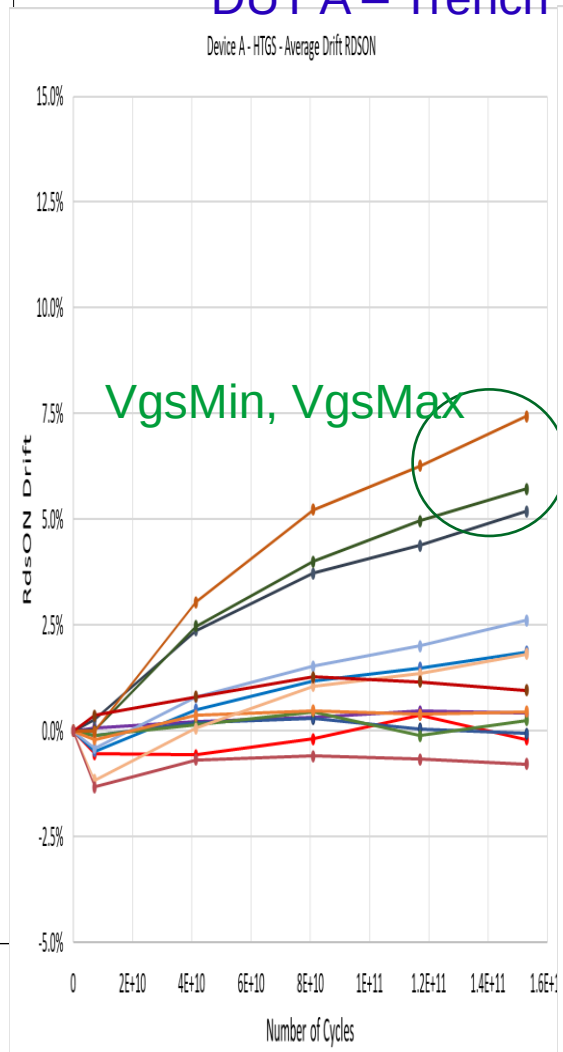
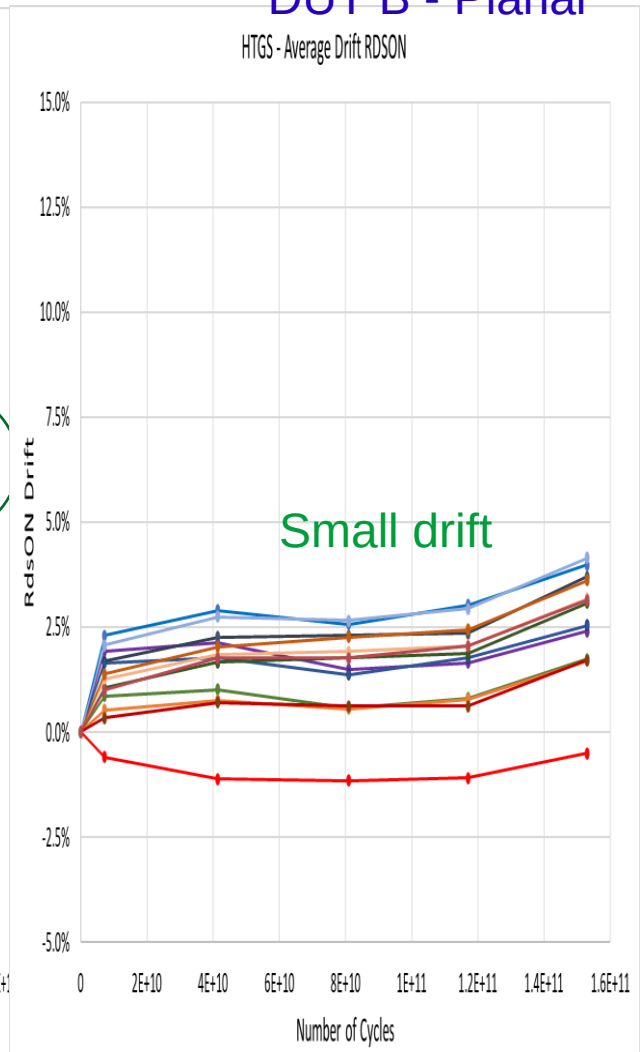
GSS : RDSON (20A) drift

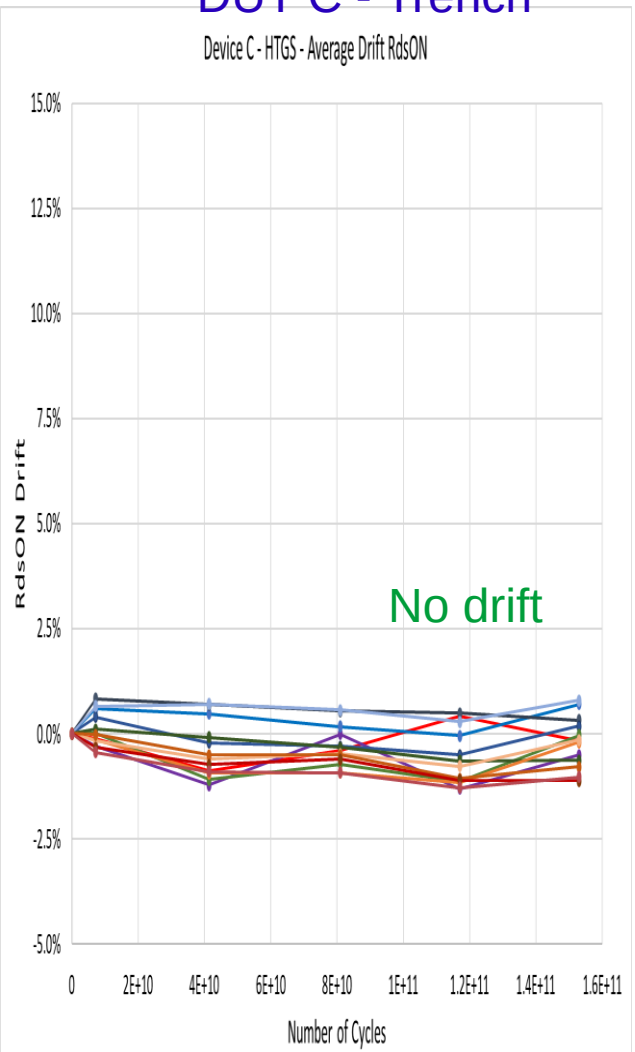
DUT A – Trench



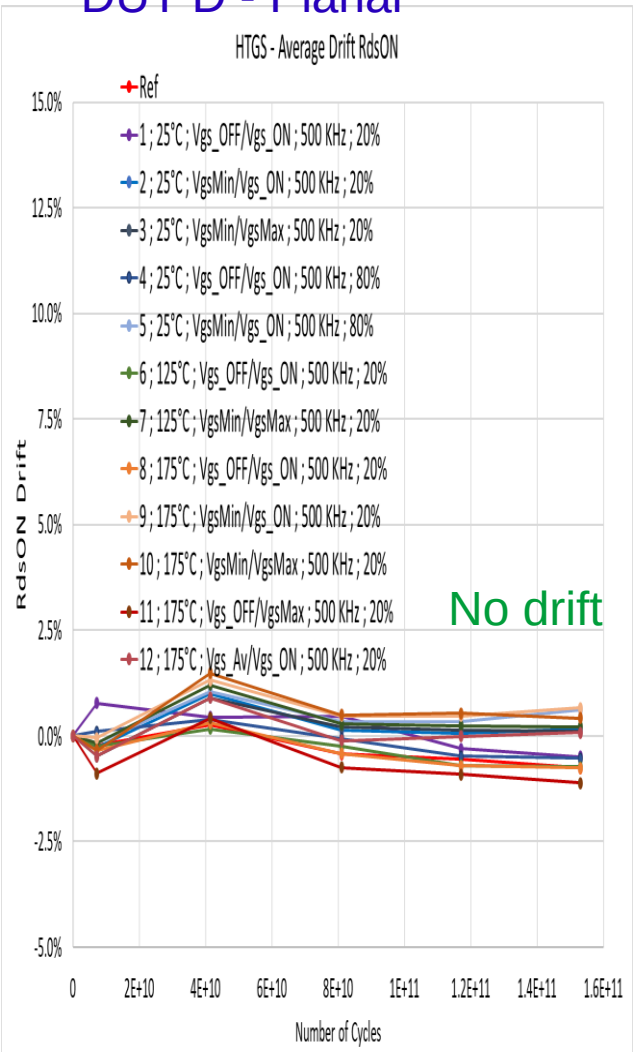
DUT B - Planar



DUT C - Trench



DUT D - Planar



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Relation between Rdson and Vth drift is not the same for each manufacturer

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Investigation Screening GSS Conclusion

&

Next steps

Conclusion

1 - Stressors impact is manufacturer / technology dependent

2 - Main stressors for Vth drift:
- Vgs Min value (common to all devices)
- Temperature
- Vgs Max Value
- Relation between Vgsmin and Vgsmax
- Relation between Vgs values and Temperature

Temperature influence cannot be neglected for some references.
In applications when the device switches, it is usually at a higher temperature than ambient temperature
Perform a standard test @Room temp or High temperature only is not suffisient to cover all Vth drift.

Excepted VgsMin, No common stressor observed between manufacturer / technology.

Next steps

Reliability **GSS** tests are On-Going up to 1E+13 number of cycles on DUT C and D (DUT A & B performed)

→ **Objective**: Build lifetime models

Reliability **HTGB** tests are On-Going up to 2000h on DUT C and D (DUT A & B performed)

→ **Objectives**:

- Build lifetime models
- Determine BTI (Bias Temperature Instability) effect on **GSS** test results

References

1 – IRT Whitepaper: "*Silicon Carbide Mosfet Gate Switching Instability – The quest of most relevant stressors*" will be publish soon.

2 – JEDEC Publications

→ JEP183: "*Guidelines for Measuring the Threshold Voltage (V_T) of SiC MOSFETs*"

→ JEP195: "*Guideline for Evaluating Gate Switching Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion*"

Thank you!

March 8th, 2023