

DELAMINATION IN PLASTIC PACKAGE - DIPP –

OSIP PROJECT 2022



ESCCON 2023 – 08/03/2023

D.DACLIN

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DIPP- INTRODUCTION

The future belongs to industrial components (such as Automotive-quality and commercial-quality components) that

- Are already used for launcher-type or short duration satellite missions.
- Revealed specific defects → delamination between the chip and the encapsulation resin.

Delamination is more likely to evolve during long term thermal cycling

- Increase of their length
- Reach out to the external sides of the packages → potential corrosion of bondings and dice.



Delamination has generally been accepted for short-term missions
(They "have not enough time" to worsen due to the short duration of the mission)

But, what's going on for long-term missions

where equipments are exposed to thermal stresses due to repeated thermal cycles and ON-OFF switching

?

SCOPE: STUDY'S OBJECTIVES

This study has been performed in the frame the **Open Space Innovation Platform campaign (OSIP)** organised by ESA.



Today, we do not have enough experience to estimate what is the level of degradation of industrial plastic packaged parts (COTS) at the end of long term space mission.

PURPOSES OF THIS STUDY

- /// To study how these **delaminations evolve** over time and the thermomechanical stresses imposed by the equipment/satellite qualification sequences and the space environment.
- /// To determine what are the most critical stresses for such type of plastic body components in the space environment.
- /// To establish a basis of criteria to be used to characterize these delaminations and their level of acceptance.

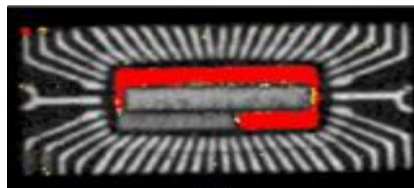
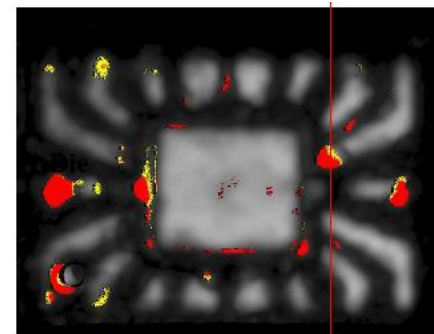


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Conclusion

OVERALL ASSESSMENT

WP progress and Status:

The project is divided in 5 work packages.

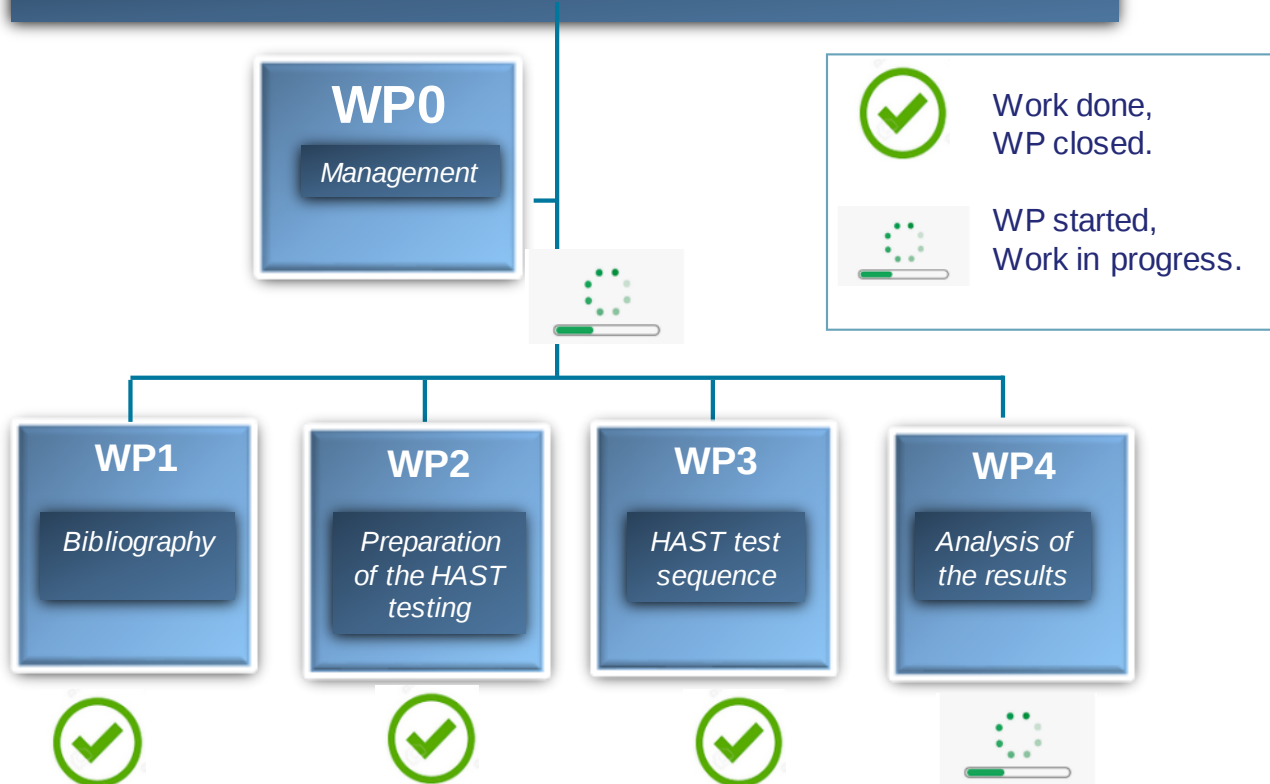


Duration: 12 months

T0 : september 2021

But 5 months delayed
(end scheduled end of
March 2023)

DELAMINATIONS IN PLASTIC PACKAGE



WP1: BIBLIOGRAPHY

Objectives

To compile technical and normative documentation (from IEEE, conference, etc...) about delaminations and voids in plastic packages components.

We are looking for information dedicated to :

- ✓ The description of types and localization of delaminations in the parts
- ✓ The most appropriate methods and tools for delaminations and voids detection , i.e the SAM (scan acoustic microscopy)
- ✓ Standards (ESA, MIL, ...), for tests methodology and defect descriptions.

Task

For each paper that will be selected for reading, we will put them in a list, with paper title, name of the paper origin, list of the authors and the organization they come from, with a quotation related to the interest of the paper in relation with the subject of the study , and a paper summary.

For the standards, small extract of the points interesting for the study will be put in a document, together with the pertinent tables or figures.

WP1: BIBLIOGRAPHY

WP1 conclusion

This bibliography is divided in two parts :

- Part 1 dedicated to a review of papers (mainly found in IEEE) related to plastic packages commonly reported defects; these papers are mainly focused:
 - ✓ on delamination
 - ✓ testing sequences developed to create these defects in order to study them
 - ✓ methods used to investigate these defects (such as Scanning Acoustic Microscopy).
- Part 2 is dedicated to a collection of methods and norms dealing with
 - ✓ the test selection,
 - ✓ the conditioning of plastic packages components for use in severe applications

This WP makes us learn that :

- ✓ the CSAM is the most relevant inspection method for delamination observation.
- ✓ the HAST sequence is the most appropriated way to age the plastic parts.

WP2: PREPARATION OF THE HAST TESTING

Objectives

In order to simulate the stresses imposed on the components throughout the space mission lifetime, we target to:

- ✓ select a large panel of different plastic packages that will be representatives of the packages already used or ready to be used in space missions
- ✓ submit them to the constraints of manufacturing operation (vapor phase assembly of packages on PCB)
- ✓ define a test plan in order to simulate the thermomechanical and electrical constraints applied on packages.

HAST sequence (Highly Accelerated Stress Test) or THB (Temperature Humidity Bias Test) are different methods that can match with the simulation of long duration space missions. We will study these methods, and use the most appropriate one.

Task

Selection and procurement of the COTS components:

- ✓ Packages of different sizes, for discrete, integrated circuits (simple and more complex) and power components and from different manufacturers.

Design/procurement of the test PCB : technology similar to the one used for internal assembly qualification of new SMT packages:

- ✓ The test vehicle will be a multilayer PCB with a technology and quality similar to the one used for internal assembly qualification of new SMT packages. The design/routing of the test vehicle and the test set up will be performed.

Definition of the test sequence (HAST / THB)

- ✓ Definition of a test plan in accordance with the norms and with space environment conditions.

WP2: PREPARATION OF THE HAST TESTING

Packages selection



Package
PLCC20



Package
DPAK-3



Package
TSSOP16



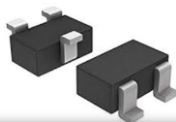
Package
TSSOP48



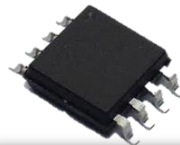
Package
MSOP10



Package
SOT23-5



Package
SOT323



Package
SOIC8



Package
SOT-223



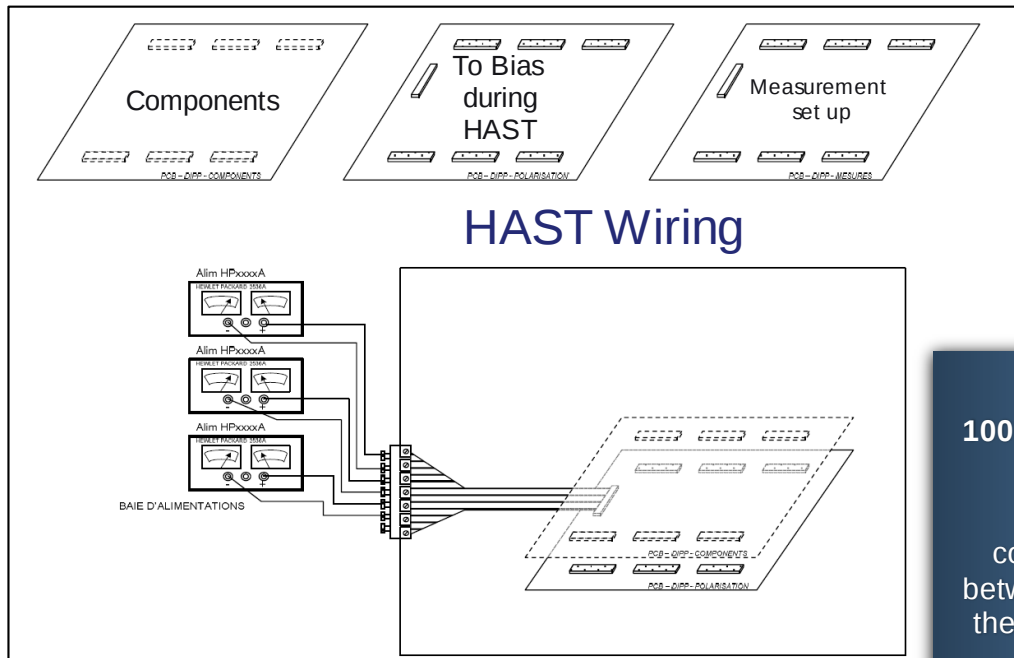
Package
PQFP-48

Selection of the type of packages that will be studied.

10 parts of each type will be used

WP2: DESIGN OF THE TEST PCB

TEST VEHICLE TESTING PHILISOPHY



Initially, we imagined the HAST set up composed of 3 boards:

- ✓ 1 board populated with the components (test vehicle)
- ✓ 1 board to bias the components during the HAST.
- ✓ 1 board needed to perform the measurement.

But this configuration required too many connections,

And the number of connections are limited by the HAST device/chamber (30 channels / lines in the I/V matrix)

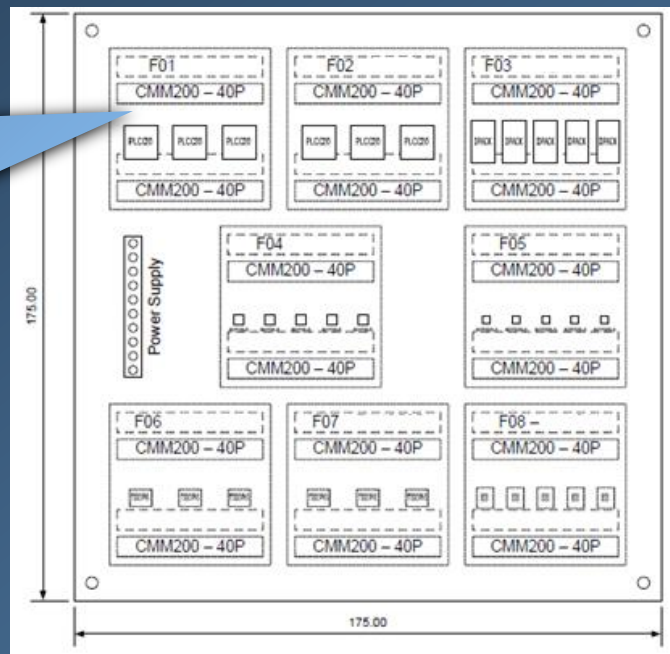
100% of the components will be biased.

Depending on the complexity of the part, between 60% and 100% of the parts will be electrical tested.

WP2: PREPARATION OF THE HAST TESTING

TEST VEHICLE DEFINITION

The test vehicle is composed of 1 “mother board” connected to “daughter boards” dedicated to each type of components, on both sides.



“Daughter boards” dedicated to each type of components.

- ✓ dimensions 48mmx48mm
- ✓ Boards with 2 connectors (40 channels each) on each side to be biased.
- ✓ PBA populated on both sides.

1 “mother board”

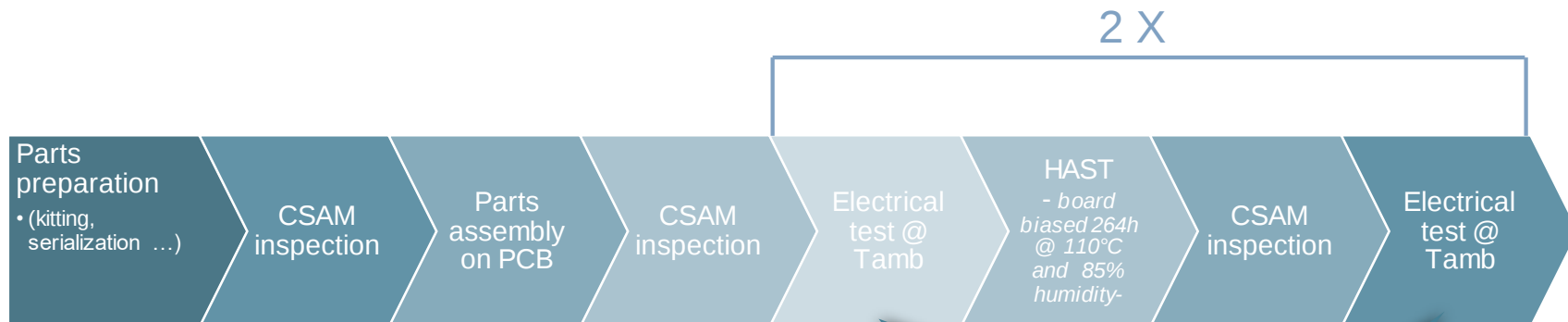
- ✓ Dimensions 175 mm x 175
- ✓ Populated with 16 “daughter board” (8 on each side)

100% of the components will be biased.

Depending on the complexity of the part, between 60% and 100% of the parts will be electrical tested.

WP2: PREPARATION OF THE HAST TESTING

TEST PLAN DEFINITION



Electrical test:

The aim is to detect leakage current variation, or bonding lifting/breaking due to delamination.

→ I/V plots : Measurement of voltage with regards to a step by step increasing of the current

WP3: HAST TEST SEQUENCE

Objectives

- ✓ To manufacture the test vehicle
- ✓ To run HAST or THB with parts biased ON, in order to be realistic.
- ✓ To perform non destructive inspections with the SAM in order to detect the initial presence and evolution of delaminations during the stress sequence.
- ✓ To measure the evolution of the (identified) defects along the test sequence, and make a classification of these defects :
 - localization of the delaminations and voids
 - size
 - Criticality
- ✓ To compare this situation with the initial one, and try to establish a list of criteria for acceptance/rejection.

Task

Test vehicle manufacturing

- ✓ The selected parts will be assembled on PCB using the methods and machines (vapor phase reflow) used for standard space PCB production

Operation and monitoring of the test sequence

- ✓ To implement the set up defined in WP2
- ✓ to run the test sequence (HAST or THB).

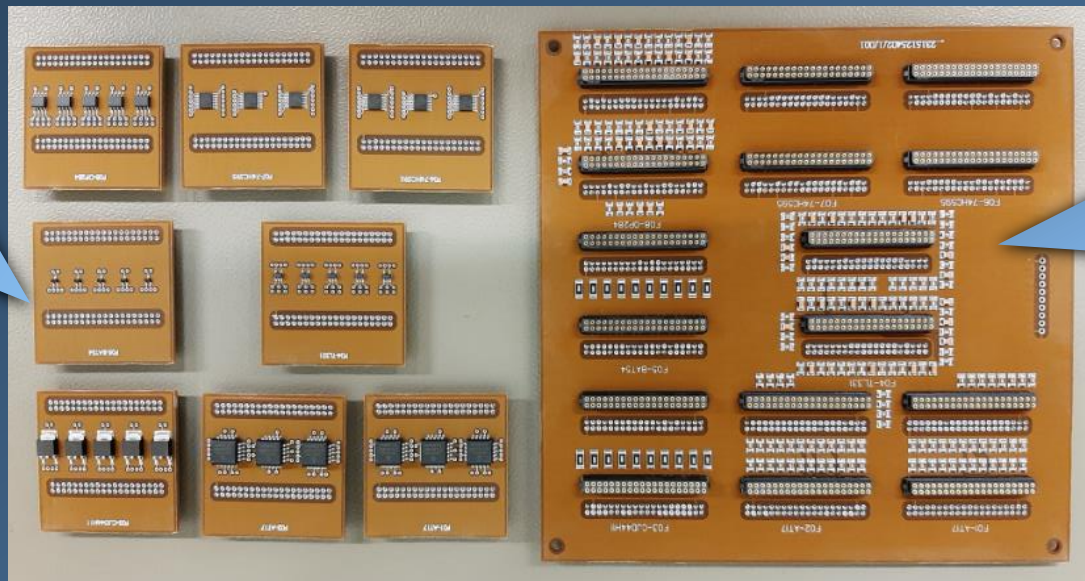
To perform SAM inspections

- ✓ SAM inspection of the parts before and after each step of the test sequence, in order to record the defects (size, location,...)

WP3: HAST TEST SEQUENCE

TEST VEHICLE MANUFACTURING

Manufacturing of the “mother board” connected to “daughter boards” dedicated to each type of components, on both sides.



“Daughter boards” dedicated to each type of components.

- ✓ dimensions 48mmx48mm
- ✓ Boards with 2 connectors (40 channels each) on each side to be biased.
- ✓ PBA populated on both sides.

1 “mother board”

- ✓ Dimensions 175 mm x 175
- ✓ Populated with 16 “daughter board” (8 on each side)

WP3: HAST TEST SEQUENCE

CSAM INSPECTION @ EACH STEP--- SUMMARY

1/2



A Trend of Delamination apparition or evolution
between T0 – HAST run1 or HAST run 1 – HAST run 2

- ➡ No new delam or no evolution → stable; poor impact of HAST
- ➡ New delam or evolution → low impact of HAST : delam, not critical
- ➡ New delam or evolution in critical location → high impact of HAST /delam, critical



		At T0			After assembly			After HAST1			After HAST2		
		Delamination observed on:											
		Header	Lead	Die	Header	Lead	Die	Header	Lead	Die	Header	Lead	Die
1	PLCC20	No	No	No	No	Yes on bonding area 100%	No	➡ No	➡ Yes on bonding area 100%	➡ No	➡ No	➡ Yes on bonding area 100%	➡ No
		Yes until 100%	Yes on bonding area until 80%	No	Yes until 100%	Yes on bonding area until 80%	Yes	➡ Yes until 100%	➡ Yes on bonding area until 80%	➡ Yes	➡ Yes until 100%	➡ Yes on bonding area until 80%	➡ Yes
2	DPAK-3	No	Yes on bonding area until 70%	No	No	Yes on bonding area until 70%	No	➡ No	➡ Yes on bonding area until 70%	➡ No	➡ No	➡ Yes on bonding area until 70%	➡ No
		No	No	No	No**	No**	**	➡ No**	➡ Yes until 50% **	➡ **	➡ No**	➡ Yes until 50% **	➡ **
4	SOT323	Yes until 100%	Yes until 20%	No	No**	No**	**	➡ No**	➡ No**	➡ **	➡ No**	➡ No**	➡ **
		No	No	No	No**	No**	**	➡ No**	➡ No**	➡ **	➡ No**	➡ No**	➡ **

** Die was in backside. So, the die assembly side could not be inspected on parts after assembly.

Date: 08/03/2023

Ref: DIPP-TASB-PPT-0021 ed.1

Template: 83230347-DOC-TAS-EN-010

PROPRIETARY INFORMATION

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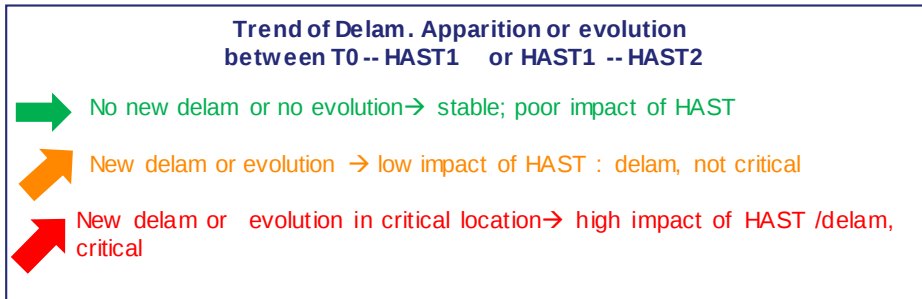
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WP3: HAST TEST SEQUENCE

CSAM INSPECTION @ EACH STEP--- SUMMARY

2/2



At T0			After assembly			After HAST1			After HAST2			
Delamination observed on:												
	Header	Lead	Die	Header	Lead	Die	Header	Lead	Die	Header	Lead	Die
TSSOP16	5	No	No	No	No	No	No	No	No	No	No	No
SOIC-8	6	No	No	No	Yes until 10%	No	Yes until 75%	No	No	Yes until 10%	No	No
TSSOP-48	7	Yes until 30%	No	No	Yes until 100%	Yes on bonding area until 20%	Yes until 80%	Yes on bonding area until 20%	No	Yes until 80%	Yes on bonding area until 20%	No
SOT-223	8	No	Yes on bonding area until 50%	No	No	Yes on bonding area until 50%	No	Yes until 20%	No	No	Yes until 20%	No
MSOP10	9	No	No	No	No	No	No	No	No	No	No	No
PQFP-48	10	No	Yes on bonding area 100%	No	No	Yes on bonding area 100%	No	Yes on bonding area 100%	No	No	Yes on bonding area 100%	No

** Die was in backside. So, the die assembly side could not be inspected on parts after assembly.

WP3: HAST TEST SEQUENCE

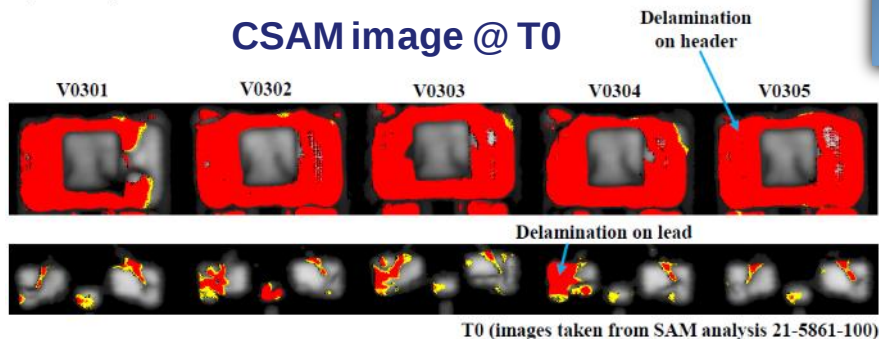
CSAM INSPECTION

LET'S FOCUS ON DPAK-3

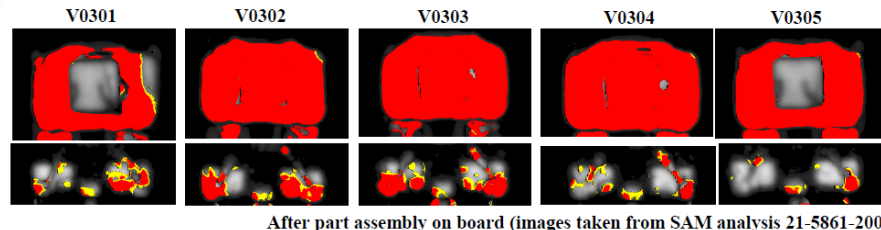


Top scanning - 15MHz

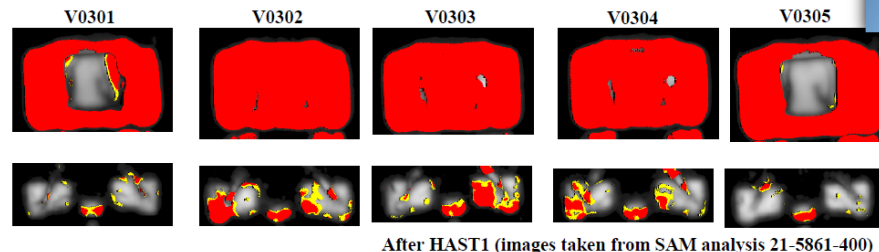
CSAM image @ T0



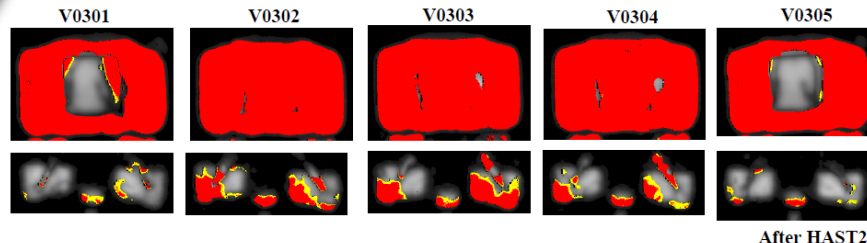
CSAM image after assembly



CSAM image after HAST -Run 1



CSAM image after HAST -Run 2



Delamination occurs till the beginning (T0) and increase after assembly.
HAST seems to have a low impact in the creation or evolution of delamination

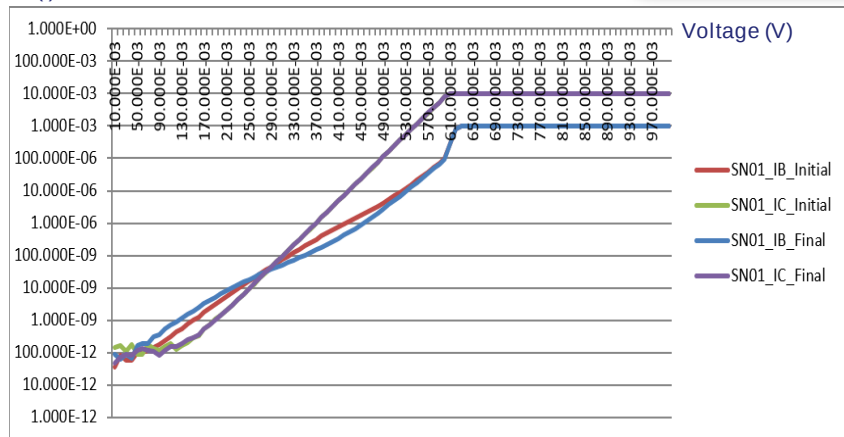
WP3: HAST TEST SEQUENCE

FOCUS ON CJD44H11 (Extract from xls file)

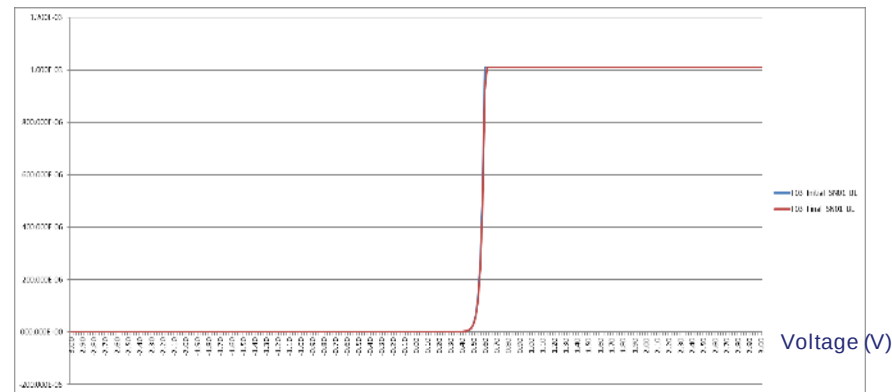
WP3: Electrical test @ each step

Example SN 01 after HAST Run #1.

Current (I)



Current (I)



The parameters are similar before and after HAST run #1. The curves are superimposed.

The junction characteristics is similar before and after HAST run #1. The curves are superimposed.

Even if the parts in DPAK-3 show dramatic delamination, we do not show nor failure nor variation in the electrical parameters measured after HAST Run #1.

WP3: HAST TEST SEQUENCE

WP3: Electrical test @ each step

Electrical Test

- ✓ A specific test plan has been defined for each component but the parameters are different.

Electrical Test has been performed before and after the HAST runs.

The parameters have been measured and compared between:

- ✓ T0 and HAST Run 1
- ✓ HAST Run1 and HAST Run 2

Measure

- ✓ The I/V plots have been created for each part, for each parameter.

Conclusion:

- ✓ No failure has been observed (no short circuit or open circuit) after the 2 runs of HAST,
- ✓ Even parts with dramatic delamination (such as the one in DPAK-3) do not show any electrical parameters variations.
- ✓ Data from electrical test of HAST Run #2 are still in analysis.

WP4: ANALYSIS OF THE RESULTS - FINAL REPORT

Objectives

- ✓ To perform a classification of the defects (types, severity, evolution)
- ✓ To make a proposition of criteria for the acceptance of delaminations at T0

Task

To perform a mapping of the defects wrt to type of packages

To analyze the evolution of the defects

- ✓ To make a description of the different type of defects found
- ✓ To make a correlation between the evolution of the defect size and the test sequence step
- ✓ To make an evaluation of the defect criticality



CONCLUSION

- Delamination occurs:
 - ✓ since the beginning (T0) or after assembly
 - ✓ not after HAST (1 run or 2 runs).
 - ✓ HAST seems to have a low impact in the creation or evolution of delamination.
- Electrical testing did not reveal major discrepancies or failure → no short circuit or open circuit have been detected.
- Data from HAST run #2 are in analysis.



**Thank you
for your attention !**

Any questions ?

For further information, you can contact Déborah DACLIN : deborah.daclin@thalesaleniaspace.com