ESCCON 2023
The European Space Components Conference
7 - 9 March 2023 | Toulouse | France

RADIATION TEST ON POWER GAN COMPONENT

Sauveplane Jean-baptiste

Power component engineer

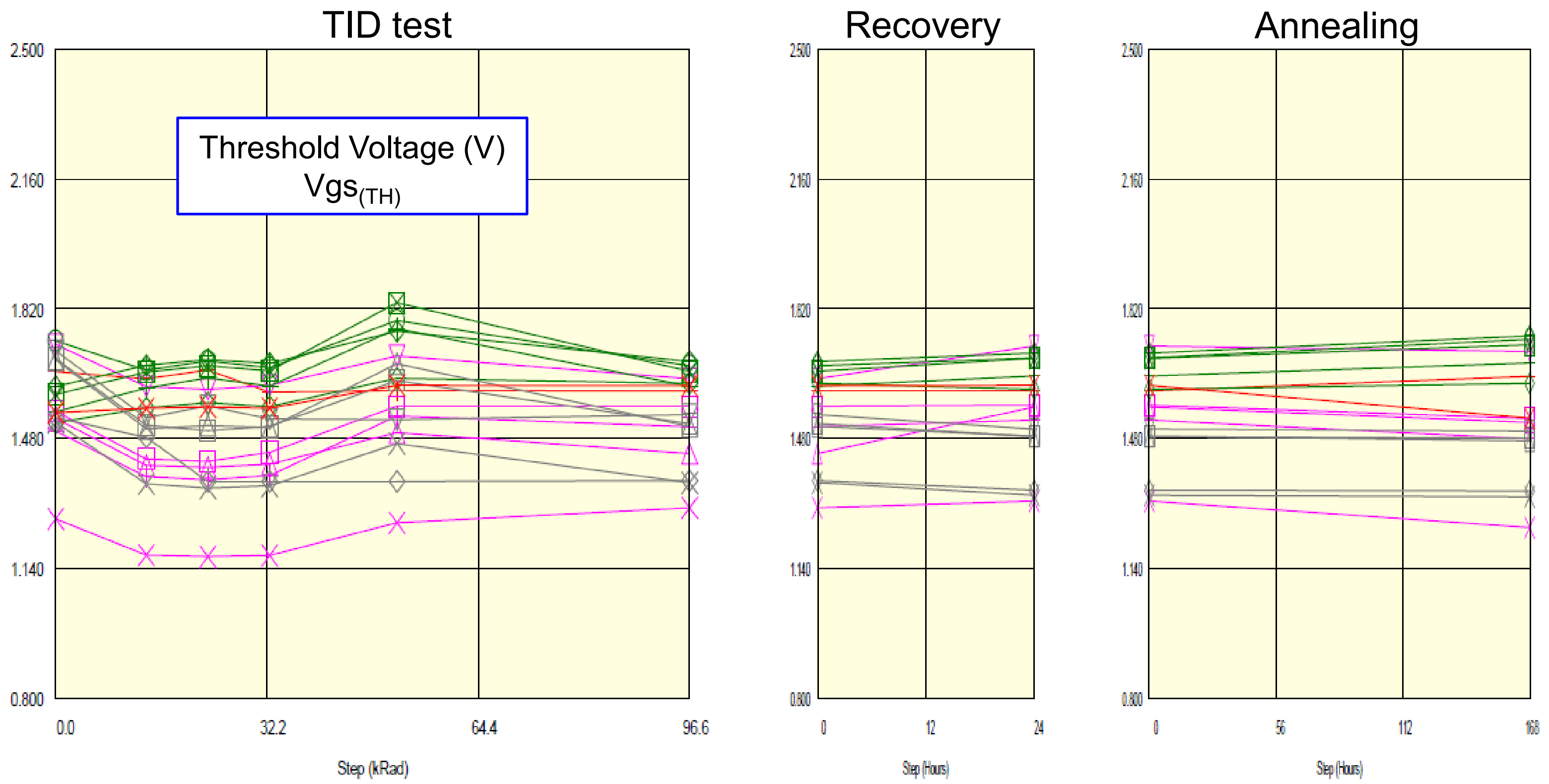
DTN/QE/CQ

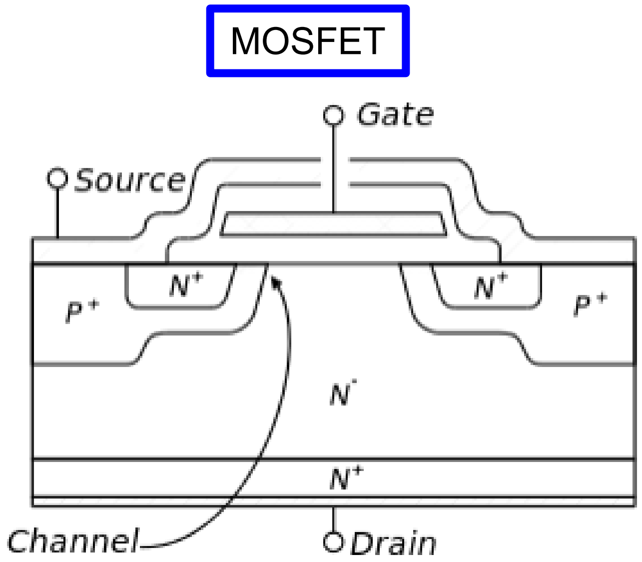
Outline :

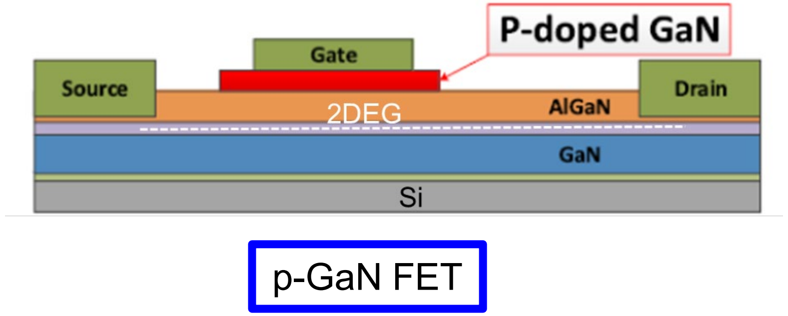
- GaN robustness against radiation
- Motivation of the study
- Component selection for SEE testing
- Component preparation for SEE test campaign
- Radiation test bench description
- SEE results
- Conclusion & Future works

GaN robustness against radiation :

- **p-GaN** power components are immune to TID
  - Fundamental property (even over efficiency)







- Single event effect (SEE, heavy ions) robustness is not so obvious

Motivation of the study :

- To investigate on commercial power GaNFET robustness against SEE
  - **Classical testing condition**

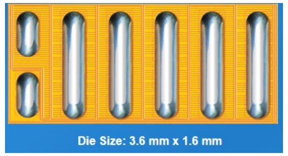
- To explore alternative SEE testing condition to find « worth case »
  - Heavy ion testing under switching condition
    - Effect of fast switching and temperature
  - Heavy ion beam highly tilted from normal incidence

Funding:

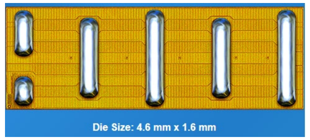
- Study was funded by CNES R&T 2020 Orbital System programme
- Beam time access was funded by the European Union's Horizon 2020 research and innovation programme under grant agreement N°101008126

Component selection for SEE testing :

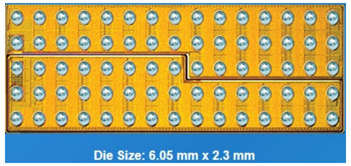
EPC2010C	EPC2215	EPC2104	EPC2102	GS66516T
Single	Single	Half-bridge	Half-bridge	Single
200 V – 22 A	200 V – 32 A	100 V – 30 A	60 V – 30 A	650 V – 60 A



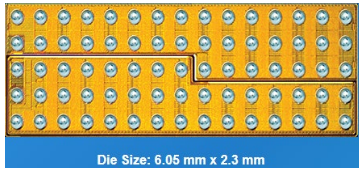
GEN 4
SRon=104mΩ.mm²



GEN 6
SRon=44mΩ.mm2



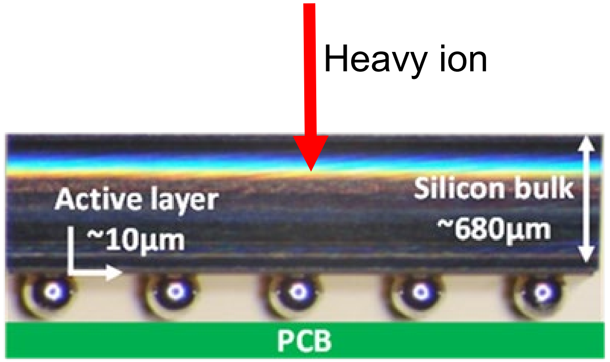
GEN 5
SRon=35mΩ.mm2



GEN 5
SRon=25mΩ.mm2

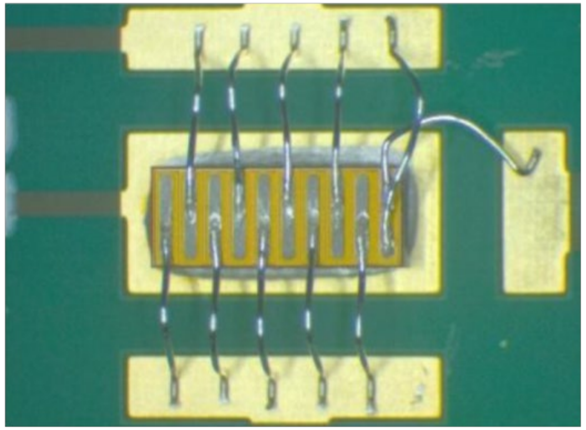
No information on Generation

- **Component preparation for SEE testing is difficult**
  - Beam energy is limited (heavy ion penetration in matter can be low)
  - Sensitive area is not directly reachable in normal mounting condition

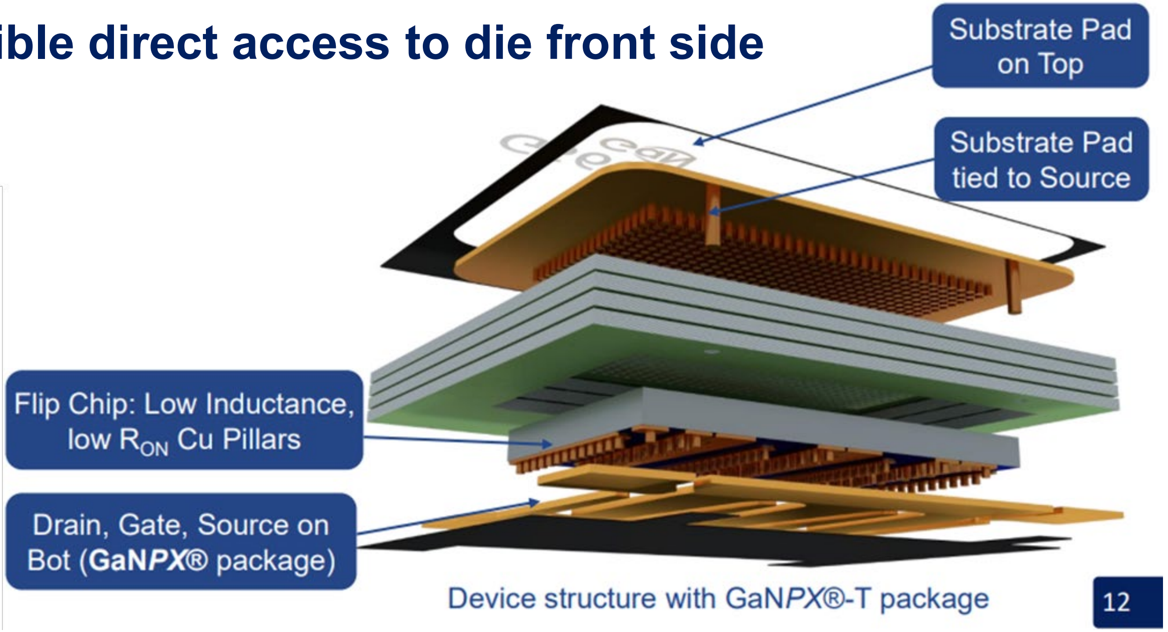


Component preparation for SEE test campaign :

1st method: Classical front side testing



- **Not compliant with EPC flip chip mounting or GanSytem package**
- **Possible to connect EPC die using wire bonding**
  - Advantage: Die easy to mount on board
  - Drawback: Bonding not easy and compliant with static testing only
- **GanSytem package solution make it almost impossible direct access to die front side**
  - Plastic opening induce a lost of electric connection
  - Thick copper plate hide die active area

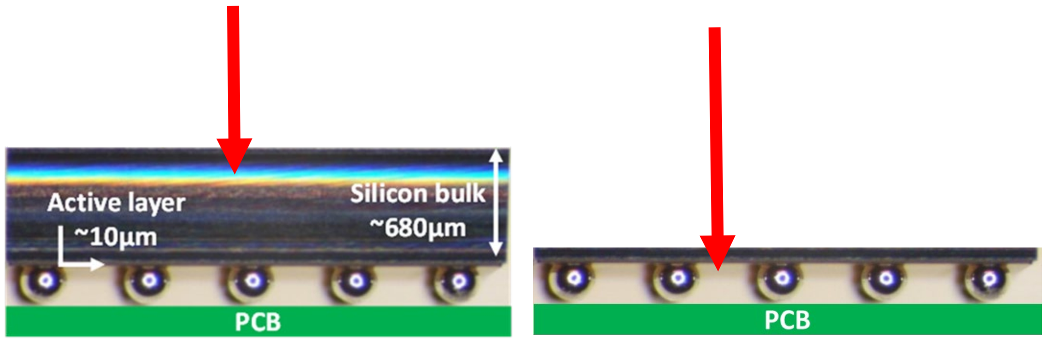


Device structure with GaNPX®-T package

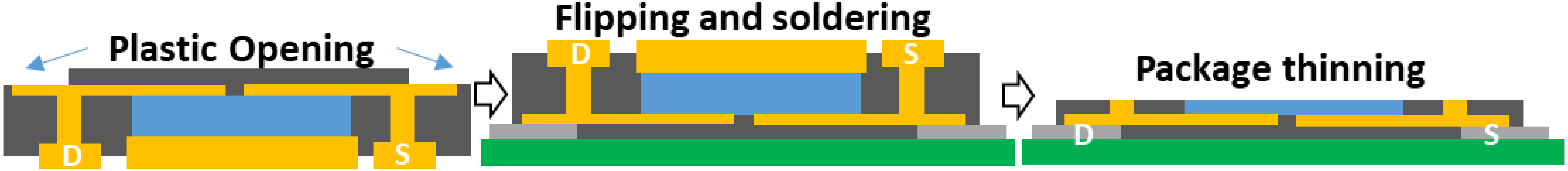
2nd method: back side testing

- **Silicon substrate shall be thinned to less than 50µm**
  - Advantage: Full AA tested, HF dynamic testing possible
  - Drawback: Gridding step shall not damage device

Heavy ion range is limited to ~50-200µm



Before thinning After thinning



J. -B. Sauveplane et al., "Heavy-Ion Testing Method and Results of Normally OFF GaN-Based High-Electron-Mobility Transistor," in IEEE Transactions on Nuclear Science, Oct. 2021

- Sample preparation was done by Alter Technology France
- Thinning objective was to be less than 50µm
- Electrical performances were controlled before and after thinning
- Very good preparation yield (almost 95%)

EPC

GS

Electrical measurements on EPC 2010C :

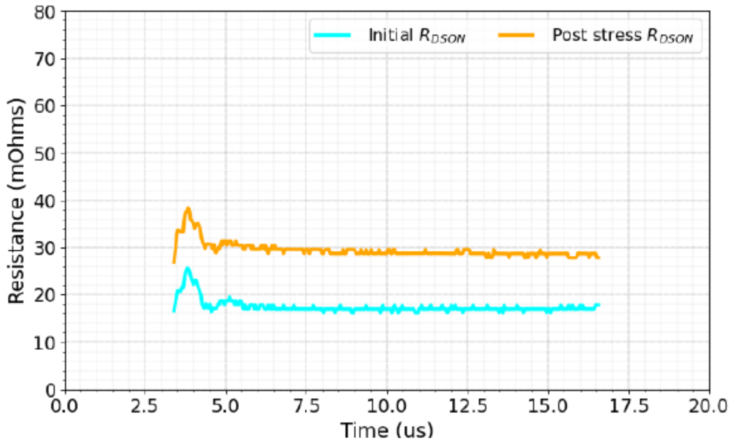
- 4 components prepared for each reference
- Maximum thickness was below 50 µm
- Thickness differences was below 5 µm
- Very good preparation yield (almost 95%)
- Negligible impact of thinning process on electrical performances

Référence	DUT #	Mesure max (µm)	Delta max (µm)
EPC2010C	3	45	5
	9	49	5
	10	45	5
	12	49	5

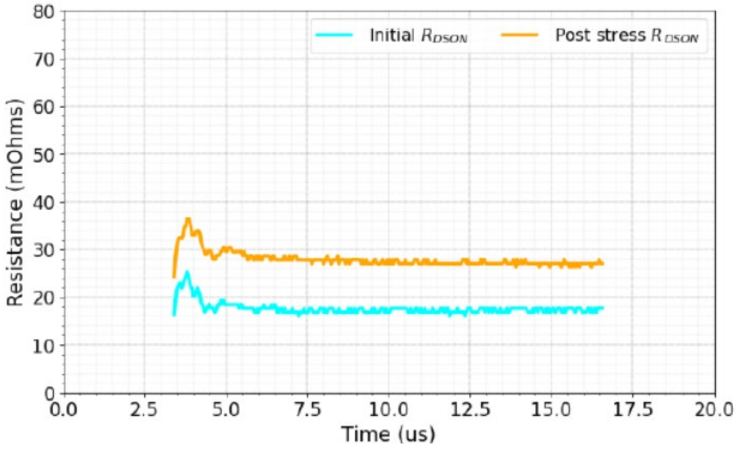
Thickness measurement after thinning

Parameter	Unit	Before	After
I_{DSS}	µA	0.113	0.121
R_{DSON}	mΩ	22.8	23.1
R_{DSON}	mΩ	22.8	23.3
V_{SD}	V	2.452	2.413
V_{TH}	V	1.953	1.936
I_{GSS} (+)	µA	1.942	1.978
I_{GSS} (-)	µA	-1.171	-1.853

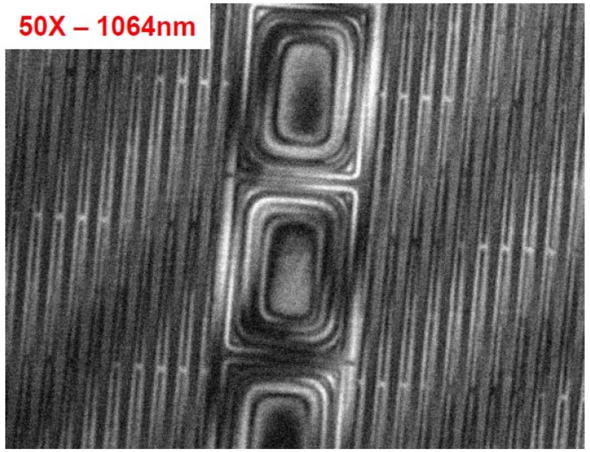
Static measurement before and after thinning



Dynamic R_{DSON} before thinning



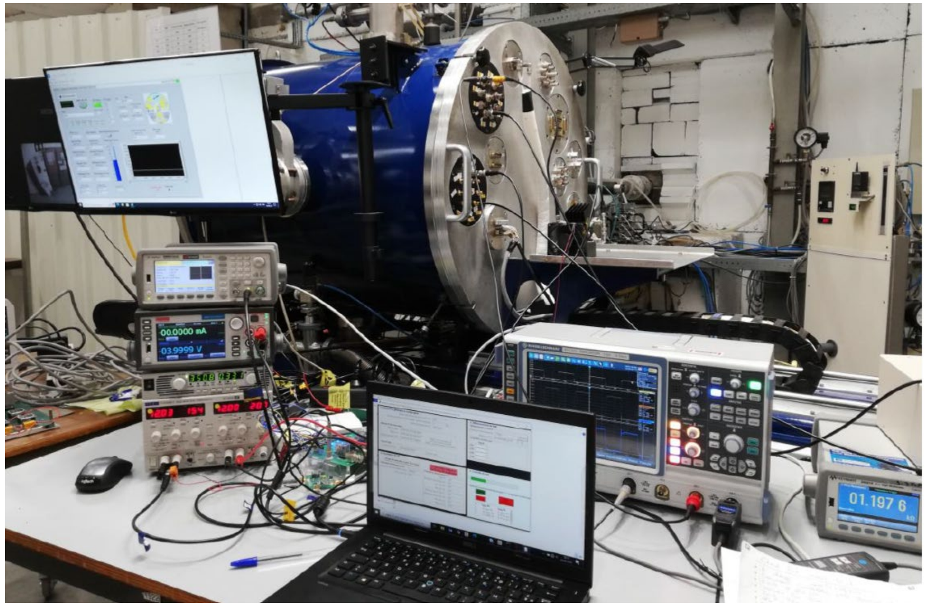
Dynamic R_{DSON} after thinning

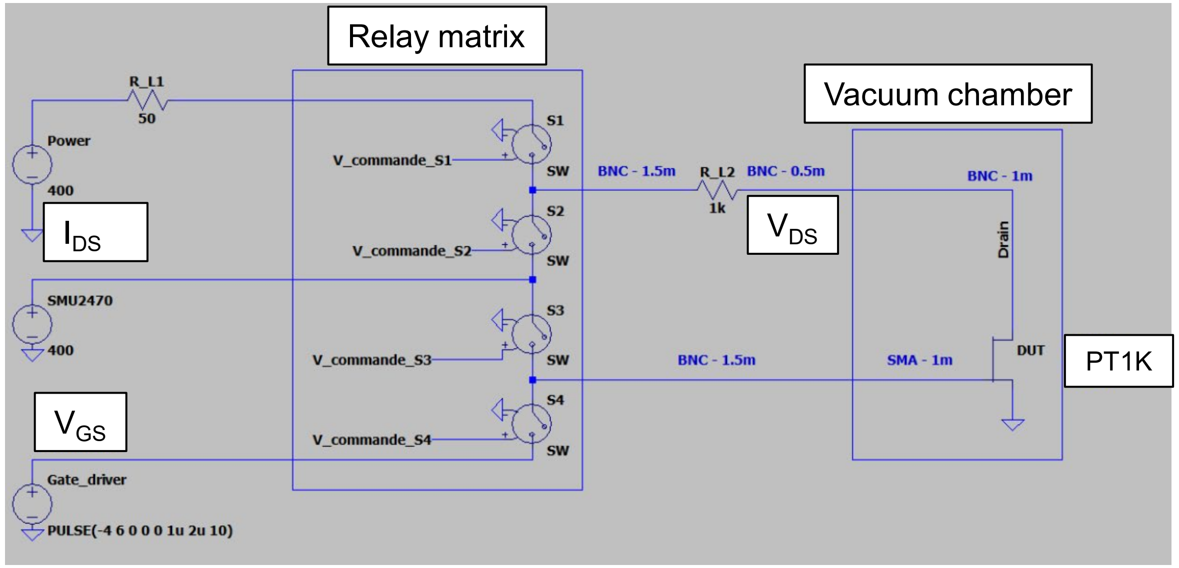


Backside infra red image of the die

Radiation test bench description :

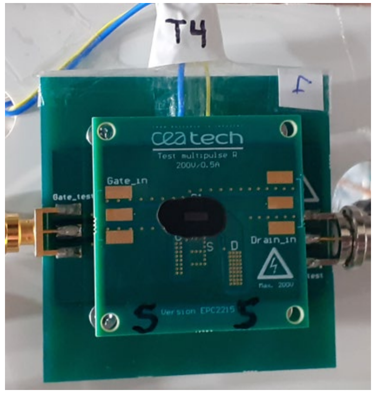
- Test bench designed and operated by CEA
- 4 relay used to switch between power on switching condition and measurement
- One SMU for measuring leakage (I_{GS} and I_{DS})
- Not possible to use a fast delatching system (because of switching)
- 1kΩ load to limit I_{DS} during Single Event Burn Out
- Monitoring of GaNFET temperature with PT1000
- 3 probes to measure V_{DS} / I_{DS} / V_{GS} (driver output)
- Driver and load are far from GaNFET
  - Advantage : Easier to manager thermal losses
  - Drawback : Parasitic inductance and capacitance

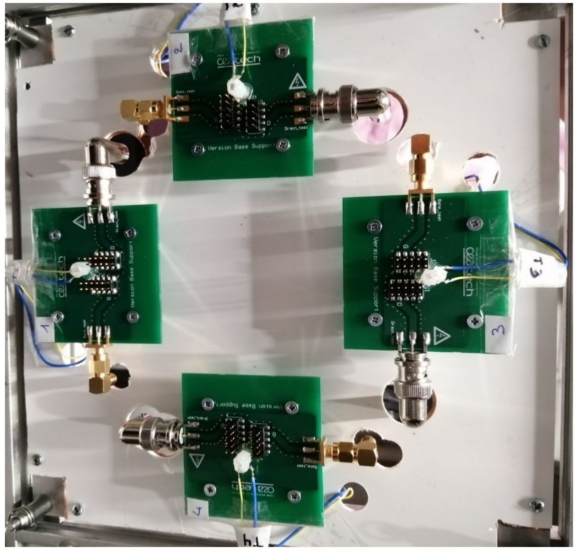


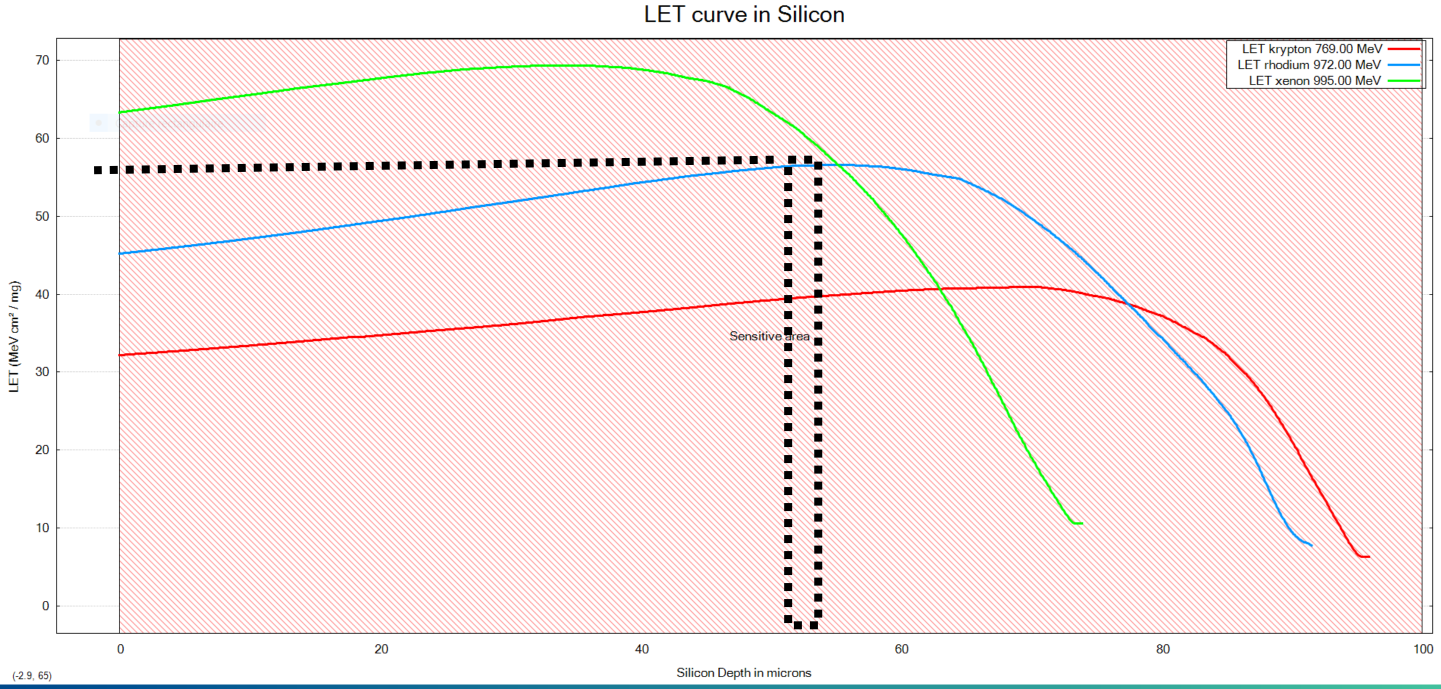


SEE test comditions:

- Safe operating area evaluation under classical testing condition
  - Normal incidence
  - 25°C
  - Static polarization condition (V_{GS}= 0V)
- Heavy ion beam characteristic:
  - Rhodium (972MeV @ UCL facility)
  - LET of 55 $MeV.cm^2/mg$
  - Flux $5000cm^{-2}.s^{-1}$
  - Total fluency $1.10^6 cm^{-2}$
- Idss et Igss are checked at the end of each run







SEE results :

Pass Fail

Run	Reference	Test configuration	VDS Max (V)	VDS Test (V)	VDS Test / VDSMAX (%)	Time (s)	Run Fluence (cm^{-2})
15	EPC2104	Statique	100	180	180	200	1,00E+06
16	EPC2104	Statique	100	200	200	36	1,80E+05
18	EPC2102	Statique	60	100	167	200	1,00E+06
19	EPC2102	Statique	60	120	200	0	0,00E+00
9	EPC2010C	Statique	200	220	110	200	1,00E+06
10	EPC2010C	Statique	200	250	125	8	4,00E+04
24	EPC2215	Statique	200	150	75	200	1,00E+06
25	EPC2215	Statique	200	160	80	66	3,30E+05
33	GS66516T	Statique	650	400	62	200	1,00E+06
34	GS66516T	Statique	650	425	65	6	3,00E+04

- **60V & 100V GEN 5 extremely robust**
- **200V GEN 4 very robust**
- **200V GEN 6 starts to need derating**
- **GS SOA is below 400V**

Low voltage and old generation references can be considered immune to SEE

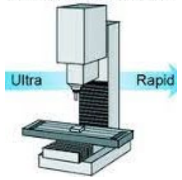
Highest voltage and newest generation references shall be considered sensitive

- **More results are planed to be presented in RADECS 2023**
  - SEE results under switching condition
  - Heavy ion beam highly tilted from normal incidence (up to 70°)

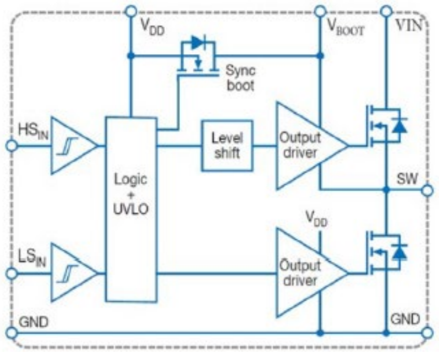
SEE test on EPC2152 :

- Half bridge with integrated gate driver
- Using EPC evaluation board
- Component preparation done in CNES lab
  - Using µ-milling thinning technic

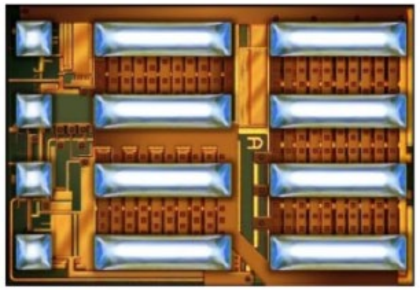
MICROMILLING



- Component functionality is validity and SEE tested in switching condition

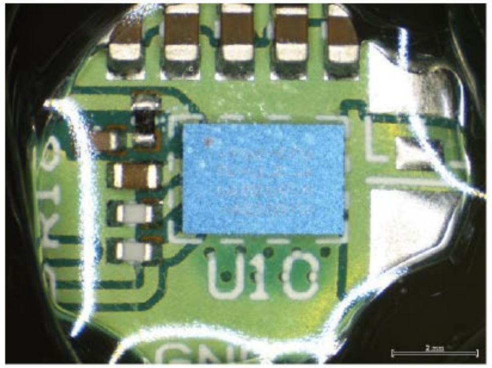


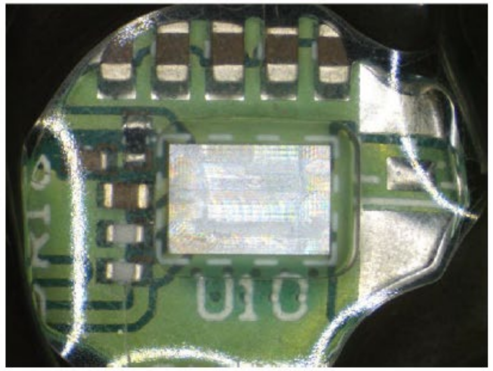
Block Diagram EPC2152
(logique + driver + GaNFET)

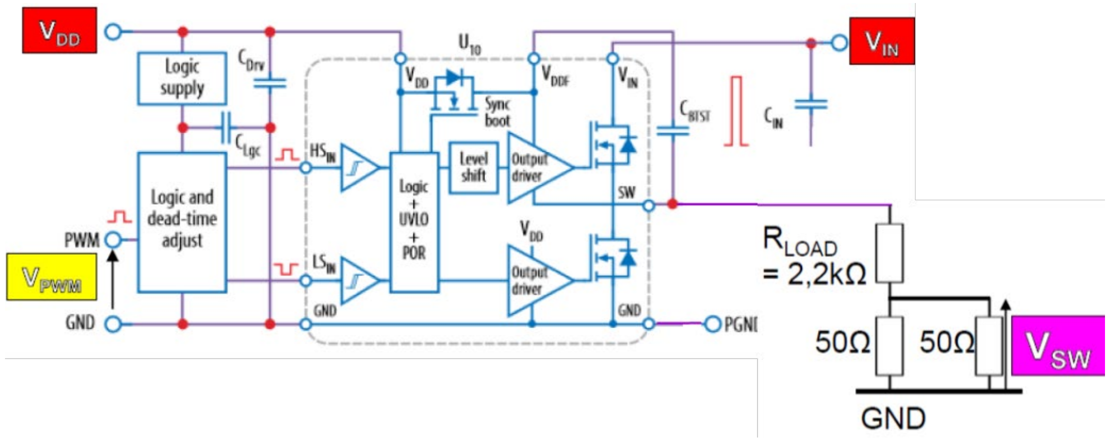


3.85 mm x 2.59 mm x 0.63 mm

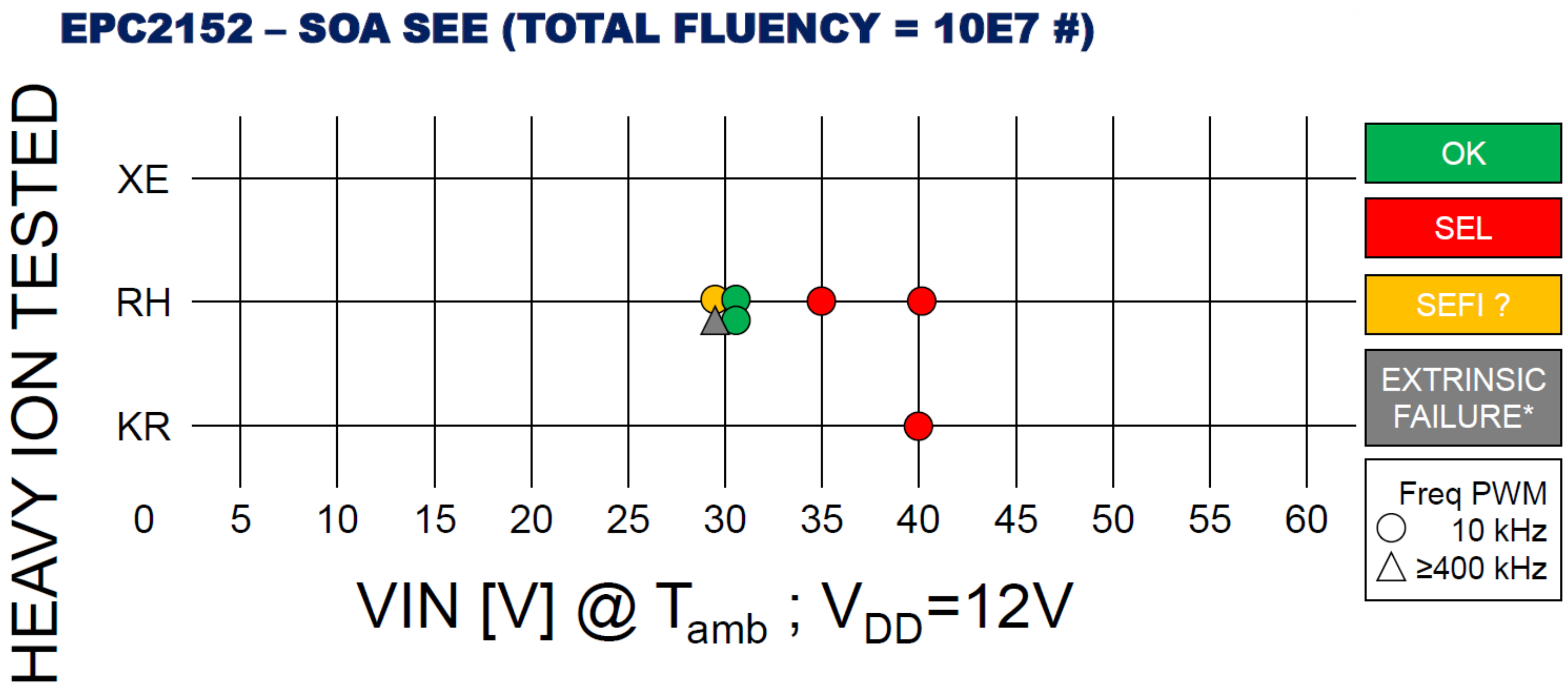
Land Grid Array (LGA)
Chip Scale Package







SEE results on EPC2152:



GaN based integrated driver and logic shall be considered sensitive to SEE

Product status being “engineering” SEE sensitivity will have to be reconsidered once in “production”

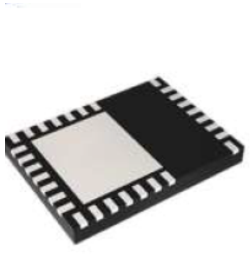
- No SEB on power FET was observed
- **Output was no longer switching (Vout=0V and Idd 50mA instead of 10mA)**

Conclusion :

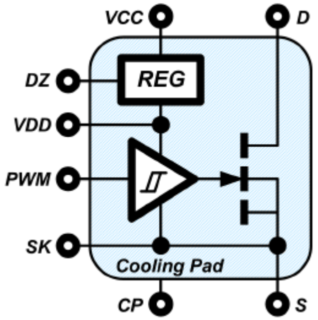
- **Today commercially available GaN are immune to TID**
  - This statement will have to be challenged with other technology (if any)
- **SEE robustness may be impressive but still need to be analyzed**
  - Low voltage and old generation references can be considered immune to SEE
  - Highest voltage and newest generation references shall be considered sensitive
  - Component with integrated driver shall be considered sensitive
- **More results are planed to be presented in RADECS 2023**
  - SEE results under switching condition
  - Heavy ion beam highly tilted from normal incidence (up to 70°)

Future work

- New GaN test campaign is foreseen in 2023-2024 using highest energy facility
  - Confirm effect of temperature
  - Confirm effect of beam angle
  - Test new references and newest generations



QFN 6 x 8 mm



Simplified schematic

Navitas: 650V /120mΩ, Monolithic integration of FET, drive and logic