ESCCON 2023
The European Space Components Conference
7 - 9 March 2023 | Toulouse | France

# EVALUATION AND QUALIFICATION STANDARDS FOR INTEGRATED CIRCUITS:

# MONOLITHIC MICROCIRCUITS, WIRE BONDED, PLASTIC ENCAPSULATED

# AND

# FLIP CHIP MONOLITHIC MICROCIRCUITS, WITH ORGANIC SUBSTRATE

*Gianandrea Quadri, EEE parts expert and CNES ESCC executive*

*Centre National d'Etudes Spatiales, Toulouse Space Center*

*gianandrea.quadri@cnes.fr*


cnes

ESCC
European Space Components Coordination

# OUTLINE

- CONTEXT (AFTER ESCCON 2021)
- CONTENTS AND FEATURES
  - Qualification standard (ESCC9000P)
  - Evaluation standard (ESCC2269000P)
- PERSPECTIVES: WAITING FOR THE RELEASE

# CONTEXT

## *WHERE WE WERE LEFT*

- In 2019, PSWG88 decided to create a working group aiming at writing an **ESCC specification for space plastic Microcircuits**
- This specification targeted high demanding applications (class 1 projects). This generic specification ESCC9000P should stay close to the ESCC9000: it is just a small adaptation of the ESCC9000 standard to a plastic part. (hermeticity test removal, THB test addition, …).
- ESCCON 2021 was the pitch for a presentation of a preliminary progress, being the standard not yet consolidated

# CONTEXT

## *WHERE WE ARE (beginning 2023)*

- Evaluation and qualification standards are consolidated and they have been submitted to the PSWG examination before final approval (last iterations are ongoing)
- A detailed specification model prepared by STM has been submitted as well
- The perimeter of both standards (ESCC9000P and ESCC2269000P) refers to:

  1) MONOLITHIC MICROCIRCUITS, WIRE BONDED, PLASTIC ENCAPSULATED

  2) FLIP CHIP MONOLITHIC MICROCIRCUITS, WITH ORGANIC SUBSTRATE

# CONTENTS AND FEATURES

- Multichip configuration and copper wire bonding are not covered by these standards
- During the evaluation, non metallic materials shall be tested in accordance with ECSS-Q-ST-0-70-02 or ASTM E595-15 to verify their outgassing requirements
- Glass transition temperature $T_g$ shall be declared in the detail specification
- Harmonization with ESCC9000 and ESCC2269000 becomes a consequence of this work, in particular with reference to terms and definitions and several test methods (ex. Scanning Electron Microscopy)
- The Working group has raised as well the need to update through DCRs:

  - ESCC 25200 (Scanning Acoustic Microscopy)→ to enlarge the panel of delamination criteria

  - ESCC 23500 (Requirements for Lead Materials and Finishes for Components for Space Application) -> to include SAC035 as a possible finish

# QUALIFICATION STANDARD chart F2 (ESCC 9000P)

| COMPONENT LOT MANUFACTURING | |
|---|---|

| WAFER LOT ACCEPTANCE | |
|---|---|
| Para. 5.2.1 | Process Monitoring Review |
| Para. 5.2.2 | Die Visual Inspection (Wafer Lot Screening) (1) |
| - | Wafer Dicing |
| Para. 5.2.3 | SEM Inspection (2) |
| Para. 5.2.4 | Total Dose Radiation Testing (2) (3) |

| SPECIAL IN-PROCESS CONTROLS (4) (5) | |
|---|---|
| WIRE-BONDED INTEGRATED CIRCUIT COMPONENTS | |
| - | Die Attach |
| Para. 5.3.1 | Die Shear Strength or Substrate Attach Strength (6) |
| - | Wire Bonding |
| Para. 5.3.2 | Wire Bond Pull and Wire Bond Shear (6) |
| Para. 5.3.3(a) | Internal Visual Inspection (6) |
| - | Encapsulation / Moulding / Lid Attach / Heat-Spreader Placement (7) |
| Para. 5.3.4 | SAM |
| Para. 5.3.5 | Lid Attach Strength (7) |
| - | Ball or Column Attach (7) |
| Para. 5.3.6 | Ball or Column Terminal Strength (7) |

| FLIP-CHIP INTEGRATED CIRCUIT COMPONENTS | |
|---|---|
| Para. 5.3.3(b) | Package/Substrate Visual Inspection (6) |
| - | Die Attach |
| Para. 5.3.7 | Bond Shear (Flip-Chip) (8) |
| - | Underfill |
| Para. 5.3.4 | SAM |
| Para. 5.3.3(a) | Internal Visual Inspection (6) |
| - | Add-on Components Attach (7) |
| Para. 5.3.8 | Add-on Components Die Shear Strength or Substrate Attach Strength (7) |
| Para. 5.3.3(c) | Visual Inspection of Add-on Components (6) (7) |
| - | Encapsulation / Moulding / Lid Attach / Heat-Spreader Placement (7) |
| Para. 5.3.4 | SAM |
| Para. 5.3.5 | Lid Attach Strength (7) |
| - | Ball or Column Attach (7) |
| Para. 5.3.6 | Ball or Column Terminal Strength (7) |

| | |
|---|---|
| Para. 5.3.9 | Dimension Check (2) |
| Para. 5.3.10 | Weight (9) |

| TO CHART F3 – SCREENING TESTS |
|---|

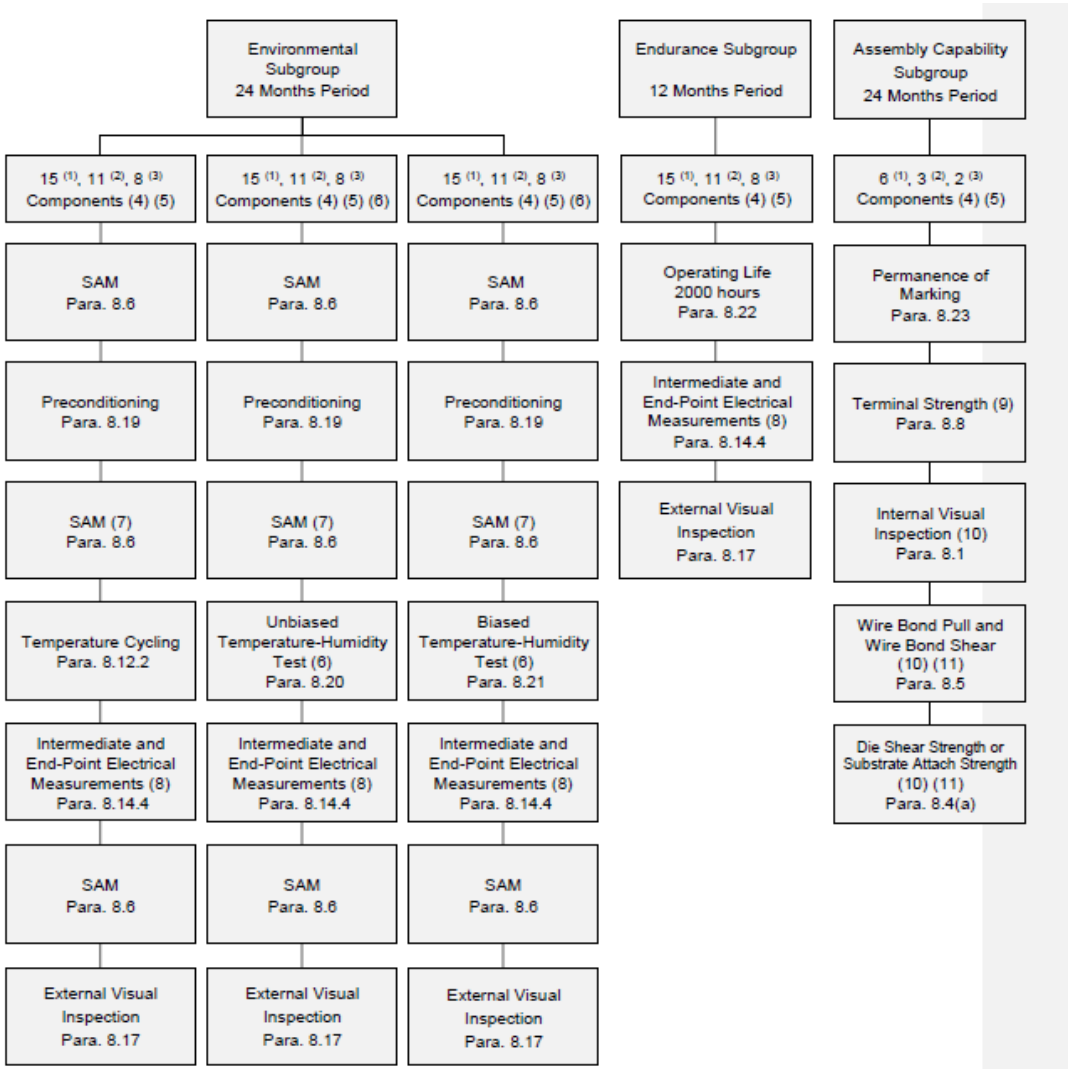
NOTES:
1. May be performed either on-wafer or after dice separation.
2. Performed on a sample basis.
3. Only required if specified in the Detail Specification and stipulated in the Purchase Order.
4. Special In-Process Controls shall be performed on a sample basis which shall be agreed with the ESCC Executive.
5. Unless otherwise specified, the sequence of Special In-Process Controls is at the discretion of the Manufacturer subject to the approval of the ESCC Executive.

# QUALIFICATION STANDARD chart F3 (ESCC 9000P)

| COMPONENTS FROM PRODUCTION CONTROL | |
|---|---|
| Para. 6.1 | Serialisation |
| Para. 8.10 | Radiographic Inspection |
| Para. 8.11.1 | Constant Acceleration (1) |
| Para. 8.12.1 | Temperature Cycling |
| Para. 8.6 | SAM (2) |
| Para. 8.13 | Bake |
| Para. 8.14.1 | Parameter Drift Values (Initial Measurements) |
| Para. 8.15 | High Temperature Reverse Bias Burn-in |
| Para. 8.14.1 | Parameter Drift Values (Final Measurements for HTRB Burn-in; Initial Measurements for Power Burn-in) (3) |
| Para. 8.16 | Power Burn-in |
| Para. 8.14.1 | Parameter Drift Values (Final Measurements) (3) |
| Para. 8.14.2 | Room Temperature Electrical Measurements (3) (4) |
| Para. 8.14.3 | High and Low Temperatures Electrical Measurements (3) |
| Para. 6.4 | Check for Lot Failure (5) |
| Para. 8.17 | External Visual Inspection |
| Para. 8.18 | Solderability (2) (3) |
| TO CHART F4A OR F4B WHEN/AS APPLICABLE | |

NOTES:
1. Only applicable to Cavity Packaged Components (see the Detail Specification for details).
2. Performed on a sample basis.
3. The lot failure criteria of Para. 6.4 apply to this test.
4. Measurements of Parameter Drift Values need not be repeated in Room Temperature Electrical Measurements.
5. Check for Lot Failure shall take into account all electrical parameter failures that may occur during Screening Tests in accordance with Paras. 8.14.1, 8.14.2, 8.14.3 subsequent to HTRB Burn-in.

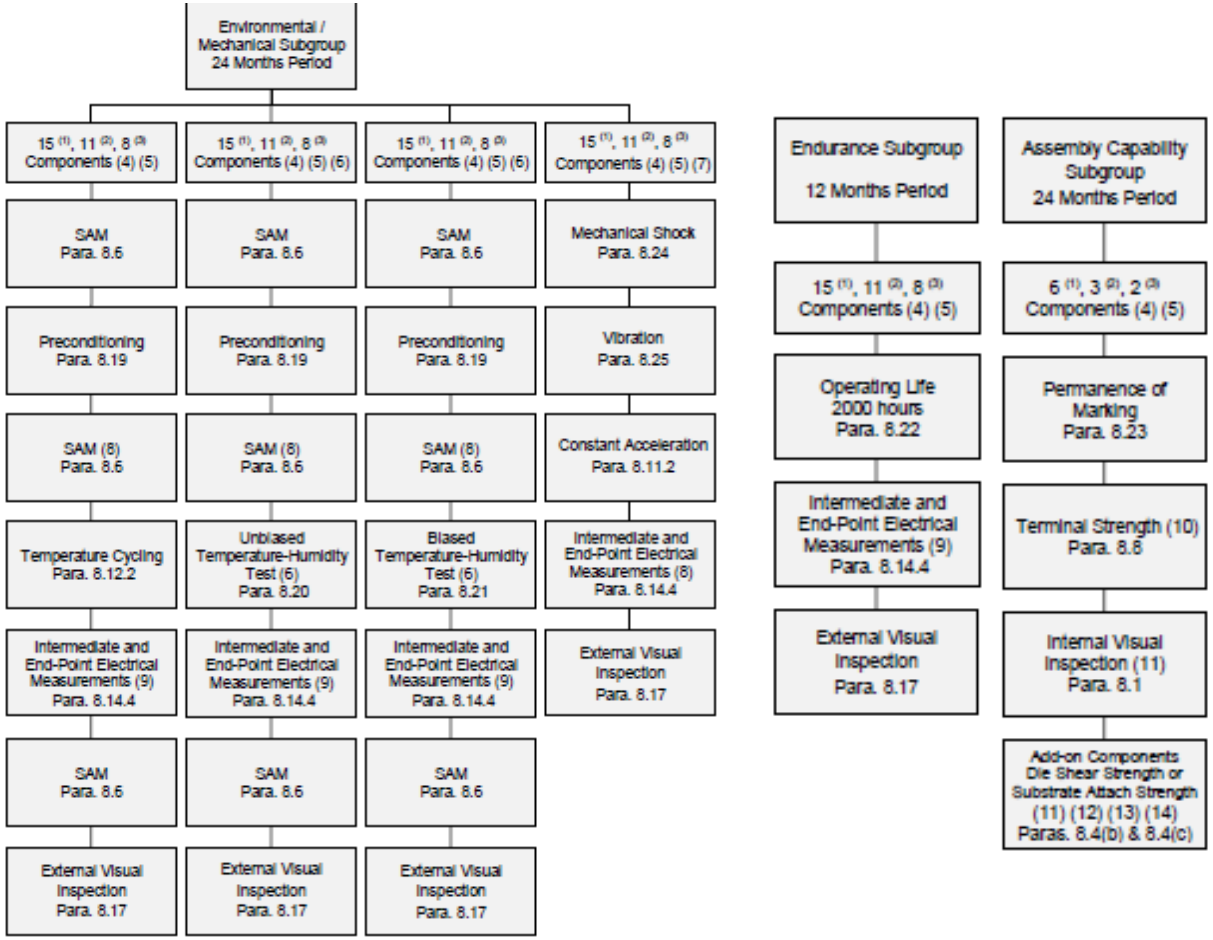
# QUALIFICATION STANDARD chart F4A (ESCC 9000P) FOR WIREBONDED INTEGRATED CIRCUIS COMPONENTS




NOTES:

1. The quantity for qualification and qualification maintenance of a single type (see Para. 7.1.2.1).
2. The quantity per type for qualification and qualification maintenance of two types selected (see Para. 7.1.2.2).
3. The quantity per type for qualification and qualification maintenance of three or more types selected (see Para. 7.1.2.2).
4. For distribution within the subgroups, see Para. 7.1.2 for qualification and qualification maintenance, and Para. 7.4 for Lot Validation Testing.
5. No failures are permitted.
6. The Manufacturer shall perform either one or both test sequence(s) containing the Unbiased Temperature Humidity Test and the Biased Temperature-Humidity Test, depending on their relevance to the component(s) under test (see the Detail Specification for details).
7. Test is optional at the Manufacturer's discretion.
8. Unless otherwise specified in the Detail Specification, electrical measurements shall be performed at room, high and low temperatures.
9. May be performed at any point during the subgroup, depending on package configuration.
10. The components shall be de-encapsulated in accordance with ESCC Basic Specification No. 25300, or equivalent, to facilitate Internal Visual Inspection, Wire Bond Pull and Wire Bond Shear, and either Die Shear Strength or Substrate Attach Strength. Any observed defect determined to have resulted from the de-encapsulation process may be ignored subject to the approval of the ESCC Executive.
11. Wire Bond Pull and Wire Bond Shear, and Die Shear Strength or Substrate Attach Strength may be replaced by a technical justification supported by Special In-Process Controls data or other verification processes which demonstrate the requirements, subject to the approval of the ESCC Executive.

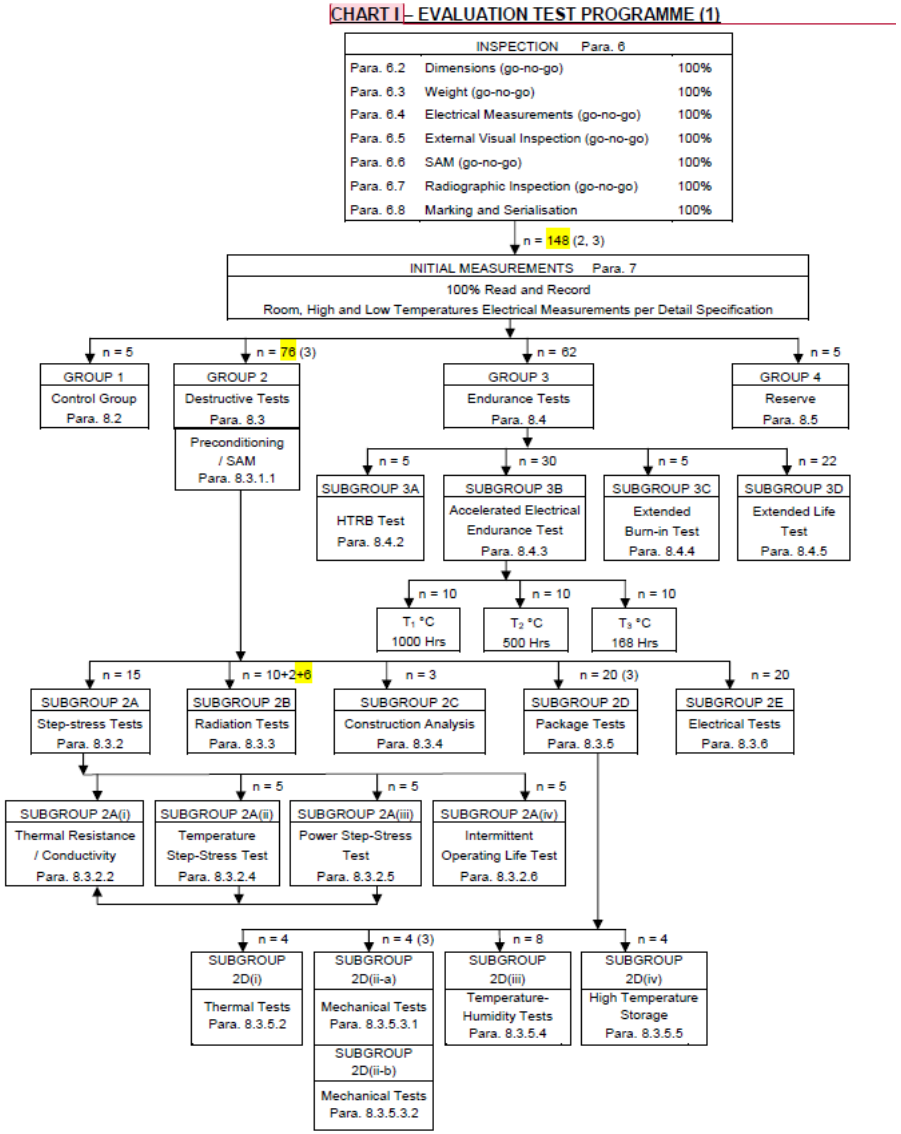
# QUALIFICATION STANDARD chart F4B (ESCC 9000P) FOR FLIP-CHIP INTEGRATED CIRCUIS COMPONENTS




**NOTES**:

1. The quantity for qualification and qualification maintenance of a single type (see Para. 7.1.2.1).
2. The quantity per type for qualification and qualification maintenance of two types selected (see Para. 7.1.2.2).
3. The quantity per type for qualification and qualification maintenance of three or more types selected (see Para. 7.1.2.2).
4. For distribution within the subgroups, see Para. 7.1.2 for qualification and qualification maintenance, and Para. 7.4 for Lot Validation Testing.
5. No failures are permitted.
6. The Manufacturer shall perform either one or both test sequence(s) containing the Unbiased Temperature Humidity Test and the Biased Temperature-Humidity Test, depending on their relevance to the component(s) under test (see the Detail Specification for details).
7. Mechanical Subgroup tests shall only be performed for Cavity Packaged Components (see the Detail Specification for details).
8. Test is optional at the Manufacturer's discretion.
9. Unless otherwise specified in the Detail Specification, electrical measurements shall be performed at room, high and low temperatures.
10. May be performed at any point during the subgroup, depending on package configuration.
11. The components shall be de-encapsulated in accordance with ESCC Basic Specification No. 25300, or equivalent, to facilitate Internal Visual Inspection, and Add-on Components Die Shear Strength or Substrate Attach Strength. Any observed defect determined to have resulted from the de-encapsulation process may be ignored subject to the approval of the ESCC Executive.
12. Only 1 sample shall be tested.
13. Add-on Components Die Shear Strength or Substrate Attach Strength may be replaced by a technical justification supported by Special In-Process Controls data or other verification processes which demonstrate the requirements, subject to the approval of the ESCC Executive.
14. As applicable (see the Detail Specification for details).

# EVALUATION STANDARD chart I (ESCC 2269000P)




**NOTES:**

1. Unless otherwise specified, the quantity of components required for testing in each Group/Subgroup is indicated by the letter n.
2. Additional test components/structures/materials may also be required (see Para. 5.1)
3. Subgroups 2D(ii-a) and 2D(ii-b) tests shall only be performed for Cavity Packaged (Flip-Chip Integrated Circuit) Components

# EVALUATION STANDARD chart I (ESCC 2269000P) : focus on SAM

8.3.1.1 *Preconditioning / SAM*

Components to be subjected to Subgroups 2A, 2C and 2D tests only shall first be subjected to the following:

(a) Preconditioning:
All components shall be subjected to preconditioning in accordance with JESD22-A113.
Prior to performing preconditioning, the moisture sensitivity level (MSL) of each component type being evaluated shall have been determined in accordance with J-STD-020 and approved by the ESCC Executive.

(b) Scanning Acoustic Microscopy (SAM): per Para. 6.6.

6.6 SCANNING ACOUSTIC MICROSCOPY (SAM) (100%)

All components shall be tested in accordance with ESCC Basic Specification No. 25200, plus additional SAM requirements as specified in the Detail Specification, including specific inspection requirements applicable to all thermal interface materials. Rejected components shall be replaced.

**NOTE:**
Components submitted to SAM shall be subjected to a final drying phase consisting of a minimum bake of duration 1 hour at $T_{amb}$ = +125°C. J-STD-033 may be used as a guideline for the appropriate drying conditions.

The following additional reject criteria shall also apply:

(a) For Wire-Bonded Integrated Circuits with a metal lead-frame:
1. No delamination on the active side of the die
2. No delamination on any wire bonding surface including the down-bond area or the lead-frame of lead-on-chip (LOC) components.
3. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, tie bars, heat-spreader alignment features, heat slugs, etc..
4. No delamination/cracking > 50% of the die attach area:
   i. in components with exposed die pad used for thermal conductivity
   ii. for components that require electrical contact to the backside of the die
5. Delamination of more than half of the backside of the die paddle/plastic interface.
6. Any void in moulding compound crossing wire-bond.

(b) For Wire-Bonded Integrated Circuits with an organic substrate:
1. No delamination on the active side of the die
2. No delamination on any wire bonding surface including the down-bond area or the lead-frame of lead-on-chip (LOC) components.
3. No delamination on any electrical contact surface of the laminate.
4. No delamination within the substrate.
5. No delamination/cracking > 50% of the die attach area:
   i. in components with exposed die pad used for thermal conductivity
   ii. for components that require electrical contact to the backside of the die
6. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, tie bars, heat-spreader alignment features, heat slugs, etc..
7. Any void in moulding compound crossing wire-bond.

(c) For Flip-Chip Integrated Circuits:
1. No delamination on the active side of the die
2. No delamination on any electrical contact surface of the laminate.
3. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, laminate, laminate metallization, PTH, heat slugs, etc.
4. No delamination/cracking between underfill resin and chip, or underfill resin and substrate/solder mask.
5. No delamination within the substrate.

# EVALUATION STANDARD chart I (ESCC 2269000P) : focus on new test methods

8.3.2.6 *Subgroup 2A(iv) – Intermittent Operating Life Test*

(a) Applicability

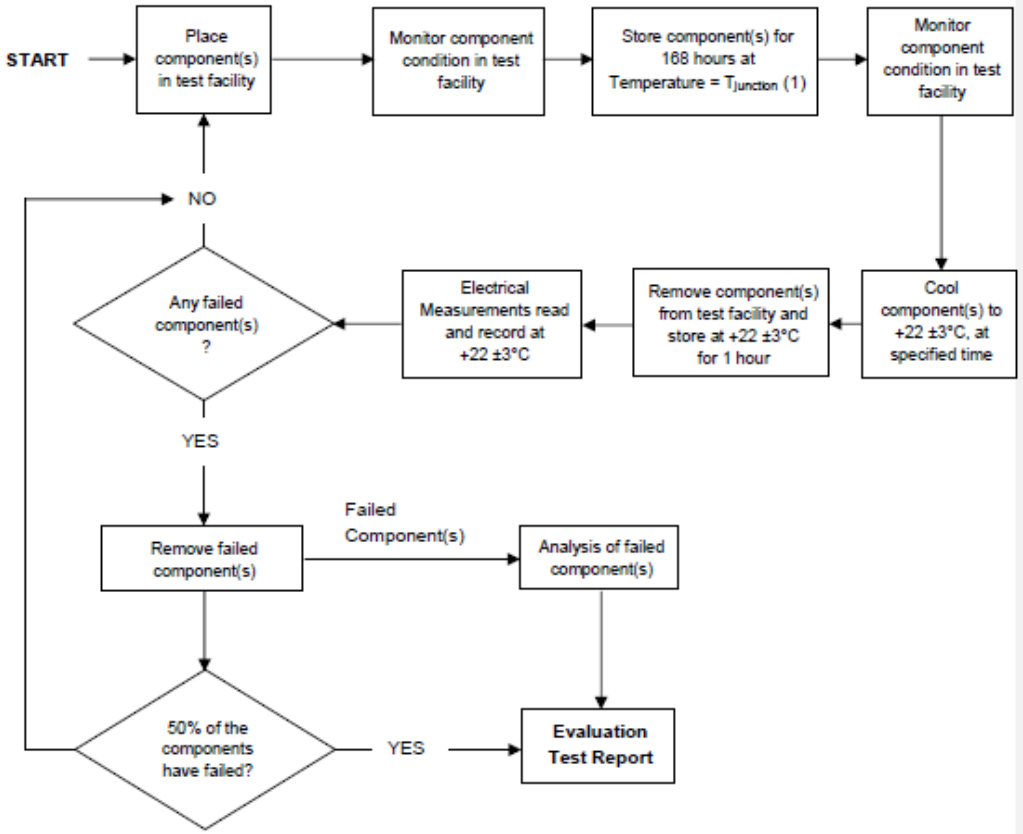
This test is only applicable to components where operation in circuits requiring transfer and dissipation of significant and/or varying levels of power is an intended feature of their design. The ESCC Executive shall review the component type and technology to determine the applicability of the test.

(b) Procedure

The Components shall be subject to an Intermittent Operating Life test until failure or up to 6000 on/off cycles, whichever occurs first, at $T_{amb}$ = +125°C per MIL-STD-883, Test Method 1006. The frequency and duration of the on and off cycles shall be as agreed with the ESCC Executive. The applied operating conditions during the on cycles shall use the maximum specified power and shall be subject to approval by the ESCC Executive.

Electrical measurements shall be performed in accordance with Para. 8.3.2.3 above before and after the test.

# EVALUATION STANDARD chart II (ESCC 2269000P) :




**NOTES**

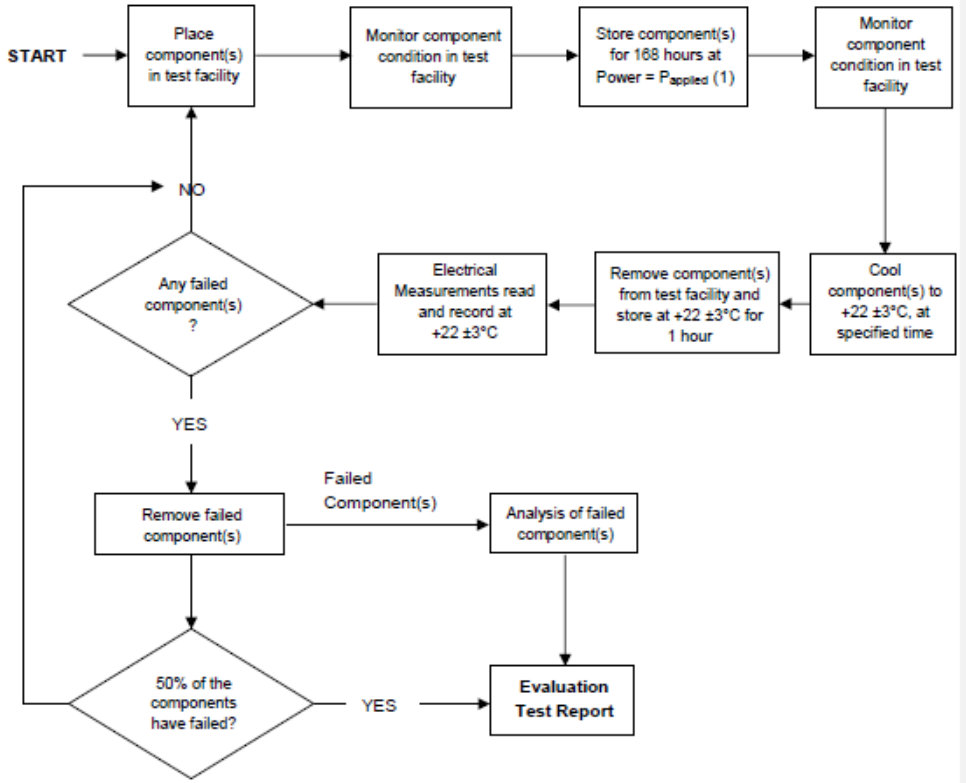
1. Temperature steps with $T_{junction}$:

   First step: $T_0$ (°C)
   $T_1$ (°C)
   $T_2$ (°C)
   Last step: $T_n$ (°C)

   with ($T_n > \ldots T_2 > T_1 > T_0$)

# EVALUATION STANDARD chart III (ESCC 2269000P) :




NOTES

1. Power steps with $P_{applied}$:
   First step: $P_0$ (W)
   $P_1$ (W)
   $P_2$ (W)
   Last step: $P_n$ (W)

   with ($P_n > \ldots P_2 > P_1 > P_0$)

*Approaching the final acceptance and release….*

| Name | Organization | Category |
|---|---|---|
| Gianandrea QUADRI | CNES | Agency |
| David DANGLA | CNES | Agency |
| Ana COLLADO | ESA | Agency |
| Juergen BEISTER | ESA | Agency |
| Federica FERRARESE | DLR technical advisor | Agency |
| Alberto MORENO | DLR technical advisor | Agency |
| Szymon BEDNARSKI | ALTER | ATH |
| Alain MOUTON | AIRBUS | Eurospace |
| Florian MOLIERE | AIRBUS | Eurospace |
| Cedric CLEMENT | AIRBUS | Eurospace |
| MICHEL CARQUET | TAS | Eurospace |
| MICHEL PERREL | TAS | Eurospace |
| J.-Noel LETRILLARD | STM | Manufacturer |
| Jean-Louis FRIGOUL | NANOEXPLORE | Manufacturer |
| Valerie LEPALUDIER | MCP | Manufacturer |
| Danny LAMBRICHTS | IMEC | Manufacturer |
| Piet DE PAUW | IMEC | Manufacturer |
| NICO BEYLEMANS | IMEC | Manufacturer |
| Joel BONNET | E2V | Manufacturer |
| Tudor CHIRILA | INFINEON | Manufacturer |
| Denis LACOMBE | ESA | Agency |
| Yves LAVIGNASSE | STM | Manufacturer |







***THANKS TO THE WORKING GROUP MEMBERS!!!!***



***THANKS FOR YOUR ATTENTION!!!!***