Plastic encapsulation process, capability and evaluation for Space

Szymon Bednarski
High Reliability and Space Programme Manager
ALTER TECHNOLOGY TÜV NORD UK Ltd
Szymon.Bednarski@uk.altertechnology.com

Matt Booker
Sales Director
ALTER TECHNOLOGY TÜV NORD UK Ltd
Matt.Booker@uk.altertechnology.com

Content

- Alter UK summary and company update
- Packaging market
- Plastic packaging technical capability, design and offer
- Pre-qual completion, design highlights
- Evaluation test plan and testing status updates

Company

TÜV NORD GROUP


ENERGY

IT


MOBILITY


HEALTH AND NUTRITION


NATURAL RESOURCES

AEROSPACE & ELECTRONIC

ALTER TECHNOLOGY LOCATIONS *Seville* *Madrid* *Toulouse* *Livingston* *Glasgow* *Germany (HTV)*

2003 Optocap founded by Scottish Enterprise

2009 Management Buy-Out

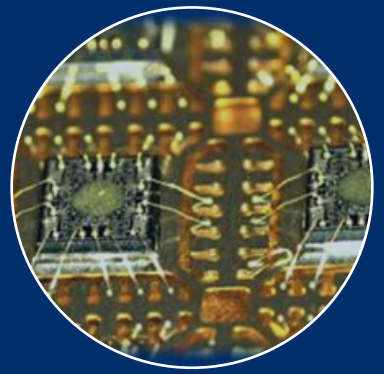
2016 Acquisition by ALTER TÜV NORD

2019 Alter Technology TÜV NORD UK

2021 Alter opens Photonics Design Centre

ALTER UK Company History

At a glance



Microelectronics Packaging

Fast Turn Prototyping
Plastic QFN
Hermetic Hi-Rel
Chip-on-board

Custom Photonics

Laser Diode Components
Optical Amplifiers
PIC Packaging

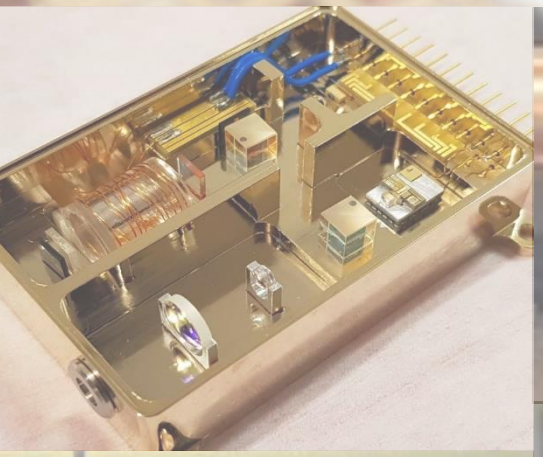
Photonics Design Centre

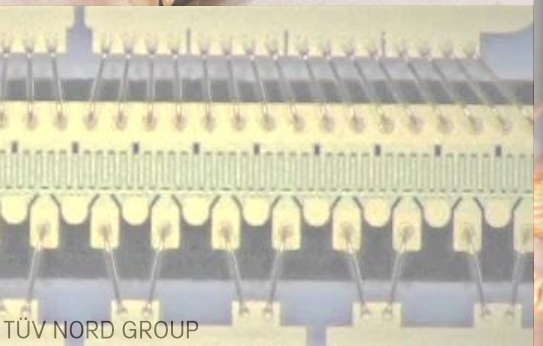
Quantum Laser Systems
Space Grade Optical Transceivers

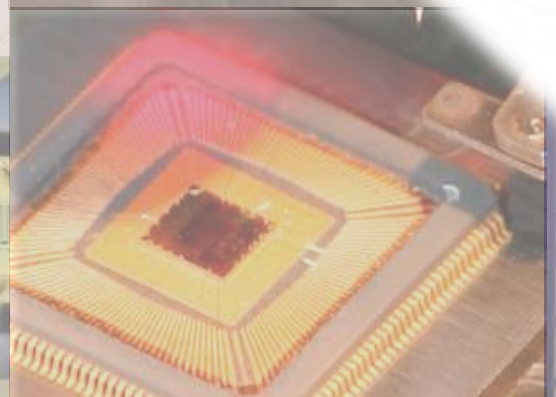
ALTER TECHNOLOGY UK

UK Packaging Services

- R & D
- Fast Turn Prototyping
- Package Design & Modelling
- Process Development
- Automated Volume Manufacturing
- Flight Module Assembly



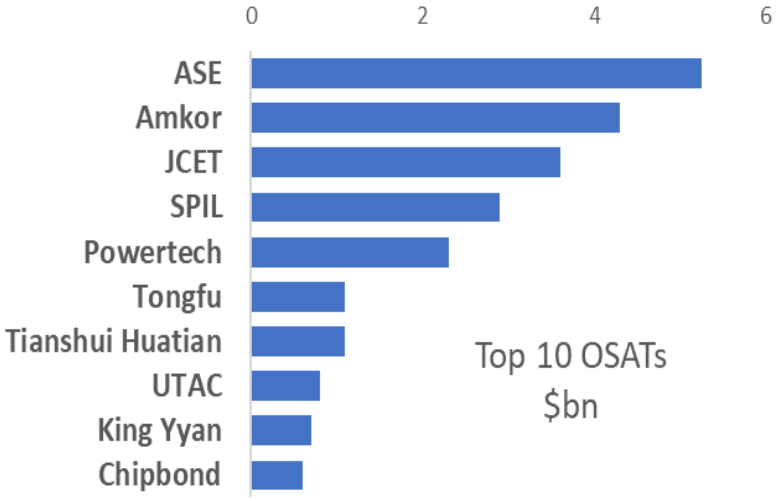


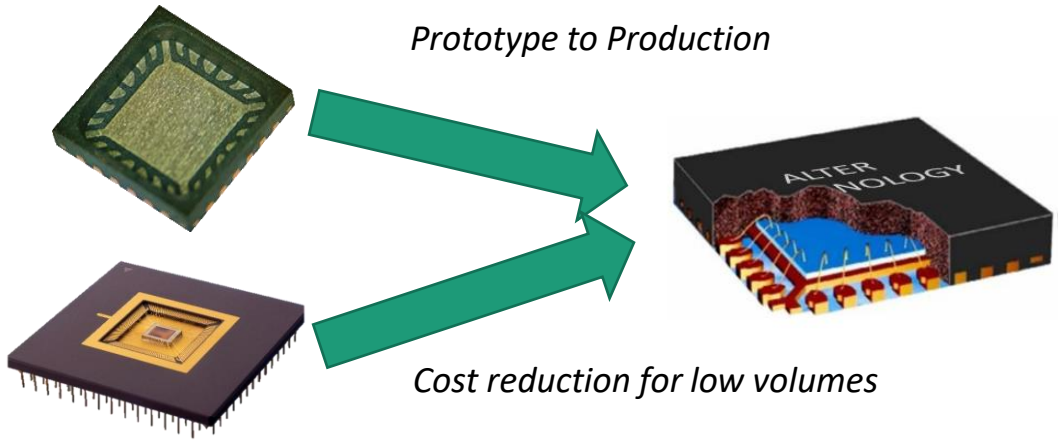


Capabilities

Current Market Offerings

- Large scale OSATs centred in Asia (top 5 OSATs = $18bn)
- High volume & very low cost (millions/day)
- Capacity dominated by consumer, mobile & automotive
- Difficult to access for low & medium volume applications
- Small batches and customers “pollute” the production lines.
- Some success stories with start-ups projecting high volume
- Specialist packaging in EU focused on sensors
- Use of single cavity packages very high cost



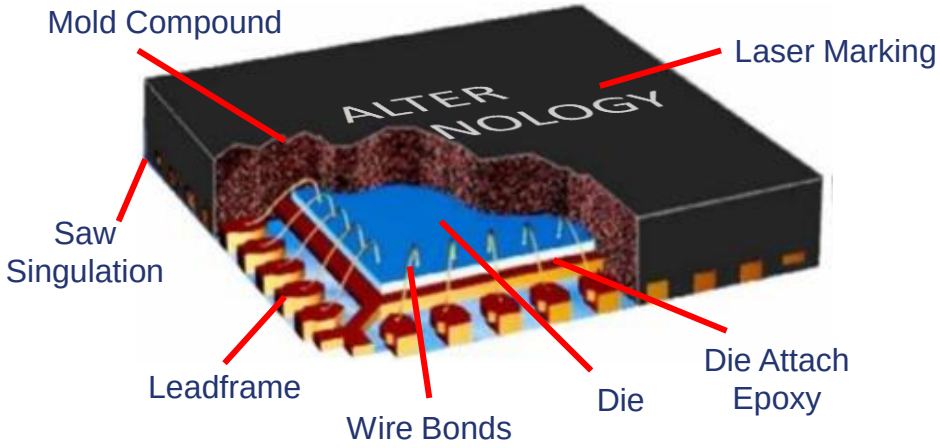


Plastic Encapsulated QFN Platform

- Alter Technology UK offer a low-cost plastic encapsulated packaging service for customers with low to medium volumes applications such as medical, industrial, space and aerospace.

- The QFN (Quad Flat No Lead) package is designed for near chip scale packaging, offering excellent electrical and thermal performance (via an exposed solderable pad).
- Recognizing that high volume lines for outsourced assembly are dominated by consumer, mobile and automotive applications, Alter have installed this technology in our Livingston (Scotland) facility.
- Alter's QFN packages are based around an etched copper alloy lead frame, over molded with epoxy mold compound and provide a cost-effective solution for a range of die sizes and pin counts.
- **Features of the QFN package:**

  Small size 3x3mm to 12x12mm
  High thermal performance with exposed pad.
  Improved electrical performance (compared to leaded plastic packages)
  Moisture sensitivity to JEDEC MSL-3 .
  RoHS compliant.



Design Rules

Technical Data – Plastic Encapsulated QFN

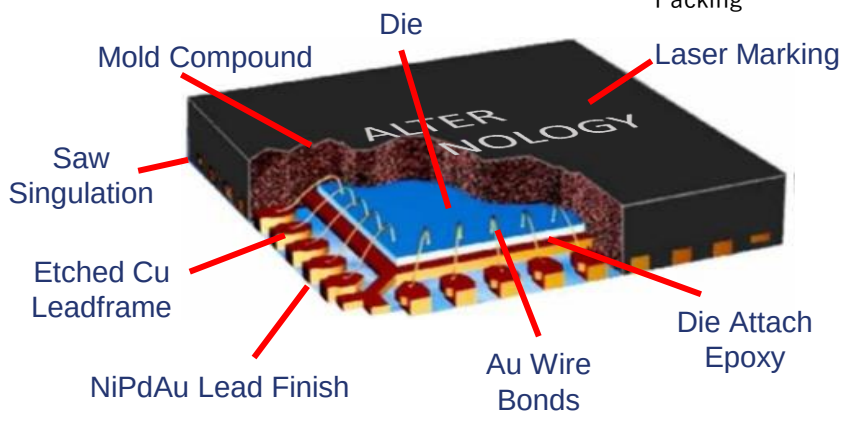
- **Alter Technology UK offer low-cost plastic encapsulated QFN packaging for batch sizes from 100pcs to several 1000s, with total capacity for millions per year.**
- The QFN (Quad Flat No Lead) package is designed for near chip scale packaging, offering excellent electrical and thermal performance via an exposed solderable pad.
- QFN packages are based around an etched copper alloy lead frame, over molded with epoxy mold compound. A range of open-tool lead frames are available to accommodate most die sizes and pin counts. Customisation of size and pin-count can be achieved for low NREs.

Features

Small size 3 x 3 to 12 x 12 mm
0.9 mm nominal thickness
Saw Singulation
High thermal performance with exposed pad
Improved electrical performance
Moisture sensitivity to JEDEC MSL-3
RoHS compliant

Materials

Die Input	Wafer / Waffle Tray / VR Gel-Pak
Die attach epoxies	Conductive Ablebond 84-1 LMISR4 Non-conductive Ablebond 84-3 Silver sintering
Wire bond	25um, 99.99% Au wire
Mold compound	Hysol GR900C, Black – Standard High Tg EMC – Under evaluation
Leadframe alloy	Cu Alloy 194, Full Hard
Lead plating	NiPdAu
Packing	JEDEC Tray



For enquiries contact
info@uk.altertechnology.com

Dimensions in mm unless stated

Package Availability

Lead count	Body Size	Designation 1	Lead pitch	Exposed pad	Die pad
24	4 x 4	VGGD 9	0.5	2.60	2.66
16	5 x 5	VHHB	0.8	3.34	3.74
32	5 x 5	VHHD 4	0.5	3.70	3.88
40	6 x 6	VJJD 5	0.5	4.34	4.74
48	7 x 7	VKKD 6	0.5	5.34	5.74
56	8 x 8	VLLD 2	0.5	6.34	6.74
64	9 x 9	VMMD 3	0.5	7.65	7.76

Thermal Performance [2]

Lead Count	Body size	Exposed pad	ΘJC C/W	ΘJA C/W
24	4 x 4	2.60	4.5	47
16	5 x 5	3.34	4.3	46
32	5 x 5	3.70	3.5	44
40	6 x 6	4.34	3.2	39
48	7 x 7	5.34	3	34
56	8 x 8	6.34	2	31
64	9 x 9	7.65	1	29

Electrical Parameters [2]

Wire	Diameter	R (milli-ohm/mm)		Ls (nH/mm)	Cs (pF/mm)
	µm	0 Hz (DC)	100MHz	100-400MHz	100-400MHz
Gold (Au-4N)	25	58.40	103.47	1.043	0.092

Dimensions in mm unless stated. [1] Ref. JEDEC MO-220. [2] Typical parameters.

Design Rules – Plastic Encapsulated QFN

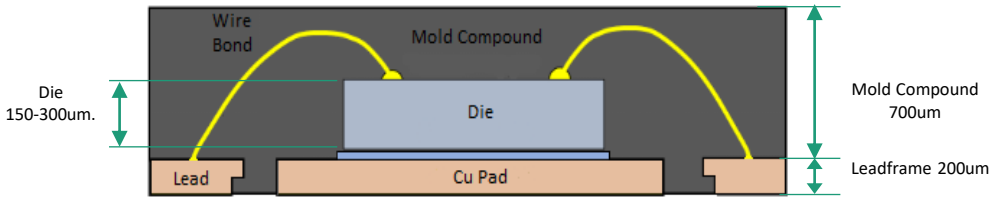
Die Size

The range of die sizes that can be accommodated in each package size is shown below.

Lead count	Body Size	Designation	Die pad size	Maximum die size	Max die size with down bonds [1]
24	4x4	VGGD 9	2.66	1.95 x 1.95	1.5 x 1.5
16	5x5	VHHB	3.74	3.0 x 3.0	2.5 x 2.5
32	5x5	VHHD 4	3.88	3.1 x 3.1	2.6 x 2.6
40	6x6	VJJD 5	4.74	4.0 x 4.0	3.5 x 3.5
48	7x7	VKKD 6	5.74	5.0 x 5.0	4.5 x 4.5
56	8x8	VLLD 2	6.74	6.0 x 6.0	5.5 x 5.5
64	9x9	VMMD 3	7.76	7.0 x 7.0	6.5 x 6.5

Note 1. Assumes down bonds on all sides, 0.25mm required per side for down bonds.

Note 2. Permitted die thickness: 150-300µm. This is based on a 0.9mm nominal package, 200µm leadframe, 250µm wirebond height and 150µm clearance from the top of wirebond to package surface.



QFN Stack-up

Wire Bonding

The wire bonding limits for QFN packages based on 25um Au wire are as follows

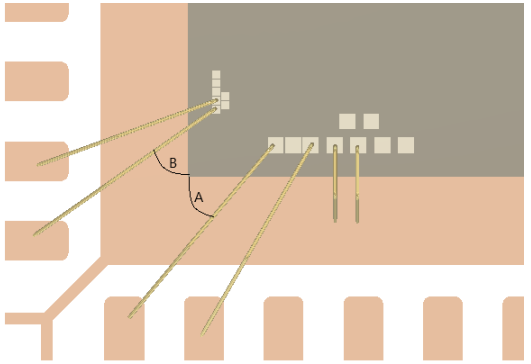
Wire diameter µm	Wire length		Minimum bond pad opening µm	Minimum bond pad pitch µm
	Min	Max		
17	0.5	2.5	50	55
20	0.5	2.5	60	60
25	0.5	3.5	70	75
33	0.5	3.5	95	100

Bond Wires per QFN terminal - A maximum of 3 wires per leadframe finger/pad is allowed.

Staggered Bond Pads on Die - If staggered pads on the die are required, the layout must be reviewed with Alter technology.

Wirebond Down Bond Locations and Numbers - Down bonds to die attach pad can be accommodated, however this reduces the maximum die size by 250µm on each side down bonds are located.

Wire Angles
For bond pad pitches of >80µm the angle of the wire to the die edge must be no less than 45 degrees to die edge for bond pad (angle A, below)
Increasing to no more than 60 degrees for pitches less than 80µm(angle B, below).



Dimensions in mm unless stated

Design Rules – Plastic Encapsulated QFN

Marking

Package size	Number of lines of text	Maximum characters per line	Minimum text height	Minimum text spacing
4 x 4	3	5	0.9	0.9
5 x 5	3	6	0.9	0.9
6 x 6	4	7	0.9	0.9
7 x 7	4	8	0.9	0.9
8 x 8	5	9	0.9	0.9
9 x 9	5	10	0.9	0.9

An example of a marking configuration for a 9x9 QFN is shown below:

Logos

Marking of logos can also be accommodated, this will reduce the available lines of text. Logo should be supplied in dxf format, please contact Alter Sales to discuss further details.

QR codes

Assembly Requests

Assembly details should be submitted in the standard template “Alter QFN Assembly Request.xlsx” accompanied by a scaled wire bonding diagram.

Packing

1st level packing is standard JEDEC trays, populated as follows

Package Size	Qty Per Tray	Array Format
4 x 4	490	14 x 35
5 x 5	490	14 x 35
6 x 6	490	14 x 35
7 x 7	260	10 x 26
8 x 8	260	10 x 26
9 x 9	260	10 x 26

2nd level packing is ESD vacuum bag.

For exceptions to these design rules or quotations contact
info@uk.altertechnology.com

Dimensions in mm unless stated

Application Note – SMT Soldering of QFN package

PCB Design Guidelines

The following are general guidelines for design of the PCB pads required to make reliable electrical and mechanical contacts to the individual terminals and exposed thermal pad of the QFN package range.

Due to the fine pitch and size of the contact pads, ensuring a good solder fillet post reflow is critical and requires correct design of the land pattern for both the QFN connections and the thermal pad. Use of IPC-SM-782 (Surface Mount Design and Land Pattern Standard) as the reference standard for the PCB layout is recommended to ensure consistent solder results.

Generally, to promote good solder fillets, the terminals pads should extend a minimum of 0.2mm away from the package centre (max 0.5mm) and also extend inward by 0.05mm from the inner edge of the QFN terminal.

To ensure that there is no solder bridging, gaps of 0.15mm between PCB solder pads (including terminal to exposed pad) should be maintained and to this end, the maximum width of the terminal pad must not exceed the maximum lead width allowed in JEDEC MO220K for lead pitches below 0.65mm.

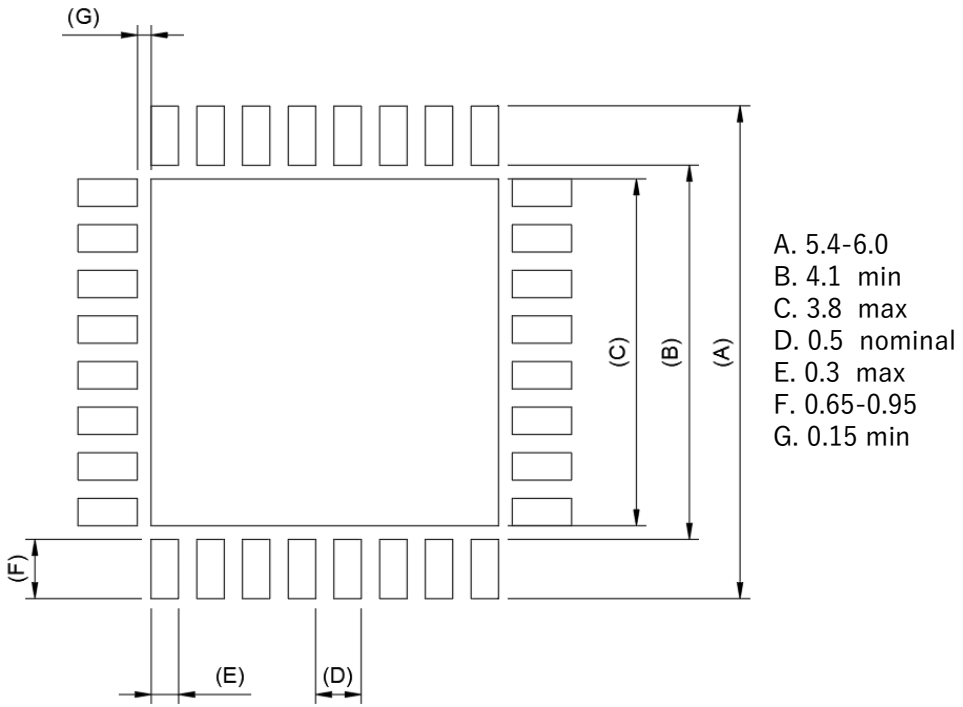
The PCB pad for soldering to the exposed pad on the underside of the QFN should also be larger than the pad itself, however the minimum solder clearance for eliminating bridging must be maintained.

Example

For a 5x5QFN 32 lead, the relevant solder pad dimensions are as follows:

Dimension	Length		Width	
QFN Terminal	0.4		0.25	
	Min	Max	Min	Max
PCB pad size	0.65	0.95	0.25	0.3
QFN exposed pad	3.5		3.5	
	Min	Max	Min	Max
PCB pad size	3.5	3.8	3.5	3.8

Based on the guidance above, a representative layout for PCB solder pads is shown for a 5 x 5 32 pin QFN, with the following key dimensions: lead pitch 0.5mm, lead length 0.4mm, lead width 0.25mm and exposed pad 3.5 x 3.5mm.

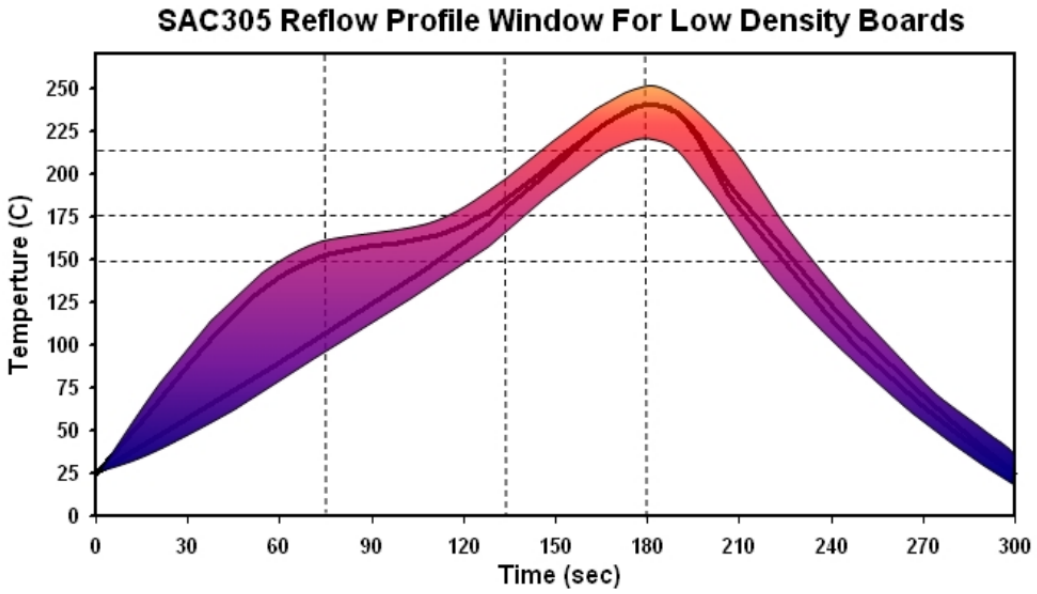


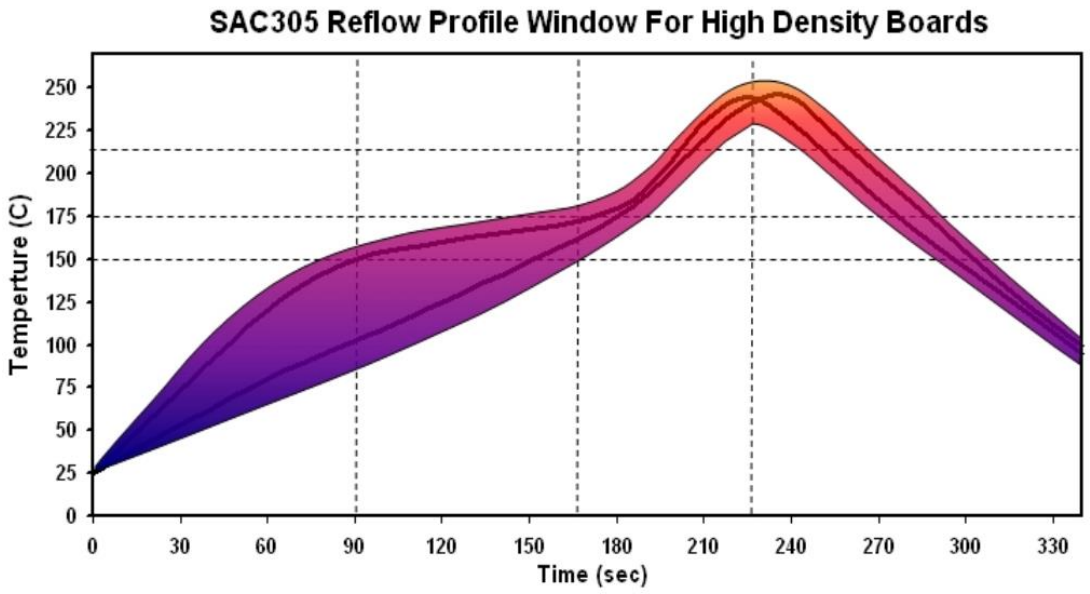
Dimensions in mm unless stated

Application Note – SMT Soldering of QFN package

Soldering Profile

Alter recommend the use of SAC 305 solder, and the profiles that are suitable for use with QFN packages are shown below (courtesy of AIM Solder).





Pre-qual Status

Initial “pre-qual” testing has been conducted on 4x4mm 24L and 9x9mm 64L

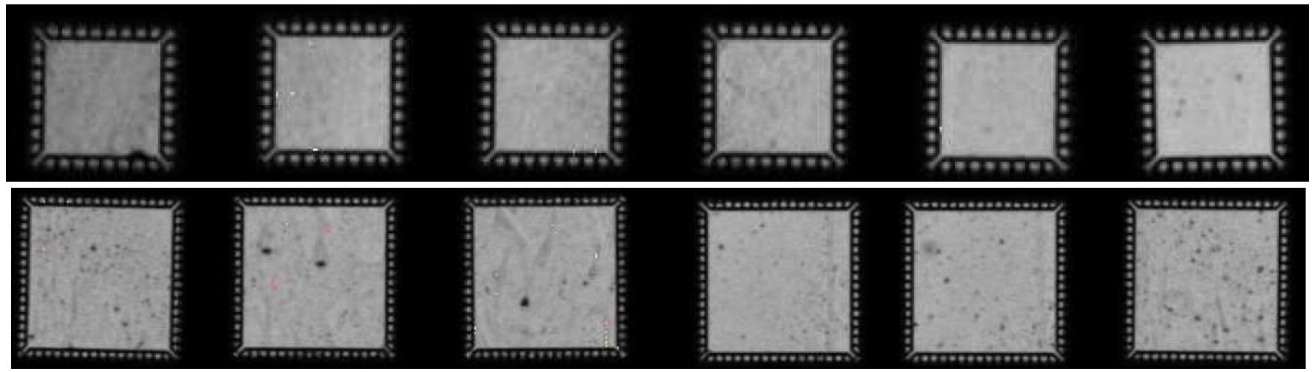
- 100 Temp Cycles -55degC to +125degC
- C-SAM
- 400 Temp Cycles -55degC to +125degC
- C-SAM
- 3 x Solder Reflow Simulation
- C-SAM

Delamination was not observed on the samples at any stage.

On this basis sales to commercial and industrial customers have commenced.

Final qualification samples have now been submitted to Alter Spain for the ESA evaluation testing.

Post TC + Reflow C-SAM

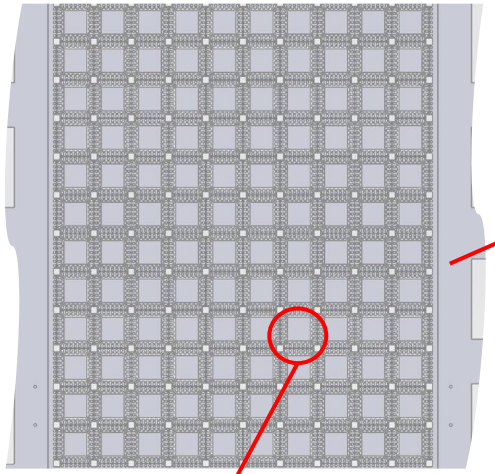


4x4mm

9x9mm

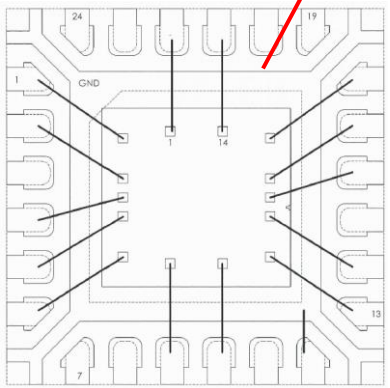
Process Highlights

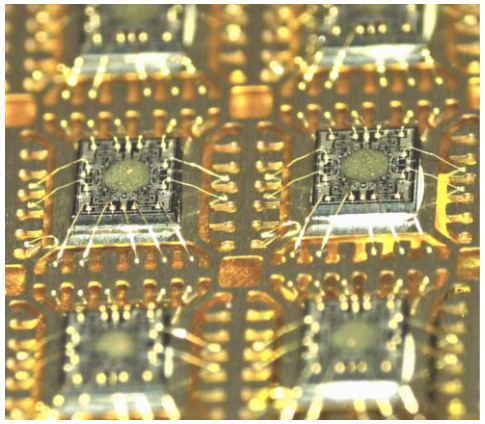
1. Array lead-frame Panel
~100's QFN positions



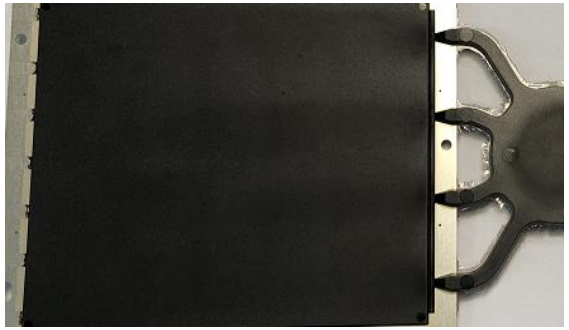
External features fixed for any design.

2. Die attach and wire bond

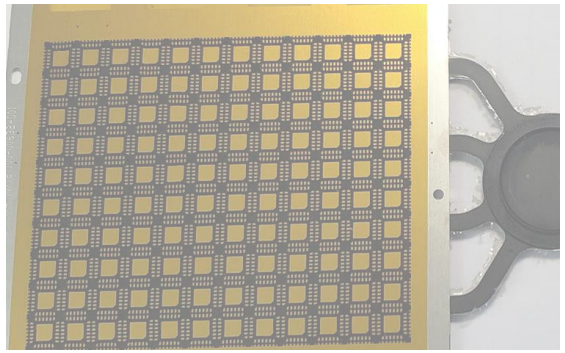




3. Block Panel Molding



Top View

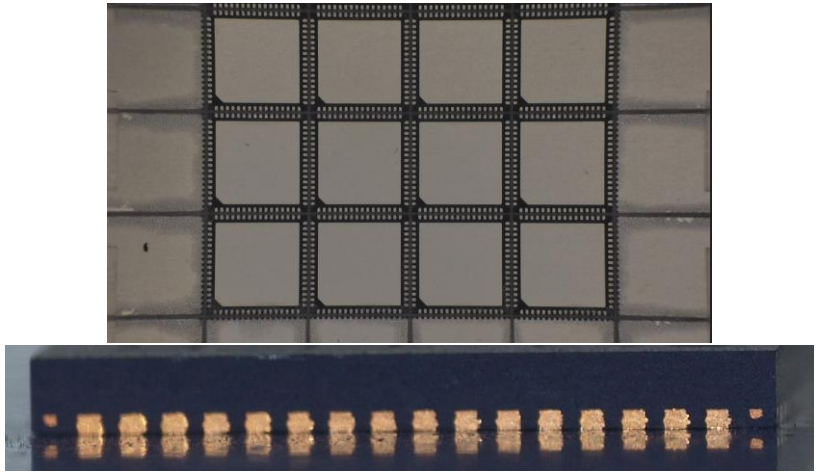


Bottom View

2 x leadframes per mold shot

4. Laser Mark Panel

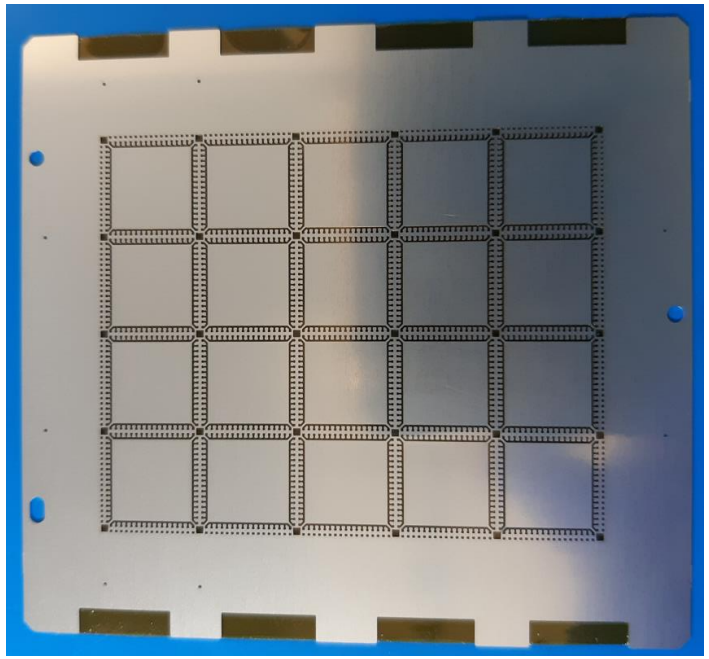
5. Saw Singulation



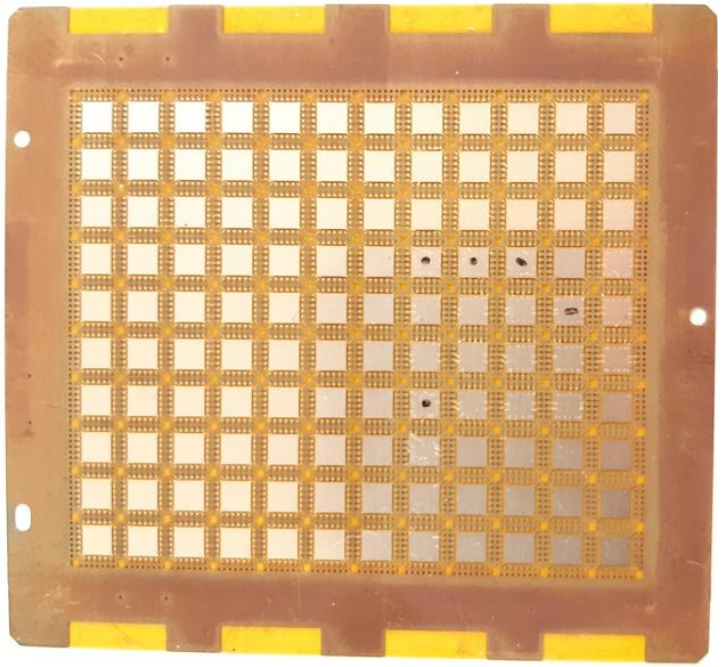
6. Load to tube or trays, transfer to Test

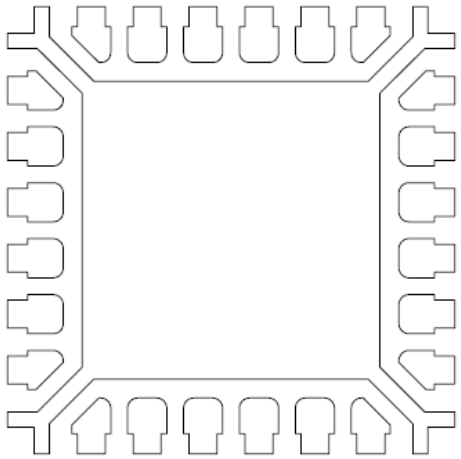
Process Highlights

Full NiPdAu plating

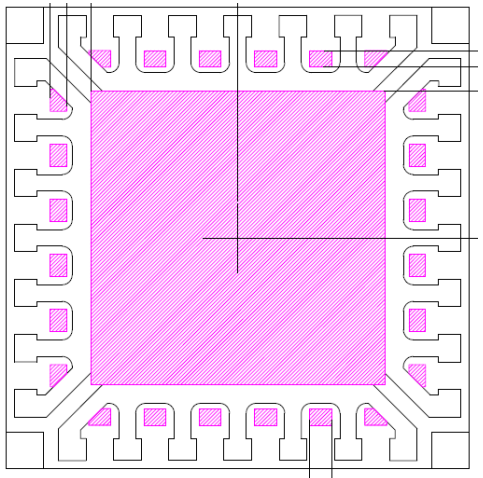


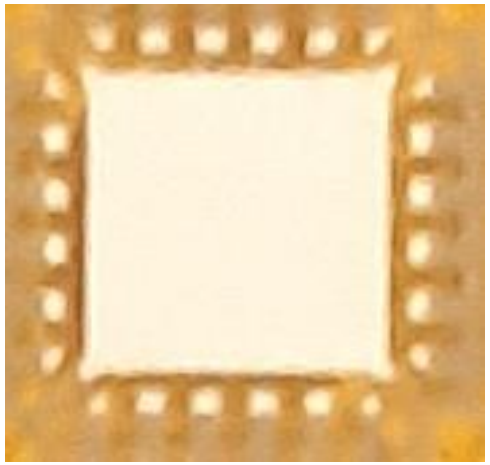
Selective NiPdAu plating



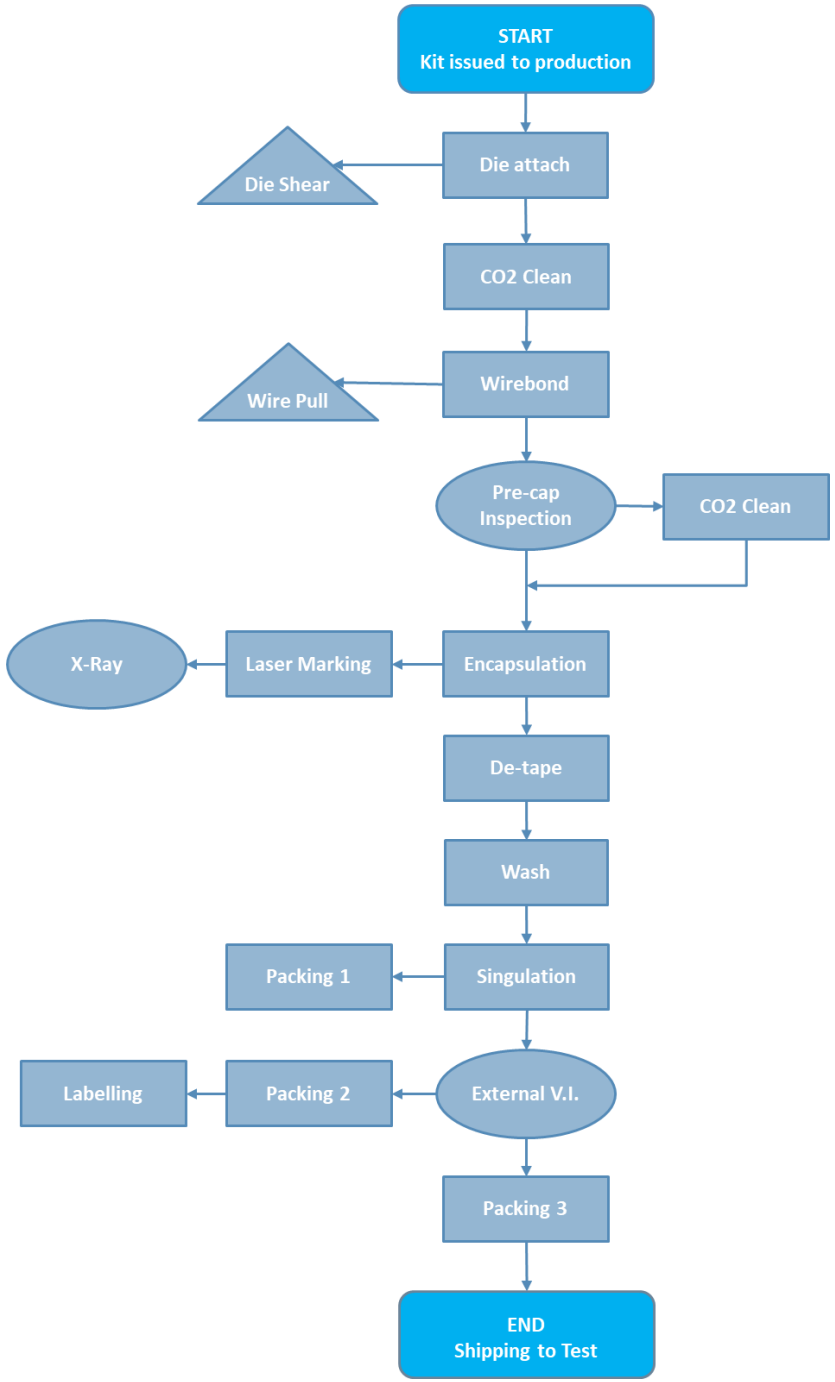


Change from full to selective NiPdAu plating for improving plastic adhesion



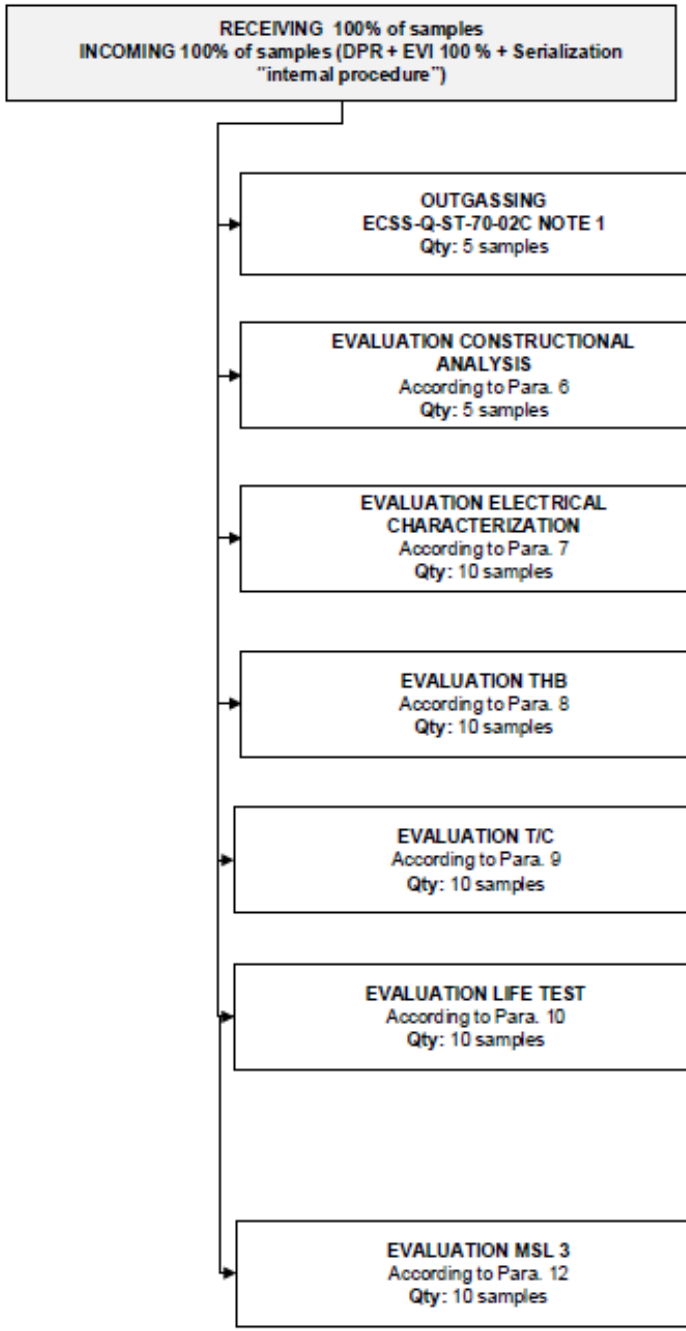


Assembly Flow Chart



Evaluation test plan – QFN4x4

ECSS-Q-ST-60-13C Class 2



Done

Done

WIP – running internal material analysis

Done

WIP – Running THB

WIP – Awaiting SAM

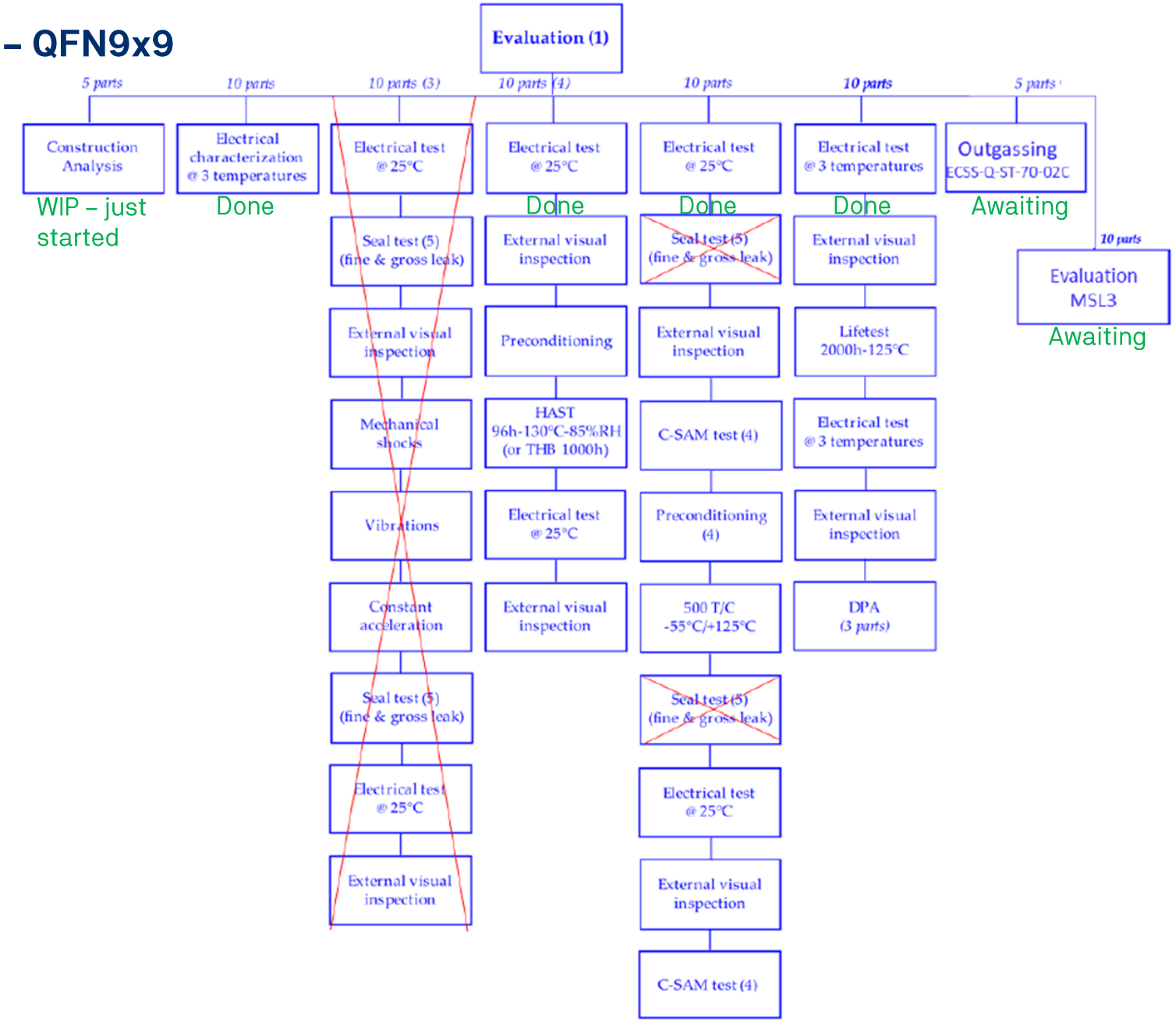
WIP – running at 2000H

Awaiting

WIP – just started

Evaluation test plan – QFN9x9

ECSS-Q-ST-60-13C Class 2



Test results QFN 4x4 – Ongoing

Incoming inspection

	QTY. INSP.	COMPLIANT	NOT COMPLIANT
INCOMING INSPECTION	**91**	**91**	**0**
EXTERNAL VISUAL INSPECTION METHOD: MIL-STD-883. METHOD 2009.14 2	91	91	0
SERIALIZATION METHOD: -	91	91	0

Outgassing

TABLE OF RESULTS FOR ECSS-Q-ST-70-02, C

SERIAL NUMBER	1	2	3	Â
TML %	0,057	0,059	0,059	**0,0583**
RML %	0,032	0,035	0,029	**0,0320**
CVCM %	0,005	0,002	IR plate	**0,0035**
RESULT	**PASS**	**PASS**	**PASS**	**PASS**

OVERALL RESULT: **ACCEPT**

Electrical characterisation

TEST	QUANTITY		
	IN	FAIL	OUT
ELECTRICAL MEASUREMENT AT ROOM TEMPERATURE METHOD: ATN-SC-903 Issue:1	10	0	10
ELECTRICAL MEASUREMENT AT HIGH TEMPERATURE METHOD: ATN-SC-903 Issue:1	10	0	10
ELECTRICAL MEASUREMENT AT LOW TEMPERATURE METHOD: ATN-SC-903 Issue:1	10	0	10

ENVIRONMENTAL CONDITIONS	
RELATIVE HUMIDITY	45±15 %
TEMPERATURE	22±3 °C

ENVIRONMENTAL CONDITIONS	
RELATIVE HUMIDITY	-
TEMPERATURE	125 °C

ENVIRONMENTAL CONDITIONS	
RELATIVE HUMIDITY	-
TEMPERATURE	-55 °C

Thank you

Any Questions?