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Thermally Enhanced Flip-Chip BGA for Space applications

Back-End R&D, STMicroelectronics

Outline

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Organic (Plastic) Package for Space

Ceramic

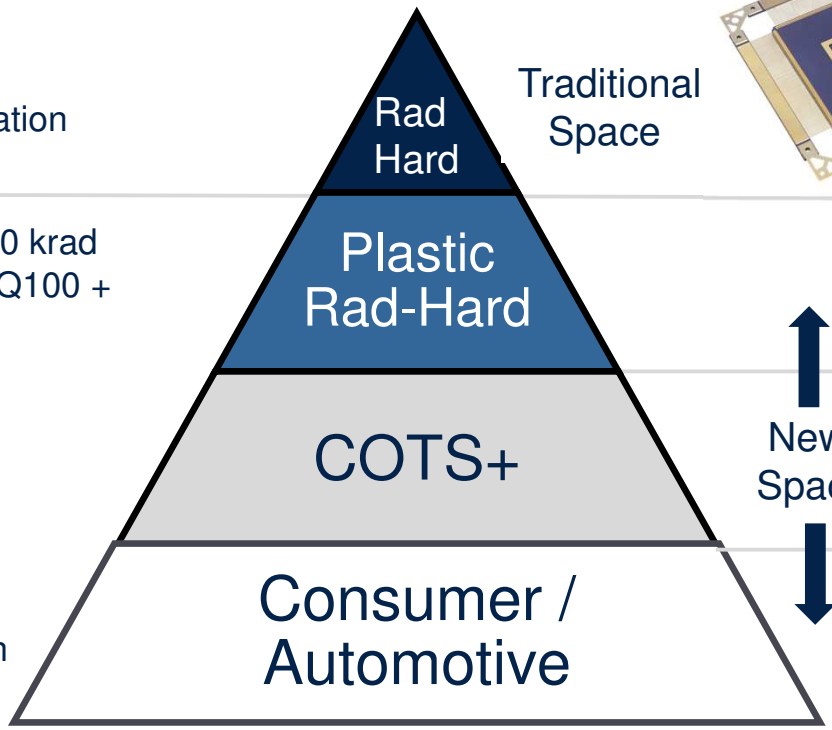
Rad-Hard: ≥ 50 Krad
ESCC / QML Qualification

Plastic

Good in radiation : ~50 krad
« According to » AECQ100 +

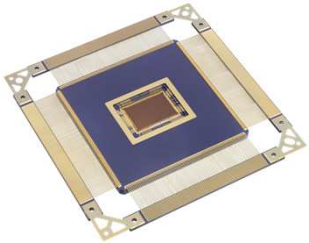
Radiation « as is »
ST Upscreen to LEO

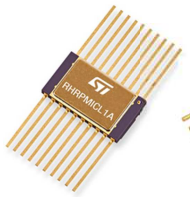
No radiation data
Standard Qualification



Traditional Space

New Space





PowerSO-20

Thermally Enhanced
Flip-Chip BGA

ASP

MOQ (unit)

10

1000

2500

5000

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Why to choose FC TE BGA ?

- *Thermal performance*
- *Electrical perf bumps vs. WireBond*
- *Number of pins / large body size*
- *Low stress assembly*

Flip Chip

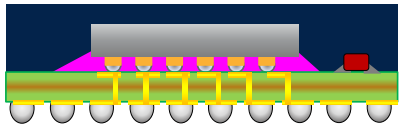
WireBond

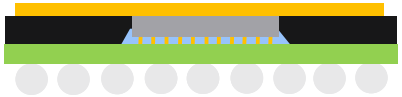
Molded BGA

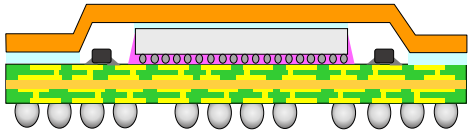
Exposed die

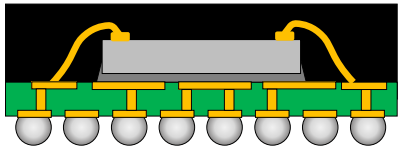
Dissipation lid

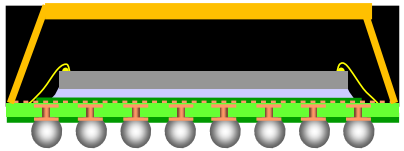
FC TE BGA











Matrix package assembly

Singulated package assembly

Thermal dissipation performance

Cost

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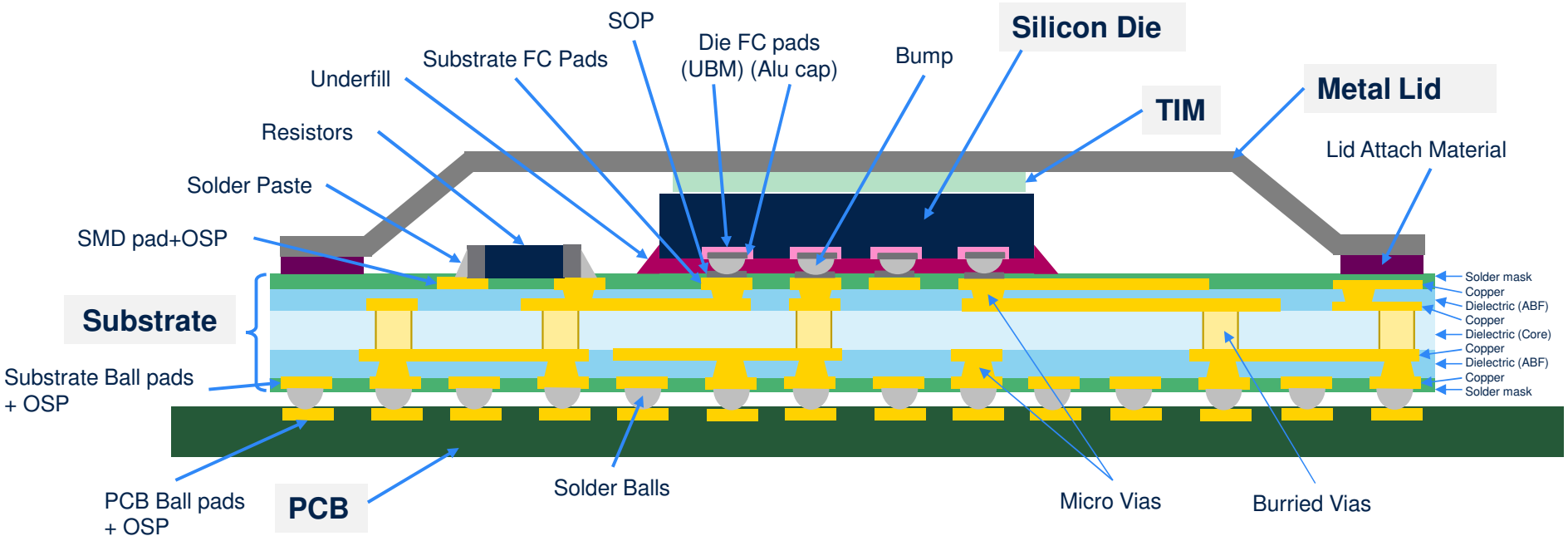
FCTEBGA – Flip Chip Thermal Enhanced Ball Grid Array



- *OSP = Organic Surface Protection = This OSP is dispensed on substrate exposed copper areas in order to avoid copper oxidation before Ball, SMD… attach*
- *SMD = Surface Mount Device = components like Capacitors, Resistors…*
- *SOP = Solder On Pad = Solder paste dispensed by screen printing or micro-balling on substrate FC pads, this is to improve FC reliability.*
- *TIM = Thermal Interface Material = this is used to conduct the heat from the die to the metal lid*
- *UBM = Under bump metallization*

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Mission Profile | Space vs. Automotive

Typical mission Profile	Automotive Grade 0	Space
Ambient temperature operating range	- 40 °C / +150 °C	- 40°C / + 105 °C
Reliability thermal cycling	- 55 °C / +150 °C 2000 cycles	- 55 °C / + 125 °C 1500 cycles
Reliability high temperature storage	+ 150 °C 2000 h + 175 °C 1000 h	+ 150 °C 2000 h
Board level - Reliability thermal cycling	- 40 °C / +125 °C 1000 to > 4000 cycles	- 55°C / + 85°C 1500 cycles
Board level - Vibrations	20 G 10 to 2000 Hz, ≥ 94 h	

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➔ **Automotive packaging knowledge re-use**

Packages challenges vs. space application

➔ Comparable to automotive MCU

Electrical Performance / Complexity

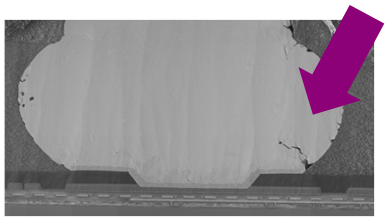
- High count of bumps from 10k to 20k
- Operating frequency from MHz to 28GHz

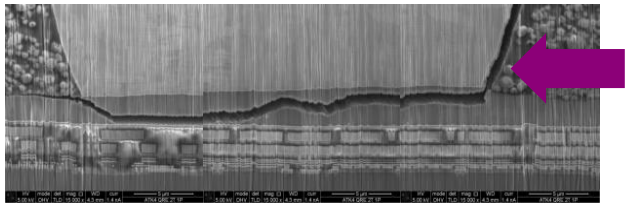
Thermal management

- Dissipation performance up to 60W/die
  - Molded package dissipation performance ~ 10 W /die
- Material selection

Reliability

- Material delamination / crack / voids
- Package warpage
- ← Board Level reliability





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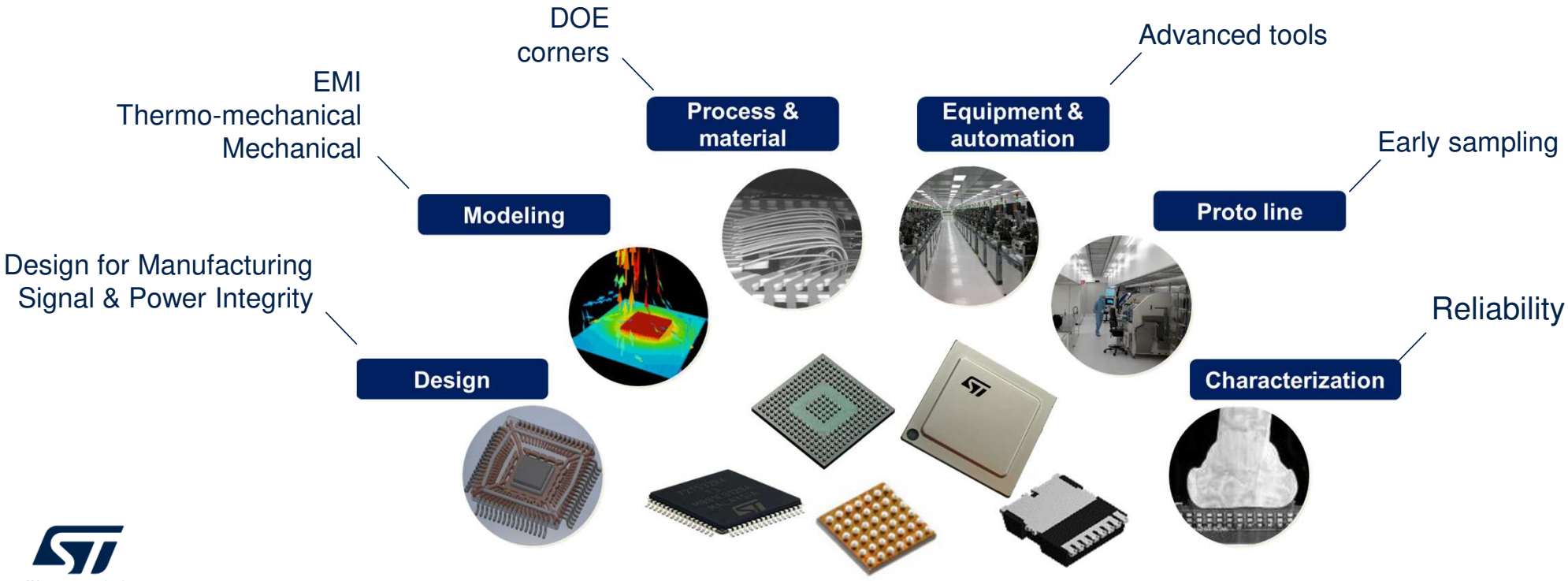
FC TE BGA : from design to production

➔ **Systematic co-design approach**

➔ **Eco-system R&D protoline – Production plants - Suppliers**



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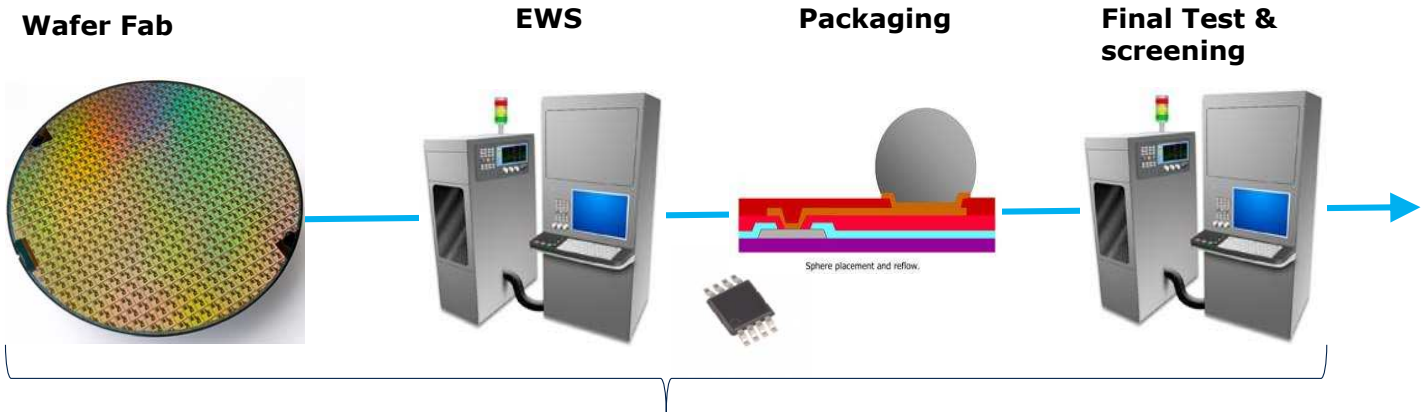
Path to production: supply chain management



ST offers full supply chain management:
from package technology selection, to package design, manufacturing, qualification and production,
based on ST and OSAT assembly and test plants

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Multiple sources integrated supply chain control

Integrated internal manufacturing and R&D for differentiated products
Partnership with foundry and OSAT for standard technologies and package
Partnership with key substrate vendors for advance technologies and secured supply chain

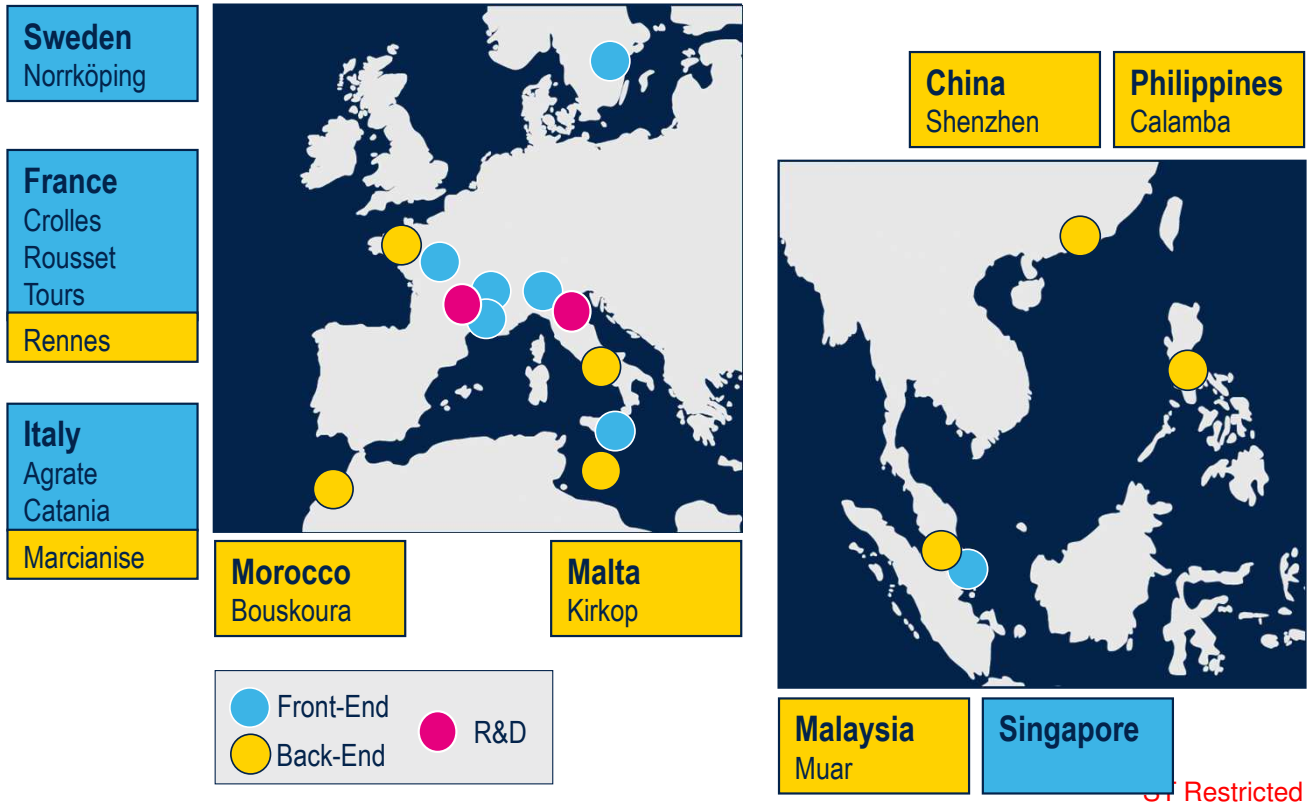
ST facilities cover the full semiconductor manufacturing process.

The manufacturing phase of an Integrated Circuit (IC) covers two major steps:

- Wafer fabrication, known as **front-end** manufacturing of the silicon chip.
- Chip assembly, known as **back-end** process of packaging.

They include two test steps:
wafer probing and **final test**.

R&D – plant ecosystem



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FC TE BGA vs. ST Our strategic objectives

Automotive

Lead in **car electrification**

Lead in **car digitalization**

Industrial

Lead in **embedded processing**

Lead in **Power & Energy Management**

Lead in **Sensors**

Accelerate in **Analog**

Personal electronics

Lead in **selected** high-volume **smartphone** applications with differentiated products or custom solutions

Leverage **broad portfolio** to address high-volume applications

Communications Equipment, Computers & Peripherals

Address **selected** high-volume **applications** with differentiated products or custom solutions

Leverage **broad portfolio** to address high-volume applications

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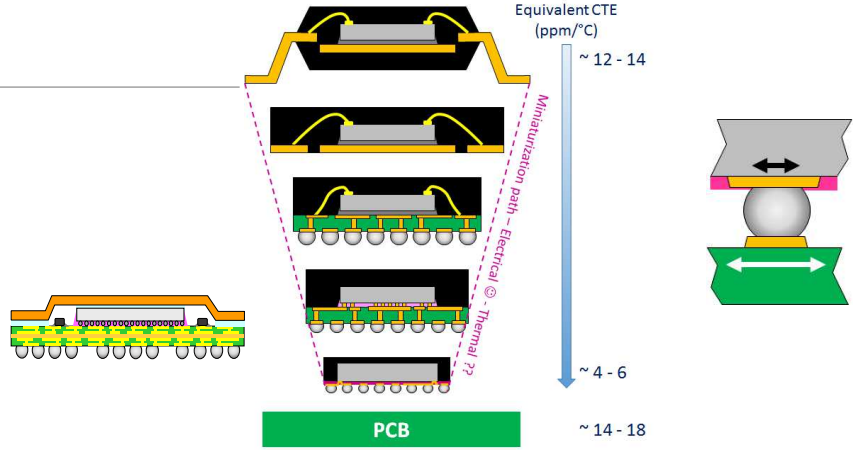
Some R&D paths

Material

Thermal Interfaces Material
Substrate properties (CTE), thermal dissipation

Process

Thin & uniform TIM layers thickness
Thermal budget for Substate warpage



Package architecture

Multi-chip integration

2.1D (FO) multi-dice

2.5D multi-dice

Thermo-mechanical & Thermal Modeling

Correlation with measurement
Predictability of aging

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Conclusion

- The **Thermally Enhanced Flip-Chip BGA** is a packaging technology developed to meet the demanding thermal requirements, and which is widely used for automotive products and now for space applications.

- This technology enables **high-reliability** and **high-thermal performance** in electronic devices, by utilizing co-design, advanced materials and manufacturing processes.

- ST leverage on its packaging experience & **Europe infrastructure** to develop FC TE BGA for Space applications

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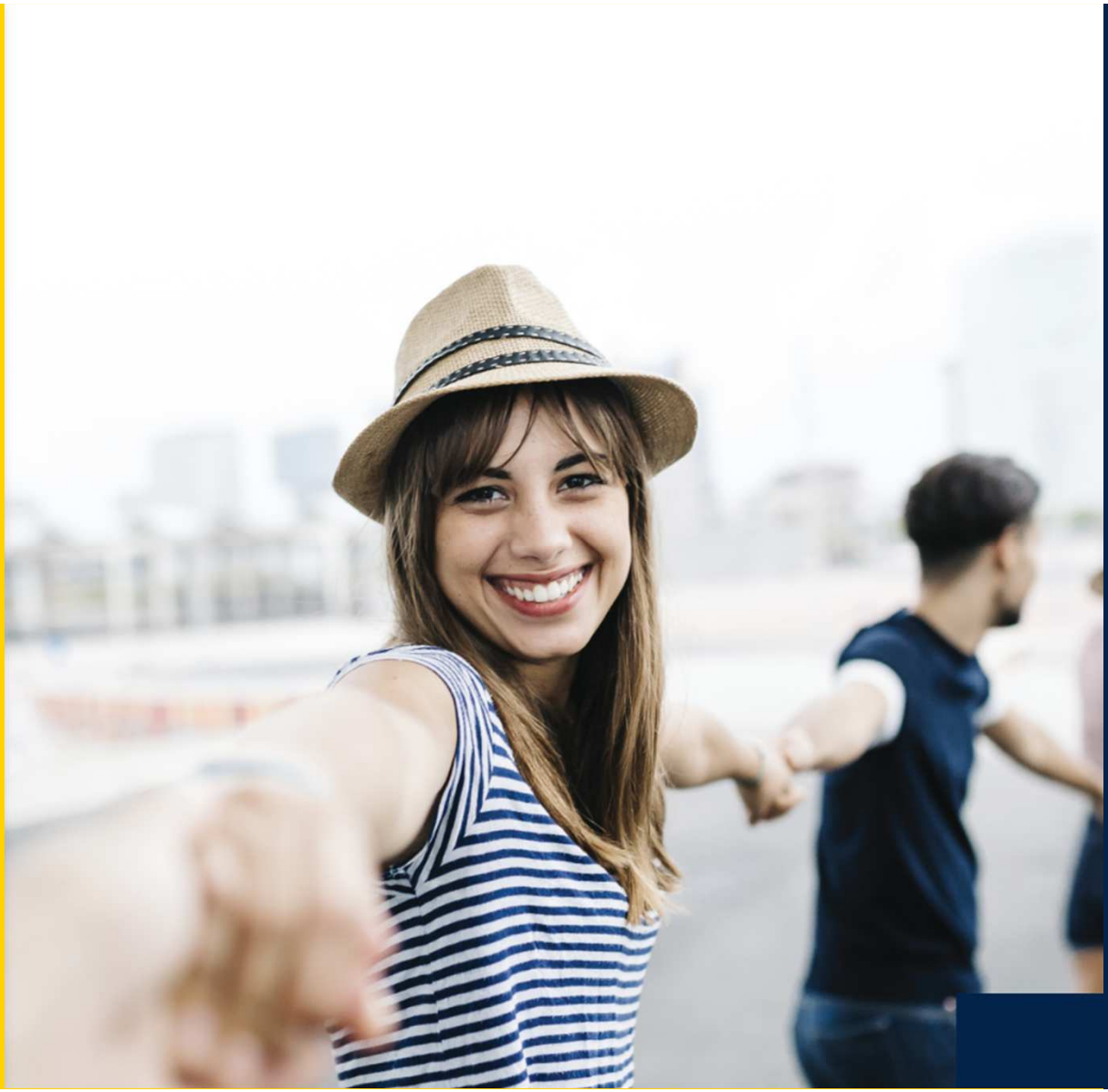

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