ECSS-Q-ST-70-61C

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ECSS-Q-ST-70-61C

The new standard merges the following Standards with some modification implemented:

ECSS-Q-ST-70-07C
ECSS-Q-ST-70-08C
ECSS-Q-ST-70-38C rev.1

ECSS

ECSS-Q-ST-70-61C
8 April 2022

Change log

ECSS-Q-ST-70-61C 8 April 2022	First issue This new ECSS Standard was created by merging and updating the content of the following three standards: • ECSS-Q-ST-70-07C "Verification and approval of automatic machine wave soldering" • ECSS-Q-ST-70-08C "Manual soldering of high-reliability electrical connections" • ECSS-Q-ST-70-38C Rev.1 "High-reliability soldering for surface-mount and mixed technology" The intention of this completely new standard was to optimize the structure of the document, following the chronological order of assembly processes and introducing criterion for new technologies that were not covered by the three standards now superseded by this new standard.

ECSS-Q-ST-70-61C

Working Group was established in 2017 with Kick off meeting Mid 2017.

25 Meetings.

Companies participating the WG: Airbus DS, ArianeGroup, Sodern, Hytek, SPUR Electron Ltd, LND SPA, Thales Alenia Space, OHB, Ruag, CNES, ESA

DRD from public review(s): 2032

ECSS-Q-ST-70-61C

In coherence with the previous soldering standards the following statement is made in the scope:

" The mounting and supporting of components, terminals and conductors specified in this standard applies only to assemblies designed to continuously operate over the mission within the temperature limits of -55 ° C to +85 ° C at solder joint level. "

Furthermore, is specified that:

" This standard does not cover lead-free soldering and associated requirements.

This Standard does not cover pressfit connectors due to the possible damage in the PCB that is not evaluated within this test requirement. "

Main changes introduced

Environmental conditions (5.2):

The use of a clean room for soldering is now mandatory. The minimum cleanliness class accepted is ISO 8.2

Environmental conditions limits aligned with the ECSS-QST-70-01C HR% 55 +/-10

Equipment and tools (5.5)

Requirements for different types of wave soldering equipment

Requirements for depanelization tools

Recommendations for Automatic inspection systems

Requirements for X-ray inspection systems

Main changes introduced

Materials (6.0):

Soldering on gold finished PCB is now allowed :

ECSS-Q-ST-70-61_1510182

b. Soldering to gold finish, ENIG, ENIPIG, ENEPIG, qualified according ECSS-Q-ST-70-60, with tin lead may be performed only when the gold finish is thinner than 0,1 µm and is approved by the Approval Authority.

More detailed requirements for component selection, use and components leads finish:

ECSS-Q-ST-70-61_1510192

h. The plating of the component lead shall be such that the lead forming does not induce any crack in the plating.

ECSS-Q-ST-70-61_1510194

j. Components to be mounted shall be designed for and be capable of withstanding the soldering temperatures of the particular process being used for fabrication of the assembly.

NOTE In case surface mounted components are soldered on both sides of the PCB, double reflow processes can be applied.

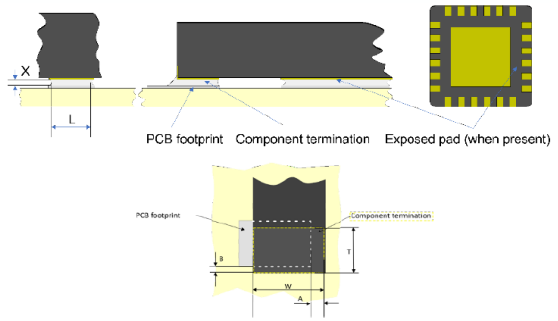
ECSS-Q-ST-70-61_1510196

b. When moisture sensitive components are used, bake out shall be performed in accordance with clause 7.4.

Main changes introduced

Assembly to Terminals and to PCB (10.0)

Requirements for a larger range of packages have been added now including QFN, Stacked modules ..



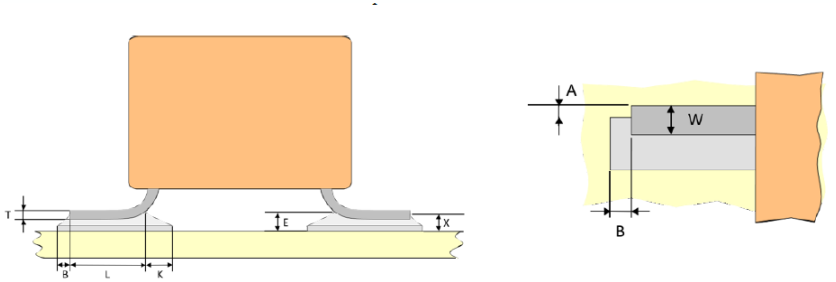
ECSS-Q-ST-70-61_1510655

Figure 10-12 Mounting of QFN

ECSS-Q-ST-70-61_1510656

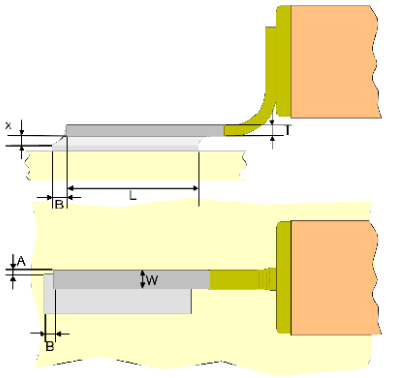
Table 10-9: Dimensional and solder fillet for QFN components

Parameter	Dimension	Dimension limits
Maximum side overhang	A	Not permitted
End overhang	B	Not permitted
Minimum termination contact length	L	Entire termination of component
Solder Stand-off (elevation)	X	Present
Solder fillet height	H	In compliance with verification results
Minimum fillet width	W-A	100% × W
Maximum tilt limit	in accordance with requirement 10.2.2f	
Termination width	W	
Termination length	T	



ECSS-Q-ST-70-61_1510673

Figure 10-16: Mounting of stacked module components with leads protruding vertically from bottom



ECSS-Q-ST-70-61_1510669

Figure 10-15: Mounting of components without stress relief

Main changes introduced

Cleanliness verification (11.1):

Introduction of Surface Insulation Resistance test (SIR) for the assessment of the cleaning process as part of the verification test activity.

ECSS-Q-ST-70-61_1510718

a. SIR test shall be implemented at first verification and after any process changes according to Table 13-1 or due to the introduction of components for which cleanliness testing is considered worst case and not covered by previous analysis.

Change in the pass-fail criteria for the Sodium Chloride ionic contamination equivalent test.

Limit has been reduced to 0,70 µg/cm2 (used to be 1.56 µg/cm2)

ECSS-Q-ST-70-61_1510726

e. The cleanliness test values shall be as follows:

1. Starting resistivity: greater than 20×10^6 Ω cm.
2. Ending value: The sodium chloride (NaCl) ionic contaminants equivalence value be less than 0,70 µg/cm^2 of PCB surface area.

Main changes introduced

Repair and rework (10.5)

Dedicated paragraph introduced addressing some general requirements for repair and rework

ECSS-Q-ST-70-61_1510693

i. Type II ceramic chip capacitors shall not be reworked.

ECSS-Q-ST-70-61_1510694

j. Wiring of chip capacitors type II soldered on its footprint as identified in the ECSS-Q-ST-70-28C shall not be performed due to possible thermal shock.

ECSS-Q-ST-70-61_1510695

k. Wiring of a chip capacitor type II soldered on its footprint may be acceptable provided that the assembly of the capacitor and the wiring is done in a single operation.

ECSS-Q-ST-70-61_1510696

l. Wiring a chip capacitor type II bonded on PCB as described in clause I.3.7 of ECSS-Q-ST-70-28 shall not be performed.

ECSS-Q-ST-70-61_1510697

m. Ceramic chip capacitors with flexible terminations shall not be reworked.

ECSS-Q-ST-70-61_1510698

n. Ceramic chip capacitors with flexible terminations may be reworked providing the use of an appropriate procedure that avoids any thermal shock and is successfully verified according to clause 13 and approved by Approval Authority.

ECSS-Q-ST-70-61_1510699

o. Wiring a tantalum capacitor bonded on PCB as described in clause I.3.7 of ECSS-Q-ST-70-28 shall not be performed.

Main changes introduced

Verification procedure (13.0):

The verification approach for wave soldering processes has been aligned with what done for Surface mount technology.

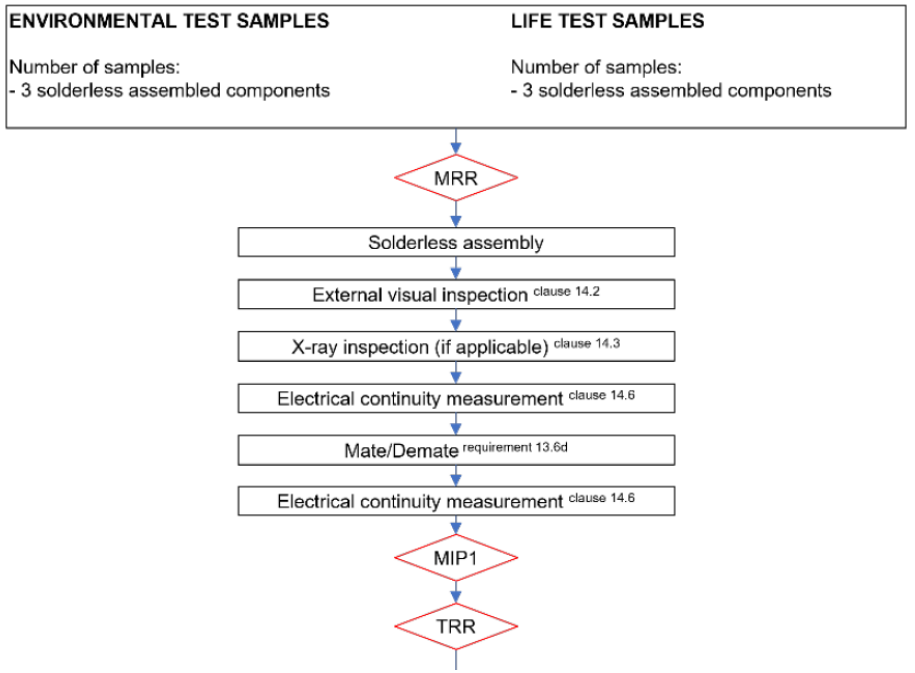
The difference in requirements for thermal cycling between Surface Mount Technology (500 thermal cycles) and Through Hole Technology (200 thermal cycles) has been maintained

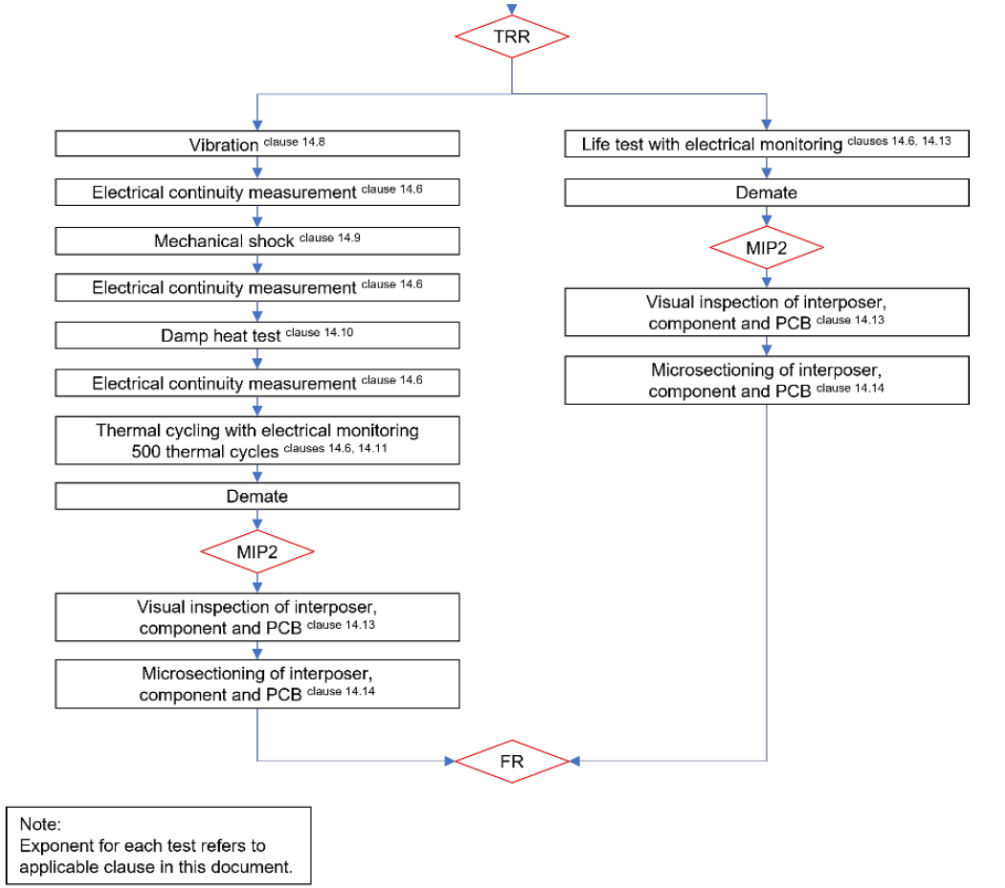
Verification flow for Solderless Connections has been defined.

Reminder: the **standard does not** cover the use of Pressfit

Main changes introduced

Solderless verification





ECSS-Q-ST-70-61_1510921

Figure 13-5: Verification procedure for solderless technology

Main changes introduced

Step thermal cycles added for Assembly sensitive parts 14.12

Chips capacitors type 2, SMD packages (SMD0.22, SMD0.5), LCCs, Ceramic QFN,...

14.12 Temperature cycling test with reduced temperature range

ECSS-Q-ST-70-61_1511001

a. Temperature cycling with reduced temperature range shall be performed as part of the special verification programme in accordance with requirements in clause 13.5.

ECSS-Q-ST-70-61_1511002

b. The stresses during temperature cycling may be reduced by modification of the temperature cycling conditions as follows:

1. Decreasing the thermal range during temperature cycling by increasing the minimum temperature from the nominal one, or
2. decreasing the thermal range during temperature cycling by decreasing the maximum temperature from the nominal one, or
3. decreasing the temperature cycling gradient from the nominal one, or
4. any combination of 1 to 3 above.

NOTE The modifications refer to changes from the nominal temperature cycling conditions as described in requirements 14.11d and 14.11f.

ECSS-Q-ST-70-61_1511003

c. The temperature cycling may be performed in several steps, with different conditions in the different steps.

NOTE A typical stepwise temperature cycling test is to perform the cycling in 2 steps as follows:

- Step 1: Temperature range tailored so that the minimum and maximum temperature on board level during the on-ground qualification conditions are covered including the minimum and maximum temperatures during cold start, non-operating and operating, as required for the intended mission. Number of cycles in this step tailored such that the on-ground qualification conditions are covered at least with a safety margin of 2.
  The lower temperatures often result in largest stresses, and it is therefore good practice to cover cold start conditions in this first step so that the number of cycles at the larger temperature range are minimized.

  Example: 20 cycles between -40°C/+85°C with a gradient of 2°C/min and a dwell time of 15 minutes corresponds to 15,5 cycles of -55°C/+100°C with a gradient of 10°C/min as calculated with the equation in requirement 14.12g.
- Step 2: Temperature range tailored so that the minimum and maximum temperature on board level during the in-orbit conditions are covered. Number of cycles in this step tailored such that steps 1 and 2 in total correspond to the nominal temperature cycling range that is required for the type of components being verified, typically 500 cycles, when re-calculated with the modified Coffin-Manson (Norris-Landzberg) equation.

  Example: 981 cycles between -10/+100°C with a gradient of 10°C/min or slightly lower and 15 minutes of dwell time. 981 such cycles correspond to 484,8 cycles -55/+100°C with gradient ~10°C/min, as calculated with the equation in requirement 14.12g.

  Thus the cycling during step 1 and step 2 in total covers the full 500 cycles (15,5 + 484,8 = 500,3) required for surface mounted components as required by requirement 13.2.1cc.

NOTE 2 The reason behind dividing the temperature cycling in different steps is to decrease the risk of thermally overstressing the assembly while not prolonging the schedule more than necessary.

NOTE 3 It is recommended to perform the tailoring of the temperature cycling such that the envelope of all intended mission requirements can be covered. A case-by-case trade-off between cost, schedule and risk is though often needed.

ECSS-Q-ST-70-61_1511004

d. The total number of cycles shall be tailored such that all the steps in total correspond to the nominal number of thermal cycles with nominal temperature cycling range that is required for the type of components being verified.

ECSS-Q-ST-70-61_1511005

e. The temperature conditions during temperature cycling shall cover the minimum and maximum board temperatures seen by the component in the intended mission profile including on ground qualification testing.

ECSS-Q-ST-70-61_1511006

f. The corresponding number of thermal cycles for the on-ground qualification and in-orbit environment shall be covered at least with a safety margin of 2.

NOTE Temperature on board level are taken into account during all the on-ground qualification conditions including the minimum and maximum temperatures during cold start, non-operating and operating, as required for the intended missions.

ECSS-Q-ST-70-61_1511007

Main changes introduced

Model to calculate ECSS equivalent number of thermal cycles added (14.12)

Tailoring of the thermal cycling for step soldering

ECSS-Q-ST-70-61_1511007

g. The modified Coffin-Manson (Norris-Landzberg) equation used for the calculation of the equivalent thermal cycles shall be the following:

$$AF = \left[\frac{\Delta T_{lab}}{\Delta T_{field}}\right]^{1.9} \cdot \left(\frac{f_{field}}{f_{lab}}\right)^{1/3} \cdot exp\left(1414 \cdot \left\{\frac{1}{T_{max\_field}} - \frac{1}{T_{max\_lab}}\right\}\right)$$

where:

AF = Acceleration factor between lab and field conditions

T_{max} and T_{min} = Maximum and minimum temperatures [Kelvin]

ΔT = Temperature difference between T_{max} and T_{min}

f = Frequency of the cycling when considering each plateau and the gradients [cycles/24h]

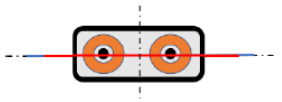
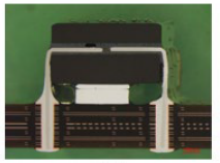
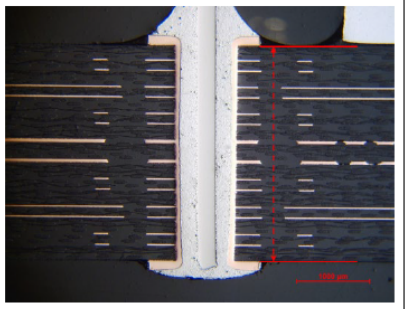
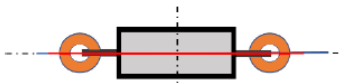
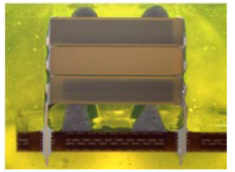
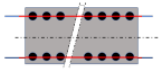
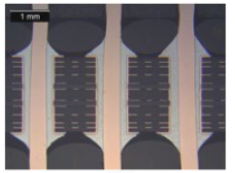
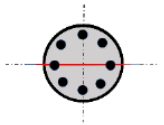
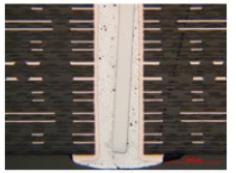
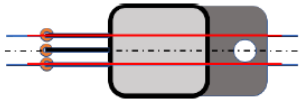
NOTE The coefficients specified are valid for soldering with SnPb solder only.

Main changes introduced

Microsectioning pass fail criteria for THT at completion of environmental test campaign

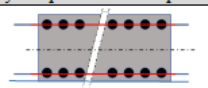
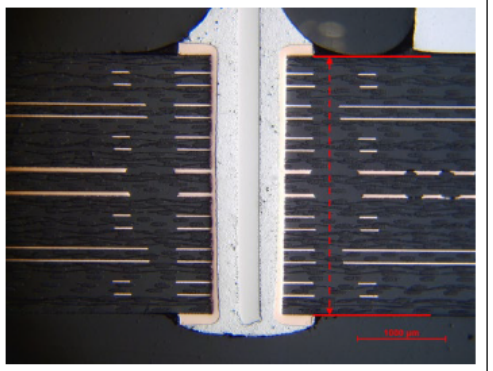
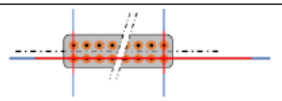
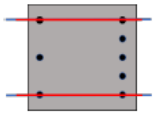
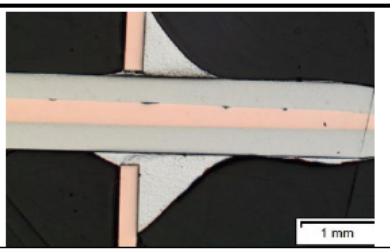
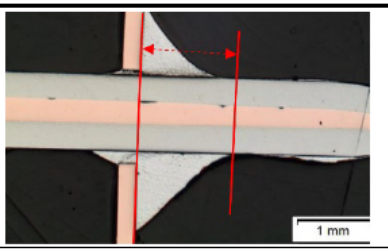
ECSS-Q-ST-70-61_1511044

Table 14-5: Component microsection location and acceptance criteria

Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
Radial component	CKR capacitors		 x20		The total sum of cracks in the solder joint is less than 25% of critical zone length
Axial components	CH capacitors CNC capacitors RWR resistors		 x25		
Stacked capacitors	-	 1 component is necessary: - parallel to the component axis for repair process on both sides	 x50		
TO package component	TO39	 Microsection in the largest distance between two leads	 x50		
TO package component with metal tab	TO254	 This package generally contains BeO that can be considered as hazardous for microsectioning. The microsectioning plane might need to be redefined after discussion with the microsectioning laboratory and asses possible health and safety issues.			

Main changes introduced

Microsectioning pass fail criteria for THT at completion of environmental test campaign

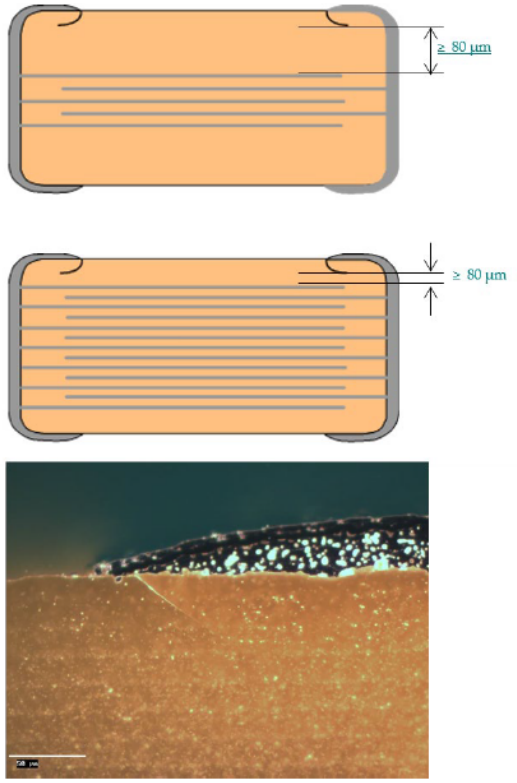
Component type	Example component	Cross section planes	Example of views at min and max magnification	Critical Zone definition	Acceptance criteria
		Terminal to cross section Symmetry axis Cross section plane		red-dotted line indicates critical zone	
Images in the table are informative examples only. Requirements are specified in text.					
Dual in Line Package (DIL or DIP)	Side brazed DIP>24 pins	 1 component is necessary: - parallel to the component axis for repair process on both sides	-		The total sum of cracks in the solder joint is less than 25% of critical zone length
Connectors		 2 components are necessary: - perpendicular to component axis for nominal assembly - parallel to component axis for repair process	-		
Radial magnetics	1553 transformers		-		
Sculptured flexible		-			No crack in the solder joint on the solder side at completion of the test.

Main changes introduced

Pass fail criteria for assessment of cracks in ceramic capacitors (14.15.4)

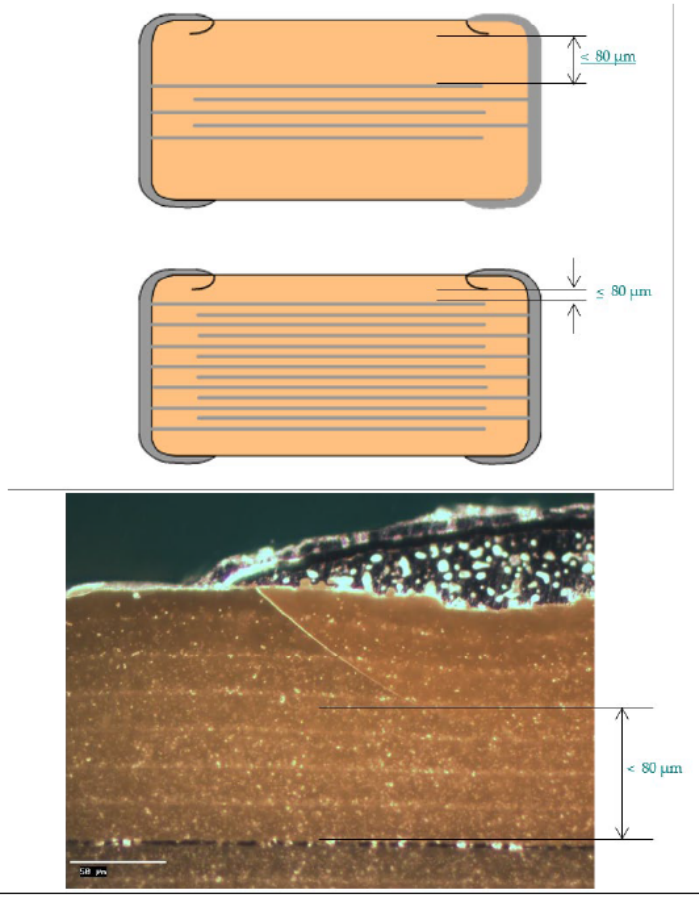
ECSS-Q-ST-70-61_1511047

Table 14-6: Acceptance criteria for internal defects in ceramic chip capacitors after microsectioning

Type of defect	Location	Case	Figure	Additional note See also notes to 14.15.4a	Acceptance criteria
Crack in solder joint	N/A	N/A	N/A	N/A	See clause 14.15.3 and Table 14-5.
Crack in ceramic	Bottom terminations	N/A	N/A	Due to the different root causes the repeatability of bottom side ceramic cracks are low.	No cracks in the ceramic on the bottom termination.
	Top terminations	Case 1a: Crack curving towards the termination on same side and remaining cover plate thickness ≥ 80µm		Example: Assembly verified component has minimum 100 µm cover plate as received and a ceramic crack which reduces the insulation distance with 15 µm, i.e. 85 µm remaining insulation which is acceptable. This would in addition be acceptable justification for all chip capacitors of the same type, provided they have minimum 95 µm cover plate as received at all 4 corners.	Crack is curving towards the termination on same side. AND No cracks in the ceramic with less than 80 µm remaining insulation to first opposite electrode. AND Assessment is made based on the longest crack projected on all 4 corners of the component. AND In case of top side ceramic crack, project specific request for deviation is submitted with assessment made on the longest crack projected on the flight batch of component which is intended to be used.

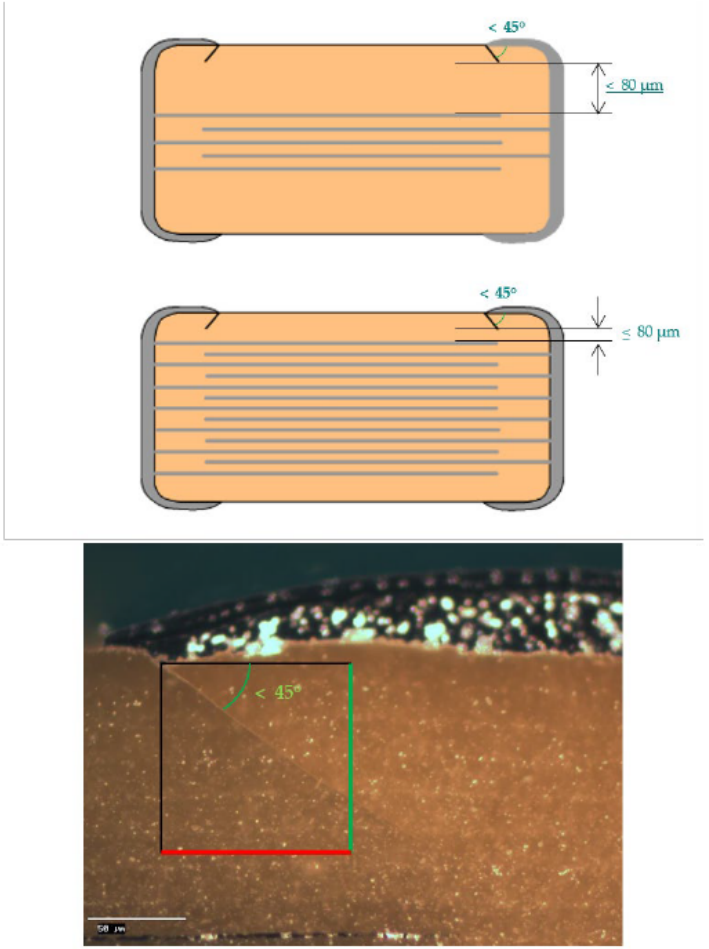
Main changes introduced

Pass fail criteria for assessment of cracks in ceramic capacitors (14.15.4)

Type of defect	Location	Case	Figure	Additional note See also notes to 14.15.4a	Acceptance criteria
Crack in ceramic	Top terminations	Case 1b: Crack curving towards the termination on same side and remaining cover plate thickness < 80µm		The review of ceramic cracks is assessed by projecting the worst crack seen on all 4 corners of the component and also by comparing it to the flight batch of the component. It is also good practice to compare the temperature cycling during verification and in the mission in which the component is intended to be used.	Not acceptable. May be accepted by project based on project specific request for deviation.

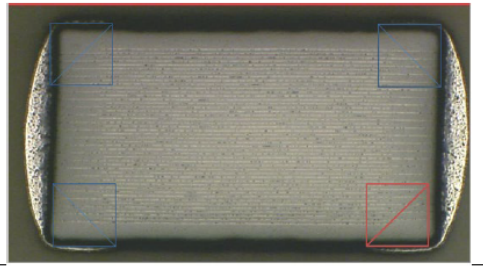
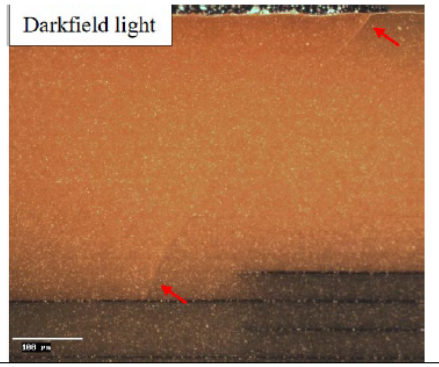
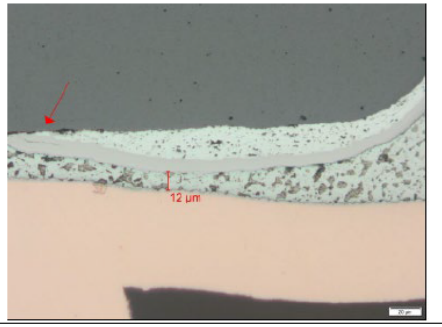
Main changes introduced

Pass fail criteria for assessment of cracks in ceramic capacitors (14.15.4)

Type of defect	Location	Case	Figure	Additional note See also notes to 14.15.4a	Acceptance criteria
Crack in ceramic	Top terminations	Case 2a: Straight crack with ≤45° angle to electrode plane and no projected crossing of opposite electrodes		It is good practice to draw a quadrat from the root of the ceramic crack to assess the crack angle. See also Case 1a for an example of calculation of allowed crack length for a different component value than was verified.	Crack has maximum 45° angle to electrode plane. AND Minimum 80 µm remaining insulation to first opposite electrode from end of crack. AND The tangent of the crack does not cross any opposite electrode. AND Assessment is made based on the longest crack projected on all 4 corners of the component. AND In case of top side ceramic crack, project specific request for deviation is submitted with assessment made on the longest crack projected on the flight batch of component which is intended to be used.

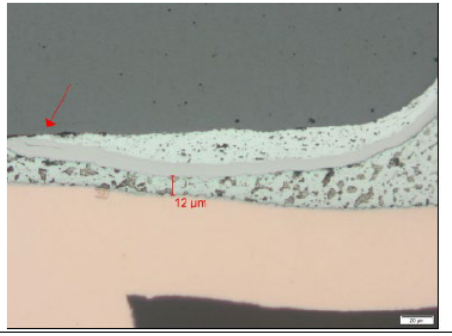
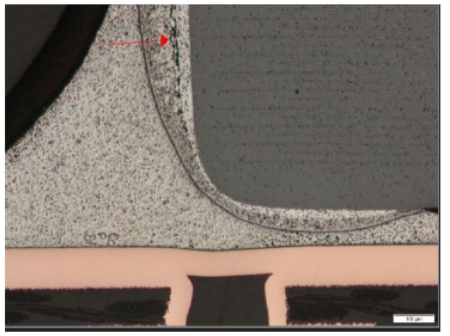
Main changes introduced

Pass fail criteria for assessment of cracks in ceramic capacitors (14.15.4)

Type of defect	Location	Case	Figure	Additional note See also notes to 14.15.4a	Acceptance criteria
Crack in ceramic	Top terminations	Case 2b: Straight crack with ≤45° angle to electrode plane and projected crossing of opposite electrodes		The review of ceramic cracks is assessed by projecting the worst crack seen on all 4 corners of the component and also by comparing it to the flight batch of the component. It is also good practice to compare the temperature cycling during verification and in the mission in which the component is intended to be used.	Not acceptable. May be accepted by project based on project specific request for deviation.
Crack in ceramic	Top terminations	Case 3: Straight crack with >45° angle to electrode plane		The review of ceramic cracks is assessed by projecting the worst crack seen on all 4 corners of the component and also by comparing it to the flight batch of the component. It is also good practice to compare the temperature cycling during verification and in the mission in which the component is intended to be used.	Not acceptable. May be accepted by project based on project specific request for deviation.
Delamination	Any termination	Chip capacitors size ≥1210		The delamination can have an impact on the size of the cracks in the solder joint as they provide stress relief.	No delamination larger than 130 µm. AND Successful assembly verification results without any delamination for at least one sample.

Main changes introduced

Pass fail criteria for assessment of cracks in ceramic capacitors (14.15.4)

Type of defect	Location	Case	Figure	Additional note See also notes to 14.15.4a	Acceptance criteria
		Chip capacitors size <1210		N/A	Not acceptable. May be accepted by project based on project specific request for deviation.
		Chip capacitors with flexible terminations		The risk of delamination in the vertical part of the flexible polymer layer can be reduced by the decreasing the solder height.	Not acceptable. May be accepted by project based on project specific request for deviation.

Thank You for your attention

Any questions ?