FRONTGRADE Gaisler

# GR765 & GR7xV

## Rad-Hard RISC-V multi-core processors

**European Space Components Conference**

ESCCON 2023

**Francisco Hernández Suárez**

Supply Chain

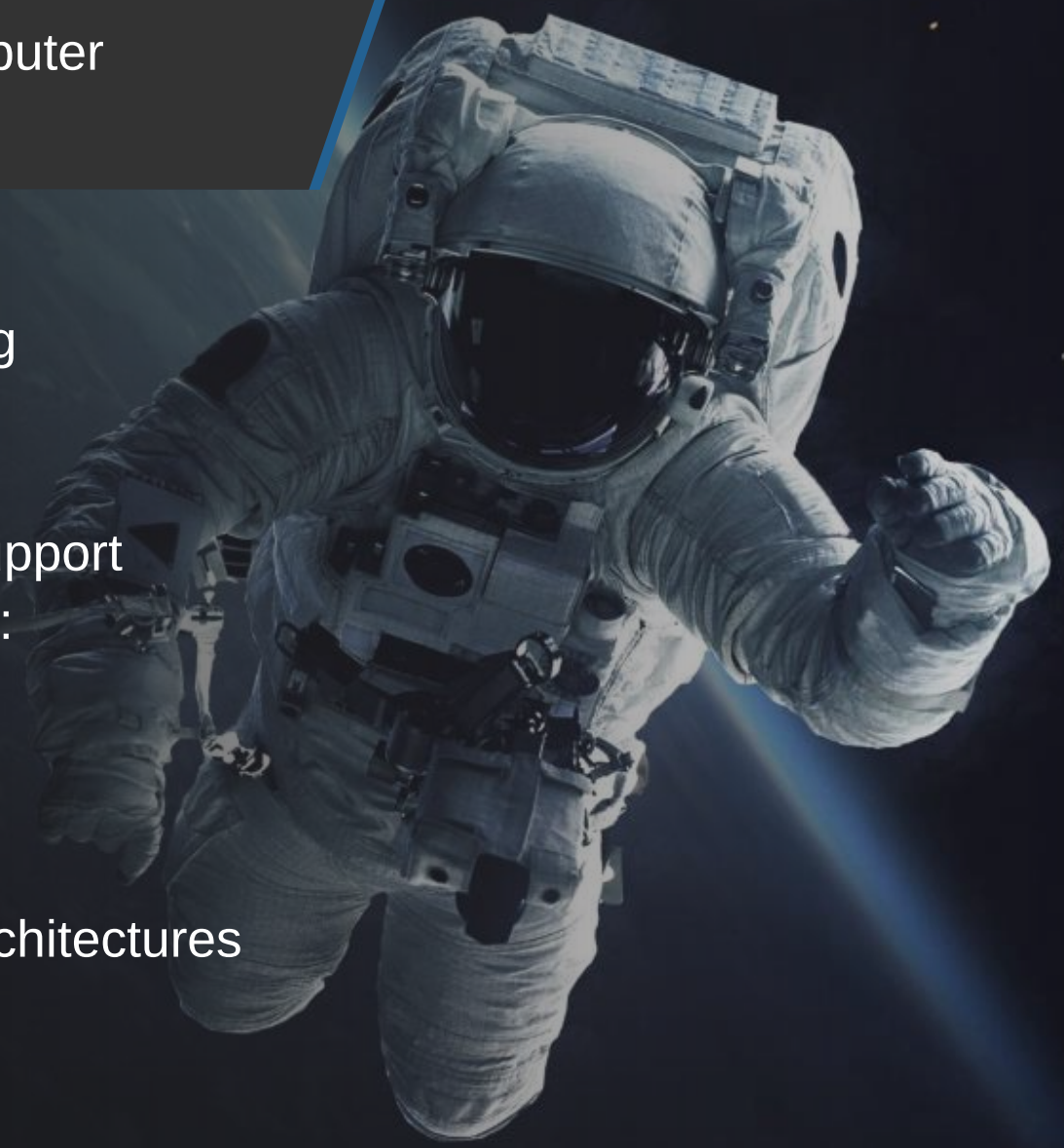
A world leader in embedded computer systems for harsh environments

Experts in fault-tolerant computing

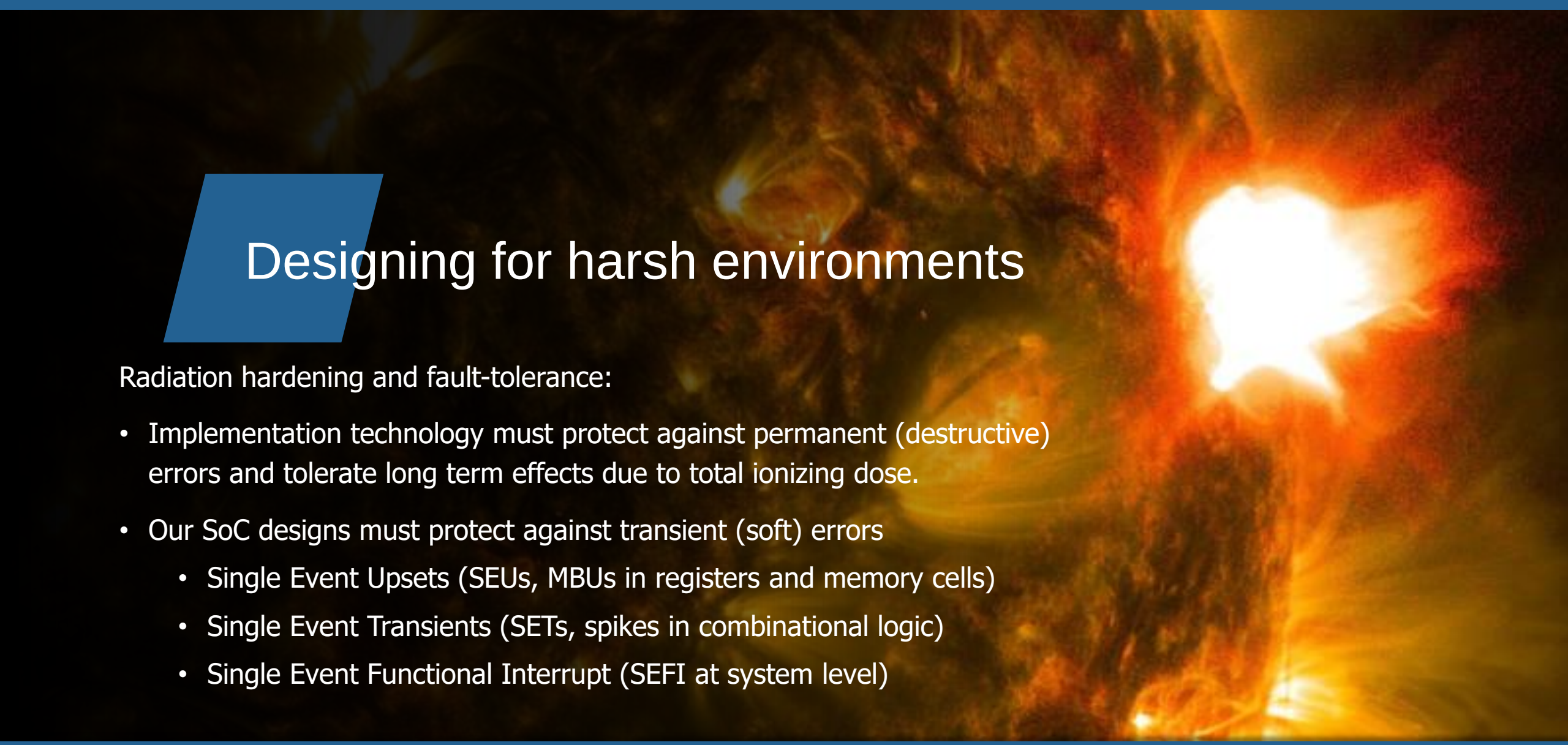
We provide a full ecosystem to support hardware and software design for:

- Standard components
- Semi-custom FPGA
- Full custom ASIC

Based on SPARC and RISC-V architectures



# Designing for harsh environments



Radiation hardening and fault-tolerance:

- Implementation technology must protect against permanent (destructive) errors and tolerate long term effects due to total ionizing dose.
- Our SoC designs must protect against transient (soft) errors
  - Single Event Upsets (SEUs, MBUs in registers and memory cells)
  - Single Event Transients (SETs, spikes in combinational logic)
  - Single Event Functional Interrupt (SEFI at system level)

# Gaisler's EEE Portfolio

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## High-reliability

- Radiation hardened
- Space qualified
- Fault-tolerant

**NOEL Processor Family**

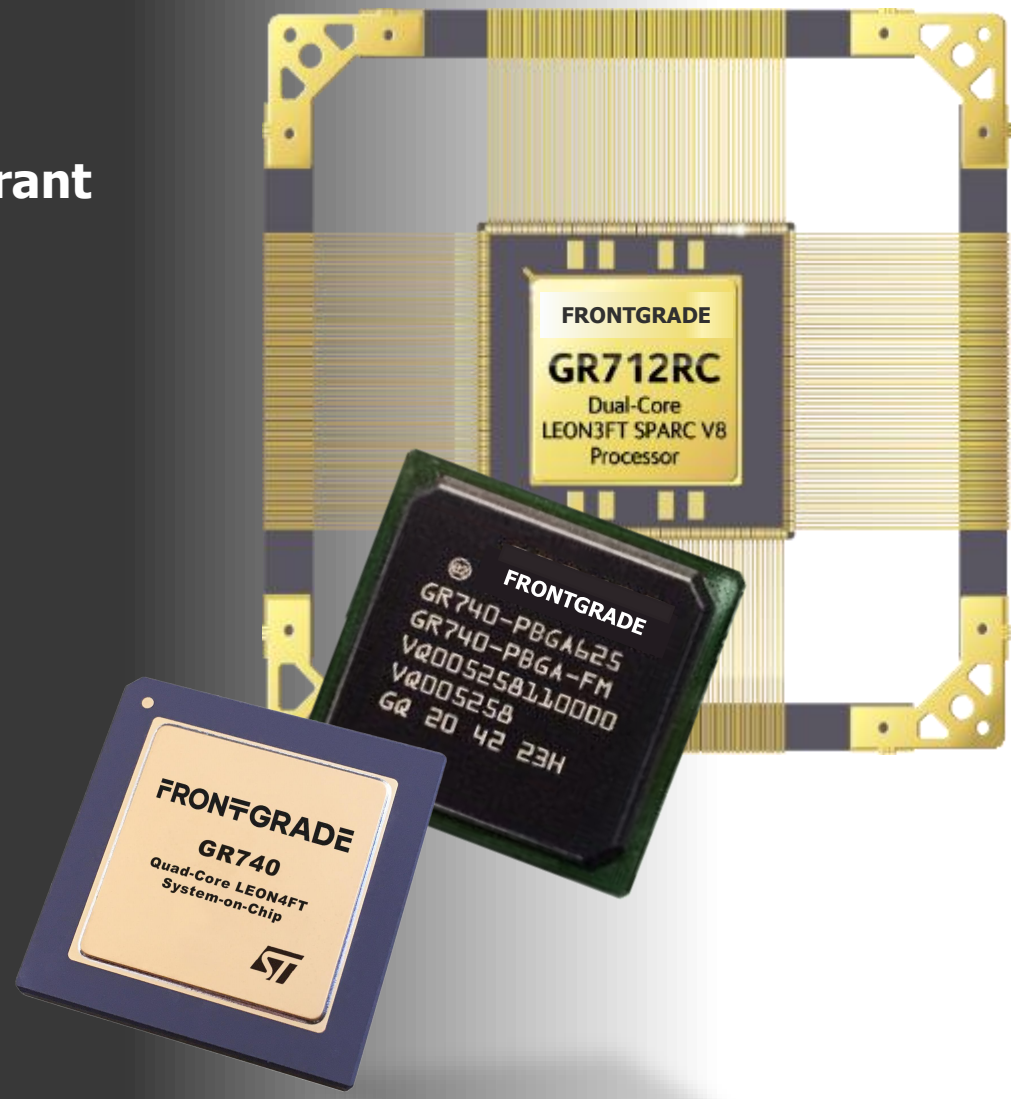
- GR7xV, NOEL-V, 16-Core, in development
- GR765, NOEL-V, 8-Core, in development

**LEON Processor Family**

- GR765, LEON5FT, 8-Core, in development
- GR740, LEON4FT, quad-core, 250 MHz, QML-Q, QML-V
- GR740 PBGA, LEON4FT, quad-core, 250 MHz, Flight units in Q1 2023
- GR716A, LEON3FT, single-core, 50 MHz, Flight units in Q1 2023
- GR716B, LEON3FT, single core 100 MHz, in development
- GR712RC, LEON3FT, dual-core, 100 MHz, Vendor class S
- UT700, LEON3FT, single-core, 166 MHz, QML-Q, QML-V
- UT699E, LEON3FT, single-core, 100 MHz, QML-Q, QML-V
- UT699, LEON3FT, single-core, 66 MHz, QML-Q, QML-V

**Interface Family**

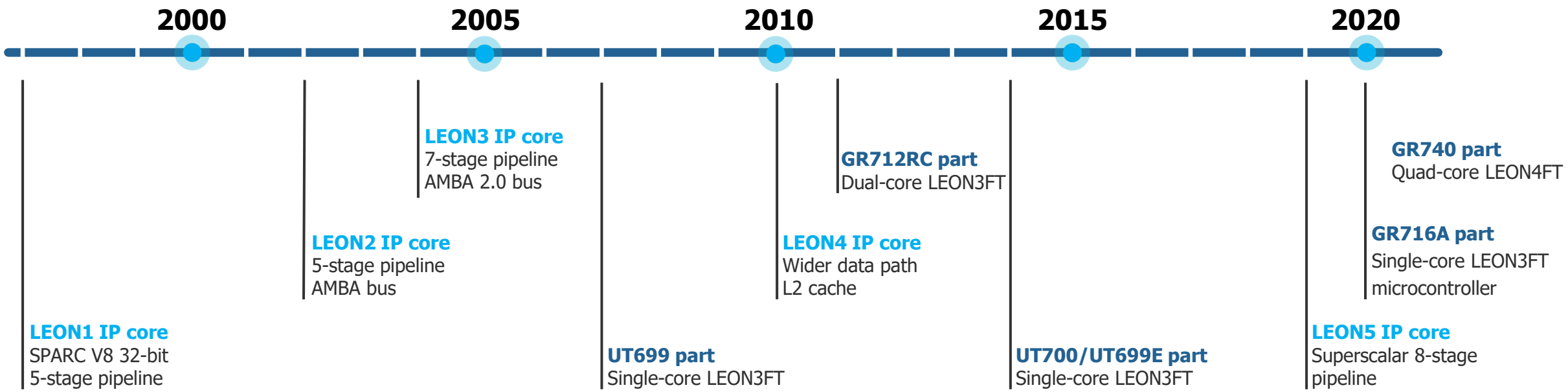
- GR718B, Radiation-Tolerant 18x SpaceWire Router, Vendor class S



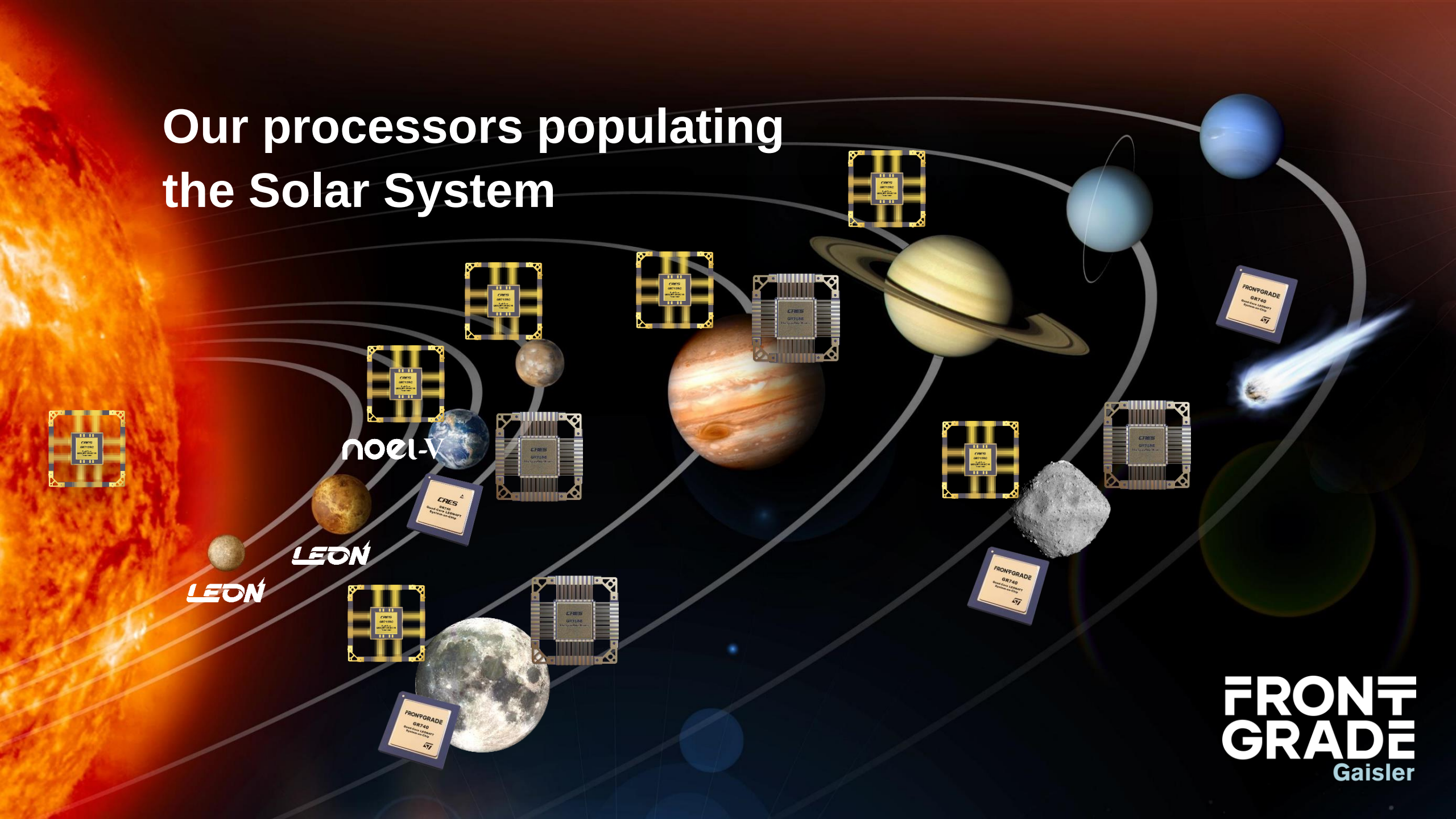
# LEON Processor History

## LEON Technology – over 20 years of space success

- Five generation LEON SPARC V8 processors
- Space proven technology
- Industry Standard Tools & Eco-System



# Our processors populating the Solar System

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# GR740 - Quad-Core LEON4FT Processor

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## What can be improved?

- Higher-pin count package enabling more interfaces simultaneously
  - No sacrifices needed
- Customers require:
  - Higher performance memory interface (DDR3/4)
  - NAND memory controller for storage
  - High Speed Serial Links Controllers
- Software vendors outside of space industry do not target SPARC
- A SBC based on the GR740 typically requires a companion FPGA

| | | | | |
|---|---|---|---|---|
| **STANDARD MICROCIRCUIT DRAWING**<br>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE<br>AMSC N/A | PREPARED BY<br>Phu H. Nguyen | **DLA LAND AND MARITIME**<br>**COLUMBUS, OHIO 43218-3990**<br>https://www.dla.mil/LandandMaritime | | |
| | CHECKED BY<br>Phu H. Nguyen | | | |
| | APPROVED BY<br>Muhammad A. Akbar | MICROCIRCUIT, PROCESSOR, DIGITAL, CMOS, RADIATION HARDENED, QUAD CORE LEON4 SPARC V8 PROCESSOR, MONOLITHIC SILICON | | |
| | DRAWING APPROVAL DATE<br>22-04-18 | | | |
| | REVISION LEVEL | SIZE<br>A | CAGE CODE<br>67268 | **5962-21204** |
| | | SHEET 1 OF 51 | | |

DSCC FORM 2233
APR 97

5962-E021-21

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

esa LEON SPARC Compliant SCD V8

# Safety-critical systems

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**Strict requirements for dependability**

- Robustness in harsh environments
- Fault tolerance, fail-operational
- Deterministic real-time behaviour

**Increasing need for performance**

- Algorithms get more complex, with larger datasets
- Adaptive or multi-mode applications, multiple applications
- Autonomous systems

**New requirements**

- Increased connectivity
- Cybersecurity
- Freedom from export control restrictions

**Source code access**

- Openness: observability, ability to document, cybersecurity audit
- Respect of standards, interoperability

# RISC-V is a game changer

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**RISC-V instruction set**

- Standard maintained by RISC-V International
- Permissive open-source license ensures wide adoption
- Efficient and modular ISA, with optional extensions
- Some peripherals : interrupt controller, MMU, etc.

**Technical Groups and Special Interest Groups**

- Security Standing Committee
- Cache Management Operation Task Group
- Functional safety SIG



# NOEL-V Processor Core

RISC-V RV64 and RV32 Processor Model

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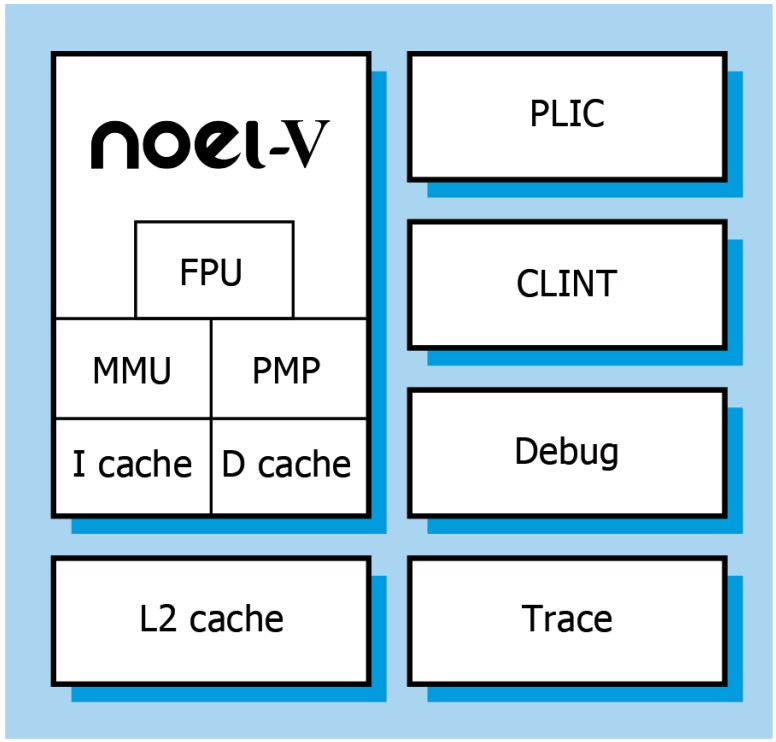
## Characteristics:

- RISC-V processor core
  - 32- or 64-bits architecture
- Superscalar – in order pipeline
- Fault Tolerance features
- Leverages RISC-V software and tool support in the commercial domain together with our offering
- Part of the GRLIB IP Core library
  - Supports both FPGA and ASIC technologies
- Highly configurable
- AHB and AXI4 built-in support

RISC-V®




https://www.gaisler.com/NOEL-V

GRLIB SYSTEM-ON-CHIP IP LIBRARY

## Performance

- Comparable to ARM cortex A53
- CoreMark*/MHz
  - dual-issue 4.41**
  - single-issue 3.05**

* GCC9.3.0 20200312 (RTEMS 5, RSB 5 (c53866c98fb2), Newlib 7947581
-g -march=rv64ima -mabi=lp64 -B /gsl/data/products/noelv/rtems-noel-1.0.3//kernel/riscv-rtems5/noel64ima/lib --specs bsp_specs -qrtems -lrtemsdefaultconfig -O2 -funroll-all-loops -funswitch-loops -fgcse-after-reload -fpredictive-commoning -mtune=sifive-7-series -finline-functions -fipa-cp-clone -falign-functions=8 -falign-loops=8 -falign-jumps=8 --param max-inline-insns-auto=20

** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.

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# GR765

## Next-Generation SoC

# GR765 – Octa-Core Processor

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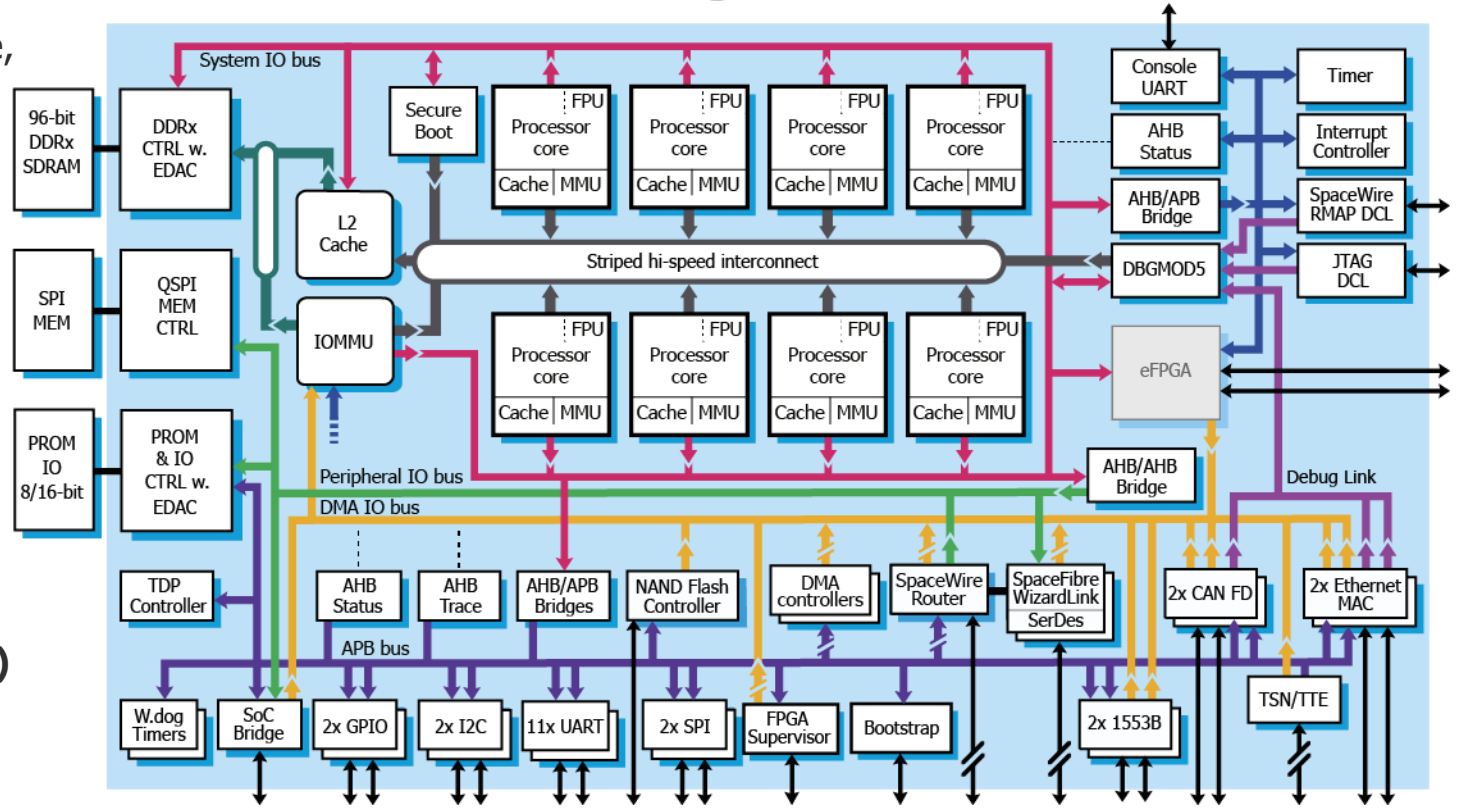
**In development**
**No guarantee of product launch**

## Baseline Features

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8 or NOEL-V RV64GCH**
  - Dedicated FPU and MMU, 64 KiB per core L1 cache, connected via multi-port interconnect
- **Target technology: STM 28nm FDSOI**
- **1 GHz processor frequency**
- 2+ MiB L2 cache, **512-bit** cache line, 4-ways
- **DMA controllers**
- **DDR3 interface with dual x8 device correction capability**
- 8/16-bit PROM/IO interface
- **(Q)SPI and NAND memory controller interfaces**
- **Secure Element, providing Secure (authenticated) boot (TBD)**
- **eFPGA ~30k LUT (TBD)**
- **High-pin count – LGA1752 package – allows using more interfaces simultaneously**
- RISC-V RV64GCBH Can run complex OS (like Linux) in full virtualization

LEON5 NOEL-V

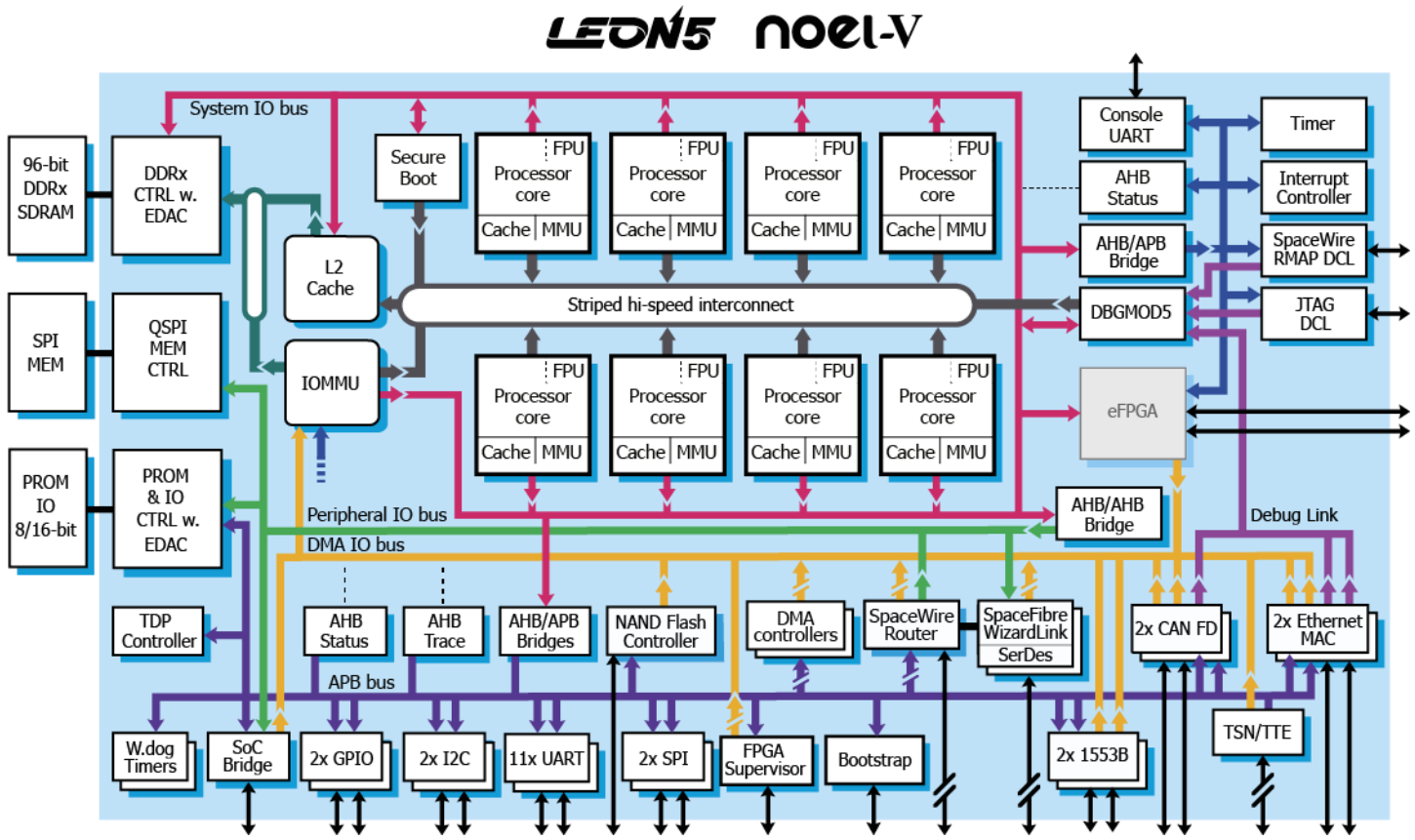



SPARC RISC-V®

# GR765 – Interfaces

- **SpaceFibre x8 lanes 6.25 Gbit/s, simpler protocols**
- **12-port** SpaceWire router with +4 internal ports
- 2x 10/100/1000 Mbit Ethernet
- **2x or 3x (TBD) TT / TSN Ethernet support**
- **2x** MIL-STD-1553B,
- **2x CAN FD**
- **2x I2C interface**
- **12** x UART
- **2x** SPI controller
- **SoC Bridge interface**
- **FPGA Supervisor interface**
- Timers & Watchdog, GPIO ports
- On-chip SerDes
- Debug links:
  - Dedicated: JTAG and SpaceWire
  - CAN, SpFi, Ethernet

**In development**
**No guarantee of product launch**




SPARC RISC-V®

# Instruction Set Architectures

## Why two ISAs in the same SoC?

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### Why RISC-V?

- Hardware and software potential for future space applications: A new class of processors requires a modern architecture
- Enabling new technologies by standardization
  - Hypervisor support
  - Vector extension, …
- Growing base of 3rd party ecosystem:
  - Toolsets
  - Libraries, engines etc.
- Attractive to talent entering the space domain
- Influx of know-how by talent entering the space domain

RISC-V®

### Why SPARC?

- Existing base of space proven HW and SW designs
- Mature ecosystem for today's space applications, e.g. qualified OS
- Accumulated development know-how in the industry
- Software backward compatible with existing LEON devices

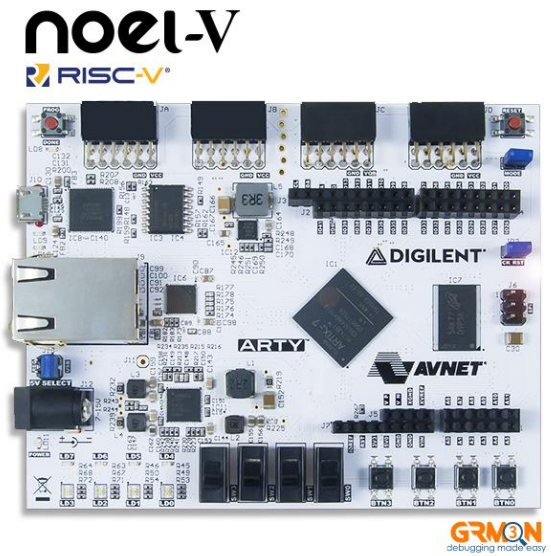
SPARC

### GR765 provides RISC-V and SPARC

- Both architectures are needed by the industry
- Faster time-to-market for RISC-V while continuing SPARC - single component development investment and qualification effort
- Minimal silicon overhead - sharing of resources on chip. User selects CPU (LEON5FT or NOEL-VFT), device cannot operate with both at the same time.
- De-risking early stages of new application development
  - The architectural choice can be evaluated easily

# LEON5 & NOEL-V availability

- LEON5 and NOEL-V are available as part of the GRLIB IP library
  - Dual licensed IP library: GPL variant available at gaisler.com/getgrlib
  - Commercial variants of the library available for different applications (COM, FT-FPGA, FT)
  - The library includes infrastructure for project file generation for most popular EDA tools and SoC template designs
- FPGA bitstreams for Xilinx and Microchip FPGA evaluation boards are available for download
- Debug monitor and software toolchains (Bare-C, RTEMS, Linux, …) are also available




NOEL-ARTYA7


LEON-PF

NOEL-PF


LEON-XCKU

NOEL-XCKU

# Software

- Complete ecosystem
- A combination of Gaisler and 3rd party software

**Tool chains, Operating systems and compilers**

- Bare-C
- Linux
- RTEMS
- VxWorks
- Zephyr

**Hypervisors**

- XtratuM/XNG (FentISS)
- PikeOS (SYSGO)
- Xvisor

**Boot loaders**

- MKPROM2
- GRBOOT Flight bootloader

**Tools**

- GRMON3
- TSIM3

GR765 and GR740 SW Compatibility

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# LEON5FT and NOEL-VFT 28nm Test Chip

## STM FDSOI28 GEO P2

# NOEL-V & LEON5 Fault tolerance overview

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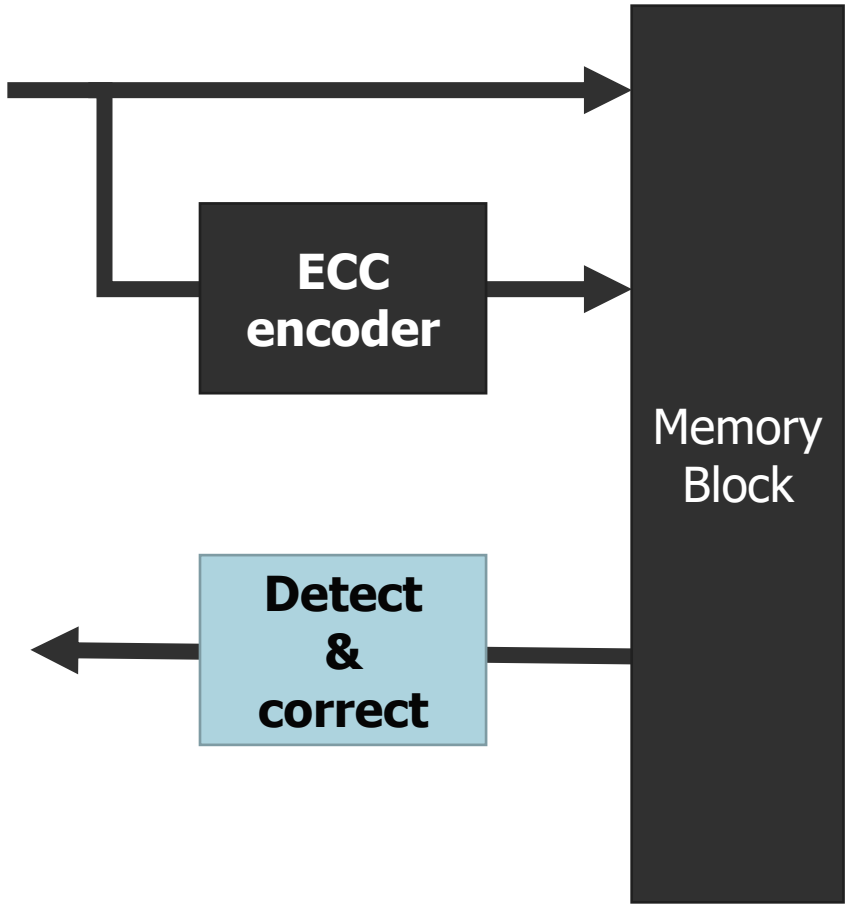
- No need for lock-step or redundant CPUs
- Protection of memory blocks (in caches & register file) using error correcting codes
- Protected with a full SECDED code with custom scheme:
  - Deliver correct data locally without causing memory access
  - Guaranteed detection also of 3-bit and 4-bit adjacent bit errors
- Hardware scrubber built into processor to avoid error build-up
  - Removes need for manual scrubbing routines
- Error counters and diagnostic interfaces
  - Monitor and inject errors



# NOEL-V and LEON5 silicon proven on STM 28nm GEO P2

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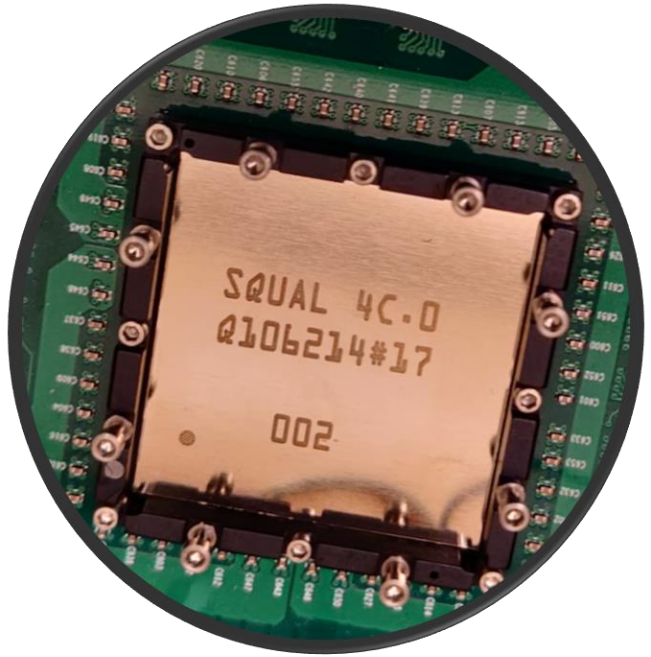
## Rad-hard demonstrator with NOEL-V RISC-V 64-bit and LEON5FT SPARC V8 32-bit

- Specialized design with LEON5 and NOEL-V sharing resources, <1 $mm^2$
- Test chip will be included in GOMX-5 LEO in-orbit experiment
- 1GHz processor frequency
- No silent data corruption
- Functional error saturation cross-section: 1E-7 $cm^2$/device
- All detected errors in memories were corrected by the fault-tolerant features of the design (on-chip RAM and L1 caches)
- No Single Event Latch-up (SEL)




| Orbit | Mean Time Between Functional errors |
|---|---|
| LEO (700 Km, incl. 98.7°) | 28,500 years |
| GEO (36000 Km) | 8,640 years |

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# GR7xV

## Next-Next-Generation SoC

# GR7xV – 16-core NOEL-V Processor

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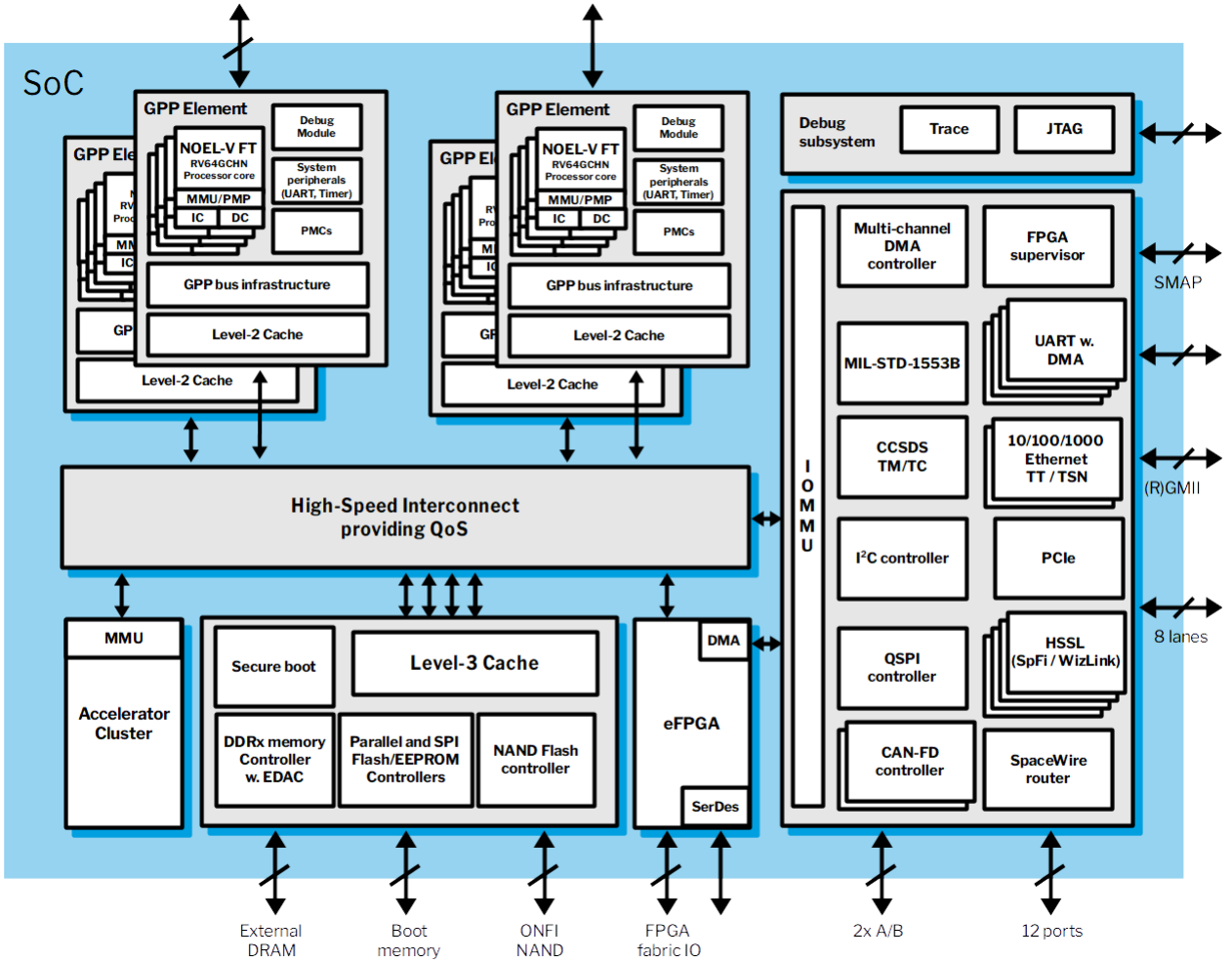
**In development**
**No guarantee of product launch**

## Baseline Features

- Fault Tolerant 64-bit RISC-V Hexadeca-core divided in four islands (named GPP element)
- Each island has four NOEL-V processors with dedicated L2 caches
- HW assisted cache coherency between GPP elements and IO system
- Shared L3 cache
- More advanced technology node compared to GR765
- Accelerator cluster for high-performance computation and ML workloads
- eFPGA fabric for glue logic




noel-V RISC-V

# GR7xV – 16-core NOEL-V Processor

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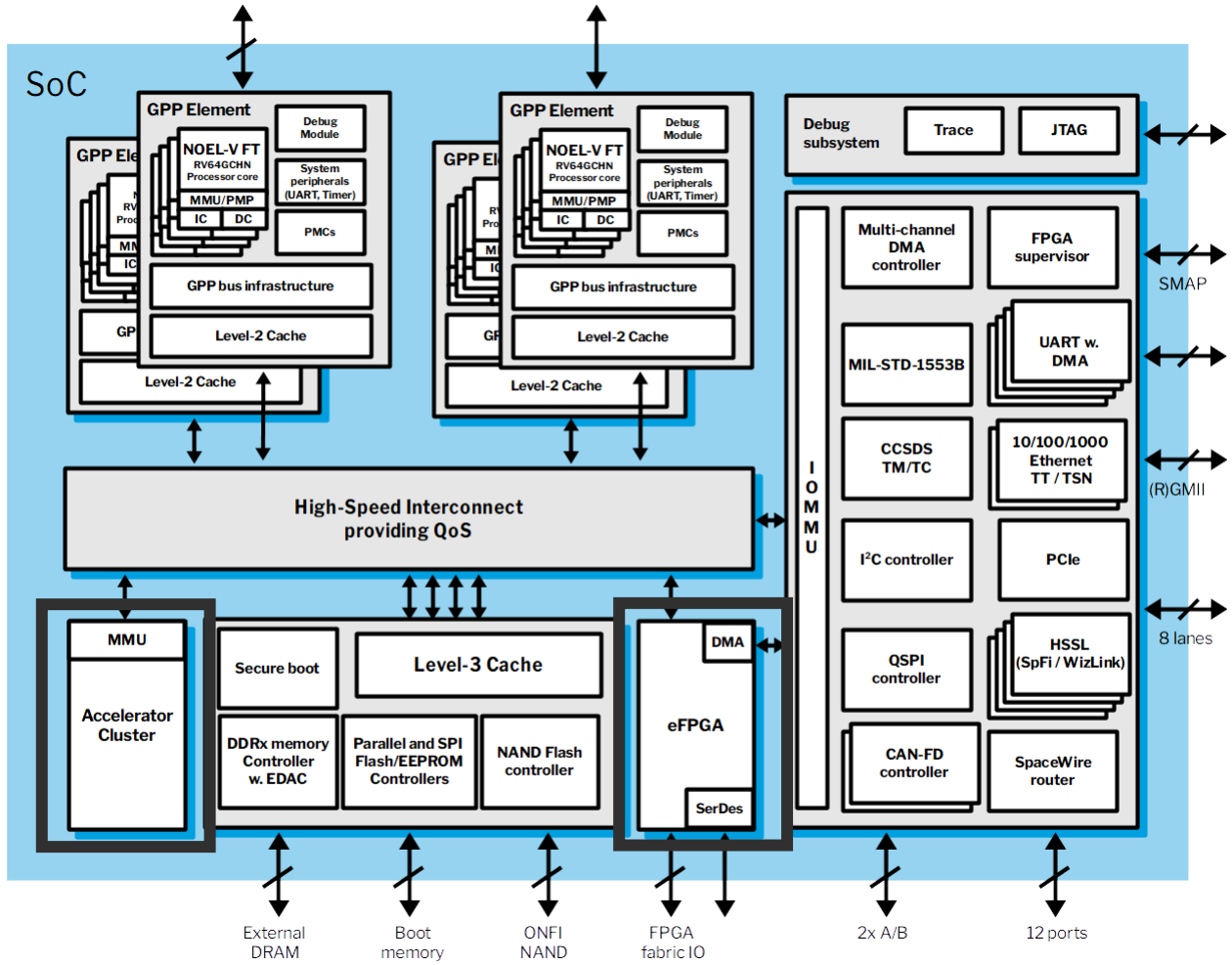
**In development**
**No guarantee of product launch**

## Accelerator

- Accelerators are being evaluated within the currently running activity
- Applications: Signal processing, ML, computer vision.
- Intent is to use accelerator for computations where the GPPs are inefficient.
- Software libraries to be provided by commercial vendor.

## eFPGA

- Approach is to provide eFPGA for glue logic
- Reduce the need for companion FPGAs such as RTAX2000 and NG-Medium, but not a replacement for a RTG4 or XCKU.



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# Conclusion

Rad-Hard RISC-V multi-core processors

# Conclusion

- Both, the GR765 and GR7xV developments put emphasis on **computational performance**, **power efficiency**, and support for **mixed criticality application**
- The GR765 development builds on the successful GR740 quad-core LEON4FT component
- The **GR765** is an **octa-core** processor. Users can enable either eight NOEL-VFT RISC-V 64-bit processor cores or eight LEON5FT cores.
- GR765 supports DDR3 SDRAM, high-speed serial link controllers and several other extensions.
- GR765 **prototypes** components will be available at the **end of 2024**
- The **GR7xV** is a **16-core** RISC-V processor
- The GR7xV targets a more advanced technology node compared to GR765
- The GR7xV will likely include accelerator cluster for high-performance computation and ML workloads