NG-Ultra

The European rad-hard SoC + FPGA suitable for future space applications

ESCCON 2023

Jean-Luc POUPAT, Airbus Defence and Space

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Key Messages Summary

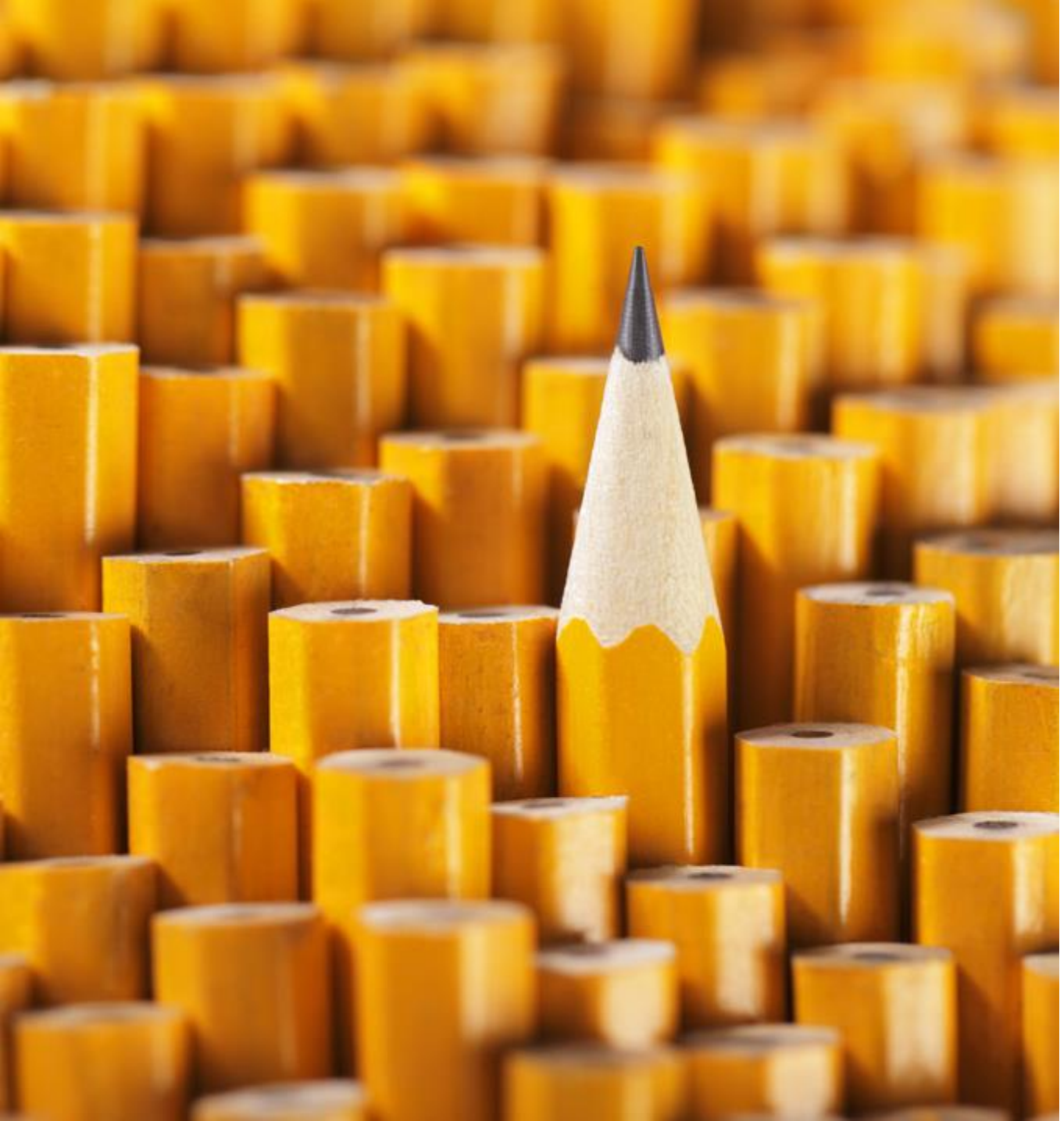
NG-Ultra is **unique** in the landscape
of available **Rad Hard** components

It is the only **European** FPGA solution **with a SoC**

It offers **performances** & **robustness** breakthroughs
with Huge FPGA + High performance processing

Tools are (now) at good **maturity** level
and continue to **improve**

NG-Ultra selected by ADS & TAS
as **technical baseline** on several on-going projects



Why NG-Ultra is unique in the landscape of available Rad Hard components?

Introduction

Performances Status

Ecosystem Status

Use Cases

Conclusion

Context

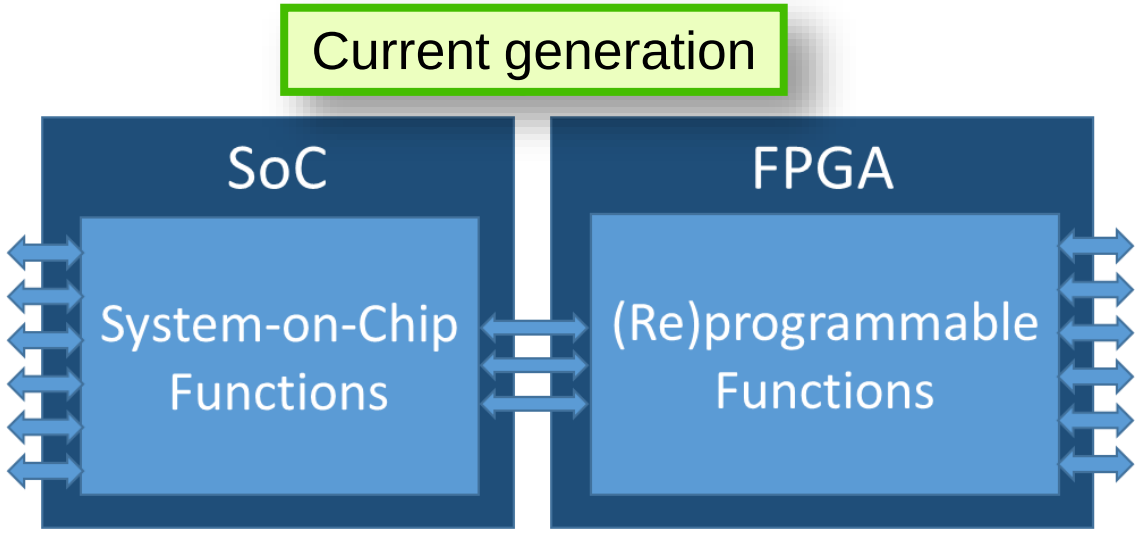
Initiated by **CNES**, collaboration between **Airbus** and **TAS** to develop a **European chip** supported by H2020

NanoXplore is the company owning and commercialising the **NG-Ultra** manufactured by **STMicro** in 28FDSOI

NG-Ultra = SoC + FPGA

Horizon 2020 was the EU's research and innovation funding programme from 2014-2020

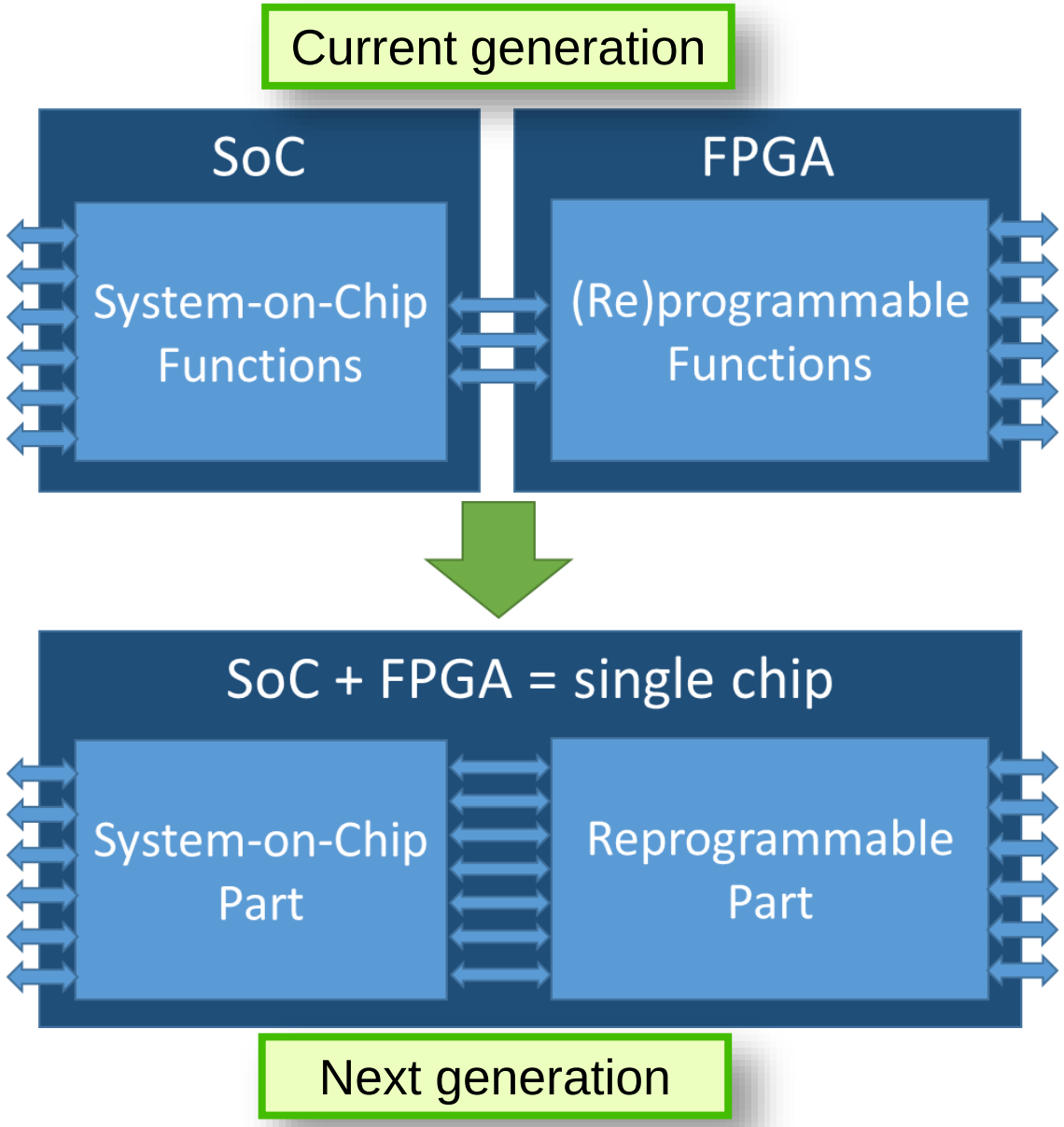
To integrated SoCs and beyond



Integrated SoC+FPGA

- Consistent with the design of processing boards
- Optimized interfaces SOC ←→ FPGA
- Key enabler for more integrated designs & cost reduction

To integrated SoCs and beyond



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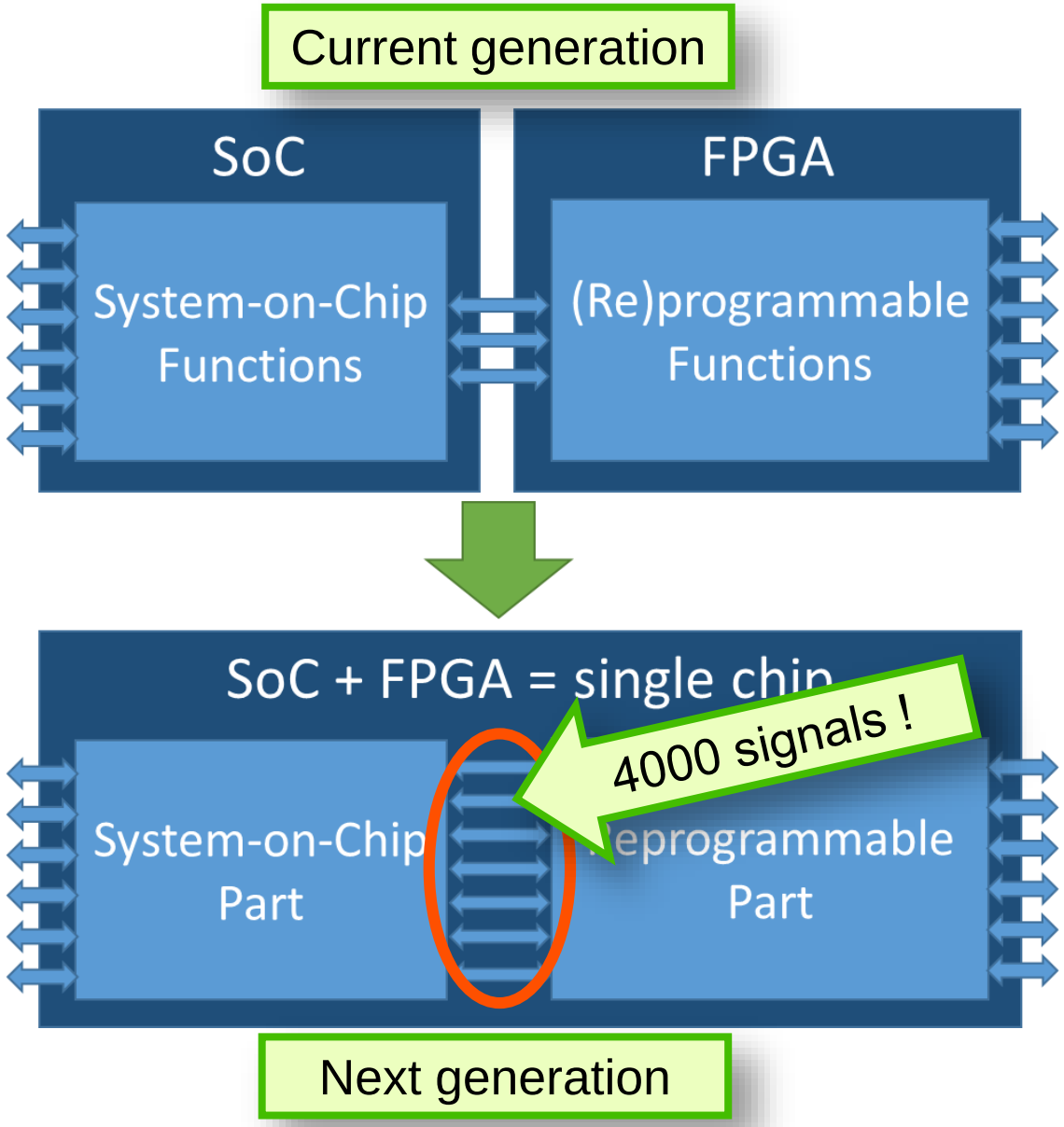

Integrated SoC+FPGA

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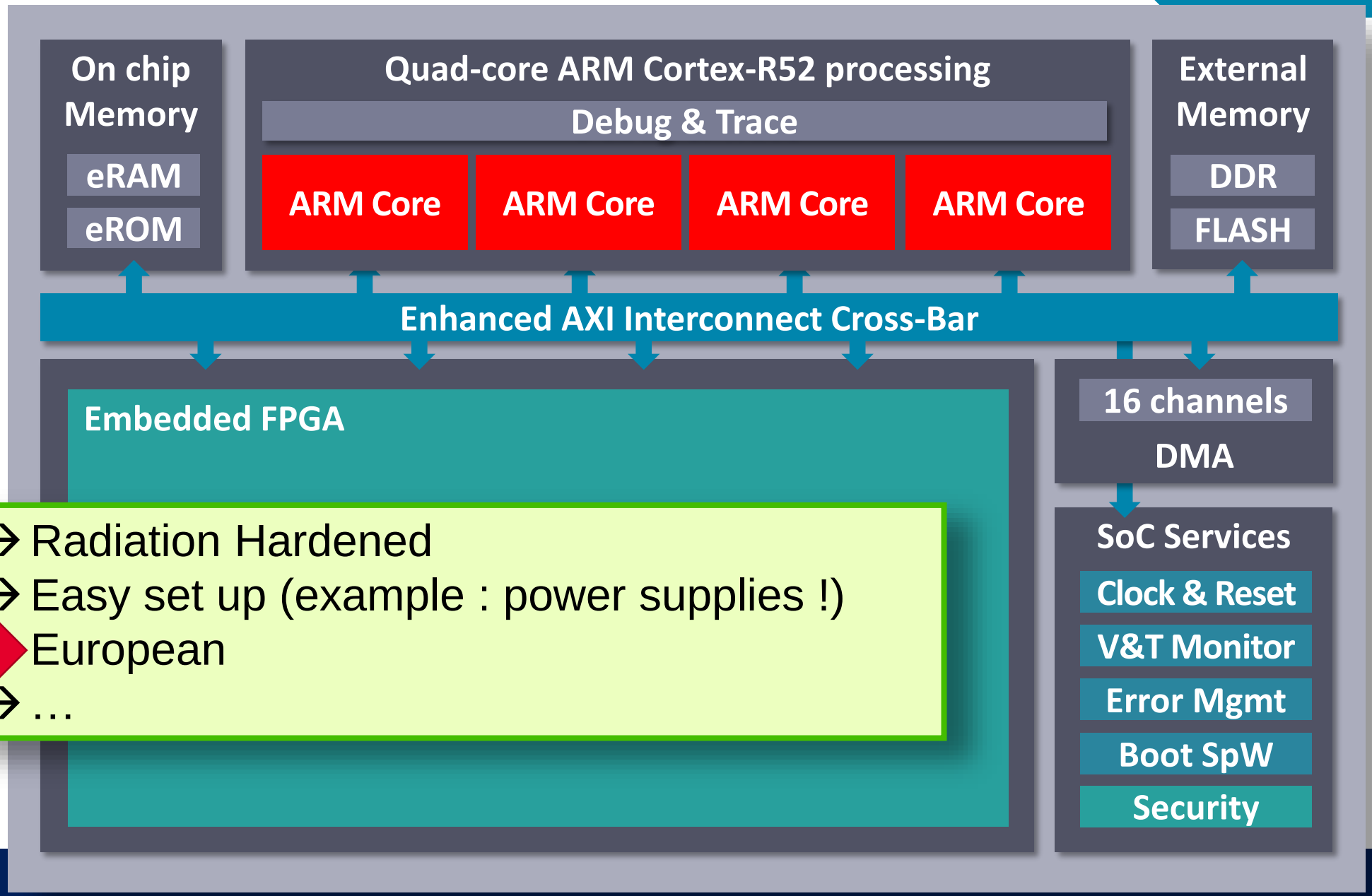
Features


On chip Memory
eRAM
eROM
Quad-core ARM Cortex-R52 processing
Debug & Trace
ARM Core
ARM Core
ARM Core
ARM Core
External Memory
DDR
FLASH
Enhanced AXI Interconnect Cross-Bar
Embedded FPGA
16 channels
DMA
SoC Services
Clock & Reset
V&T Monitor
Error Mgmt
Boot SpW
Security
→ Radiation Hardened
→ Easy set up (example : power supplies !)
→ European
→ …

Why European strategic non-dependence is a key point ?

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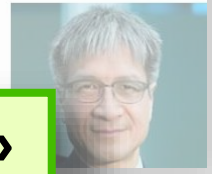
Xilinx Cuts Huawei From Future Forecasts

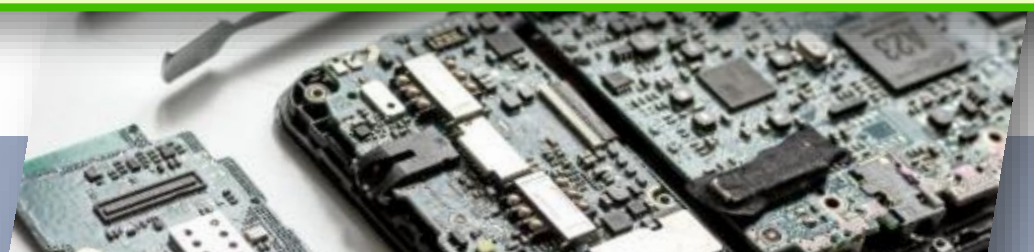
October 28, 2019 Leave a comment Featured, Featured Articles By Barbara Jorgensen

Xilinx Inc. is planning a future that does not include Huawei Technologies, CEO Victor Peng told analysts last week.

The chip maker has not received the necessary approvals to ship products to the Chinese networking giant, which the U.S. government has deemed a security risk.

Xilinx shipped $50 million worth of product to Huawei in its first fiscal (June) quarter -- just prior to U.S. trade restrictions imposed in May. "Considering the continued trade restrictions with Huawei and the uncertainty presented to





« If the Xilinx chip needs to be changed out, they will be in trouble »

Comments about Huawei reported in 2019

Features – What else ?

NanoXplore

https://nanoxplore.org

https://nanoxplore-wiki.atlassian.net

3.1.1 Processor System description

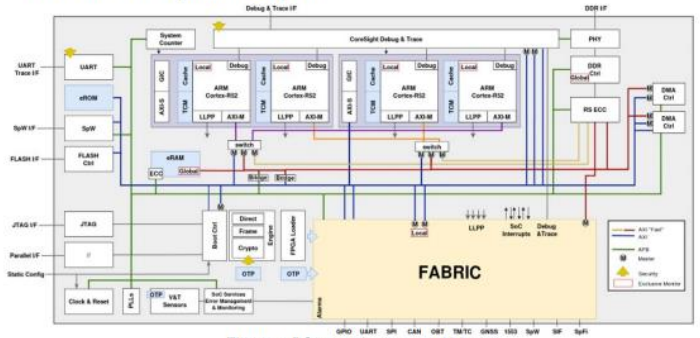


Figure 2: PS comprises several blocks:

- Processing Unit
  - Quad-Core Cortex-R52 (ARMv8-R) 2.2 DMIPS/MHz @ 600MHz
  - 3 TCM 128KB per Cortex-R52
  - GIC
  - Debug and Trace
- Several Interconnect connected to the PL by:
  - 2 AXI4 Master 128b
  - 2 AXI4 Slave 128b
  - 1 APB4 32b
  - 4 LLPP – AXI4 32b
  - 1 AXI4 Master 128b dedicated DDR
- DDR controller with Reed Solomon
- 2 DMA Controller with 8 channels
- eRAM (2MB + 0.25MB ECC)
- Security Manager

Interconnect link between PS and PL can reach 200MHz at 125°c.

Processor system is described in NG-ULTRA NX2H540ATSC PS USER MANUAL document.

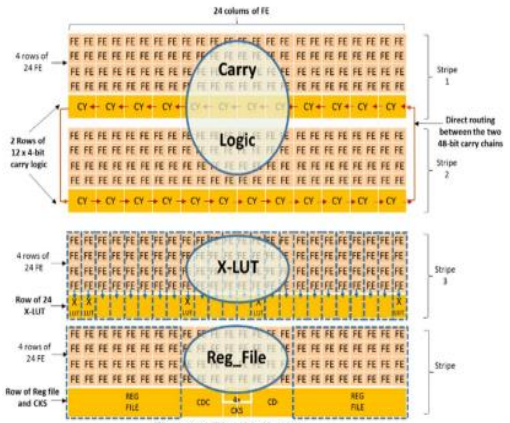


Figure 4: Tile distribution

3.3.1.1 Fundamental Element

FE features
Four inputs and one output truth table • implements any 1 to 4-input Boolean function
Optional register on output • 1-bit edge sensitive flip-flop (DFF) • Programmable synchronous / asynchronous reset • Programmable positive / negative clock edge • Programmable Load enable
DFF initialization by bitstream

Table 5: FE features

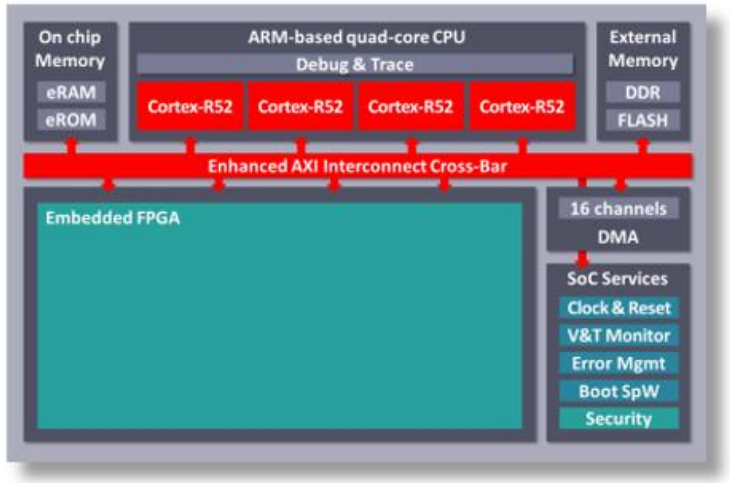
The random logic is implemented with 4-input look up tables (LUT). The LUT output signal can be optionally stored in a register. The terminals I1, I2, I3, I4, and OUT are connected to the TILE interconnect network. The inputs RST, LE and CLK are connected to the TILE low skew network.

What are the breakthroughs (*) of NG-Ultra architecture and detailed performances ?

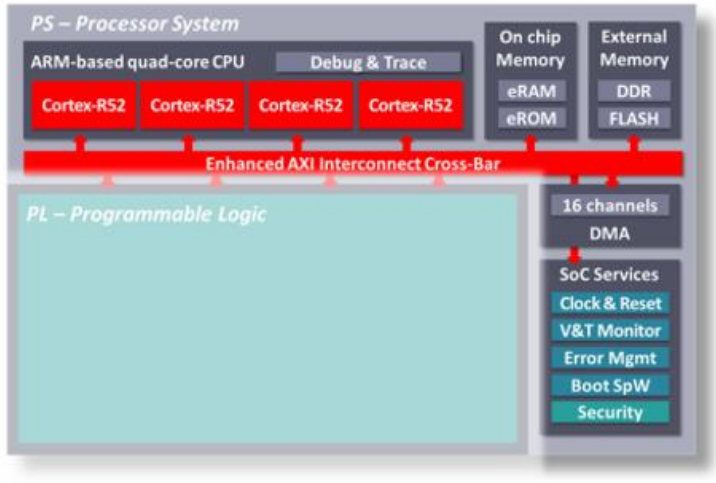
(*) for a rad-hard component

High level performances comparison

SoC + FPGA



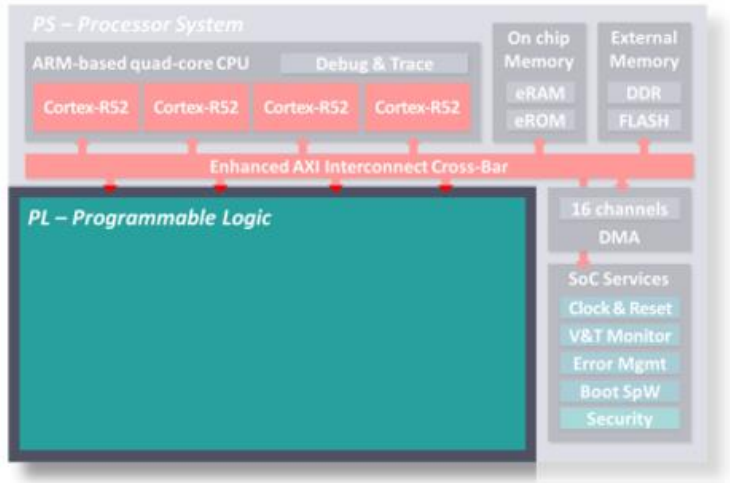
SoC only



NG-Ultra processing perfo
1 818 CoreMark / core
1 250 DMIPS / core

CPU Performance
→ 40 x SCOC3
→ 2 x GR740

FPGA only



NG-Ultra FPGA capacity
~530 KLUT

FPGA Capacity
→ 2 x RTG4 (*)
→ 25 x RTAX2000 (*)

(*) estimation of realistically useable FPGA size at ESCCON 2023 date, twice more to be expected considering theoretical LUTs resources and the strong momentum deployed on tools improvement

High level performances comparison

Table: Power Supply Ramp Time

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO}	0.2	40	ms
T_{VCCINT_VCU}	Ramp time from GND to 95% of V_{CCINT_VCU}	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$	0.2	40	ms
$T_{VCC\_PSINTFP}$	Ramp time from GND to 95% of $V_{CC\_PSINTFP}$	0.2	40	ms
$T_{VCC\_PSINTLP}$	Ramp time from GND to 95% of $V_{CC\_PSINTLP}$	0.2	40	ms
T_{VCC_PSAUX}	Ramp time from GND to 95% of V_{CC_PSAUX}	0.2	40	ms
$T_{VCC\_PSINTFP\_DDR}$	Ramp time from GND to 95% of $V_{CC\_PSINTFP\_DDR}$	0.2	40	ms
T_{VCC_PSADC}	Ramp time from GND to 95% of V_{CC_PSADC}	0.2	40	ms
T_{VCC_PSPLL}	Ramp time from GND to 95% of V_{CC_PSPLL}	0.2	40	ms
$T_{PS\_MGTRAVCC}$	Ramp time from GND to 95% of $V_{CC\_MGTRAVCC}$	0.2	40	ms
$T_{PS\_MGTRAVTT}$	Ramp time from GND to 95% of $V_{CC\_MGTRAVTT}$	0.2	40	ms
T_{VCCO_PSDDR}	Ramp time from GND to 95% of	0.2	40	ms
$T_{VCC\_PSDDR\_PLL}$	Ramp time from GND to 95% of			
T_{VCCO}	Ramp			

Comparing performances is important but not enough. Many other criteria shall be considered such as package, radiation hardening, cost, hardware setup (memories, power supply…), hardware and software ecosystem, risk mitigation of export control limitation, support to a European solution…

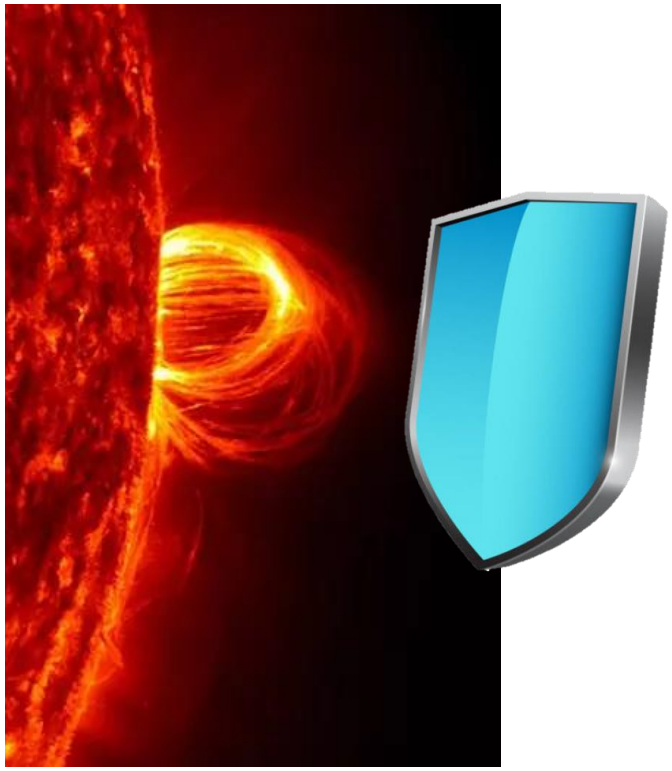
Space environment is hostile - Radiations

NG-Ultra radiation robustness is… impressive !

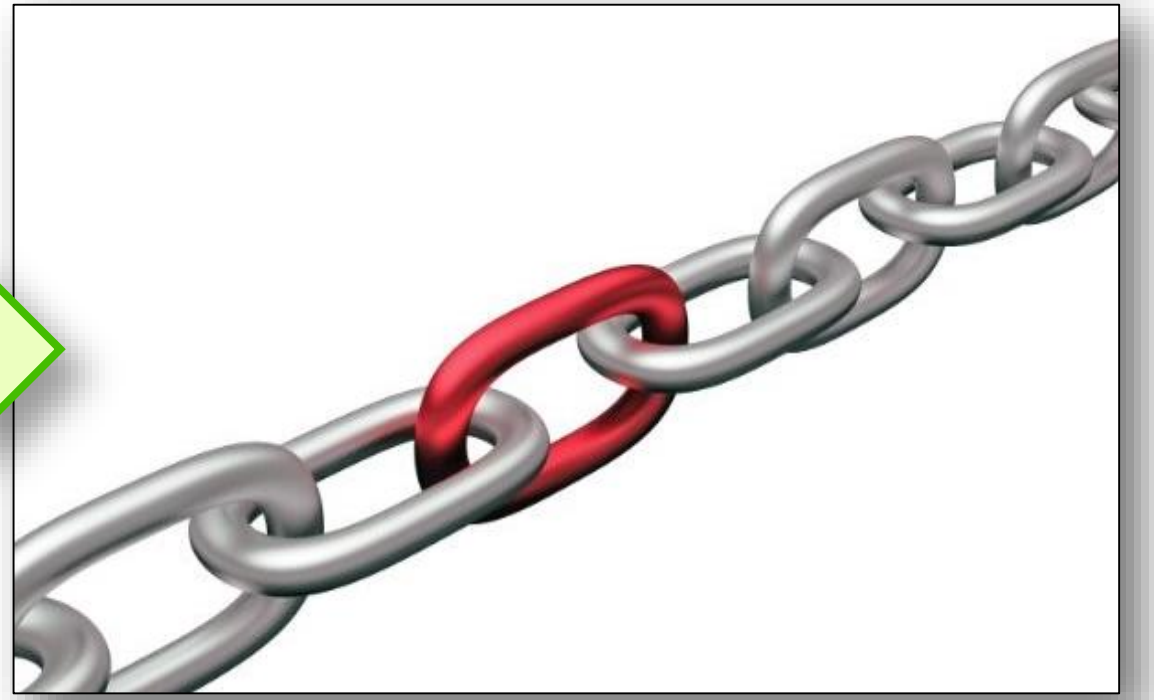
- 28FDSOI technology intrinsically latch-up immune → **no SEL**
- NG-Ultra tested during 2 radiation campaigns → **no SEFI**
- Robustness confirmed (**no SEU, no SEFI**) on v1, ok for v2

DDR memory protection → a game changer

- Supporting DDR2, DDR3 and **DDR4** / 8-bit & 18-bit devices
- Reed-Solomon for **SEU** high level of memory protection
- **Robustness against SEFI** up to the loss of two 16-bits devices



NG-Ultra architecture approach – No « weakest link »



Having a high performance and very robust component is not enough, because if it is associated to sensitive components (such as peripheral memories), the overall robustness will depends on the “weakest link”.
As an example, if you need to reboot each time you have an upset in a memory, this will drive the way you operate your processing module… this is an issue…

NG-Ultra solves this issue, since (1) it offers a robust Radiation Hardened By Design (RHBD) chip and (2) it provides unprecedented protection mechanisms for all of its peripheral components (Flash, DDR) allowing to use it without risk of introducing a “weakest link”.

What is the ecosystem status for developing hardware and software with NG-Ultra ?

Toolsuite

For **software** development

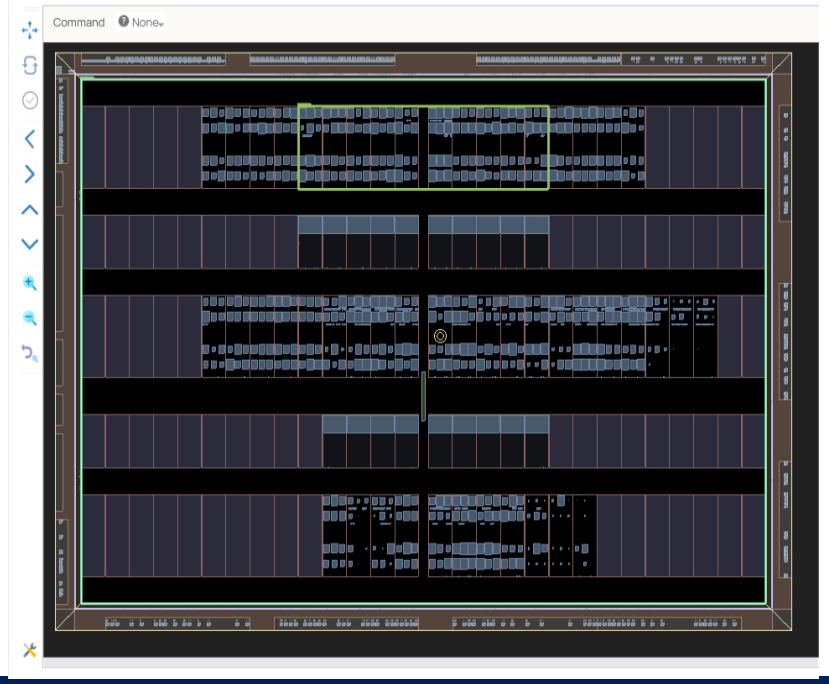
Debug and trace → ARM ecosystem

- Supported as predefined chip in Lauterbach

For **hardware** development

Synthesis, Place & Route → NXMap → Impulse

- Synthesis → maturity on going, agreement with Mentor Precision RTL
- Place & Route → automatic optimization not yet reached, can be get round with manual place & route tasks with NX support
- Noticeable tools improvements after each release (cf OPERA results)



Bitstream loading → NXBase2

- Available & Mature

What about first use cases targeted by Airbus & TAS with NG-Ultra ?

NG-Ultra on TAS Projects

- A FPGA without a Place & Route tool is nothing
  - NanoXmap toolsuite was oriented to cover NG-Medium & NG-Large variant
  - NX needed to refine their algorithms for NG-Ultra with the help of end users

- OPERA H2020

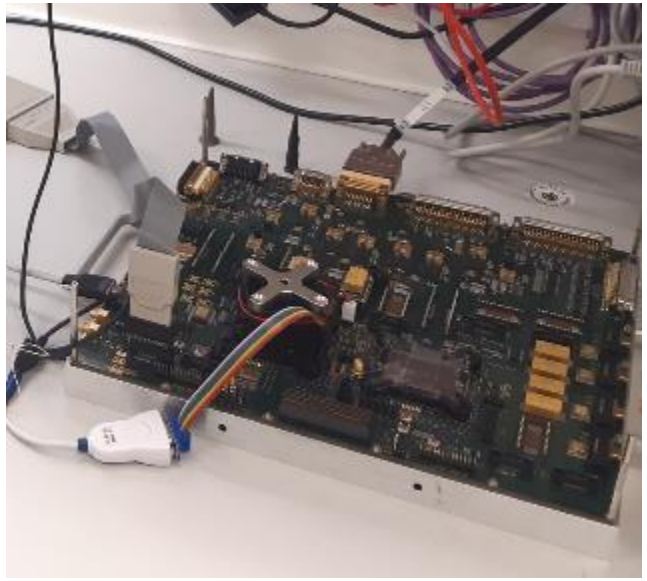
Horizon 2020 was the EU's research and innovation funding programme from 2014-2020

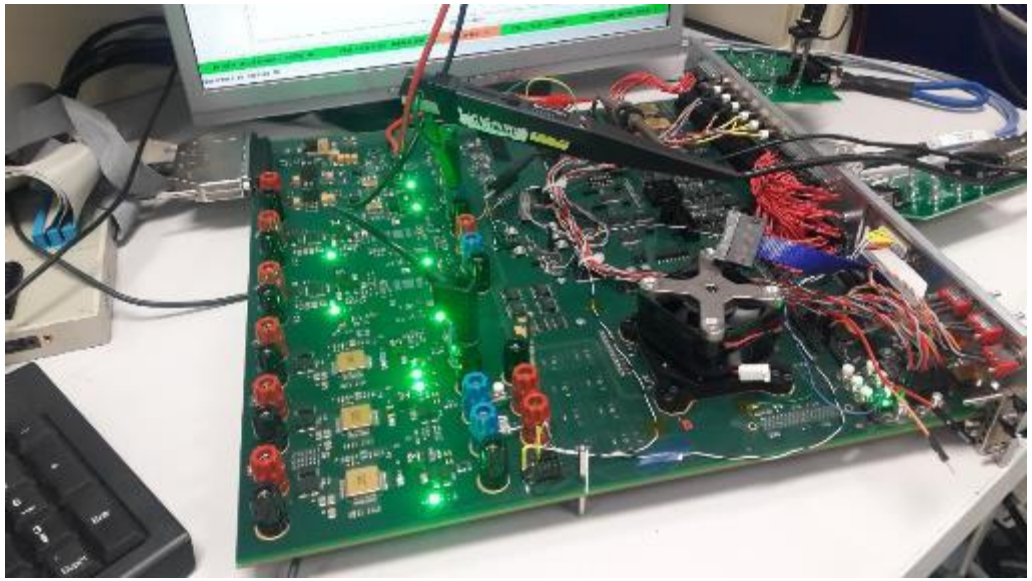
  - Objectives were
    - To assess the performances that can be achieved by some designs in NG-ULTRA technology and compare it with performances achieved in the reference technologies
    - Mature the NanoXmap toolsuite as fast as possible

It allows TAS to jump into NG-Ultra technology !

NG-Ultra on TAS Projects

- Several TAS projects with NG-Ultra as technical baseline are on going
  - Breadboards already under tests





  - Flight Model design (board layout / PCB manufacturing) in progress
  - NG-Ultra present in both platform & payload roadmaps, and competiveness for both commercial and institutional markets

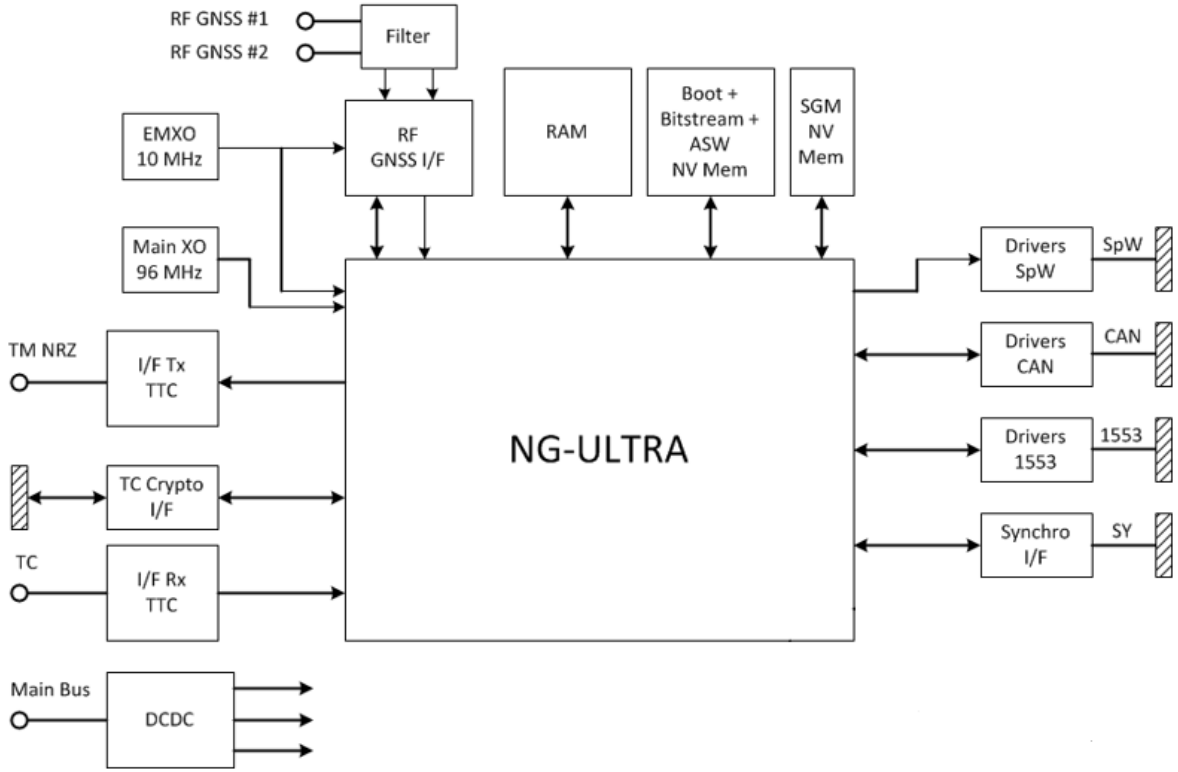
NG-Ultra is a reality !

OBC-D Architecture

- **The OBC-D is composed of**
  - The main board containing the NG-ULTRA and the drivers IF
  - A mezzanine board for the RF GNSS Rx function
  - A mezzanine board for the DCDC function

- **Maximum integration**
  - All computer functions in only one component
  - Simplified board design
  - Gain of mass from previous OBC generation (50%)
  - Gain of size/volume, power consumption & costs
  - Gain in performances

- **OBC-D development status**
  - CDR process on going including computer HW, FPGA firmware and Low Level SW : up to beg 2023
  - Functional validations on FUMO :
    - Started Q4 2021, with NG-ULTRA Run1 including FPGA firmware, Low Level SW and GNSS.
    - Delta validation completion after FUMO upgrade with NG-ULTRA Run2 : started September 2022
  - EQM & FM PCB in manufacturing



What about first use cases targeted by Airbus & TAS with NG-Ultra ?

NG-Ultra on ADS Projects – OPERA H2020

Horizon 2020 was the EU's research and innovation funding programme from 2014-2020

Several designs from low to higher complexity synthesized on both **NG-Ultra** and **RTG4** targets

- **Synthesis**
  - ✓Synthesis time → **similar performance** on both technologies
  - ✓Clock frequency → **similar performance**, Libero/RTG4 slightly better handles complex design
  - ✓Resource utilization → **performance in favor of NG-Ultra**: factor of 1.5 in nb of LUT, factor 2 improvement on large memories due to NG-Ultra larger BRAM, larger DSP width +++ for algo
- **Place and Route**
  - ✓Not easy to obtain a good layout in one run whatever the target → **similar performance**

Conclusion

- Satisfying tools performance, frequency ok (~100MHz reached), still margin for improvement

NG-Ultra relevance confirmed for ADS future projects !

NG-Ultra on ADS Projects - Platform OBC-Ultra

NG-Ultra present in both platform & payload ADS roadmaps

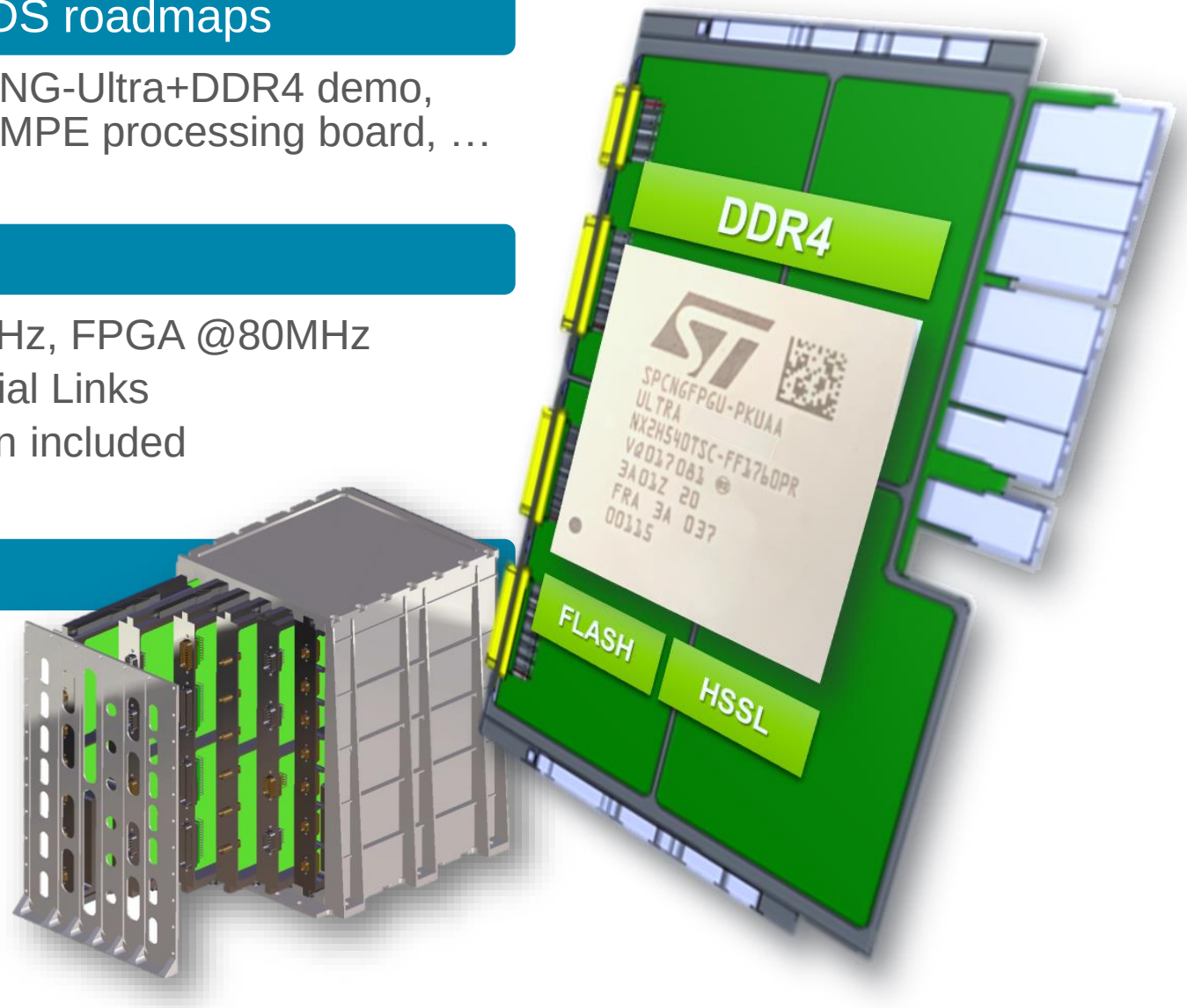
- Several boards under development → **Q2 2023** / NG-Ultra+DDR4 demo, **Q3 2023** / OBC use case demonstrated with OLYMPE processing board, …
- One main component = simplified board design

NG-Ultra-based OBC offers

- High performances multicore processing @600MHz, FPGA @80MHz
- NAND Flash + **DDR4 Memory** + High Speed Serial Links
- Enhanced Security features / Bitstream encryption included
- ADHA-compatible format

Highly integrated OBC

- Gain in performances confirmed through studies
- More than **500kLUT** compared to ~20kLUT for previous generation with RTAX2000
- More embedded functionalities
- **Very compact product**



NG-Ultra on ADS Projects - Payload Missions

Payload missions requirements analysis

- Very performant FPGA (fast clocking, huge matrix)
- High DDR bandwidth
- High Speed Serial Links

NG-Ultra suitability ? Confirmed !

- Huge 500k LUT matrix
- > 1000 **Large** DSPs
- DDR4 100Gbps
- HSSL

NG-Ultra-based board for payload processing under development at Airbus

- Ground demonstrator ready for **Q4 2023**

What can be concluded considering the overall picture and status on NG-Ultra ?

NG-Ultra in a nutshell

Key Features

- **Huge FPGA + High performance processing** quad-core ARM in a single chip
- **Rad Hard** confirmed by very promising results from radiation campaigns
- Flash + DDR interface with **very high level of protection** against radiation effects

Key Points

- Key component for **European non-dependence** on such strategic domain
- **Qualification** in Q4/2023 (organic package) & 2024-2025 (ceramic package)
- FPGA tool suite development + Software ecosystem status confirmed
  - **Confidence in tools capacity to meet performances** for complex designs use cases (cf OPERA)

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NG-Ultra is **unique** in the landscape
of available **Rad Hard** components

It is the only **European** FPGA solution **with a SoC**

It offers **performances** & **robustness** breakthroughs
with Huge FPGA + High performance processing

Tools are (now) at good **maturity** level
and continue to **improve**

NG-Ultra selected by ADS & TAS
as **technical baseline** on several on-going projects

Questions ?

AIRBUS

ThalesAlenia Space
a Thales / Leonardo company