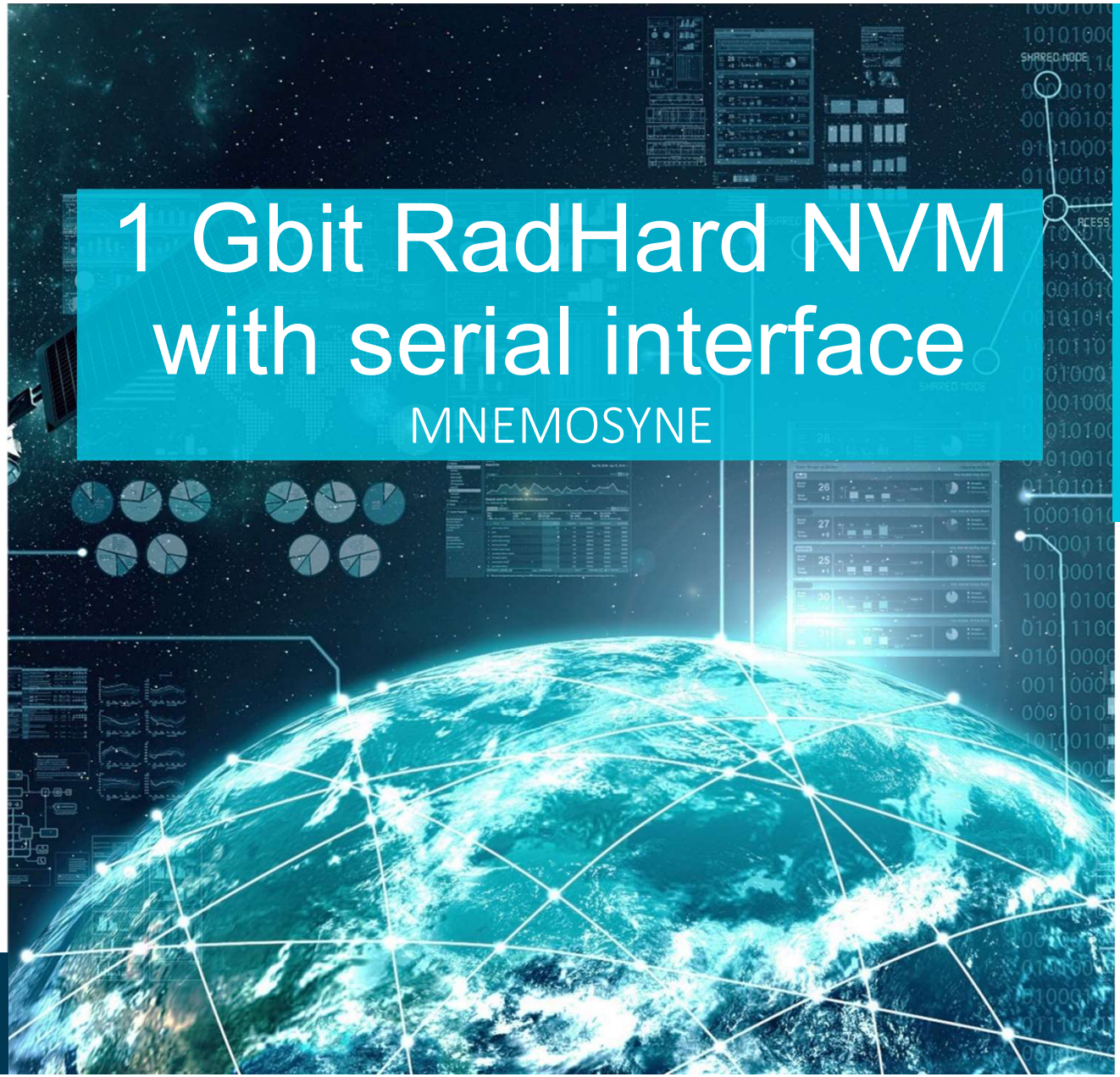


1 Gbit RadHard NVM with serial interface

MNEMOSYNE

Jeanne TONGBONG

ESCCON 23, Toulouse

March, 9th, 2023

AGENDA

MNEMOSYNE: Magnetic non-volatile Random Access Memory for space with serial interface

INTRODUCTION

- What is MNEMOSYNE project ?
- Project pillars
- Advantages forseen

FIRST DESIGN

- The test vehicle (TV)
- Rad-hard design techniques
- Tests and results

PRODUCTS

- Prototype
- Architecture
- Presentation
- Positioning

CONCLUSION

INTRODUCTION

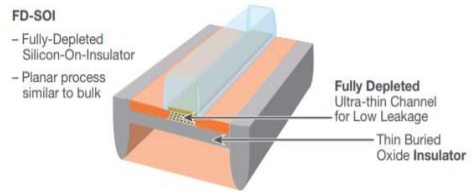
MNEMOSYNE: Magnetic non-volatile Random Access Memory for space with serial interface

- **Context:** Enhance EU independence on the space market
- Funded by **EU Horizon 2020** research and innovation program
- **Goal:** Design and prototype the new generation of rad-hard high density NVM with serial interface based on most-advance and matured technology
- Applications:
  - **Boot code storage** for microcontrollers and microprocessors
  - FPGA **configuration bitstream storage**
- **Consortium members:**

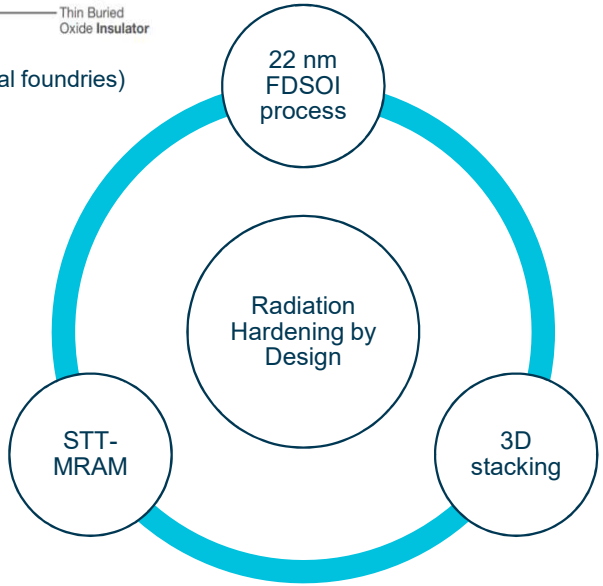
3plus a HEICO company · imec · Università degli Studi di Padova · TRAD Tests & radiations · beyond gravity · NanoXplore

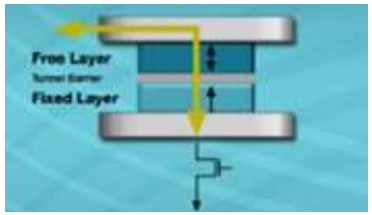
MNEMOSYNE project

Project pillars

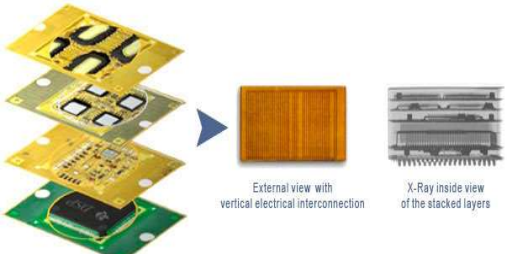


FD-SOI Technology (Credit Global foundries)

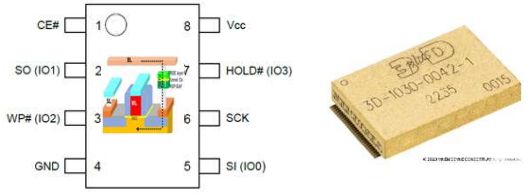




STT-MRAM Memory Cell (Credit Everspin)



3D stacking (Credit 3D PLUS)



INTRODUCTION

Advantages forseen

- STT-MRAM technology provides **SEU immunity to memory cell.**
- FD-SOI (Fully-Depleted Silicon-On-Insulator) process brings **SEL immunity.**
- 22nm FD-SOI provides: **up to 40% die scaling, and nearly 70% power saving** relative to the standard 28nm node, or similar power efficiency to FinFET technology**.**
- 3D PLUS technology is used to **increase the device density.**

2 FIRST DESIGN

Test vehicle

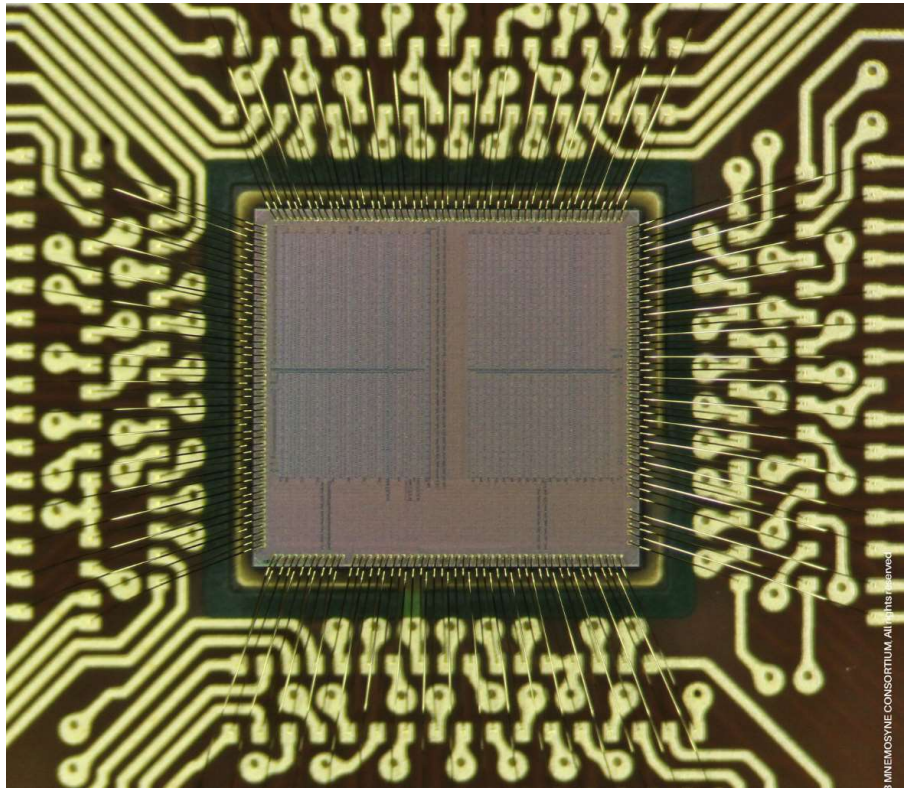
- A 64 Mb test vehicle was manufactured and tested during 2022 Summer.
  - STT-MRAM memory arrays with embedded ECC
  - A memory controller
  - A fuse-based read-only configuration memory
  - A Power Management Unit (PMU)
  - Two SPI interfaces (1.8 V and 3.3 V).

Test vehicle module

FIRST DESIGN

Test vehicle: Rad-hard design techniques

- Rad hard design techniques on control logic and interfaces
  - Redundancy, restricted cell sets on SEU critical parts.
  - SET immune on clock and reset trees
  - Glitch filters on strategic nodes
  - Derating accounting for device aging and TID.
  - Leakage reduction (body bias, process)



Test vehicle ASIC

2 FIRST DESIGN

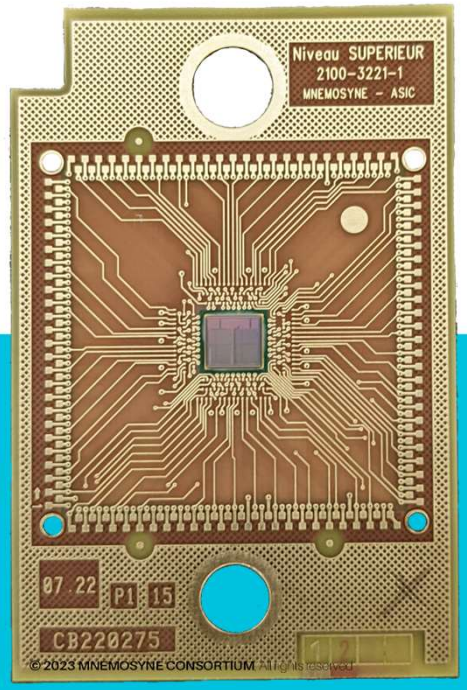
Results summary

TID > 100 krad(Si)

SEL/SEU LETh > 60 MeV.cm²/mg

1000h Life test passed with 3Θ measurements

QSPI/SPI interface validated

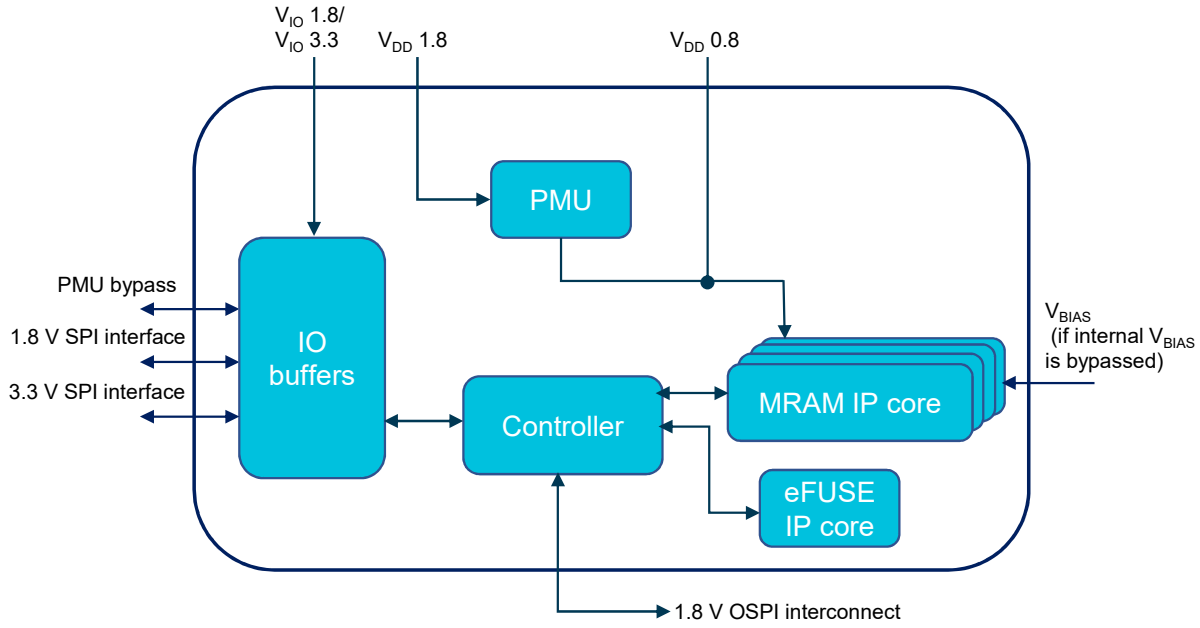


MNEMOSYNE TV ASIC bonded

3 PROUCTS

128 Mbit Prototype

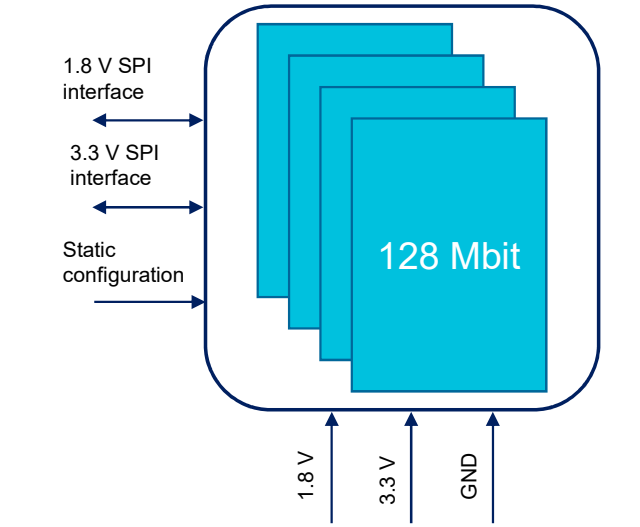
- Design update
- Goals:
  - Density increase
  - TV errors correction
  - EEPROM interface
- Manufacturing in progress
- Available by Q2‘23



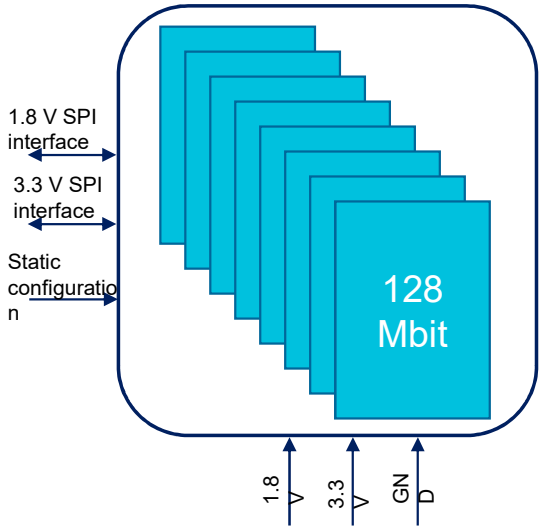
128 Mbit prototype architecture

PRODUCTS

Architecture



512 Mbit



1 Gbit

3 PRODUCTS

Up to 1 Gbit rad-hard NVM with serial interface

KEY FEATURES

- 512 Mb, 1 Gb density
- Up to 100 MHz
- Embedded ECC
- Power management embedded
- 1.8 V SPI interface (3.3 V optional)
- SPI, QSPI, DSPI, OSPI modes supported
- 100 k P/E cycles
- 20 years data retention

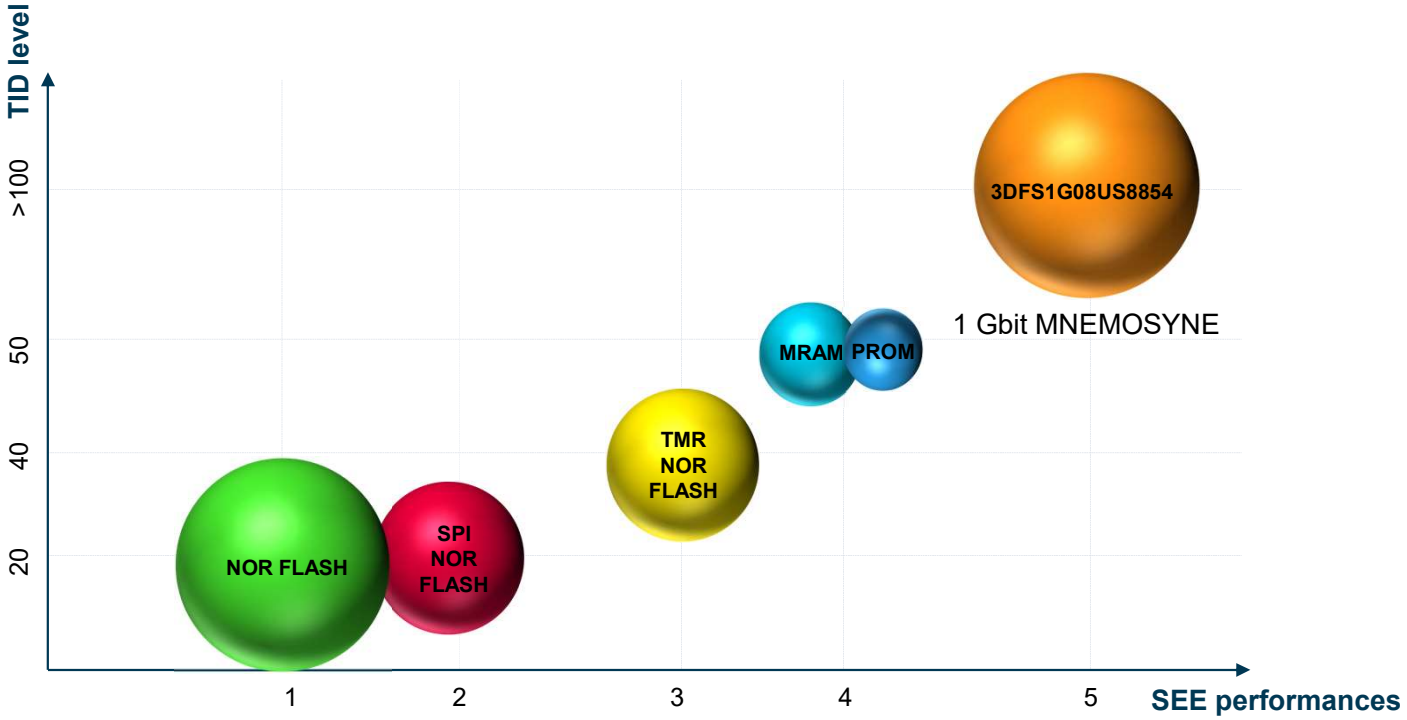
RADIATION PERFORMANCES

- TID > 100 krad(Si)
- SEL > 60 MeV.cm²/mg
- SEU > 60 MeV.cm²/mg
- SET > 60 MeV.cm²/mg
- SEFI > 60 MeV.cm²/mg

The SEE LET threshold would be tested in other facilities with 80 MeV.cm²/mg target

CONFIGURATION MEMORIES

3D PLUS portfolio update

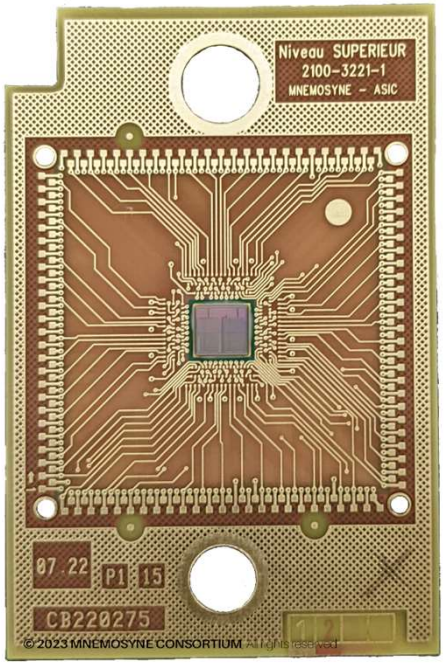


Ball size ~ density
1= lower SEE
2= medium SEE
3= good SEE
4= very good SEE
5= excellent SEE

4 CONCLUSION

- The Next Generation Radiation Hardened space serial Non Volatile Memory up to 1Gb density with proven TID >100Krad(si) and SEL/SEU LET threshold > 60MeV.cm²/mg.
- This product while enhancing EU independence on the space market will be the best in class of program/configuration memory combining that level of reliability with such density.
- **512 Mbit/ 1 Gbit density modules available by Q4 ‘23**

- Authors would like to thank the European Commission and all the members of the consortium that are driving this project.
- MNEMOSYNE project used the results of another Horizon 2020 project named EFESOS.



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