Training Course on Printed Circuit Board Technology

20 Nov 2023
Materials and Processes Section TEC-MSP
Stan Heltzel

ESA-TECMSP-HO-2023-003430

ESA UNCLASSIFIED – For ESA Official Use Only

Outline

1. Introduction, manufacturing
2. Qualification, standards, COTS, mission class
3. Design, technology development
4. Procurement, supply chain
5. Quality, process engineering
6. Project review in MPCB
7. Project qualification / RFA
8. Inspection, failures

Who am I?

1994 Moved to Leiden
to study physics

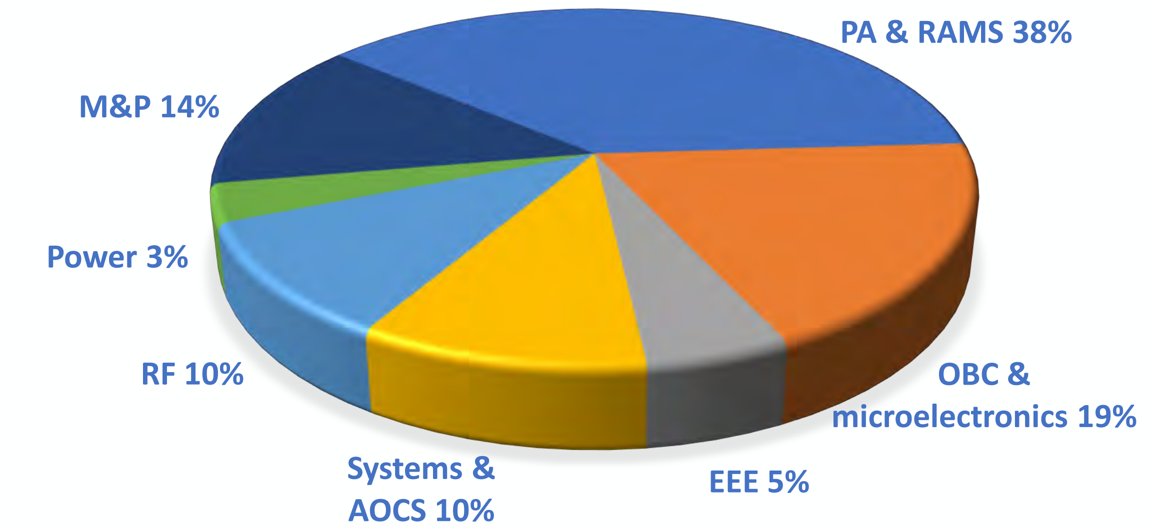
2001 esa
environmental testing

2008 PCB

Objectives of a PCB training course

Holistic description of PCB technology in ESA

- Design
- Technology drivers and development
- Quality assurance, qualification
- Project review, procurement
- Failures

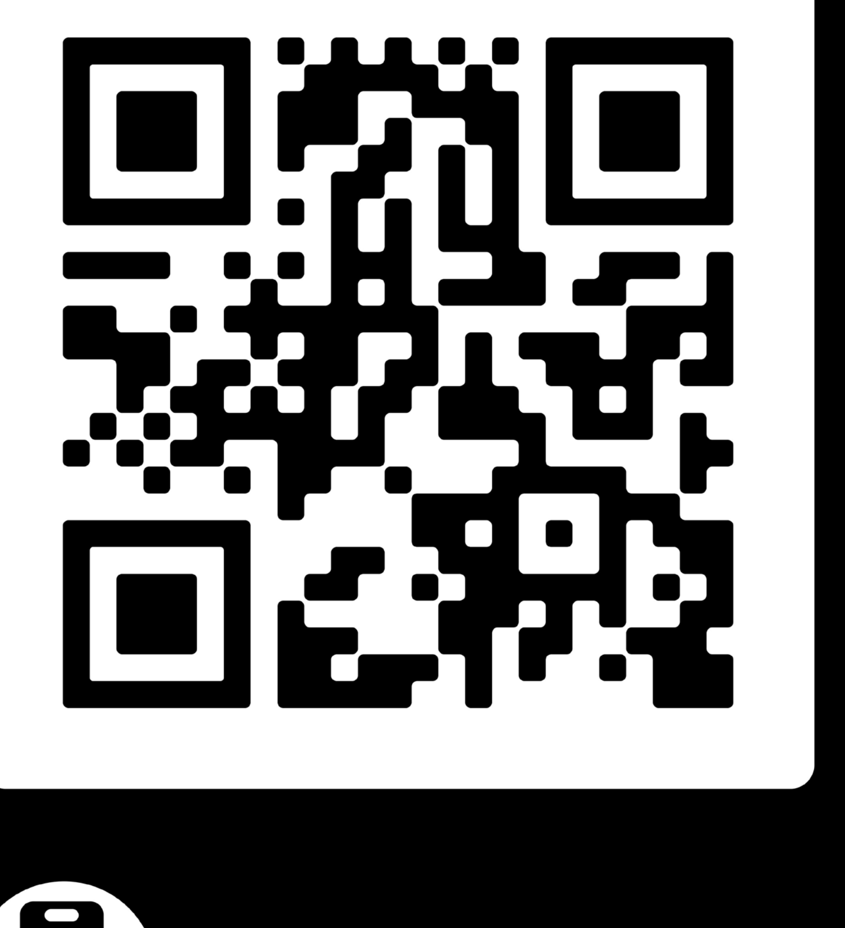


Technical detail for selected relevant topics

Provide a better generic understanding of limitations and critical issues.

Provide guidelines on autonomous review and expert involvement.

Objectives of a PCB training course



QR code to the questionnaire for

PCB & EA training course.

Alternatively, access to the survey may be obtained using this simple URL:

https://qrco.de/pcbea

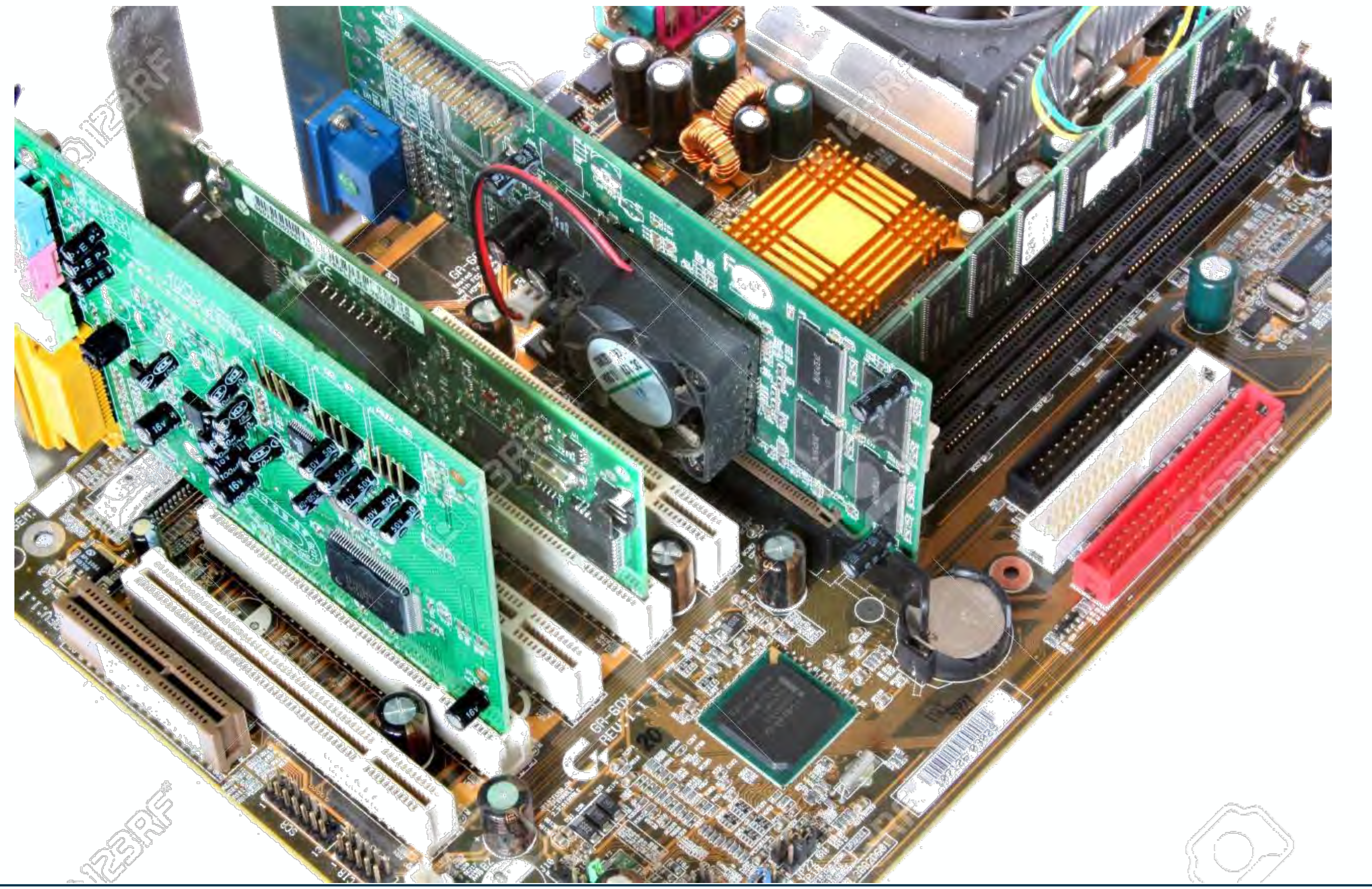
Download this presentation at

www.escies.org/pcb

What are PCBs?

Printed Circuit Boards (PCB) are a complex combination of materials to provide a stable **mechanical** and **thermal** platform for the **electrical** interconnection of components.

Electronic Materials & Processes are a cross-cutting engineering discipline.



Anatomy of a spacecraft

instruments

mechanisms

power control & distribution

thermal control

structures

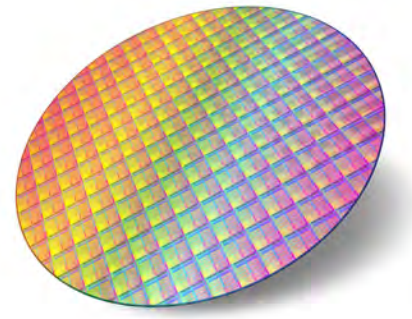
power & propulsion

data processing & interfacing

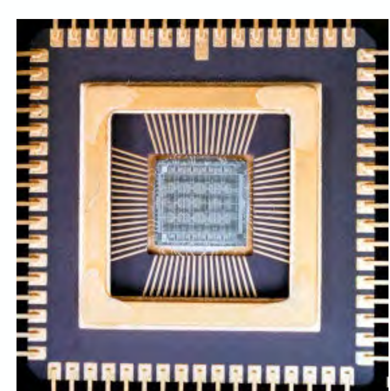
PCBs are the **nerves and veins** of the spacecraft.

Electronic packaging levels

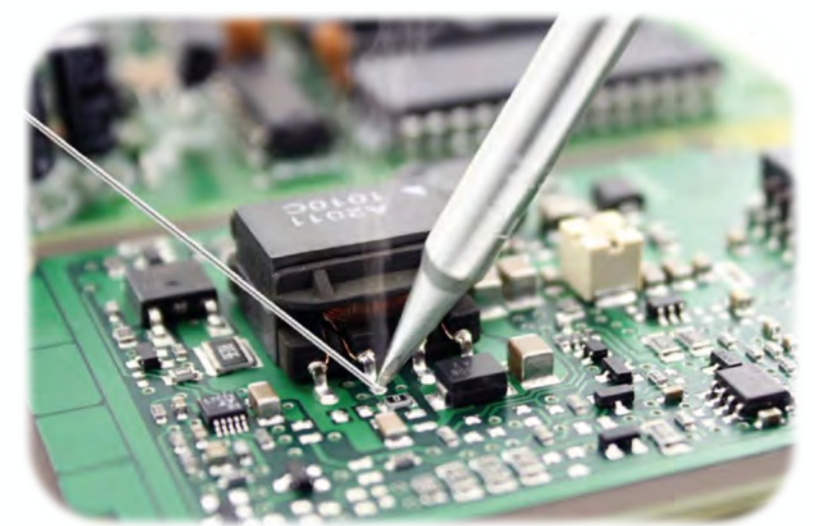
Level 0 Chip, bare semiconductor die



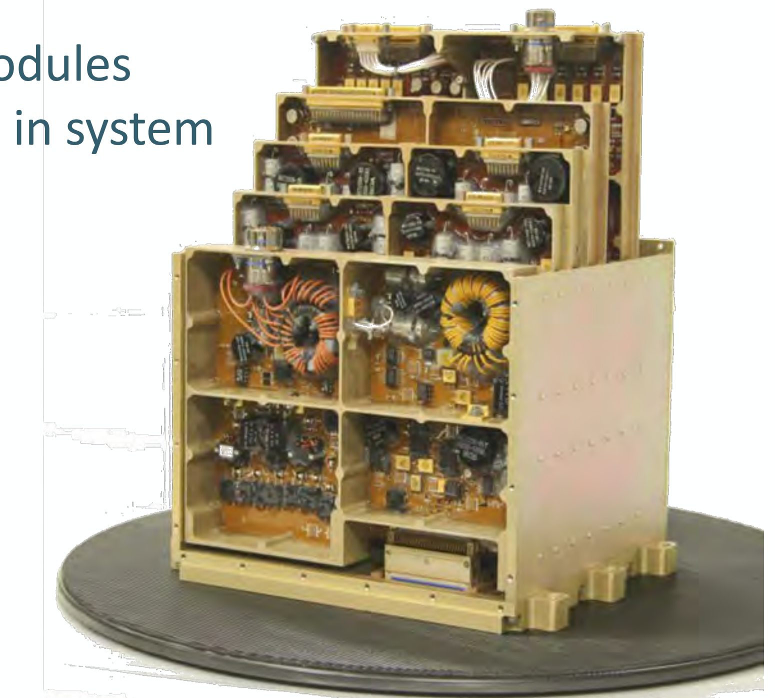
Level 1 EEE component, back-end packaging



Level 2 Assembled EEE components on PCB



Level 3 Modules integrated in system



Electrical routing in a PCB

Plated through-hole interconnecting layer 1 to layer 4,

passing through clearances in the planes on layer 2 and 3.

Pad and track on outer layer

Plated hole wall

(non-functional) pads

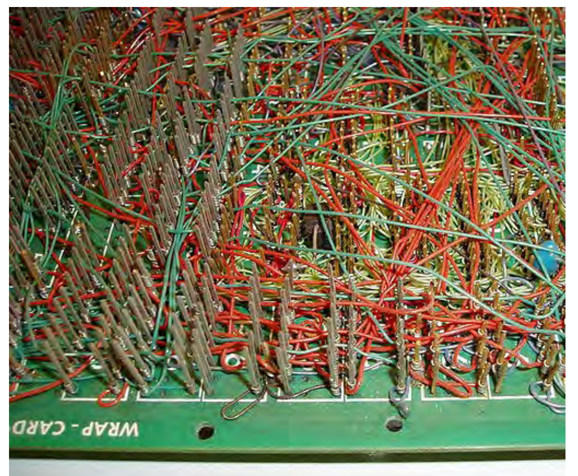
Clearance hole in plane (no connection)

Plane layer

History of PCB

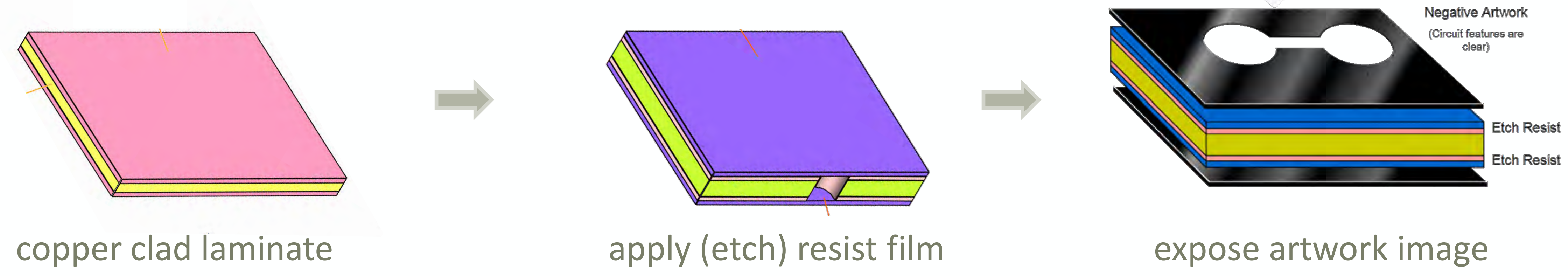
<1960	Point-to-point construction and wire wrap
<1925	Development of lamination, print-and-etch, plating processes
1936	Paul Eisler (AUS) patented the PCB, as part of a radio set.
1943	US military developed PCB technology for proximity fuzes in WWII.
1952	Motorola introduced PCBs in consumer electronics.
1950s	Development of Cordwood circuit and Integrated Circuit
1980s	Surface mount started to replace through-hole assembly.
1990s	Use of computers and CAD software enabled complex routing using multilayers, rigid-flex and microvias.

1948 Motorola TV ↑
point-to-point wiring ↓



Cordwood circuit

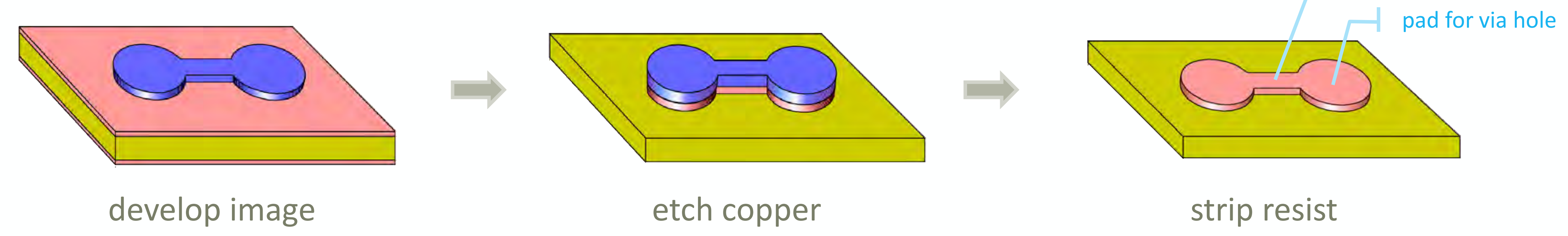
PCB manufacturing – inner layer pattern



copper clad laminate

apply (etch) resist film

expose artwork image



develop image

etch copper

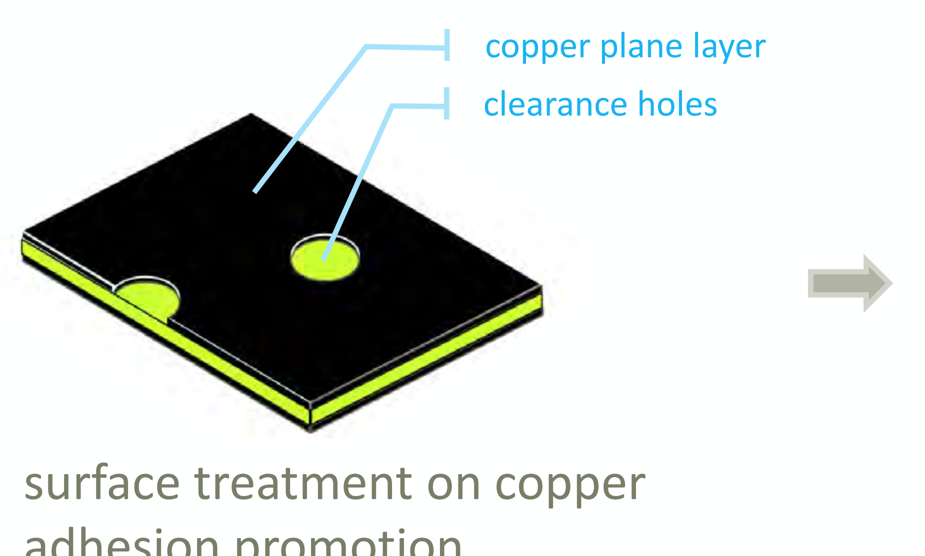
strip resist

Manufacturing – inner layer pattern

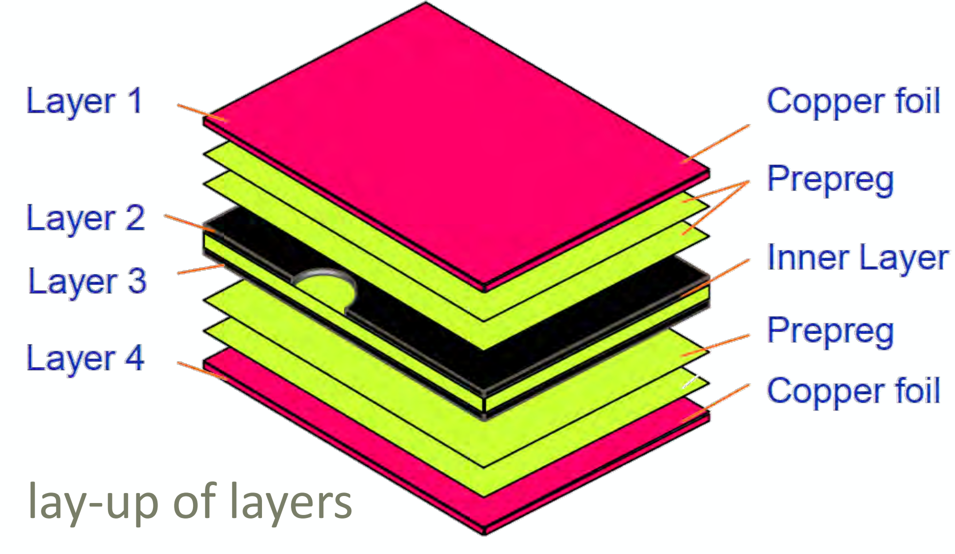
Development Etch Strip DES line

https://youtu.be/Su0PIw5OaYQ?t=33
0:33-2:39

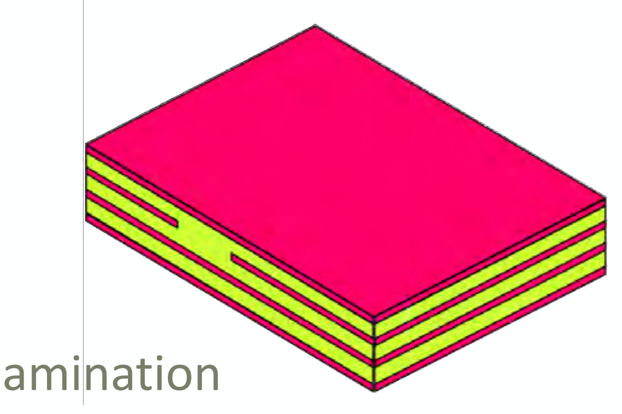
Manufacturing – lamination, drilling



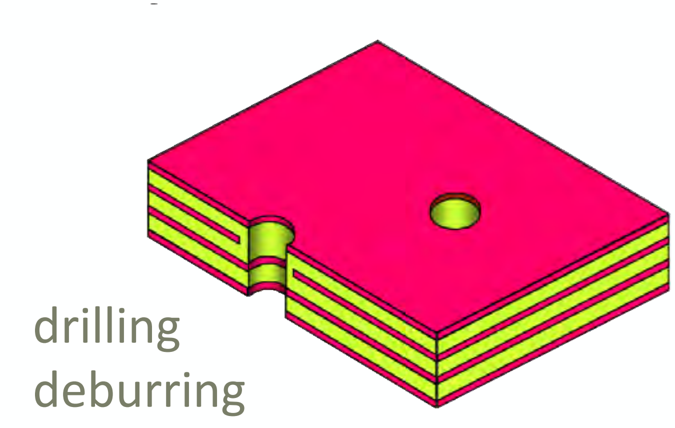
surface treatment on copper
adhesion promotion



lay-up of layers



lamination



drilling
deburring

Manufacturing – lamination, drilling

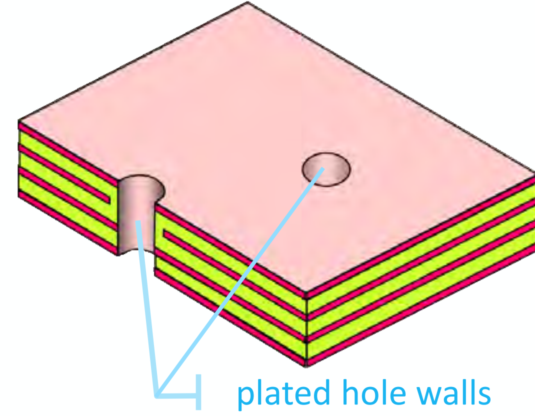
Lamination press

https://youtu.be/Su0PIw5OaYQ?t=216
3:36-5:39

Drilling

https://youtu.be/Su0PIw5OaYQ?t=385
6:25-7:45

Manufacturing – plating



- desmear: plasma, permanganate
- microetch (on glass, resin, inner layer Cu)
- catalyst: palladium
- chemical copper (electroless)

- electroplate copper (panel)

for sequential build-up:

Develop pattern and
proceed to another cycle for lamination/drill/plating.

Manufacturing – plating

electroless Cu

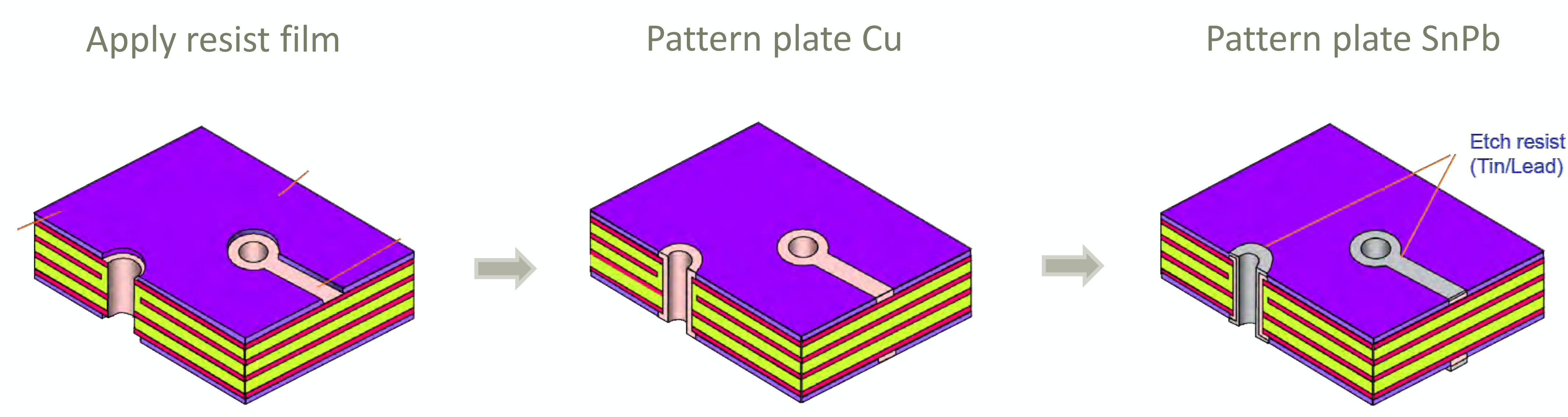
https://youtu.be/Su0PIw5OaYQ?t=465
7:45-8:44

and

electroplated Cu and SnPb

https://youtu.be/Su0PIw5OaYQ?t=626
10:26-11:55

Manufacturing – outer layer pattern



Manufacturing – outer layer pattern

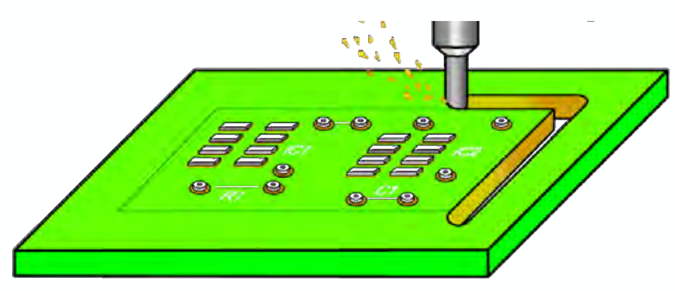
strip resist film

copper foil +
panel plated copper

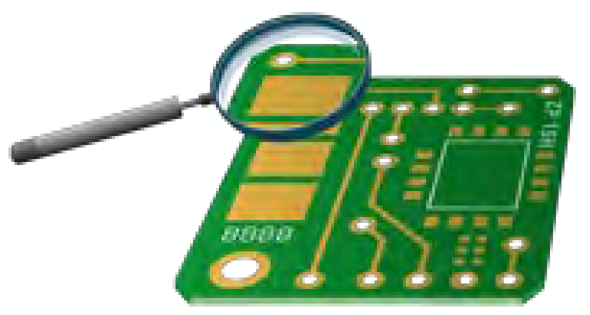
etch copper
reflow the tin-lead surface finish

optional:
solder mask &
alternative surface finish

Manufacturing – finishing up



machining of PCBs and coupons from production panel



final inspection & test
packaging

PCB manufacturing processes:

- Subtractive: etching, drilling
- Additive: plating, lamination

Via cross section

500 µm

Rigid laminate with woven glass reinforcement

prepreg

Flex laminate

Hole wall, plated Cu

Inner layer pads, Cu foil

Surface finish reflowed SnPb

Life cycle of a PCB

Quality Specification → Design → Procurement PCB MRR → Qualification: - Technology - Manufacturer - (Project qual) → Materials & Processes Control Board

Procurement PCB MRR ↓ Outgoing Inspection → Accelerated Coupon Test → Incoming inspection

→ Assembly MRR → KIP/MIP → Unit level acceptance testing → DRB → AIT

Procurement cycle

Project review

Assembly cycle

Integration

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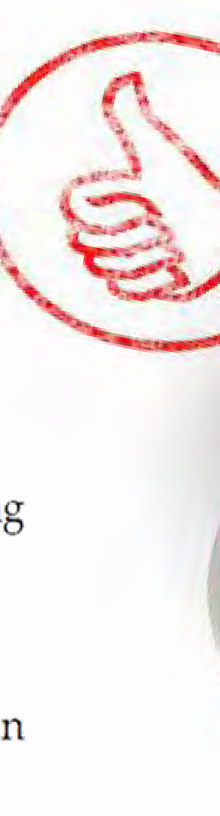
Quality standard

5.1 Qualified PCBs

a. Qualified PCBs for space applications shall meet all the following conditions:

1. the PCB is procured in conformance with clauses 6 and 8,
2. the PCB is procured from a PCB manufacturer that is qualified in conformance with clauses 5 and 7 and as specified in the PID,
3. the PCB design is in conformance with the requirements of ECSS-Q-ST-70-12.



ESCIES

E uropean

S pace

C omponents

I nformation

E xchange

S ystem

www.escies.org

www.escies.org/pcb/

ESCIES
European Space Components Information Exchange System
ESCC

Our activities | Technologies | Other resources | Account | Logout | Search:

ESA Components Radiation
ESA Components Activities
EEE Testing Capabilities
ECI
ESA PCB Qualification
ESA SMT Verification
Miscellaneous

- Virtual Event
ailable on ESCIES
view

ESCCON 2021

The European Space Components Conference was a Virtual Event held from 9 -11 March 2021. Presentations are Available NOW, please click HERE

Start

What's new on ESCIES

ESCC Specifications | QPL | QML | ESCC HPCL | EPPL

ESA Radiation Activities | ESCC brochure | ECI | PCB qualification | SMT verification

Applicable standards

ECSS-Q-ST-70-12 PCB design
(2014 - present)

ECSS-Q-ST-70-60 PCB qualification and procurement
(2018 - present)

Several ESA memos address ad hoc guidelines.

ESCIES: Printed Circuit Boards

ESA Approved Manufacturers and Qualification Status of PCBs

- ESA Qualification Status of PCB technology
- ESA Approved PCB Manufacturers - contact details

ECSS standards

- ECSS-Q-ST-70-10C Qualification of printed circuit boards (superseded by 70-60)
- ECSS-Q-ST-70-11C Procurement of printed circuit boards (superseded by 70-60)
- ECSS-Q-ST-70-12C Design of printed circuit board (active)
- ECSS-Q-ST-70-60C Qualification and procurement of printed circuit boards (active)

- Gerber data for THB test vehicle as per clause 9.7.2 from ECSS-Q-ST-70-60
- Gerber data for CAF test vehicle as per clause 9.7.3 from ECSS-Q-ST-70-60

Active ESA memos and checklists

- QT/2014/361/SH ECSS standards for PCB design
- ESA-TECMSP-MO-7424 Project qualification of Thermount 85NT PCBs
- ESA-TECMSP-MO-11532 ECSS standards for PCB qualification and procurement
- ESA-TECMSP-MX-11559 Checklist to ECSS-Q-ST-70-60 for PCB manufacturers
- ESA-TECMSP-MX-11320 Checklist for ENIG ENEPIG ENIPIG finish
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- ESA-TECMSP-MX-14192 Input to checklist for MRR
- ESA-TECMSP-MX-16451 Compliance matrix ECSS vs IPC6012DS
- ESA-TECMSP-HO-19825 PCB training course presentation (18MB)
- ESA-TECMSP-TN-19672 Microvia process guidelines

Applicable standards

Old flow:

ECSS-Q-ST-70-12C PCB Design → ECSS-Q-ST-70-10C PCB Qualification → ECSS-Q-ST-70-11C PCB Procurement → ECSS-Q-ST-70-38C Assembly Surface Mount Devices → ECSS-Q-ST-70-08C Assembly Through-Hole Devices

New flow:

ECSS-Q-ST-70-12C PCB Design → ECSS-Q-ST-70-60C PCB Qualification and Procurement → ECSS-Q-ST-70-61C Assembly PTH+SMT

Requirements in PCB & EA

Quality and Product Assurance 33%

PCB & EA 10%

Roles and definitions

PCB Manufacturer

Procurement Authority (customer of the PCB manufacturer; supplier to ESA)

Design Authority

Assembler

Fabless…?

or same company

Qualification Authority (ESA/CNES, also referred to as 'customer' of a project)

PCB	Printed Circuit Board (in US: PWB - Printed Wiring Board)
PCB	Parts Control Board
PCBA	PCB Assembly (= module)
EA	Electronic Assembly
M&P	Materials and Processes
EM&P	Electronic Materials and Processes, i.e. PCB and Electronic Assembly
MPCB	Materials and Processes Control Board

Acronyms

AAD	Area Array Device (CGA, BGA)
CGA	Column Grid Array
CAF	Conductive Anodic Filament (type of electrochemical migration)
HDI	High Density Interconnect
IST	Interconnect Stress Test
IPC	Industrial Policy Committee
IPC	Global electronics industry association (formerly: Institute for Printed Circuits)
PID	Process Identification Document
PTH	Plated Through Hole
SMT	Surface Mount Technology
OEM	Original Equipment Manufacturer
EMS	Electronics Manufacturing Service provider (assembler)
DPA	Destructive Physical Analysis (microsectioning)
FAI	First Article Inspection

Qualification scheme

ESA and CNES are qualification authority for PCB technology.

- Support letter from key customers to initiate qualification
- Testing and evaluation of samples in ESTEC lab
- Audit of company, supported by key customers
- 2-yearly renewal by audit and sample evaluation
- Evaluation of major Process Change Notifications PCN

ECSS-Q-ST-70-60

§ 5.4, 5.5, 5.13, 5.15

Qualification status

The comments on failed qualification renewal are provided for transparency. A prudent customer is encouraged to enquire with the PCB manufacturer if the reason for the failed and ongoing renewal can have an impact on their orders. However, normally this should not be the case.

As long as the “qualification status” shows “qualified” there are no restrictions, even with a failed renewal.

See 5.16c of ECSS-Q-ST-70-60.

ESCIES
European Space Components Information Exchange System

ESCC

Our activities | Technologies | Other resources | Search:

Company	Build	Laminate	PID reference	Qual. Expiration	Qual. Status	Comment, [ref to ECSS-Q-ST-70-60]	Status date	Reference
ACB	sequential rigid	Polyimide	PID_SeqRigid_v180618 ed4	Oct-21	Qualified		Apr-20	ESA-TECMSP-LE-018533
	sequential rigid-flex	Polyimide	PID_FR_v190531 ed4	Oct-21	Qualified		Apr-20	ESA-TECMSP-LE-018533
AMPHENOL-INVOTEC	sequential rigid	Polyimide	SM18T.iss.04	Jul-22	Qualified		Jul-21	ESA-TECMSP-LE-023847
	sequential rigid-flex	Polyimide	SM19T.iss.04	Dec-21	Qualified		Nov-19	ESA-TECMSP-LE-015965
CIRETEC - Elvia	sequential rigid	Polyimide	PID 2015-02 ind 01	Mar-22	Qualified		Mar-21	ESA-TECMSP-LE-022352
	sequential rigid-flex	Polyimide	PID 2015-03 ind 02	Sep-20	Qualified	Renewal failed and ongoing [5.16c]	Sep-18	ESA-TECMSP-LE-022619
Issue date:	16/07/2021							

Qualification renewal failed

5.16b “In case nonconformances are observed during qualification renewal, the qualification authority should indicate the qualification status as **“not qualified”** until acceptable completion of the qualification renewal, including a comment to the qualification status in conformance with the requirement 5.12c, except in case of 5.16c.”

5.16c “In case the PCB manufacturer demonstrates that nonconformances observed during qualification renewal are of a **one-time occurrence**, the qualification authority should indicate for a maximum period of 6 months the qualification status as **“qualified” with a comment to identify the failed and ongoing qualification renewal**.”

NOTE 1 “A one-time occurrence of a nonconformance **does not invalidate the qualification** of other orders in case the efficiency of outgoing inspection is verified…”

ECSS-Q-ST-70-60

Scope of qualification - environmental

Standard qualification PCB assemblies covers for an operational range of -55 to +85 degC.

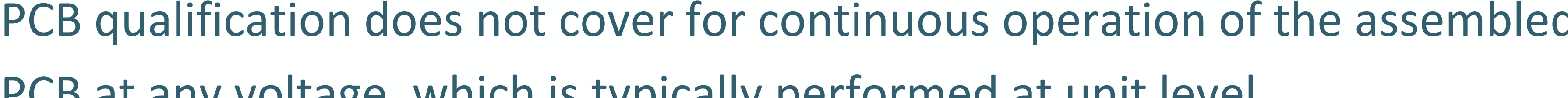
ECSS-Q-ST-70-60 § 5.1b, 70-61 § 13.2.1a

Self-heating of conductor $\Delta T < 10$ degC, Tmax < 95 degC.

ECSS-Q-ST-70-12 § 13.6.2

Voltages > 500 V shall be subject to specific qualifications of the design.

ECSS-Q-ST-70-12 § 13.8.2l



PCB qualification does not cover for continuous operation of the assembled PCB at any voltage, which is typically performed at unit level.

Bare PCBs are not subject to tests and requirements for rating and derating.

ECSS-Q-ST-70-60 § 9.6.4a Note 2

Dynamic applications (flex PCB) shall be project qualified.

ECSS-Q-ST-70-60 § 5.3.2g

Scope of qualification - products

Ceramic PCBs as per ECSS-Q-ST-70-60.

Thick / thin film processes on ceramic substrates as per ESCC-2566000.

Flexible PCBs as per ECSS-Q-ST-70-60, including “flat cable”, “flexprint”, “ribbon flex”, “FFC”. Also “sculptured flex” are included.

Heaters as per ESCC-4009.

Cables as per ESCC-3901.

Bus bars, slip rings (pancake), antennae, Insulated Metal Substrate IMS as per ECSS-Q-ST-70-60.

ECSS-Q-ST-70-60 § 5.2, 5.3

COTS

Guidelines for the utilization of COTS components and modules in ESA ESA-TEC-TN-021473 iss 2.0 16-03-22

COTS EEE components and modules

Cost per item →

"Reliability" expectation →

← Risk taking

Trace code	**Unclear Trace code homogeneity** (lot homogeneity aimed at but not sure)		**Expected Trace code homogeneity** (expected lot homogeneity, including diffusion mask and wafer fab for radiation sensitive components)		
Area	**" Informative " area** (no covered <u>yet</u> by ECSS or ESA requirements)		**"Normative" area** (covered by ECSS requirements)		
Approach	**Set of guidelines elaborated and agreed among experts**		**Use ECSS-Q-ST-60-13C (for COTS EEE components)** Use ECSS-Q-ST-60C (for HiRel EEE components)		
Subsystem (equipment, module) criticality categories for modules, equipment, subsystems or systems	**Q_2**	**Q_1**	**Q0**		
			Class 3	Class 2	Class 1

COTS

Normative standards	COTS		ECSS	
Criticallity category	Q2	Q1	Q0	No COTS
PCB	IPC class 2	IPC class 3 with amendments in Annex 5	RFA for use of IPC, as per 7.7.2p of ECSS-Q-ST-70-60	ECSS-Q-ST-70-12/60
Electronic Assembly	IPC class 2	IPC class 3 with amendments in Annex 6	RFA for COTS assembly as per Annex 6	ECSS-Q-ST-70-61

Mission classification

	1	2	3	4	5
Performance spec					
Design spec					
Project qual					
MPCB					
MRR					
Outgoing inspection					
IST					
Surface finish					
Incoming inspection					
Company qual					
Technology qual					
Assembly MRR					

ECSS

IPC class 3 + space

IPC class 3

IPC class 2

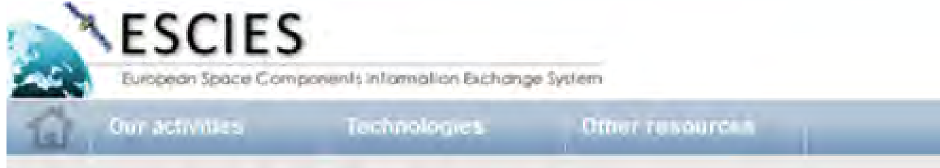
IPC standards

IPC-6012E class 1, 2, 3 (class 3 is for high-rel)

IPC-6012ES space addendum (f.k.a class 3A)

ESA-TECMSP-MX-16451

Compliance matrix ECSS vs IPC6012DS



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Main concerns:

IPC allows potentially a wide range of designs, some of which are undesirable/challenging.

IPC usually does not include qualification testing, assessment by a qualification authority, company audits.

IPC compliance is a unilateral declaration of conformance to 1000s of requirements by a checkbox on CoC from PCB manufacturer.

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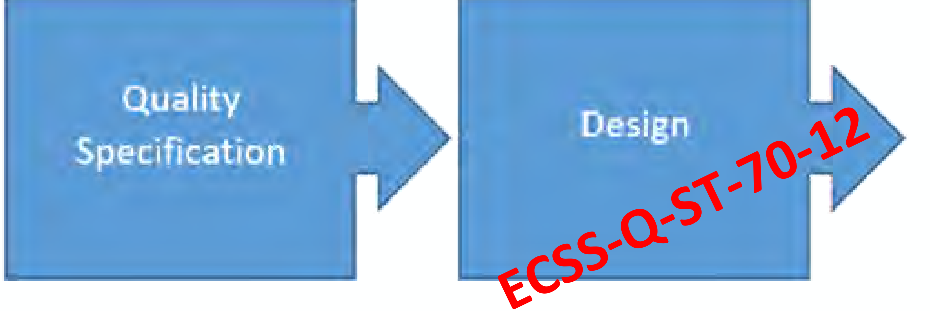
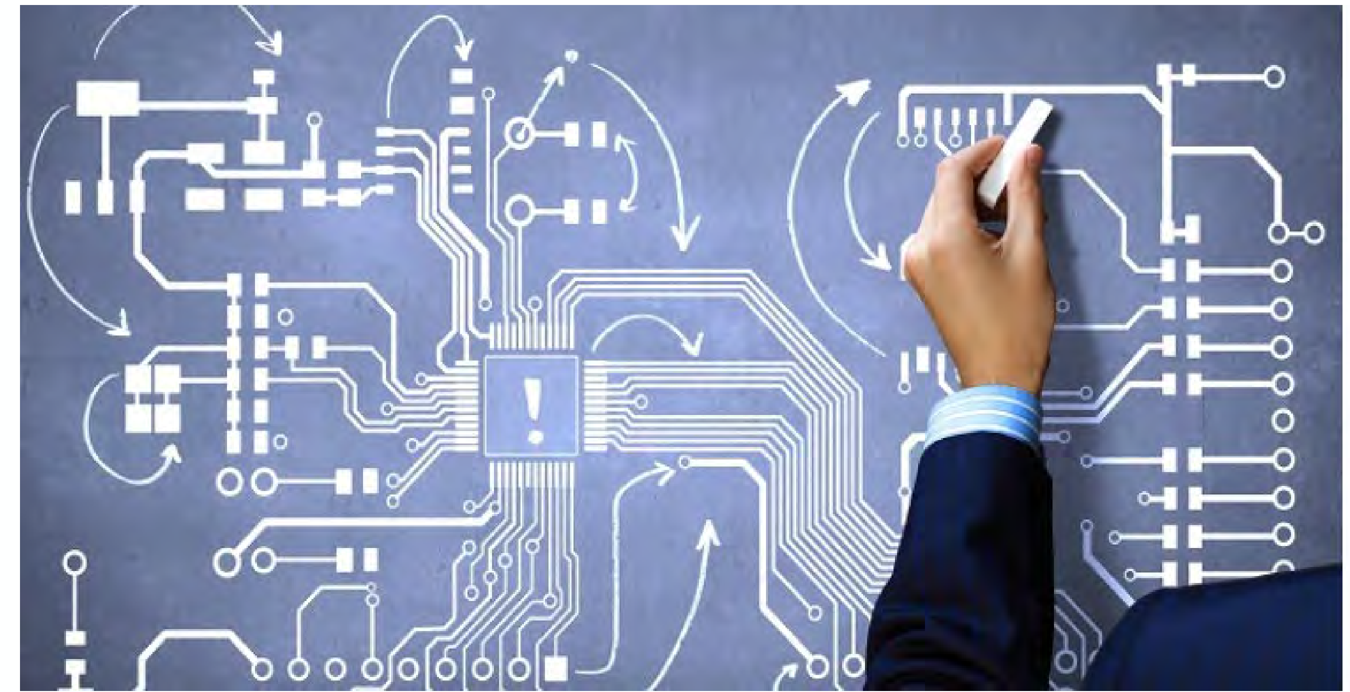
Design





Design - Functionality vs Reliability

Operational performance requirements at equipment level **may** not be unifiable with reliability requirements at PCB level.

- Assembly of EEE components
- Complex routing in PCB
- Signal integrity and RF
- Current carrying capacity
- Voltage rating and double insulation
- Dynamic mechanisms
- Thermal and mechanical environment

Design with margin

ECSS-Q-ST-70-12

§ 4.3 and 6.1a

Review Items can impact **manufacturability** and **reliability**.

"Design for Manufacturability DfM, Design for Reliability DfR"

Reliability should be taken (better) into consideration when defining the **performance** of an equipment.

"We have to use this design if we want to meet the performance requirements."

Design standard specifies **MINIMUM** dimensions permitted. This does not mean they can be used in combination with all technology. Check with PCB manufacturer!

"(Inexperienced) designers use minimum dimensions,

not because they must, but because they can."

Designing with several technology features that each are within, but at the limit of, the capability of the manufacturer is a well-known pitfall that can easily generate **an unqualified, unreliable or even an unmanufacturable PCB**.

Technology design choices

5.11 PID

a. The PCB manufacturer shall issue the PID in conformance with the DRD of Annex D.

b. The specific parts of the PID shall be issued, in conformance with D.2.1.2, for the following PCB technologies in separate documents:

1. Polyimide rigid
2. Polyimide rigid/flex
3. Epoxy rigid
4. Epoxy rigid/flex
5. HDI
6. RF
7. Flexible
8. Sculptured flex
9. Low thermal expansion materials

Technology design choices

Dielectric materials:

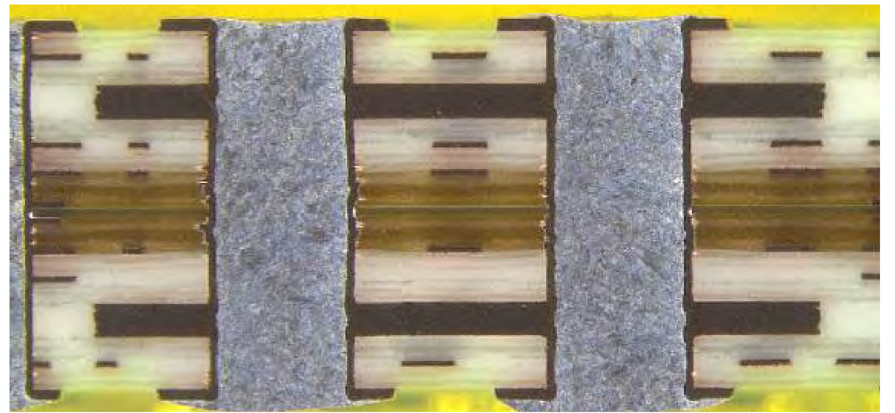
polyimide – Arlon 35N, 85N, Ventec VT901, Neltec 7000-3

epoxy (FR4) – Isola 370HR, IS420

high speed – Rogers RT/Duroid 6002, 5880, CLTE, Panasonic Megtron 6, 7N, ECM EM528, Isola Tachyon 100G

low-CTE – Arlon 85NT (aka Thermount), Showa Denko (Hitachi) MCL-E-700G and -705G

flex – Dupont Pyralux, Panasonic Felios, Thinflex



Build-up:

double sided, multilayer, sequential, HDI

copper weight, dielectric thickness, glass style,

heat sinks, CTE limiting inserts (Invar sheets, Molybdenum inserts)

Lay-out and build-up

2.87mm ±10%

Layer	Material	Thickness
1		0.017
	ARLON Polyimide 35N	0.100
	ARLON Polyimide 35N 106	0.056
2		0.035
	ARLON Polyimide 35N	0.125
3		0.035
	ARLON Polyimide 35N 106	0.056
	ARLON Polyimide 35N	0.100
4		0.070
	ARLON Polyimide 35N 1080	0.073
	ARLON Polyimide 35N 106	0.056
	ARLON Polyimide 35N 1080	0.073
5		0.035
	ARLON Polyimide 35N	0.100
	ARLON Polyimide 35N 106	0.056
	ARLON Polyimide 35N 106	0.056
6		0.070
	ARLON Polyimide 35N	0.100
	VENTEC VT901 NF LCTE 106	0.060
	VENTEC VT901 NF LCTE 106	0.060
7		0.035
	DUAP-AP9121	0.050
8		0.035
	VENTEC VT901 NF LCTE 1080	0.075
	VENTEC VT901 NF LCTE 106	0.060
	VENTEC VT901 NF LCTE 1080	0.075
9		0.035
	DUAP-AP9121	0.050
10		0.035
	VENTEC VT901 NF LCTE 106	0.060
	VENTEC VT901 NF LCTE 106	0.060
	ARLON Polyimide 35N	0.100
11		0.035
	ARLON Polyimide 35N 106	0.056
	ARLON Polyimide 35N 106	0.056
	ARLON Polyimide 35N	0.100
12		0.017
	ARLON Polyimide 35N 2116	0.115
	ARLON Polyimide 35N 106	0.056
	ARLON Polyimide 35N 2116	0.115
13		0.035
	ARLON Polyimide 35N	0.100
	ARLON Polyimide 35N 106	0.056
14		0.035
	ARLON Polyimide 35N	0.125
15		0.035
	ARLON Polyimide 35N 106	0.056
	ARLON Polyimide 35N	0.100
16		0.017

as7002

Surface finishes

Hot oil reflowed SnPb

Galvanic Au (soft and hard)

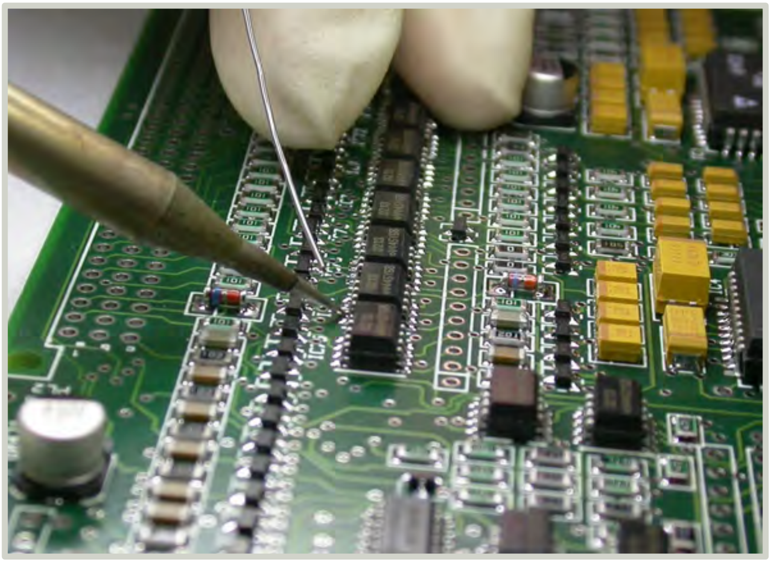
ENIG

ENEPIG/ENIPIG

solder mask

Lead-free

Nickel-free



Rigid-flex PCB

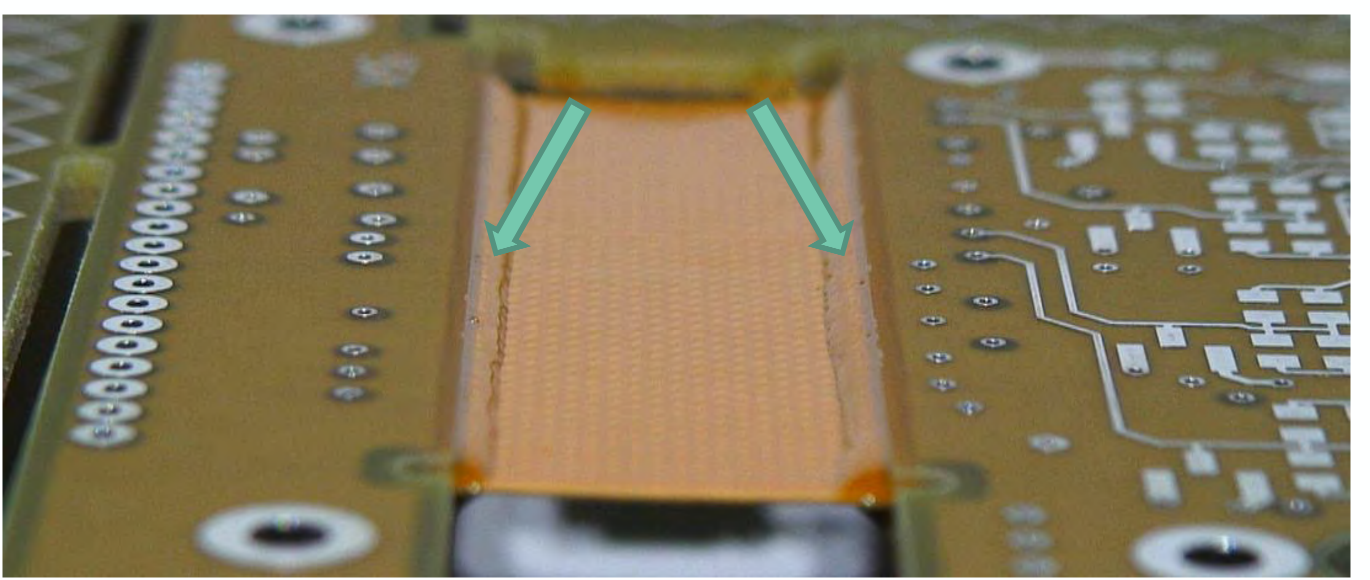
Rigid-flex transition zone is critical.

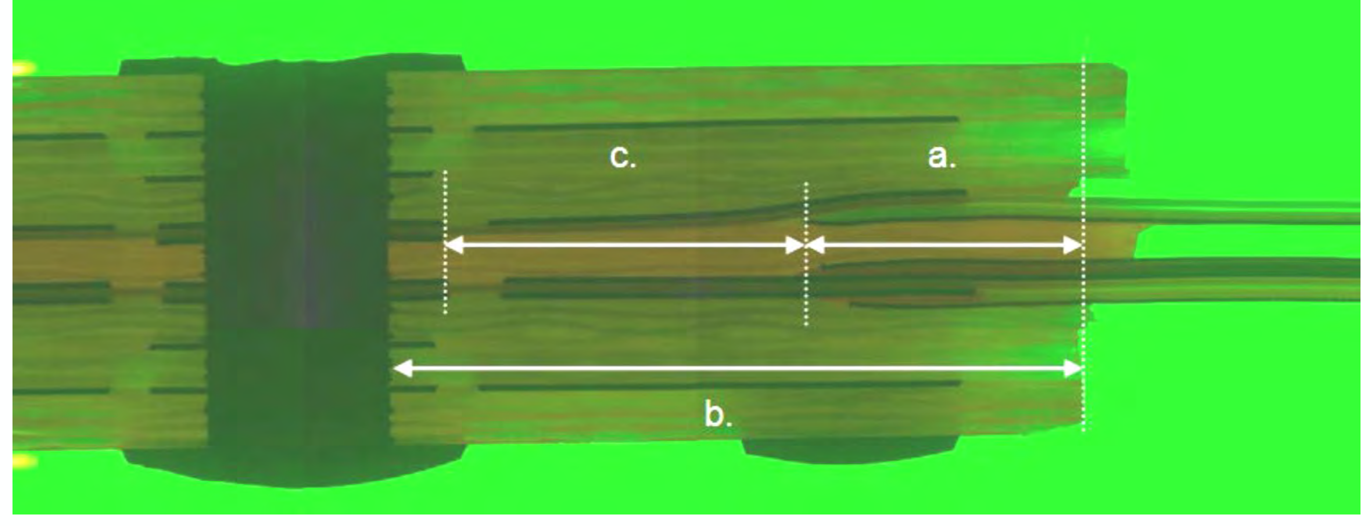
Coverlay limited to flex section.

Adhesive fillet or double coverlay.

Rigid section bonded with prepreg, not with adhesive.

No-flow prepreg has high z-CTE.





Recurrent Design

Heritage:

ECSS-Q-ST-70-12 § 4.1

- Flight? Qualification? In a relevant environment?
- Without nonconformances?
- Identical design and materials? Identical processes and its operators?

PA requirements of space projects use this standard as applicable document. Based on their heritage, suppliers can propose the re-use of existing PCB designs that are "recurrent" and that are not in compliance with all design requirements of this standard. The possible acceptability of those cases is reviewed by the project on case by case basis. The PCB design is "recurrent" only when no changes are made in the artwork, routing, lay-out, build-up, material selection.

Via technologies

plated through-hole
PTH

blind via
(depth-controlled drilled)

microvias
staggered

via-in-pad
plugged and cap plated

blind via
(in pad)

core via
(buried)

(through) via

buried via

core via
plugged and
cap plated

microvias
stacked

Technology drivers

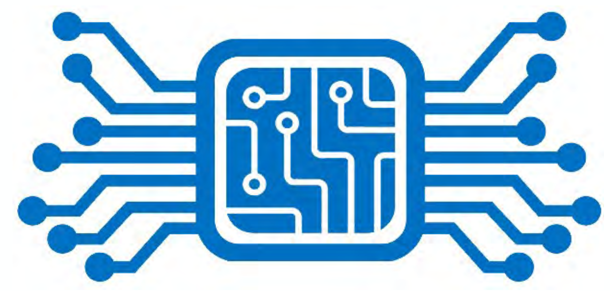
PCB technology is driven by:

- (Electrical) performance / functionality
- Manufacturability
- Reliability

Manufacturability and Reliability depend on:

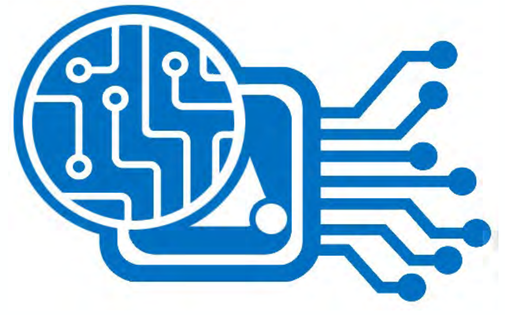
- Design and materials
- Capability and processes

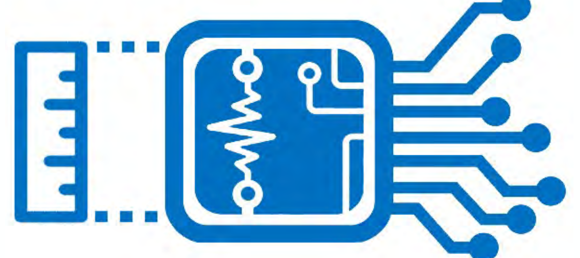
Technology drivers



High pin count causes
complex routing

Miniaturization requires
dense routing





Signal integrity requires
short routing

Technology drivers

Apollo Guidance Computer	vs.	Top end Smart Phone
1969	year	2021
200'000 now: 1.5M	price	1'000
30 kg	weight	0.2 kg
4 KB	RAM	12 GB
72 KB	ROM	256 GB
0.043 MHz	processor(s) speed	8 x 2.2/2.9 GHz

Smart phone is 0.5 - 3.0 million times more 'powerful' than AGC.

It weighs 100x less and costs 1000x less.

HDI roadmap

Complexity

1 mm pitch CGA
1752 I/Os
V5, RTG4

0.8 mm pitch COTS
CBGA 323
PBGA ~3000 I/Os

Single uvias
Polyimide
SnPb

Staggered uvias

Semi-stacked uvias
High speed dielectric
Backdrilling on core vias
ENIG and solder mask

3 stacked uvias
Spread glass weave
Smooth copper foil
Ni-free finish

6.25 Gbps | 15 Gbps | 28 Gbps | 56 Gbps | Data rate

Harmonisation

ESA **harmonisation** of PCB and Electronic Assembly 2022

Send email to harmo@esa.int to obtain login credentials to Harmonisation Data Management System (HDMS).

Links to technology dossier (THD) and roadmap (RM):

https://tec-polaris.esa.int/eclipse/public/redirect?url=/eclipse/i-layout?applicationId=dccm&projectId=1303&goto=/web/document/document-edit!view?document.id=35849&configFile=true

https://tec-polaris.esa.int/eclipse/public/redirect?url=/eclipse/i-layout?applicationId=dccm&projectId=1303&goto=/web/document/document-edit!view?document.id=35848&configFile=true

- ✓ Technology description
- ✓ Critical supply chain analysis
- ✓ Market drivers and market assessment
- ✓ Legislative drivers
- ✓ Technology drivers and development
- ✓ Roadmap

Key points from harmonisation

PCB and EA provide key **building blocks** for electronic equipment for all space projects.

Space projects can be significantly impacted due to **high effort** of development, qualification and procurement.

Supply chain is vulnerable due to legislative and economical market drivers.

Process control is notoriously difficult and expected to benefit tremendously from **Industry 4.0**.

COTS, NewSpace and mission classification drive novel approaches for standardization and qualification.

Operational drivers include 5G/6G, on board processing, power electronics and extreme space environmental conditions, among others.

Miniaturization of electronics is an enabling capability, most evident in consumer electronics. **Spin-in** to space market is already imminent due to COTS. **Pb-free** transition needs to be implemented.

European (New)Space programmes require wide availability of PCBEA technology, building competencies and influencing global standardization.

Outline

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2. Qualification, standards, COTS, mission class
3. Design, technology development
4. <u>Procurement, supply chain</u>
5. Quality, process engineering
6. Project review in MPCB
7. Project qualification / RFA
8. Inspection, failures

Organigram with external stakeholders

- National space agencies
- Space industry (Eurospace)
- Parts manufacturers
- Observers (academia, EC, EDA, oversees agencies…)

SCSB
Space Components
Steering Board

ESCC
Executive

ESCC
Secretariat

PSWG
Policy & Standards
Working Group

CTB
Components
Technology Board

MPTB
Materials & Processes
Technology Board

PCB/SMT WG

Hybrids &
Packaging WG

Passives WG

Lead-free WG

PCB/SMT working group

… and… the qualified PCB manufacturers

ESA qualified PCB manufacturers

Amphenol invotec

SYSTRONIC Groupe CIMULEC

elvia PRINTED CIRCUIT BOARDS

A&P Lithos Chateaubourg
Qualification in progress

(Ciretec discontinued due to fire)

ACB
ADVANCED CIRCUIT BOARDS
ATLANTEC CIRCUIT BOARDS

TESAT

CISTELAIER
Qualification in progress

Interactions of supply chain in PCB/SMT WG

EUROPEAN
SPACE
AGENCY

Qualification
test audit NCR

PCB
MANUFACTURER

ECSS
Standardization

PCB/SMT WG
R&D
NCs

Projects
MPCB RFx NRB

Procurement
MRR inspection NCR

PRIME,
OEM, EMS

Electronics manufacturing supply chain

glass yarn
woven glass
resin: epoxy, polyimide...
fillers
flame retardant, additives
copper foil
prepreg
laminate
Raw material &
Laminate supplier

chemicals, consumables
etching
lamination
PCB
drilling
surface treatment
plating
test, inspection (CoC)
PCB manufacturer

EEE parts
soldering
stiffener, box
adhesive bonding (stacking)
PCB assembly (module)
cables
wire bonding
test, inspection (MIP)
Assembler, EMS

equipment (unit)
Instrument / system
OEM

spacecraft
Prime,
Satellite integrator

Interactions in supply chain

PCBs are too much treated as **commodity**.

Failures can occur even when all requirements are met.

Rather, PCB manufactures should be **partner** in the supply chain:

- Complex designs require early involvement of PCB manufacturer,
- Technology development needs expertise and resourcing on both sides of the supply chain,
- Qualification and continuous improvement need support from supply chain,
- Problem areas are addressed by supplier development programmes, and residents.

EU PCB supply chain

[Steep decline](#) of PCB manufacturers in EU !

Small EU market volume of 2.4% (1.8 B€)
vs 4.3% in US; 67% in China

Incomplete EU supply chain for resin, glass, laminate, copper foil, chemistry, equipment, educated personnel.

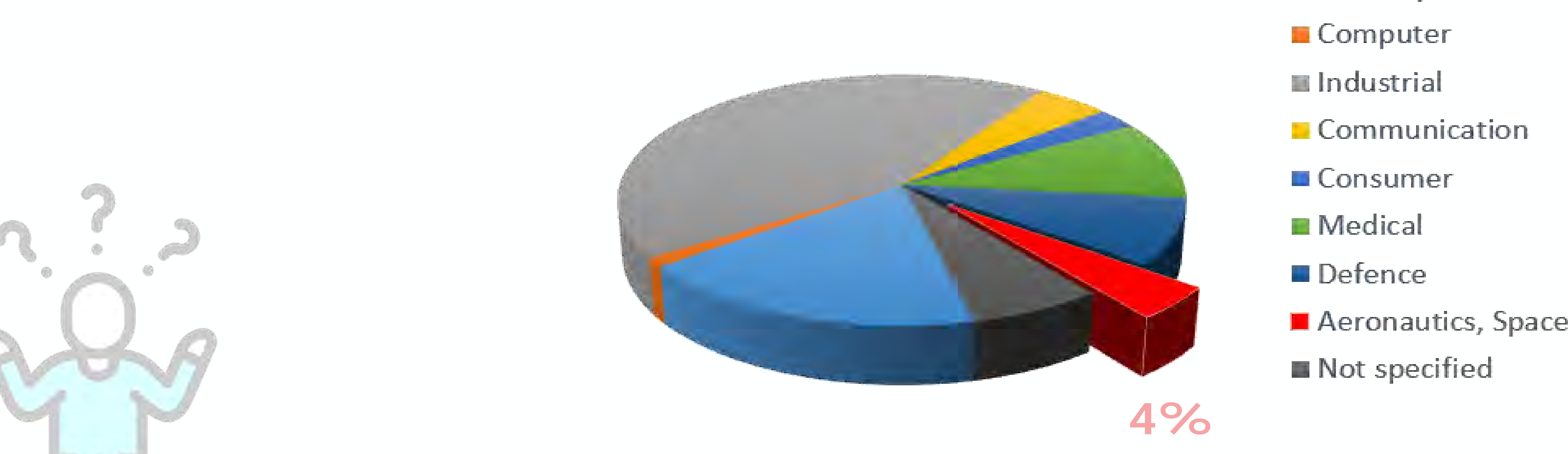
[Protecting PCB and substrates Act](#) proposed in US in May '23.

Nr of PCB manufacturers
1600
1400
1200
1000
800
600
400
200
0
2000
2010
2020
Revenue [B€]
5
4
3
2
1
0
Europe
North America
China
South East Asia
EU revenue B€

EU PCB supply chain

Space technology harmonization identified the PCB supply chain development as a critical topic.

But difficult to solve through R&D for space.



How can European PCB supply chain be improved for the benefit of all industry (not just space)?

Eurospace PCB Supply Chain white paper

EU PCB supply chain needs support for all market segments (not only in high-rel supply chain).

Chips Act is not inclusive of PCB, EMS and system level packaging.

EC, ESA, EDA implement R&D for high-rel segment.
But this does not address the supply chain deficiencies in the broad fundament of the volume market segments of consumer electronics, automotive, aeronautics.

https://eurospace.org/eurospace-white-paper-supporting-electronic-assemblies-and-pcbs-for-a-resilient-and-competitive-eee-components-supply-chain-in-europe/

ASD-EUROSPACE

SUPPORTING ELECTRONIC ASSEMBLIES AND PCBS FOR A RESILIENT AND COMPETITIVE EEE COMPONENTS SUPPLY CHAIN IN EUROPE

FINAL FOR Distribution - March 2023

- *Subject: white paper on Space Electronic Assemblies & PCBs in the EU Chips Act*
- *Contributors: Eurospace, Components Technology Board and its PCB/SMT working group*
- *Addressees: European Commission DG DEFIS, DG CONNECT, European Defence Agency*
  - *to: T. Pesonen (D/DEFIS), R. Viola (D/CONNECT), J.F. Ripoche (EDA), cc: T. Henriksen (ESA)*
  - *fwd: EC: E. Kavvada, G. de la Brosse, F. Vitobello, E. Papantoniou, I. Poldrugo; EDA: P. Langlois; ESA: B. Schade, T. Ghidini, E. Williams; DLR: B. Gökgöz; CNES: A. Mallet, F. Malou; ASI: G. D'Amore.*

Summary

This white paper provides a review of the Printed Circuit Board (PCB) and Advanced Packaging supply chains in Europe, from the point of view of critical applications, such as for space (and defence) programmes, and also from the point of view of the main leading industry organisations such as the IPC and the EIPC. **It notes that against the key trends identified in electronics technologies the European PCB supply chain exhibits a few weak spots**, which affect a broad range of industrial sectors, from consumer electronics to high-performance/high-reliability sectors like automotive, aerospace and defence.

This situation is critical for Europe, also because it impacts the space (and defence) industries. There is a direct impact, because space systems and equipment integrators often procure their PCBs outside Europe, especially when triggered by cost and timeline constraints, and an indirect one, as the European PCB ecosystem is losing ground to its competitors, the workforce landscape is shrinking, capabilities are less readily available, and basic supplies, including equipment and raw materials, are growingly difficult to source in Europe.

This paper includes a call for the more comprehensive development of PCB technology and for the strengthening of the PCB supply chain benefiting all user sectors.

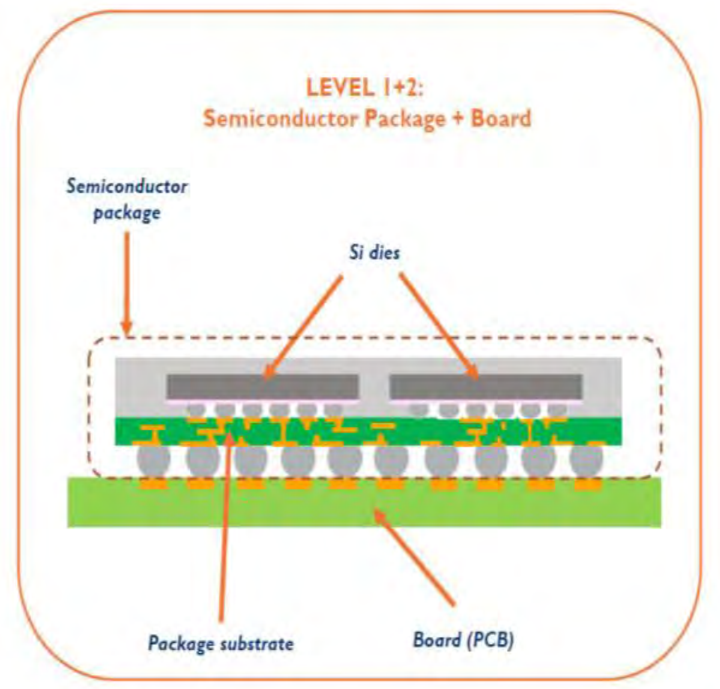
The EU Chips Act is seen as a major opportunity to consistently address the issues identified.

This white paper was authored by a representative group of experts from the space PCB and space electronics stakeholder community, involving customers, integrators and manufacturers. It was endorsed and released by Eurospace. See details in the annexes.

Eurospace PCB Supply Chain white paper

Request support from EC for the broad development of the PCB supply chain:

- ✓ Holistic roadmap and technology development for advanced PCBs in all market segments,
- ✓ Incentives to attract the raw material and process equipment supply chains,
- ✓ Wide-spread introduction of state-of-the-art process equipment,
- ✓ Education of personnel for front-end engineering, process control and servicing of equipment,
- ✓ Corrective measures for legislation, trade tariffs and increased energy cost.



Eurospace PCB Supply Chain white paper

Joint advocacy effort with EC and IPC-Europe, EIPC, EDA, ESA.

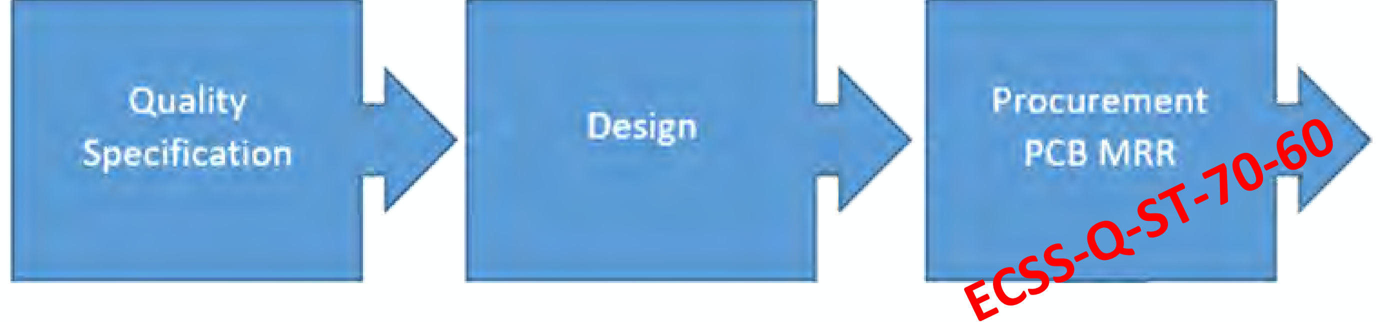
Eurospace white paper issued Mar-23, downloaded >300x.

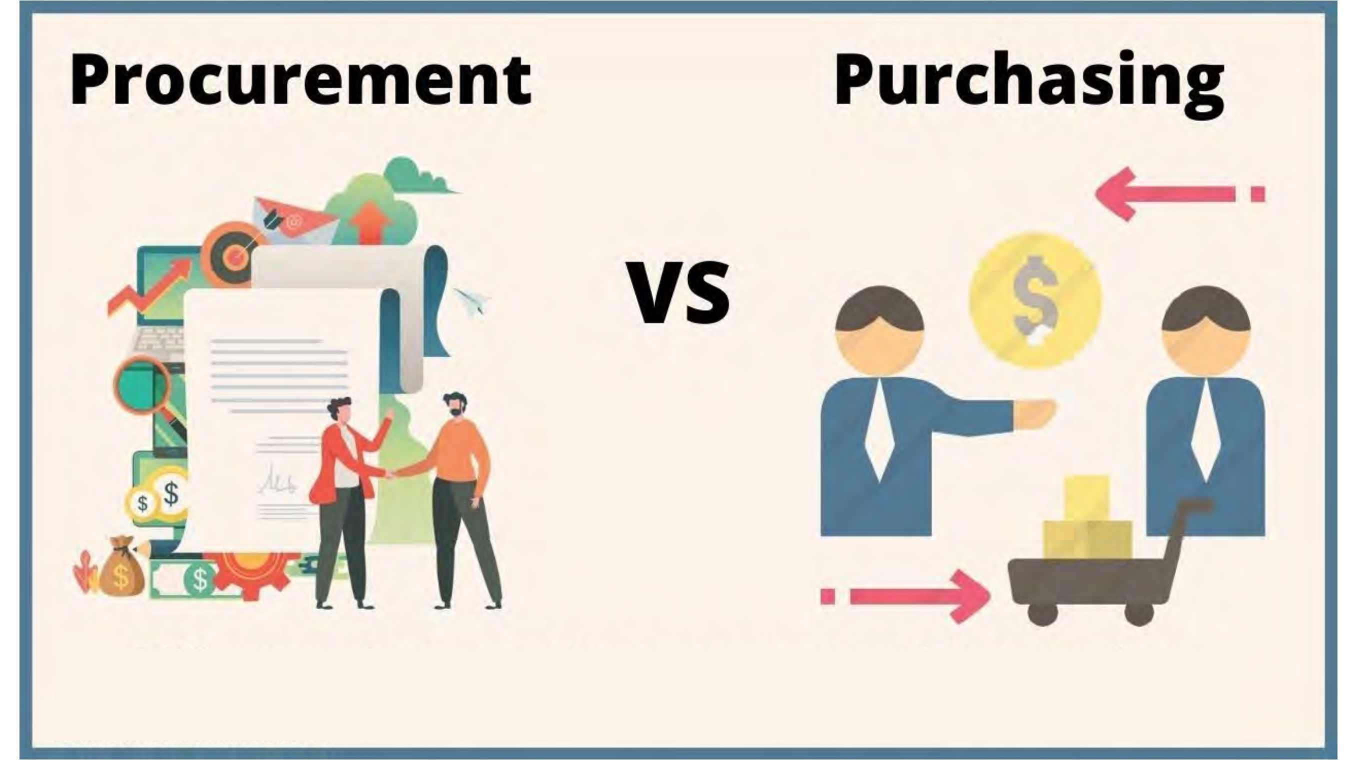
IPC/iMAPS meeting Brussels Apr-23

EC DG GROW Structured Dialogue Meeting on Electronics Manufacturing - Brussels Jun-23

IPC industry report and SWOT analysis issued to EC Jul-23

Procurement





Procurement Cycle

- ☑ Specify/confirm that PCB design, procurement and qualification is **as per ECSS-Q-ST-70-12/60**. This may include a partial compliance covered by RFD and/or RFA.
- ☑ Procurement Authority prepares **PCB Definition Dossier**:
  - can be a draft, updated in various iterations with the PCB manufacturer,
  - includes Review Items,
  - records Double Insulation.

ECSS-Q-ST-70-60 § 6.2

ECSS-Q-ST-70-12 § 5.2

- ☑ **Request for Quotation** to PCB manufacturer and submit (draft) PCB Definition Dossier.
- ☑ PCB Manufacturer performs **Design Review (DR)**, confirms compliance to PID and provides the quotation.
- ☑ Procurement Authority issues **Purchase Order** and MRR checklist, e.g. annex G of ECSS-Q-ST-70-12.
- ☑ PCB manufacturer completes the MRR checklist and performs the **MRR**.

Review items – Pad size

as-designed dimensions ± manufacturing tolerances = as-manufactured dimensions

It may be possible to use smaller designed values…

… as long as the as-manufactured values are ok

… but is it really necessary to take such risk?

f. For via holes and component holes on component side the diameter of external pads should be the diameter of as-manufactured hole plus ≥ 0,6 mm.

g. For via holes and component holes on component side the diameter of external pads may be the diameter of as-manufactured hole plus ≥ 0,5 mm in case:

1. the as-manufactured annular ring as specified in the requirement 7.5.2b, and.
2. it is recorded as a Review Item in the PCB definition dossier.

ECSS-Q-ST-70-12 § 7.5.2

Procurement specification

The procurement specification shall be directly the ECSS-Q-ST-70-60.

Do NOT use a company specific procurement spec that embeds the ECSS, because

- amendments and compliance to ECSS are not transparent,
- PCB manufacturer and qualification authority cannot categorize to ECSS (e.g. on CoC).

Additional requirements from the procurement authority, such as
extra inspection, tighter tolerances or specific technology features,
can be specified in the PCB definition dossier or on an annex of the purchase order.

ECSS-Q-ST-70-60 § 6.2.2

PCB MRR Manufacturing Readiness Review

- ☑ Meeting between PCB manufacturer and Procurement Authority, usually requiring several iterations. Can be done off-line by email if simple, for recurrent designs.
- ☑ Design Review (generic) and assessment of Review Items (specific)
  - Listed in annex A.2.1<7> of ECSS-Q-ST-70-12
  - “Input to the MRR checklist” ESA-TECMSP-MX-14192 is issued on ESCIES, with 130 items to check. The use of this checklist by the procurement authority may be required through the PARD.
- ☑ Compliance to ECSS and PID
- ☑ Build-up, panelisation, coupon locations
- ☑ Risk assessment (1-5), based on Review Items.
  - Enter in risk register for risk ≥3
  - Cost sharing for risk ≥4
- ☑ Approval of PCB Definition Dossier and PCB Manufacturing Dossier
- ☑ Authorization to proceed with manufacture. Normally no ESA involvement.

ECSS-Q-ST-70-60 § 6.2.6

ECSS-Q-ST-70-12 annex G

PCB MRR example – Annex G of ECSS-Q-ST-70-12

Supplier Specification:

(To be completed by supplier procurement with additional information where applicable from the responsible design authority.)

PCB Manufacturer		Project	
Supplier Article or Reference No:		Issue/revision	
Article title:		Issue/revision	
Supplier purchase order No:		Purchase order Date	
Feature Set			
Is this a new or a recurring design?			
If recurring please define all changes made to data set since the last purchase or state none.			
If recurring please reference ALL occurrence reports raised against previous procurements of this or state none.			
Is the design fully compliant with ECSS-Q-ST-70-12?			
If the design is not compliant to ECSS-Q-ST-70-12 please list all deviations.			
Has method and position of identification marking been defined?			

Additional risks:

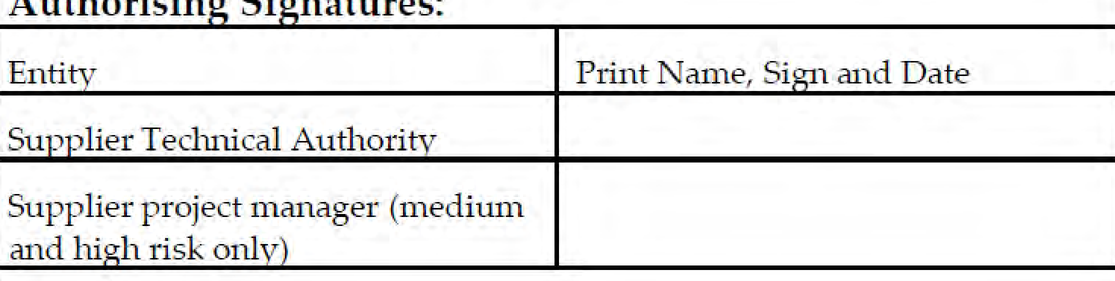
Have any additional risks to the manufacture of this product been identified

Additional risk identified	Risk Rating (1 Low, 5 High)	Risk Parameters requiring control

Manufacturer Completing Signature:

Please ensure that copies of the PCB construction and a screen dump of the approved panel layout are attached to this MRR before signature.

Position	Print Name; Sign and Date



Authorising Signatures:

Entity	Print Name, Sign and Date
Supplier Technical Authority	
Supplier project manager (medium and high risk only)	

Current space market

- Order volume is high due to post-pandemic recovery, high space activity, loss of one qualified PCB manufacturer due to fire.
- Lead times are much longer than normal… Up to 30 weeks!
- Allow for failure of PCB at outgoing inspection and potential new manufacturing run.
- Add to project's LLI, CIL and risk register.
- Implement double sourcing for critical technology (complex, non-qualified, with long lead time and schedule critical)

Phase	Rigid non sequential	Rigid sequential	Flex rigid	HDI
Tooling including design review and MRR	2-3 wk	2-3 wk	2-3 wk	2-3 wk
IST coupon design data	2 wk	2 wk	2 wk	2 wk
MRR approval	0,5-1 wk	0,5-1 wk	0,5-1 wk	0,5-1 wk
Manufacturing & inspection	4 wk	5-6 wk	5-6 wk	6-7 wk
IST	2,5-4 wk	2,5-4 wk	2,5-4 wk	2,5-4 wk
Total	11-14 wk	12-16 wk	12-16 wk	13-17 wk

Table 6-1 ECSS-Q-ST-70-60

Outline

1. Introduction, manufacturing
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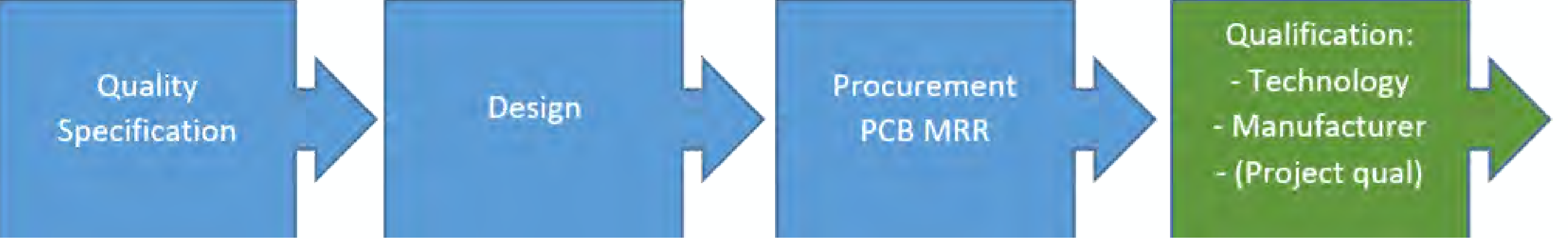
Quality, Qualification



Quality

Capability:	ability to manufacture a design
	(also: functionality of a design)
Quality:	as-manufactured build integrity
Reliability:	performance under operational environmental stress
Robustness:	performance under excessive environmental stress

Failure mode:

Open circuit failure – the unintended opening of a piece of circuit

Short circuit failure – the unintended breach of a piece of insulation

Failure can occur stable as-manufactured, or latent, intermittent and evolving.

PCB acceptance is based on dozens of quality indicators that influence its reliability, and thus probability of failure.

Cost of Quality

Cost of Quality

Cost of Non-conformance

Cost of Conformance

Cost of External failure

Cost of Internal failure

Cost of Appraisal

Cost of Prevention

NCR

Key Process Indicators

Quality Control

Innovation, Investment

Total Cost of Quality

Cost of implementing Quality

innovation

Cost of rectifying Defects

COST

High

Low

QUALITY

Low

High

Cost of error

Operation

Launch

AIT

Assembly, Test

Acceptance

Design

Requirements

Cost of error

Product life cycle

Cost of Quality

PCBs and assembly need to be comparable to EEE components in terms of reliability and complexity, but at a fraction of the cost.

PCB ~ 5k€

Area Array Device ~ 50k€

The bitterness of poor quality remains long after the sweetness of low price is forgotten.

BENJAMIN FRANKLIN

"IF YOU THINK GOOD DESIGN IS EXPENSIVE, YOU SHOULD LOOK AT THE COST OF BAD DESIGN"

DR. RALF SPETH, CEO JAGUAR

Triangle of constraints in project management

GOOD

FAST

CHEAP

in your dreams

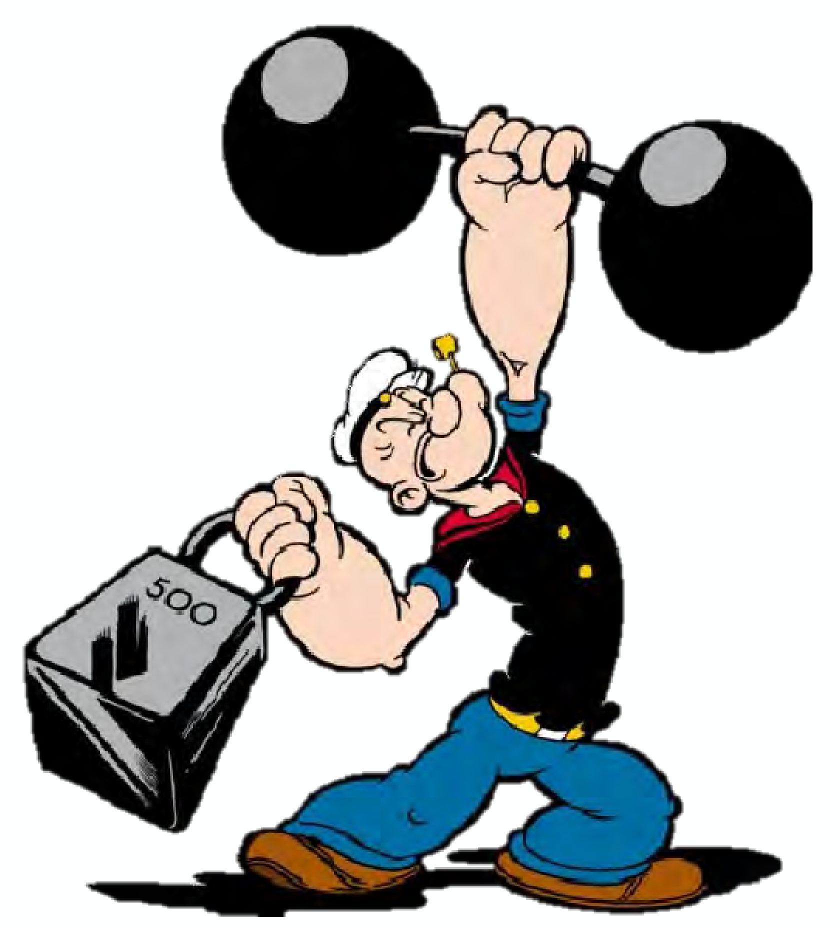
Stress-strength analysis

Failure does not occur if:

manufactured strength > > specified strength

But these are not discrete values,

and usually subject to variability.



Process engineering

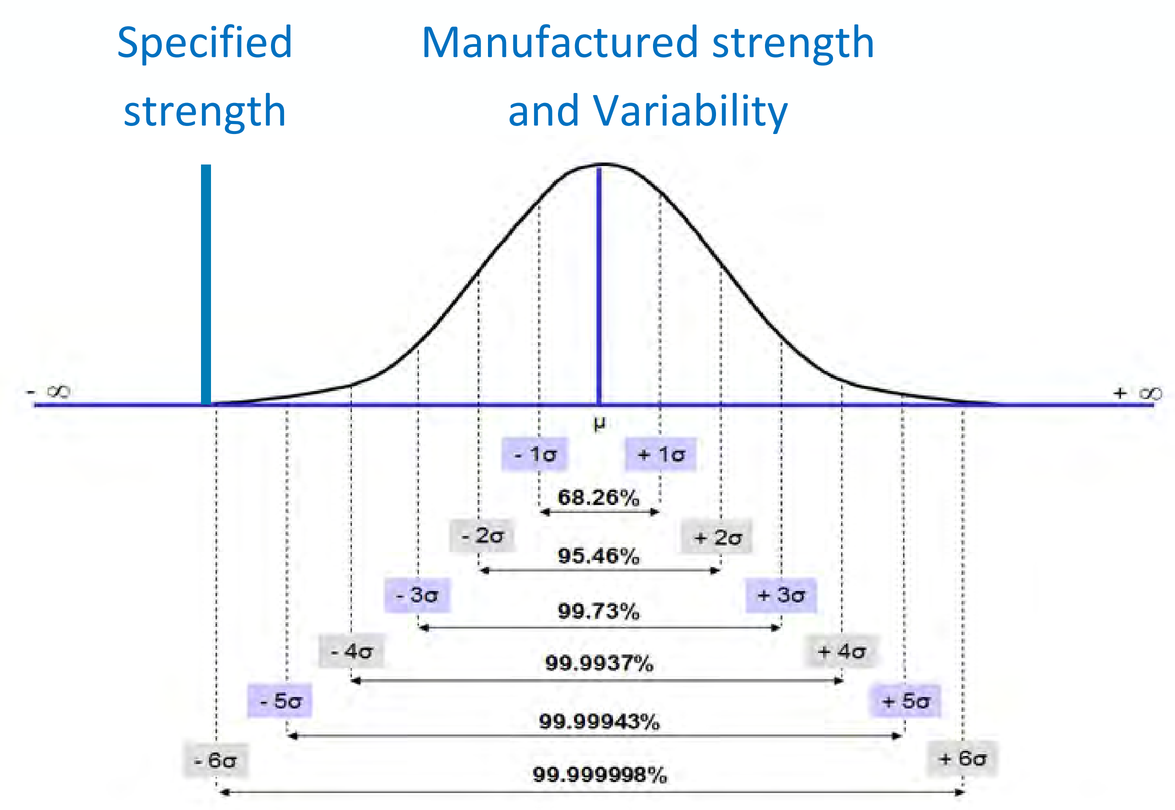
Process engineering tools:

- Six Sigma → reducing variability
- Lean manufacturing → reducing waste of resources

6σ quality meets specification by
6 standard deviations of the process variability.

This leaves 3.4 DPMO defects per million opportunities.
Or half that, in case of a single specification limit.

A batch of 10 PCBs with 10 layers and 2000 vias may have 0.4 MO, and thus potentially 1 defect…



Confidence interval of stress-strength analysis

occurrence

Manufactured strength
and Variability

Application stress
and Variability

Failure can occur

Strength increased,
variability remains

Strength is equal,
variability reduced

strength

Confidence interval of stress-strength analysis

Infant mortality

A subset of weak products does not withstand the application stress.

Useful life

A (very) low amount of random failure

Wear-out

Strength is reduced over time by application stress until failure occurs.

Product life cycle

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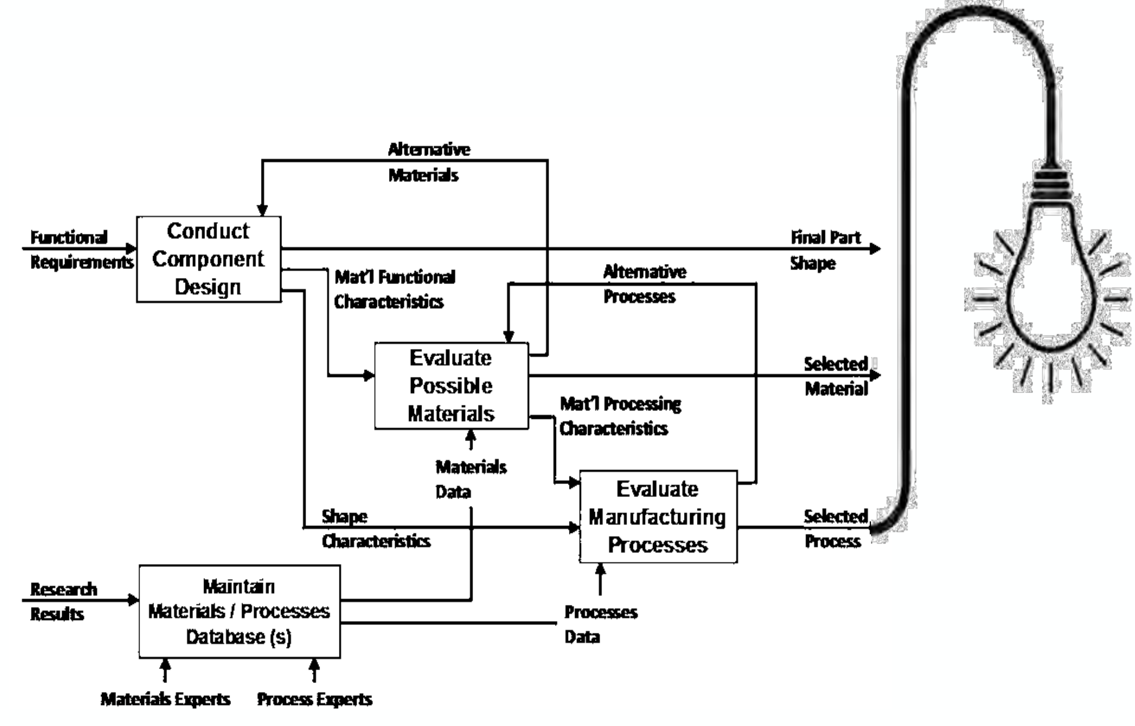
Project review in MPCB



Materials & Processes Section TEC-MSP

M&P

Focal points for MPCB

Advanced Manufacturing

Modelling

Josef Aschbacher
Director General

Dietmar Pilz
Dir. of Technology, Eng. & Quality
D/TEC

Tommaso Ghidini
H/Mechanical Department

Thomas Rohr
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Organigram – interfaces within ESA

simplified organigram,
indicating collaborative interfaces

D/TEC

TEC-S
TEC-E
TEC-Q
TEC-M

TEC-SA
Navigation,
AOCS sensors
and systems

TEC-SP
Projects

TEC-SY
Systems

TEC-EP
Power, Battery,
Harness,
Solar Array

TEC-ED
Microelectronics,
Data, Components

TEC-EF
RF Payloads,
Antennae

TEC-QE
Materials,
Components,
Standardisation

TEC-QQ
PA,
Supply chain

TEC-MS

TEC-MM
Opto-
electronics

TEC-MT
Thermal

TEC-MSP
Materials &
Processes

TEC-MSM
Mechanisms

TEC-MSS
Structures

PCB
S Heltzel
J Hokka

Assembly
C Villette
G Corocher
E Peraud

Project review in MPCB

ESA-TECMSP-MX-12940

Checklist for review of PCB technology in MPCBs

ESCIES: Printed Circuit Boards

ESA Approved Manufacturers and Qualification Status of PCBs

- ESA Qualification Status of PCB technology
- ESA Approved PCB Manufacturers - contact details

Active ESA memos and checklists

- QT/2014/361/SH ECSS standards for PCB design
- ESA-TECMSP-MO-7424 Project qualification of Thermount 85NT PCBs
- ESA-TECMSP-MO-11532 ECSS standards for PCB qualification and procurement
- ESA-TECMSP-MX-11559 Checklist to ECSS-Q-ST-70-60 for PCB manufacturers
- ESA-TECMSP-MX-11320 Checklist for ENIG ENEPIG ENIPIG finish
- ESA-TECMSP-MX-12940 Checklist for review of PCB technology in MPCBs
- ESA-TECMSP-MX-14192 Input to checklist for MRR
- ESA-TECMSP-MX-16451 Compliance matrix ECSS vs IPC6012DS
- ESA-TECMSP-HO-19825 PCB training course presentation (18MB)
- ESA-TECMSP-TN-19672 Microvia process guidelines

Project review in MPCB

The checklist contains the following:

- 2 line items that are statements as a guideline to the MPCB process;
- 11 key line items Q1 to Q11 to be verified for MPCBs;
- 3 line items Q12 to Q14 that only apply for project qualification under RFA;
- 1 line item Q15 for equipment MRR, which is not applicable for MPCBs.

It is the intention of the 11 key line items to provide sufficient detail for a robust approval process of the PCB technology, while also maintaining a reasonably short review process.

It is the intention that Materials and Process (M&P) Engineers who are not expert in PCB technology can conduct this review with confidence, using this checklist, with the following outcome:

- Approval of qualified PCB technology;
- Identification of any non-qualified technology or any deviation to requirements;
- Preparation of the contents of RFAs.

Non-qualified technology, deviation to requirements and RFx are recommended to be reviewed, and eventually approved, by PCB experts, not only by M&P Engineers.

The checklist is provided to the equipment supplier (contractor) in an editable excel format in Annex 1, to complete the self-assessment and to provide the response. The management of the organisation is responsible for the correctness and completeness of the response.

Project review in MPCB

esa_tecmsp_mx_012940_checklist_for_approval_of_pcb_technology_in_mpcbs_signed.pdf - Adobe Acrobat Pro (64-bit)

File Edit View E-Sign Window Help

Home Tools esa_tecmsp_mx_01... ×

1 / 6 53.2%

The validity of the document certification is UNKNOWN. The author could not be verified.

Attachments

Name

Annex 1 of ESA-TECMSP-MX-012940 Ch

ESA UNCLASSIFIED - For Official Use

esa

estec

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MATRIX / COMPLIANCE

Checklist for approval of PCB technology in MPCBs

Project review in MPCB

Question	Reference from ECSS-Q-ST-70-60	Primary assessment method for projects that have ECSS-Q-ST-70-60 as applicable document.
Q1	6.14g	The procurement authority shall specify in the DML for each PCB technology the following: 1. PCB manufacturer; 2. PCB procurement specification; 3. PCB technology description as per 6.14e (see Q3 below); 4. traceability to individual PCBs and their PCB approval sheet.
Q2	6.14a 6.2.2a	ECSS-Q-ST-70-60 shall be applicable for procurement of PCBs for flight models and for qualification models.
Q3	6.14e	The procurement authority shall list in the DML each PCB technology as a separate item: 1. Polyimide rigid 2. Polyimide rigid/flex 3. Epoxy rigid 4. Epoxy rigid/flex 5. HDI 6. RF 7. Flexible 8. Sculptured flex 9. Low thermal expansion materials
Q4	6.14f	The PCB technology is listed as a single line item in the DML covering all materials and processes for its manufacture. Individual raw materials and PCB manufacturing processes are not listed in the DML and DPL as separate items.

ESCIES
European Space Components Information Exchange System

Project review in MPCB – PCB approval sheets

Question	Reference from ECSS-Q-ST-70-60	Primary assessment method for projects that have ECSS-Q-ST-70-60 as applicable document.
Statement	6.14s	The approval of the item in the DML shall be based on the review of PCB approval sheets of all PCBs covered by the item of the DML.
Statement	6.14o	Customer approval of PCB approval sheets shall be based on the compliance of technology parameters to the PID, as declared on the PCB approval sheet part 2.
Q5	6.14h, I, m	The procurement authority shall complete a PCB approval sheet part 1 for each individual PCB type as per the DRD in Annex G and submit it for approval by the MPCB prior to the PDR.
Q6	6.14j, k, m	The procurement authority shall complete a PCB approval sheet part 2 for each individual PCB type as per the DRD in Annex G and submit it for approval by the MPCB prior to the CDR.
Q7	ESA-TECMSP-MO-11532	The PCB approval sheet includes evidence of the qualified status. This can be obtained from the public web portal www.escies.org/pcb/.

Project review in MPCB

Question	Reference from ECSS-Q-ST-70-60	Primary assessment method for projects that have ECSS-Q-ST-70-60 as applicable document.
Q8	6.14d	The procurement authority shall ensure that all procured PCBs meet the project requirements. NOTE: Examples of applications for projects with specific requirements are human spaceflight, long-term storage, detector technology, planetary exploration.
Q9	5.1b	In case of operational use of PCB (and assemblies) below -55 degC and/or above +85 degC, the technology is subject to project specific qualification under RFA.
Q10	6.14b, c	The same PCB manufacturer should be used for PCB manufacture for flight models and qualification models. In case a different PCB manufacturer or different PCB material is used for flight models compared to qualification models, the procurement authority shall analyse in a technical note the impact on the following items: 1.Electrical performance of the equipment; 2.Mechanical performance of the equipment; 3.Thermal performance of the equipment; 4.Assembly approval status; 5.Any modifications of the PCB definition dossier done by the previous PCB manufacturer.
Q11	6.14n, r	The following documentation is available for possible review during MPCB: 1. FAI (First Article Inspection) on PCB as per clause 8.5; 2. PCB definition dossiers.

Project qualification RFA

Project qualification RFA

Question	Reference from ECSS-Q-ST-70-60	Primary assessment method for projects that have ECSS-Q-ST-70-60 as applicable document.
Q12, if applicable	6.14p, q	In case of non-compliance of a technology parameter to the PID, a delta qualification plan and associated RFA shall be submitted to the customer for review during the MPCB.
Q13, if applicable	7.7.2d	Before the PCB procurement, the procurement authority shall submit to its customers for approval the RFA part 1 including the following: 1.PCB approval sheet in conformance with Annex G; 2.Compliance matrix to ECSS-Q-ST-70-60 for PCB qualification and description of the non-qualified aspects; 3.Compliance matrix to ECSS-Q-ST-70-12 for PCB design; 4.Compliance matrix to the PID from the PCB manufacturer; 5.Compliance to inspection on PCB and coupon for procurement in conformance with clause 8. 6.Description of the thermal, electrical and mechanical environment of the application; 7.Project qualification test plan; 8.Technical justification in case a single PCB design is intended to cover several PCBs to be used for the project; 9.Verification and inspection to be performed in case several batches are manufactured to cover for the qualification vehicle and the FMs. 10.Batch traceability of FM PCBs and the one submitted to the project qualification.
Q14, if applicable	7.7.2n	After PCB procurement, the procurement authority shall submit to its customers for approval the RFA part 2 including the following: 1.project qualification test report; 2.test report for specific evaluation on coupons and PCBs in conformance with 7.7.2i and 7.7.2j; 3.outgoing inspection on PCB and coupons in conformance with 8.1 and 8.2; 4.CoC and its lab reports in conformance with 8.3a; 5.incoming inspection in conformance with 8.4.

Project qualification RFA

In case the technology is not covered by generic ESA qualification:

It shall be project qualified under RFA by:

- Group 6 test on a spare PCB of the FM batch
- IST > 400 cycles to failure
- For HDI: CAF risk assessment

ECSS-Q-ST-70-60

§ 7.7.2

§ 5.3.2

Design Review with customer is recommended.

This also applies to procurement as per IPC-6012, see rqt 7.7.2p.

For flex PCBs (long harness, dynamic application) see rqt 5.3.2.

Group 6

Group 6 test: "Short assembly and life test"

- Test vehicle is a spare PCB from FM batch
  (FM ensures representativity, but provides late feedback)
- Vapor phase simulation on entire PCB
- Rework simulation on PTH and SMT with via-in-pad (representative!)
- Thermal cycling 200x, -60 to +140 degC
- Evaluation by microsectioning of all features subject to qualification

ECSS-Q-ST-70-60

§ 9.8

"The test levels for thermal cycling are not only driven by space environment. Thermal cycling to the levels specified in clauses 9.6.2 and 9.8.2 provide reference to the heritage test levels that assess robustness of the PCB construction."

CAF assessment

- Risk assessment of minimum insulation distance for propensity of CAF (conductive anodic filament) formation by comparing to the footprints on the CAF test vehicle from § 9.7.3.
- CAF propensity can be considered low if insulation distances of the PCB exceed the max distances reported in tables 9-2, 9-3 and 9-4.
- In case the CAF risk assessment is not low, a CAF test should be performed.

ECSS-Q-ST-70-60C Corrigendum 1
1 March 2019

Table 9-2: CAF pattern dimensions – via-to-via straight

Description	Pattern	Drill diam. (µm)	Pad diam. (µm)	Via edge to via edge (µm)
X and Y-direction 1020 pitch	IPC A1	750	860	270
	IPC A2	650	810	370
	IPC A3	500	750	520
	IPC A4	350	690	670
	ECSS A4	300	600	720

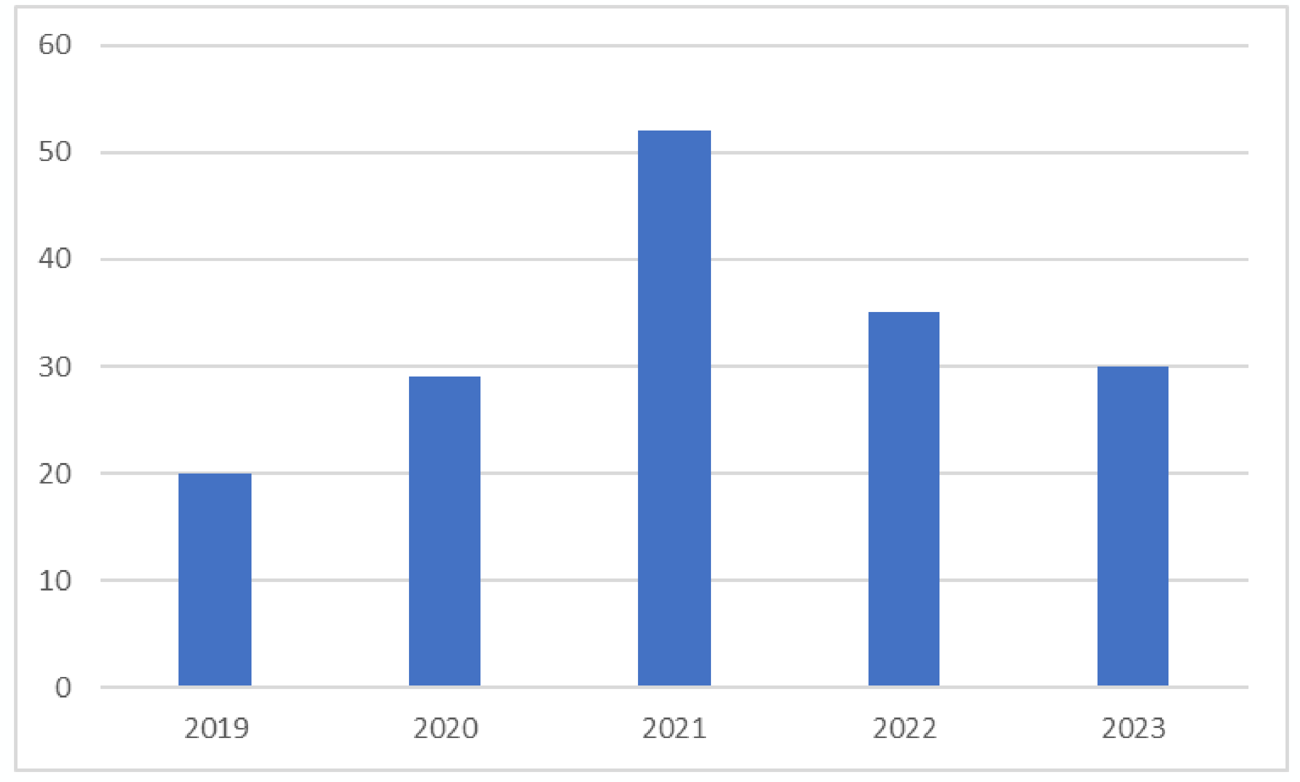
Table 9-4: CAF pattern dimensions – via-to-plane

Description	Pattern	Drill diam. (µm)	Pad diam. (µm)	Clearance diam. (µm)	Via edge to plane (µm)
	IPC C1	350	none	640	145
	IPC C2	350	none	700	175
	IPC C3	350	none	850	250
	IPC C4	350	none	960	305

RFAs

Project qualification under RFA:

- Occurs frequently
- Pragmatic test, but it still adds cost (4 k€) and time (4 wks)
- Risk to fail the qual
- Risk to have undetected issues
- Risk to miss the need for RFA



Assembly MRR

Quality Specification → Design → Procurement PCB MRR → Qualification: - Technology - Manufacturer - (Project qual) → Materials & Processes Control Board

Procurement PCB MRR ↓ Outgoing Inspection → Accelerated Coupon Test → Incoming inspection

→ Assembly MRR →

Assembly MRR

Question	Reference from ECSS-Q-ST-70-60	Primary assessment method for projects that have ECSS-Q-ST-70-60 as applicable document.
Q15, n/a for MPCB	6.14t	The CoC of the PCB (including traceability to any repair as per rqt 6.10.2e.), its records of incoming inspection and any associated RFA shall be made available by the procurement authority at the equipment MRR.

Outline

1. Introduction, manufacturing
2. Qualification, standards, COTS, mission class
3. Design, technology development
4. Procurement, supply chain
5. Quality, process engineering
6. Project review in MPCB
7. Project qualification / RFA
8. Inspection, failures

Inspection and test

Quality Specification → Design → Procurement PCB MRR → Outgoing Inspection → Accelerated Coupon Test → Incoming inspection

ECSS-Q-ST-70-60

Outgoing inspection

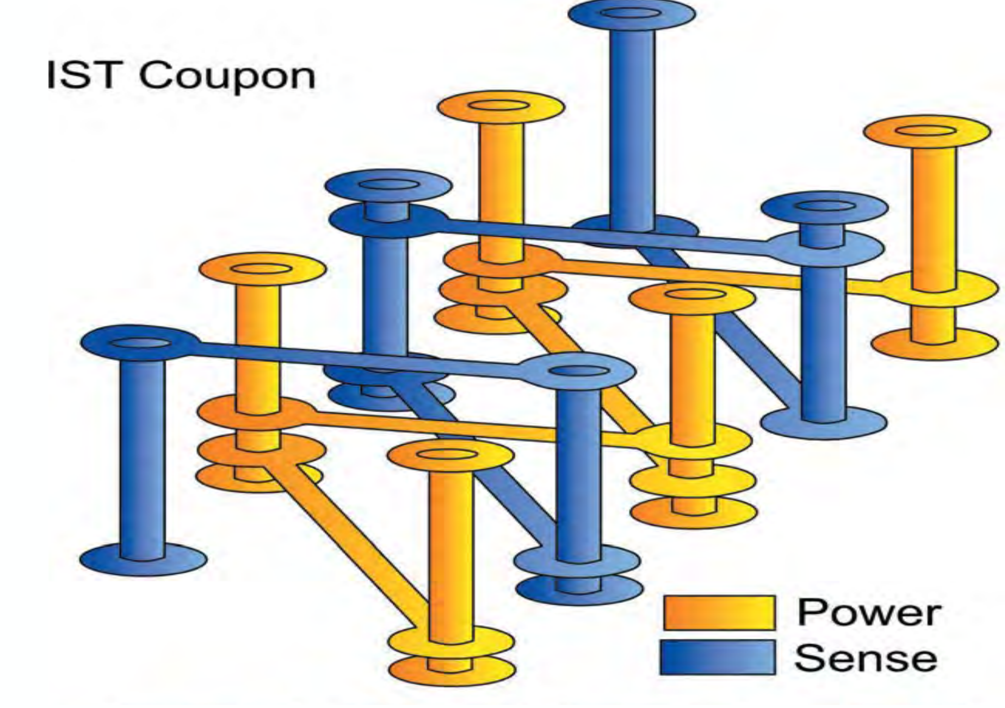
High resistance electrical test

Visual inspection on 100% of PCBs

DPA on coupons before and after thermal stress

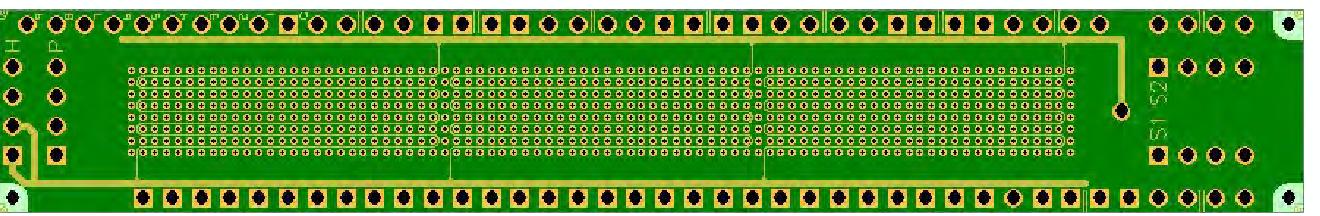
IST – Interconnect Stress Test

- ≥0,3mm no-flow prepreg
- Epoxy PCB with ≥12 layers
- Rigid-flex PCB with ≥12 layers, or ≥2 flex laminates, or asymmetric build-up / lamination
- HDI PCB with microvias or with aspect ratio > 7.

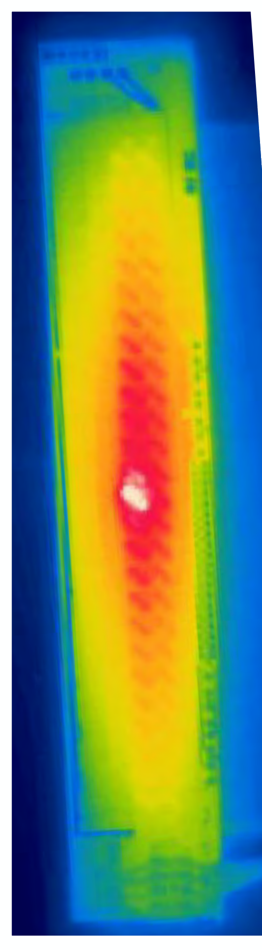


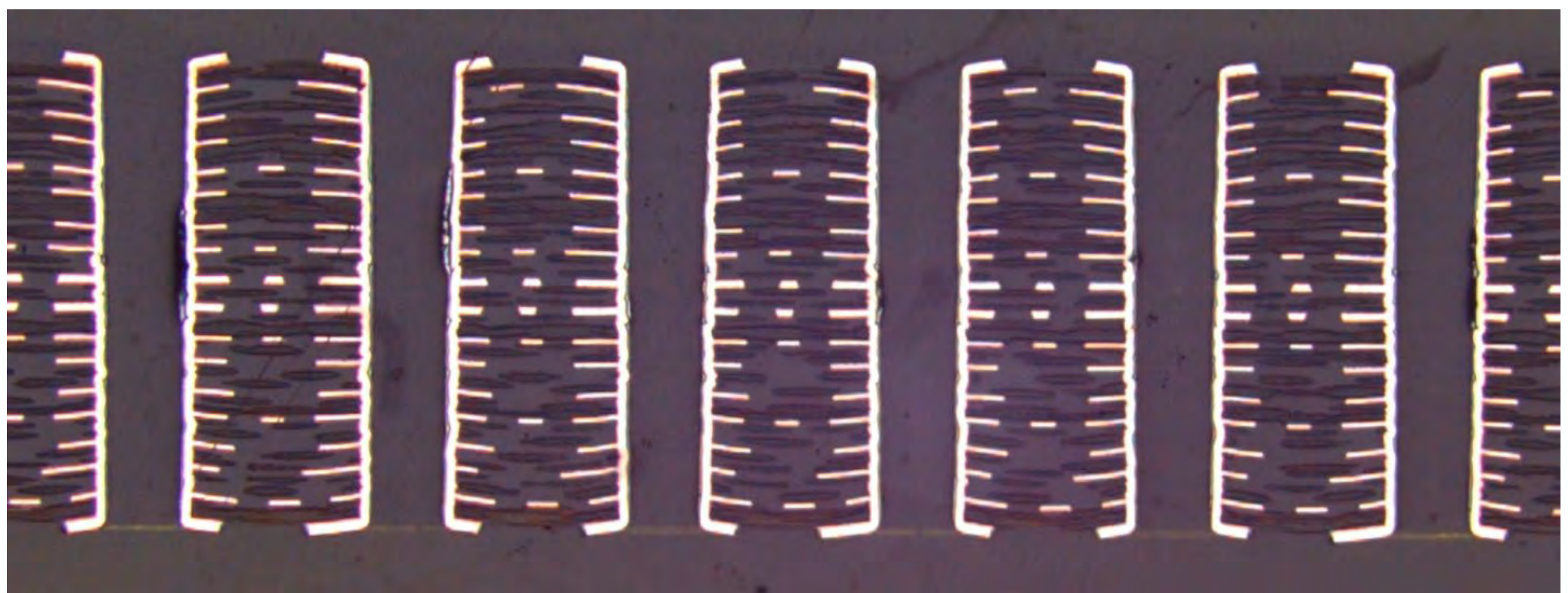
ECSS-Q-ST-70-60

§ 9.3, § 9.5, § 9.5.5.2.2



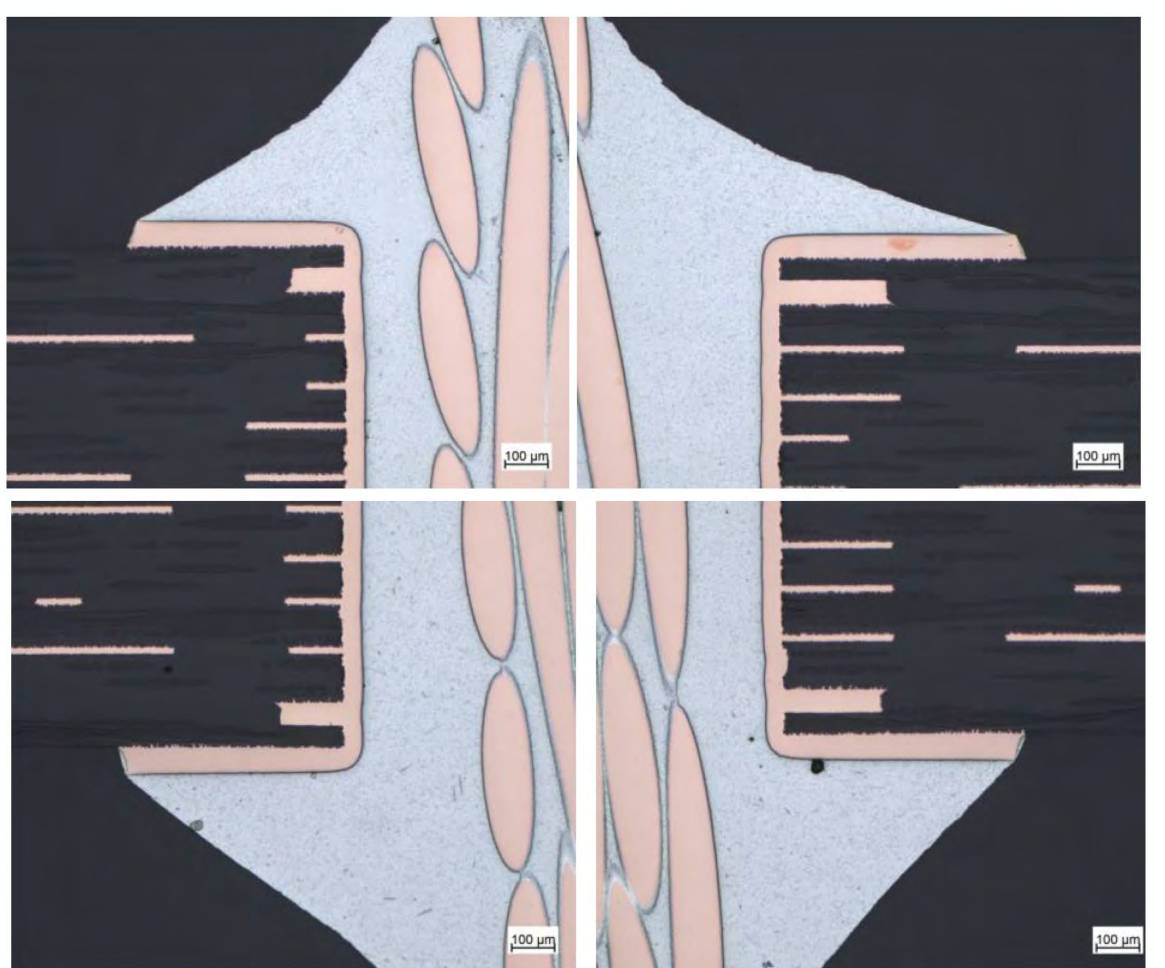
Outgoing inspection - IST



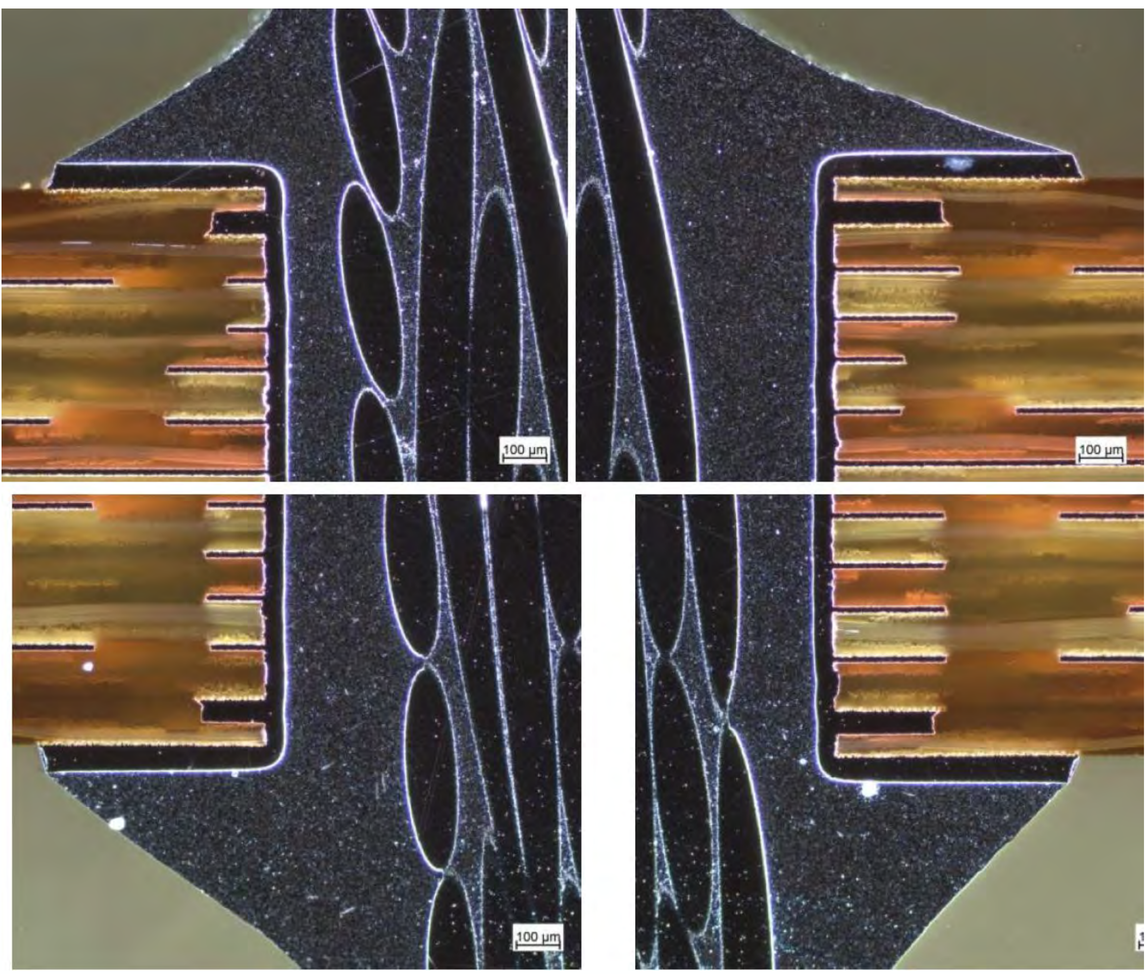


Optical microscopy

Bright field inspect metallization



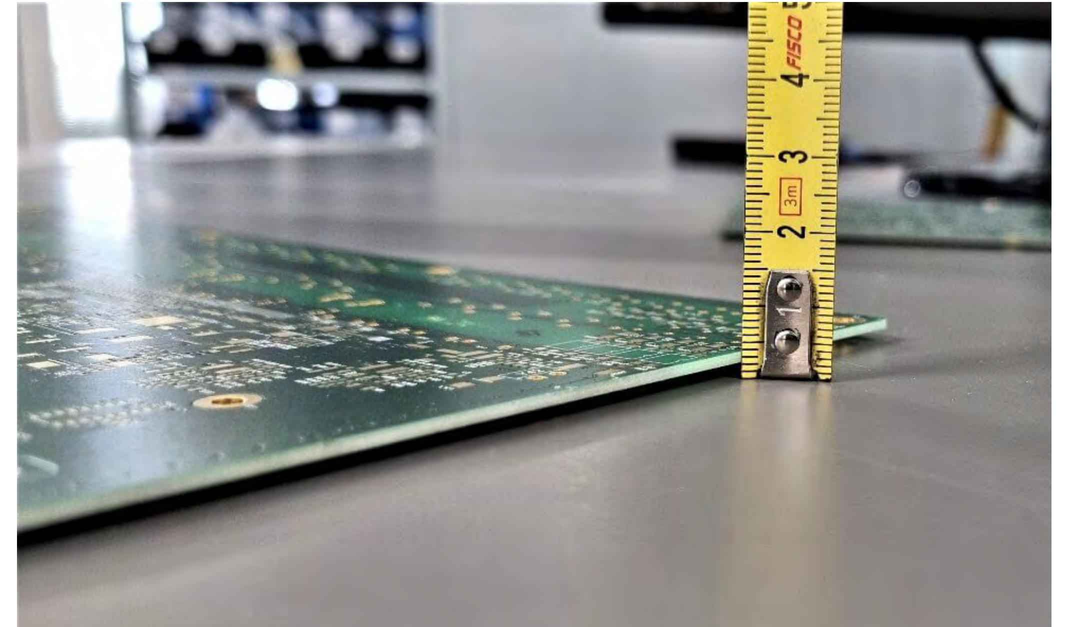
Dark field to inspect dielectric



Review items - Flatness

PCB flatness is affected by:

- Symmetry of build-up: dielectric thickness, copper foil thickness, lamination sequence
- Symmetry of copper thickness on individual laminates
- Uniform copper distribution within the layers



Warp, twist <1.5%

Procurement Authority may specify

more stringent rqt for critical SMT, e.g. <0.75%

ECSS-Q-ST-70-12 § 7.1.1, § 7.1.2

ECSS-Q-ST-70-60 § 9.3.3.2 and its NOTE3, § 9.3.3.3

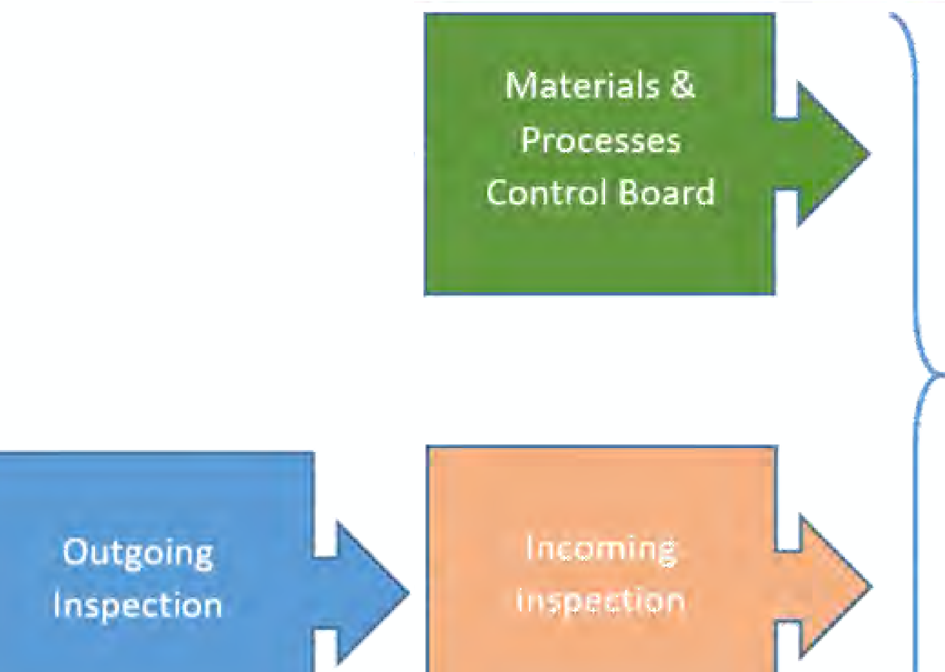
Incoming inspection

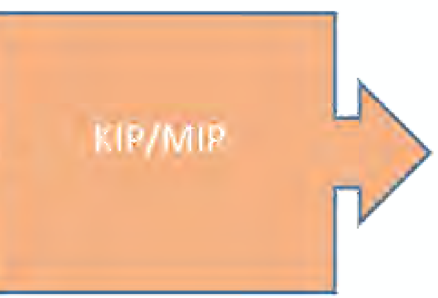
- ✓ Visual inspection on 100% of PCBs
- ✓ Microscopy on coupons before and after thermal stress by one of the following means:
  - procurement authority
  - external third-party lab
  - assembly house
  - PCB manufacturer using another inspector than the one for outgoing inspection.
- ✓ Verification of CoC, documentation and packaging

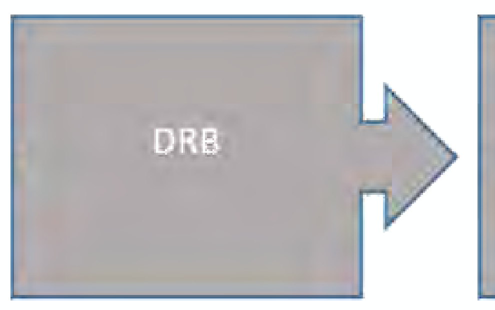
First Article Inspection FAI is microsectioning one PCB of a batch for first procurement.

ECSS-Q-ST-70-60 § 8.4, 8.5c

Late failures







Thermo-mechanical strain in PCB

PCB is mostly affected by thermo-mechanical stress in z-direction, not so much by mechanical stress or radiation.

Assembly is mostly affected by thermo-mechanical stress in x,y direction and mechanical stress (vibrations).

Animations courtesy of PWB Interconnect

Barrel crack

Interconnect separation

Electrochemical migration

Electronic Components and Materials Laboratories

- Microsectioning
- Mechanical polishing, chemical etching, ion beam polish
- Optical microscopy
- Scanning Electron Microscopy SEM
- Energy Dispersive X-ray spectroscopy EDX
- Xray Fluorescence XRF
- Focussed Ion Beam FIB
- Climatic chambers for humidity testing THB, CAF, SIR
- Environmental chambers for thermal cycling in ambient and vacuum
- Interconnect Stress Testing IST
- Computer Tomography CT Xray
- Infrared IR Thermography
- Solder bath float, rework simulation, vapor phase simulation
- Ionic cleanliness

https://technology.esa.int/lab/materials-electrical-components-laboratory

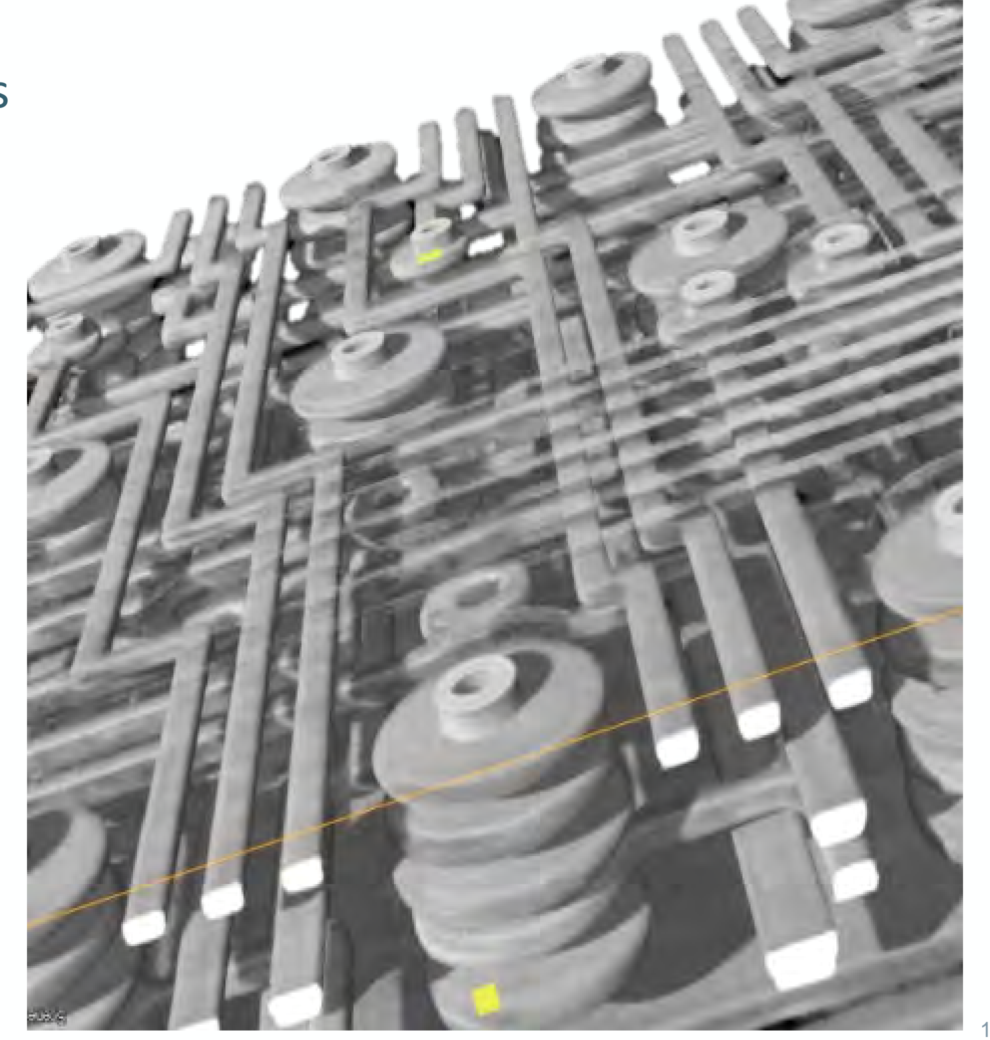
Computed Tomography X-ray

CT X-Ray does not provide the spatial resolution to detect cracks

CT X-ray does not provide enough contrast to detect imperfections in the dielectric

But it is an easy tool, non-destructive, and frequently used.

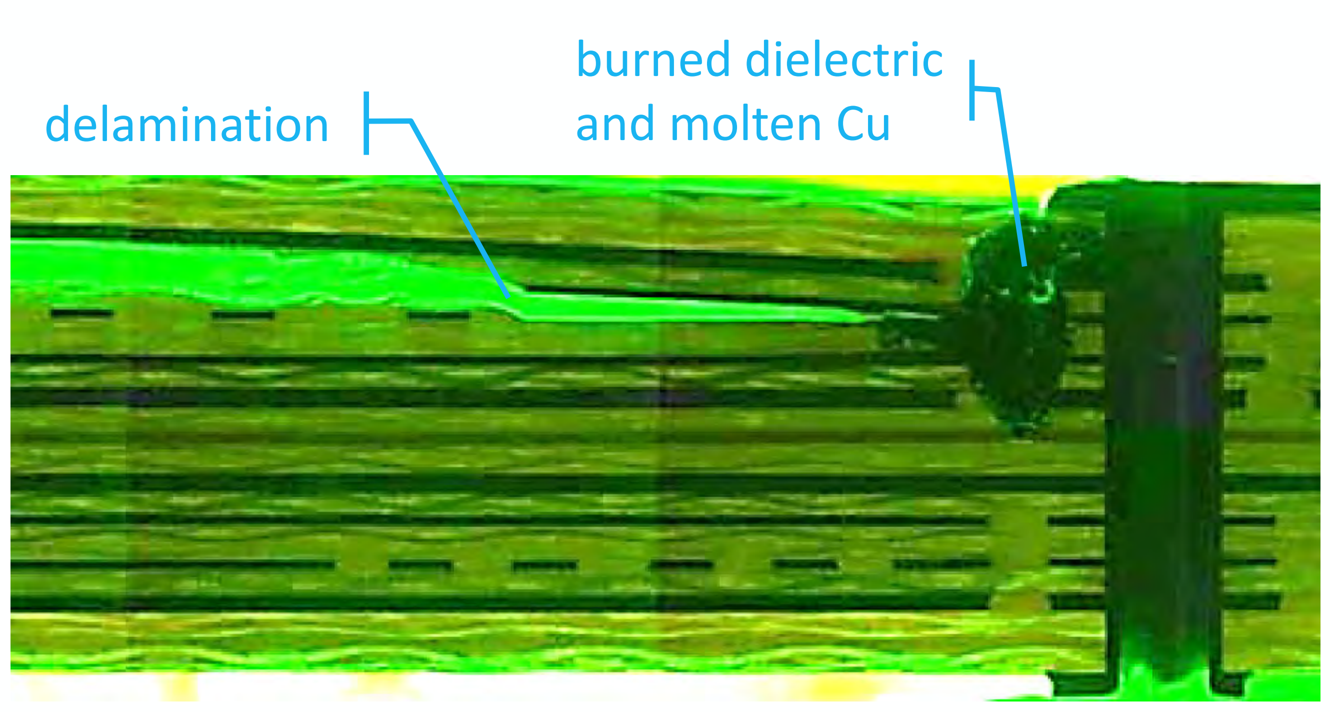
Microvias CT Xray

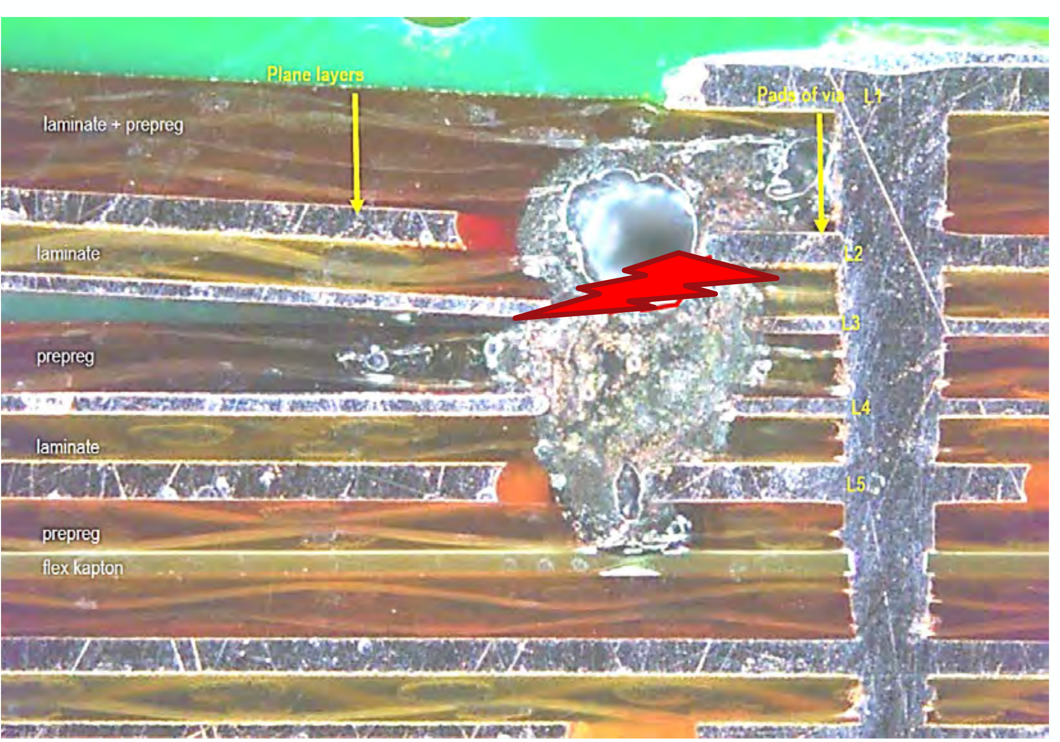


Case study – short circuit fqilure

power conditioning and distribution unit

- Unclean materials
- Design without margin





Design – Voltage rating and Double Insulation

Risk mitigations against latent short circuit – design aspects:

- Specify **insulation distance** as function of voltage
- Implement margin for **double insulation** of critical signals
- Take account of tolerances in **dielectric thickness**
- Take account of **etching tolerances** for in-plane clearances
- Specify presence of **non-functional pads** in thick planes
- Specify **2 sheets of glass** reinforcement between copper layers

Example: 4 mil laminate with 2 oz Cu can have a min projected peak-to-peak dielectric thickness of 68 μm.

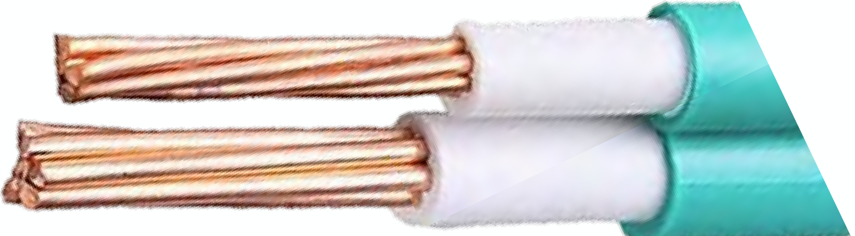
Design – Voltage rating and Double Insulation

Critical nets are subject to double insulation:

1. non-protected sections of a main bus power distribution system up to and including the first protection device,
2. nets that are a single point failure SPF for the system,
3. nets on which a loss of insulation can result in electrical failure propagation to a critical net,
4. cross-strapped functions and associated common links from source to load.

Double insulation in general applications:

Apply two redundant and individually cured insulators in case the distance between nets is ≤ 1 mm.



Design – Voltage rating and Double Insulation

Double insulation in PCB design:

Option 1: Apply margin by increasing insulation distance (in x,y,z). If possible, staggering nets (instead of superimposing) is recommended. However, 1 mm distance cannot be obtained in PCBs.

Option 2: Apply two redundant and individually cured insulators. For example: prepreg and (flex) laminate, but not 2x prepreg.

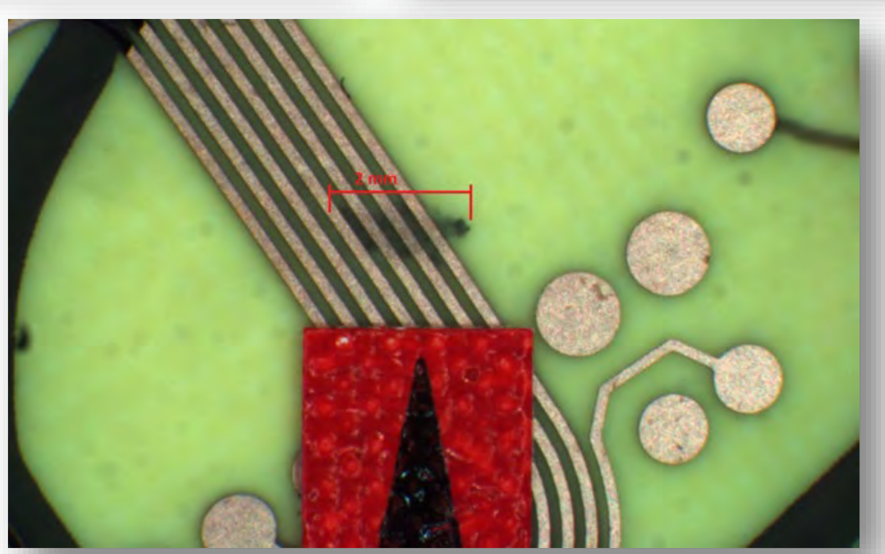
In case double insulation applies:

- Specify in PCB definition dossier
- Clean raw materials as per Appendix A of IPC-4101
- Raw material supplier has passed an audit, as per Appendix A of IPC-4101.
- First article inspection: microsectioning a PCB to verify dimensional spacing and dielectric integrity

Case study - contamination in CCL

Inspections on base laminate

- Incoming sample inspection
- In-process visual inspection on etched layers
- Automated Optical Inspection
- Outgoing inspection on external layers



Case study - contamination in CCL – App A

Appendix A of IPC-4101E specifies a better class of cleanliness of laminate and prepreg, by reinforcing:

- the acceptance criteria for (sub)surface imperfections
- the sampling for inspection (visual and AOI)
- the consequences of rejection

IPC-4101

3.8.3.1.6 Surface and Subsurface Imperfections

e. The foreign inclusions are translucent.

f. Opaque foreign fibers are ≤13 mm [0.512 in] in length and average no more than one per 300 mm x 300 mm [11.81 in x 11.81 in] inspected.

g. Opaque foreign matter other than fibers **shall not** exceed 0.50 mm [0.019 in]. Opaque foreign inclusions <0.13 mm [0.005 in] **shall not** be counted. Opaque foreign inclusions between 0.50 mm [0.019 in] and 0.13 mm [0.005 in] inclusive **shall** average no more than two spots per 300 mm x 300 mm [11.81 in x 11.81 in] inspected.

Appendix A

A.3 - LAMINATE

A.3.1 Acceptance Criteria for Laminate The requirements of 3.8.3.1.6 shall apply for imperfections on laminate, with the following modification:

– Requirement 'f' shall be deleted and the following shall apply: Opaque foreign matter shall not exceed 0.50 mm [0.019 in]. Opaque foreign inclusions <0.13 mm [0.005 in] shall not be counted. Opaque foreign inclusions sized between 0.13 mm [0.005 in] and ≤0.50 mm [0.019 in] shall average no more than two spots per 300 mm x 300 mm [11.81 in x 11.81 in] area inspected.

Case study - contamination in prepreg

Contamination can be introduced by raw materials supplier,

But the higher risk is with the lay-up process during PCB manufacture.

Case study – contamination at PCB lay-up

The PCB manufacturer shall treat all processes from innerlayer bond promotion until lay-up as critical processes with respect to cleanliness.

Cleanliness control procedure:

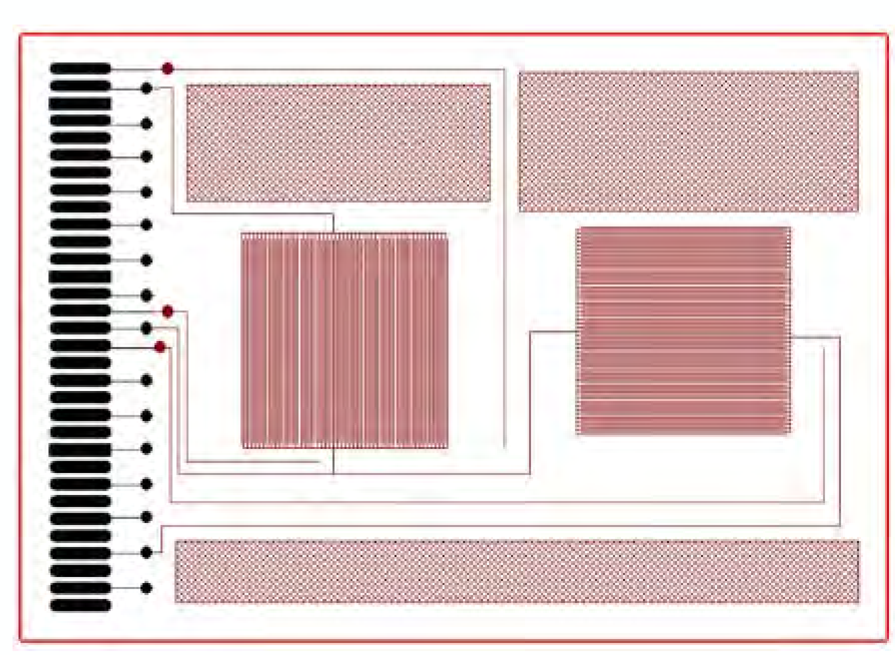
- Overpressure and filtered air supply
- Class 100‘000 in lay-up room
- Monitoring of air quality
- Restrictions on the use of materials that show static charging
- Segregation of epoxy resin dust from polyimide lay-up
- Class 1‘000 cleanroom on laminar flow bench lay-up station
- De-ionisation equipment at lay-up
- Keep processed innerlayers clean and covered.
  Progressively transport them towards cleaner rooms.

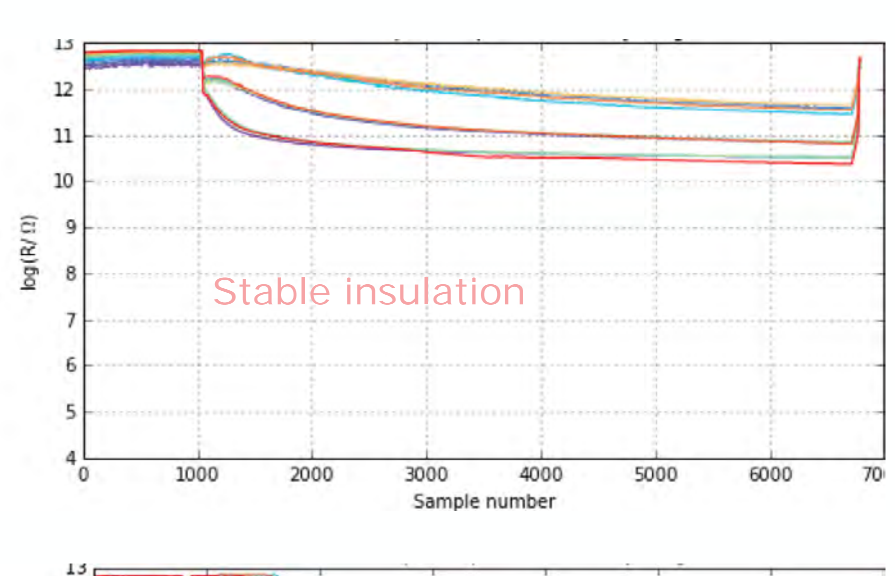
Case study – contamination, THB test

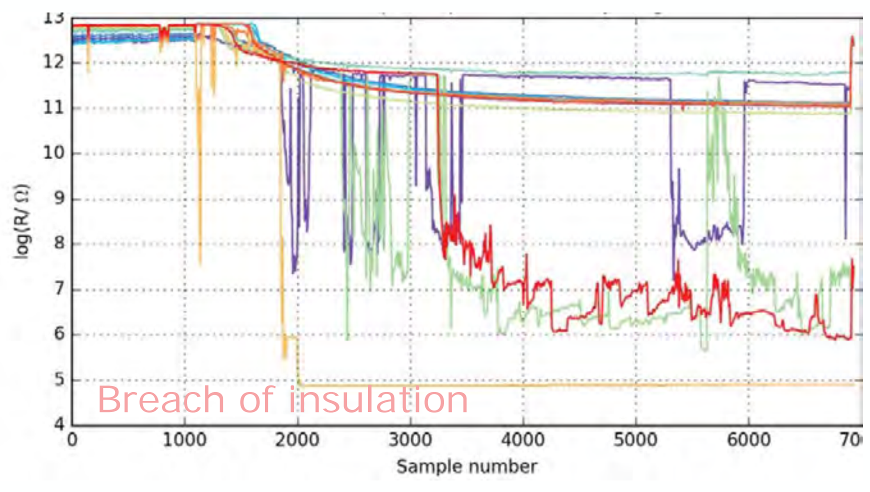
Temperature Humidity Bias test

85^0C, 75%RH, 50V, 150h

on comb pattern with 150 um spacing

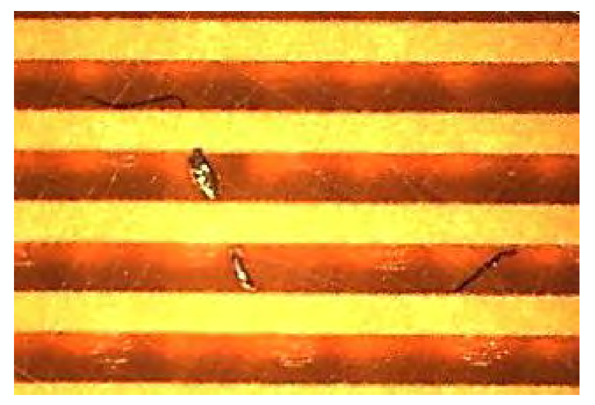


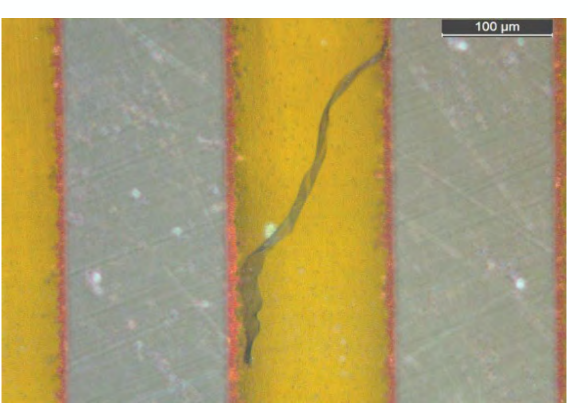


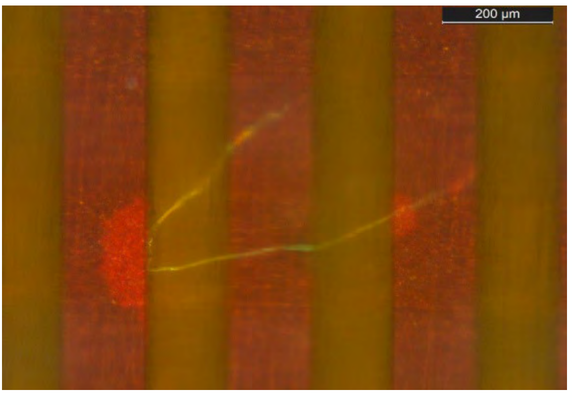


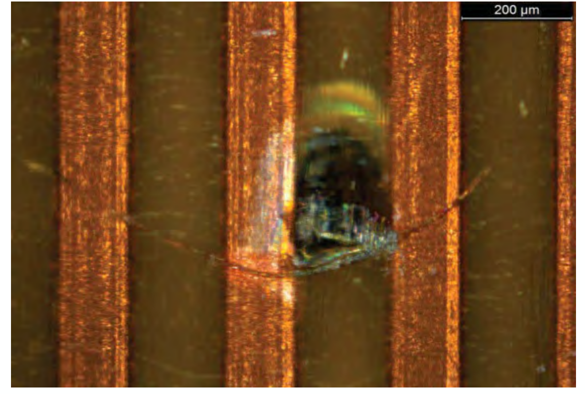
Case study – contamination, THB test

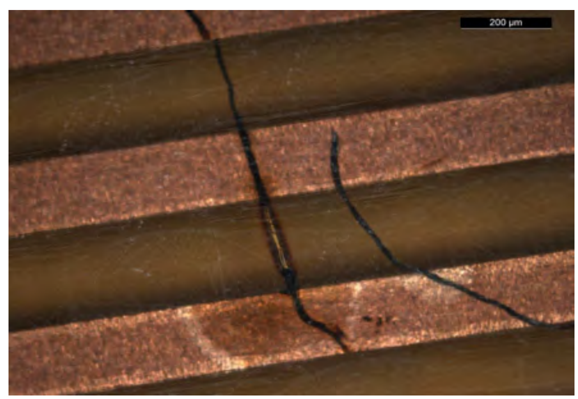
Non-conductive contamination in dielectric can cause latent short circuit failure. At first a leakage current is established, after which an intermittent short can eventually lead to a permanent failure.

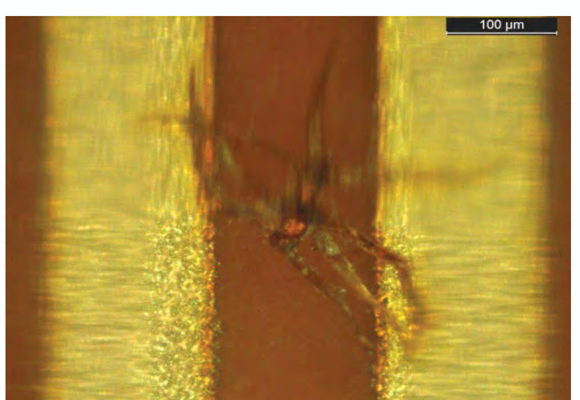












Case study – contamination, electrical test

High resistance electrical testing

IPC-9252	IPC6012ES class 3 w space add.	ECSS-Q-ST-70-60
10 V	250 V	250 V
10 MΩ	100 MΩ	1 GΩ

- 1 GΩ threshold
- V drop during ramp up constitutes a failure
- Direct resistive testing
- 1.27 mm adjacency

Case study - delamination

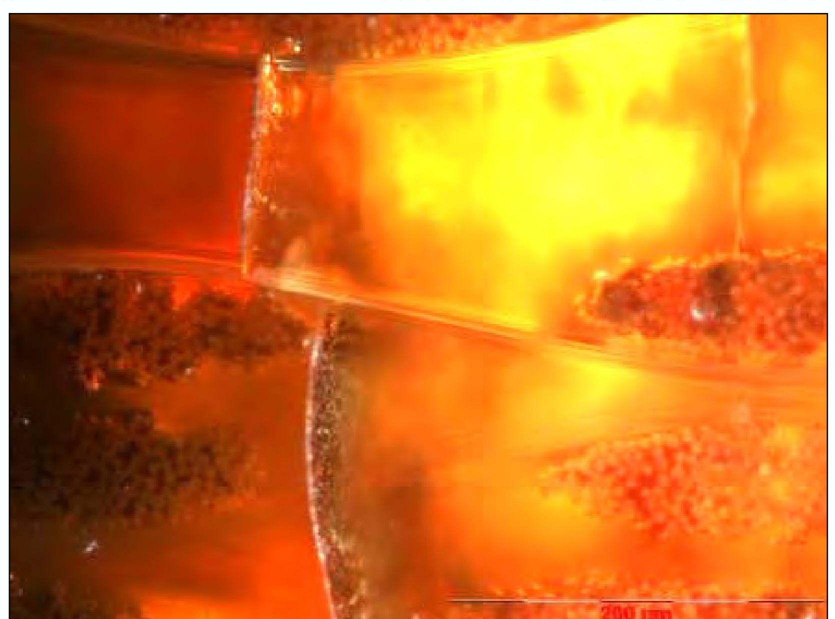
- Rigid-flex technology is inherently weak(er) -> delamination
- **Thick copper** plane layers provide a high profile which cause non-uniform pressure
- Absence of non-functional pad on flex laminate
- Coupons were not representative of presence of planes

500 µm

Case study – resin cracks

- Poor mechanical properties of polyimide resin: EA-2010-MAT-12A
- Inspection with **dark field** missing
- **Thick copper** planes cause resin rich volumes
- Absence of **nonfunctional pads** in plane layers cause resin rich volumes
- Technology (PCB & Cu thickness) was not covered by **qualification**

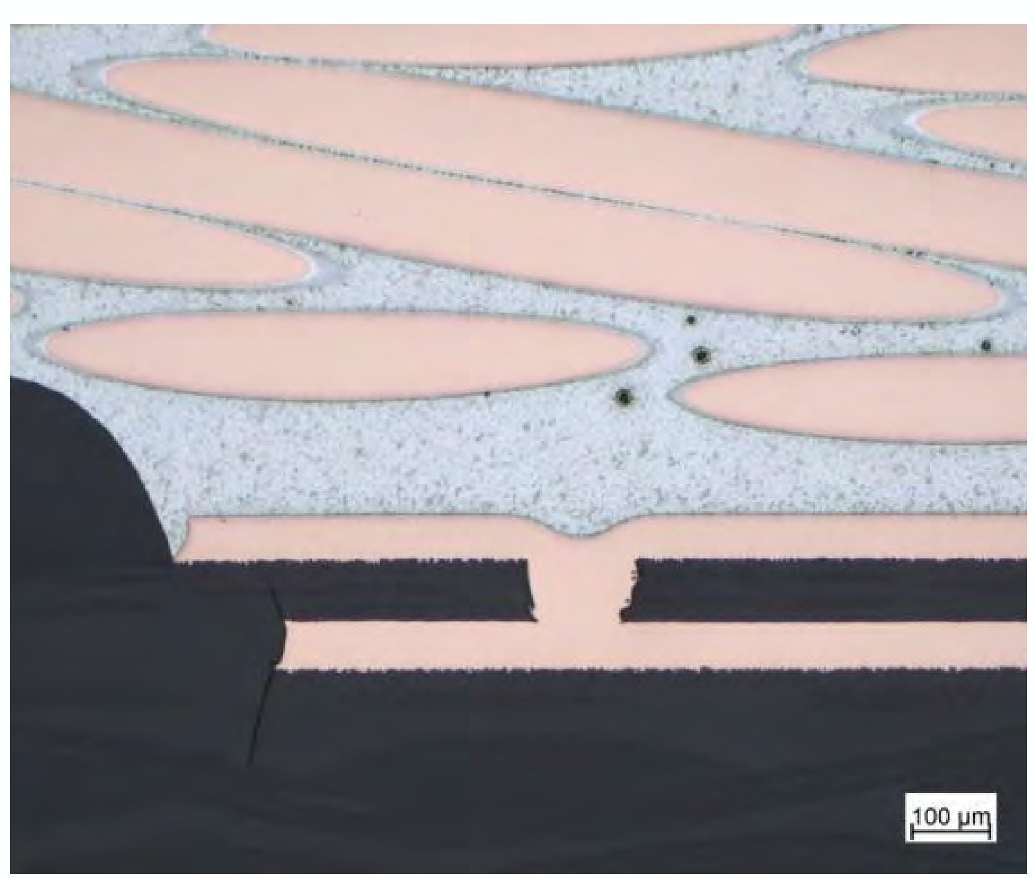
Case study – resin cracks

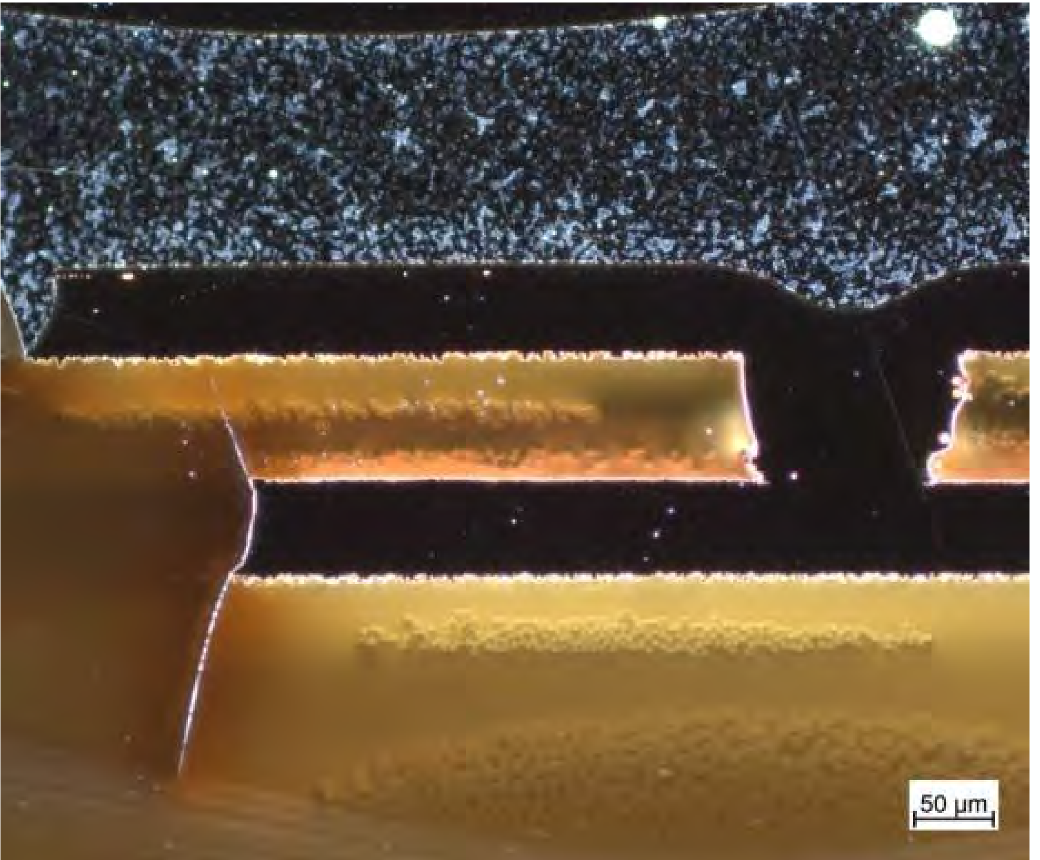


500 µm

Case study – dielectric integrity

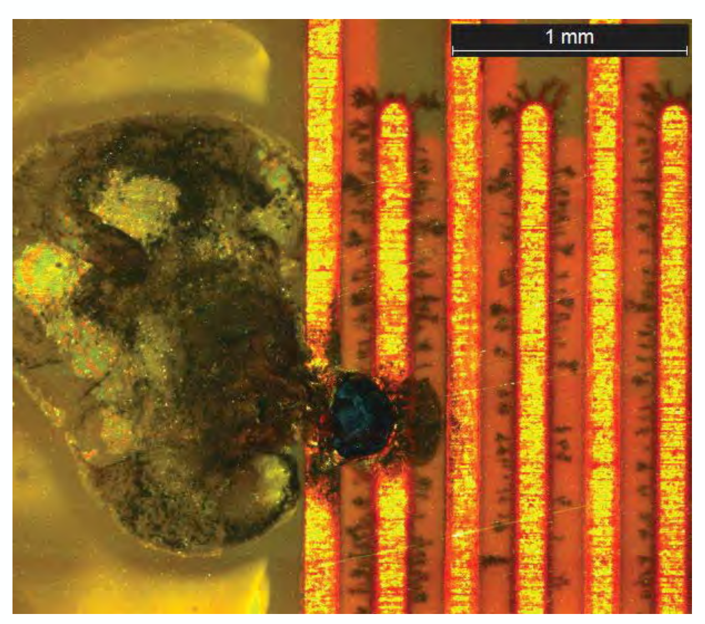
Dark field microscopy is paramount for evaluating dielectric integrity, including cracks, contamination and other types of inhomogeneity that may be located subsurface.

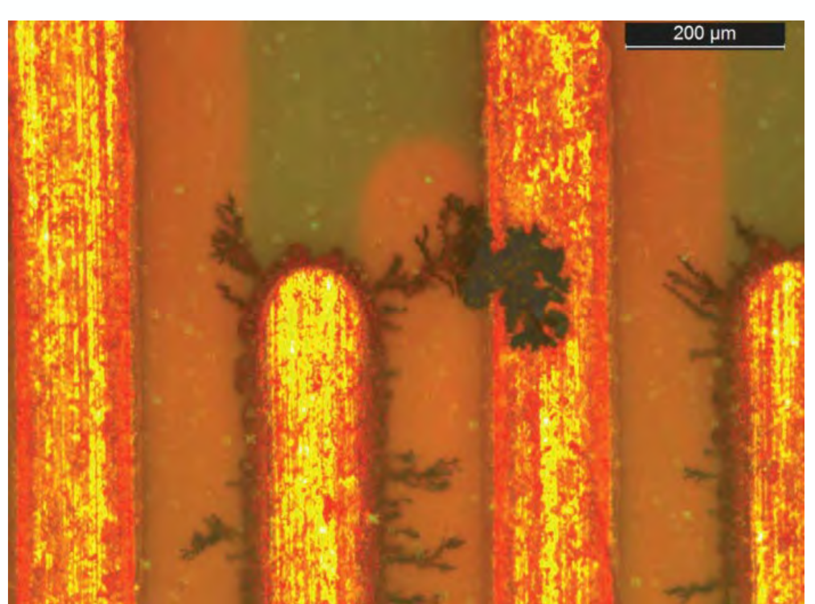


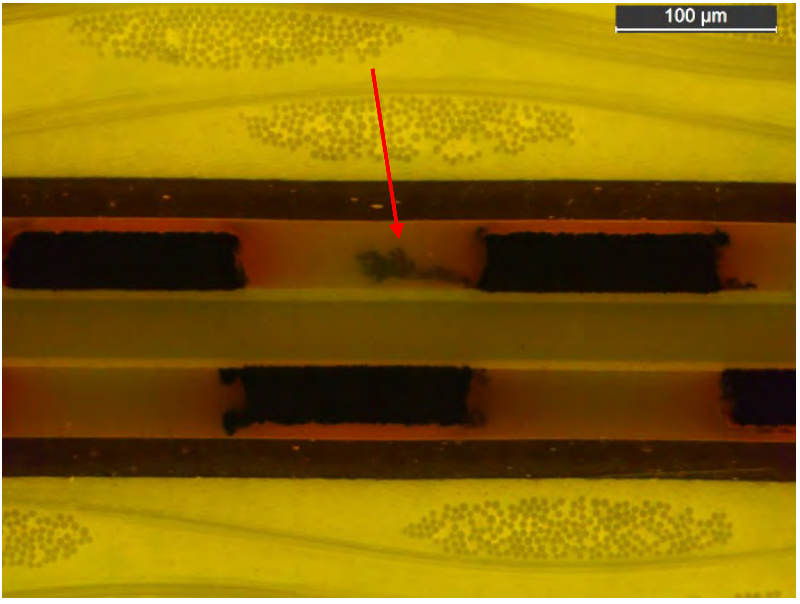


Case study – Coverlay adhesive

Acrylic adhesive in coverlay for rigid-flex PCBs is very susceptible to dendritic growth, even without contamination.







Case study – burn-in test

To mitigate ECM (in PCBs), a burn-in test can be done at module or equipment level:

Prior to burn-in, the board may be submitted to screening thermal cycles (next slide).

a) Immediately before burn-in, the board is conditioned in normal clean room environment for 7 days (thus, not baked and not exposed to vacuum).

b) The burn-in is for ≥ 168 hours in ambient clean room conditions with all nets powered, as much as possible in nominal operation. The burn-in is dedicated and continuous for its duration.

c) The burn-in is followed by functional and performance testing.

5.5.1.1 of ECSS-E-ST-10-03

Case study – screening thermal cycles

Screening thermal cycles can be done to mitigate **infant mortality by open circuit failure**.

a) min 4x thermal cycles at acceptance levels

b) followed by functional and performance testing
at min and max (operational) acceptance temperature levels

5.5.4.1k of ECSS-E-ST-10-03

May be followed by burn-in testing.

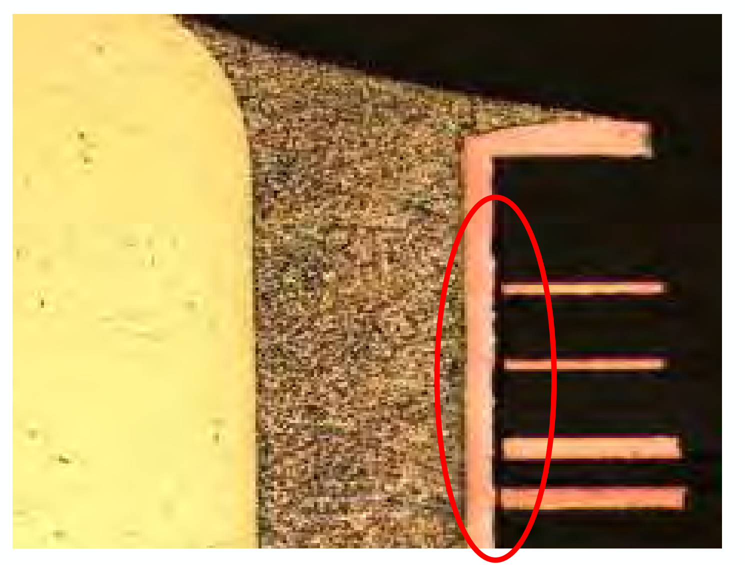
Case study – open circuit failure

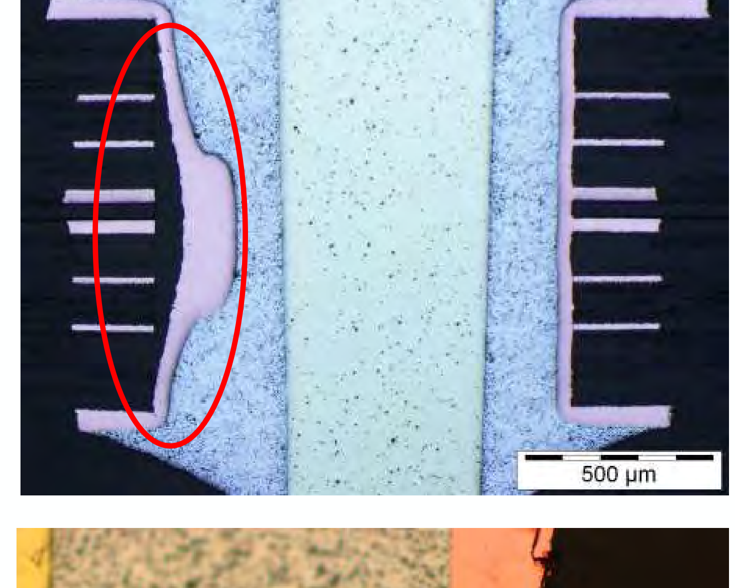
EA-2014-EEE-3B

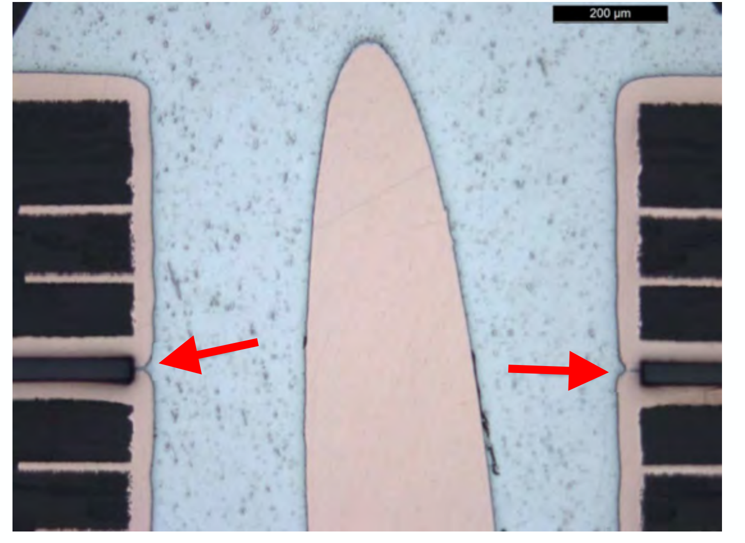
Inadequate outgoing inspection

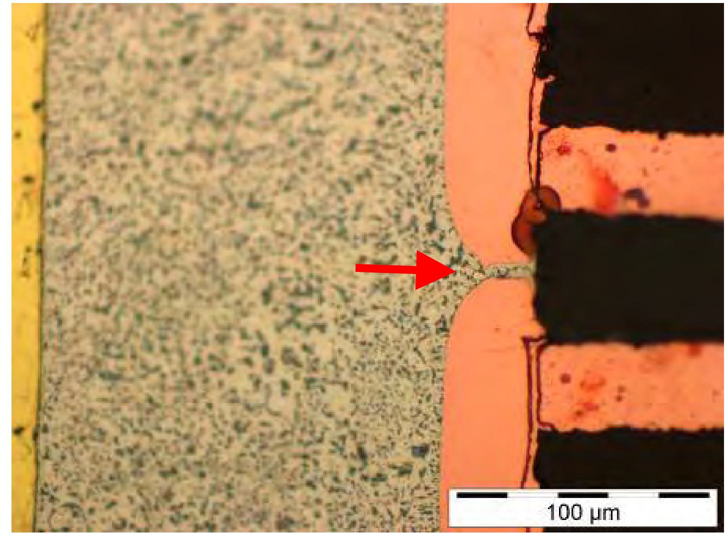
and process quality issues:

- Interconnect defect
- Skip plating on flex laminate





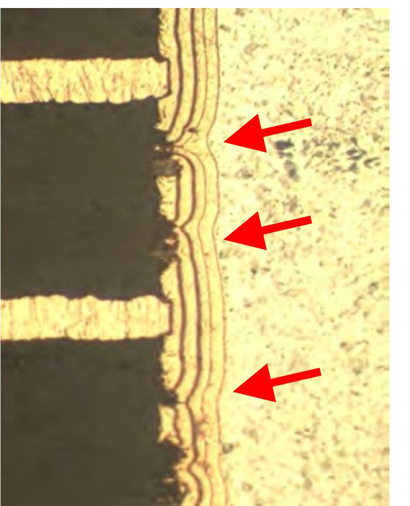


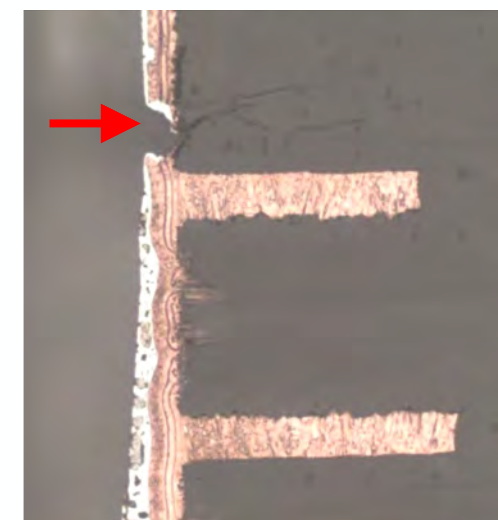


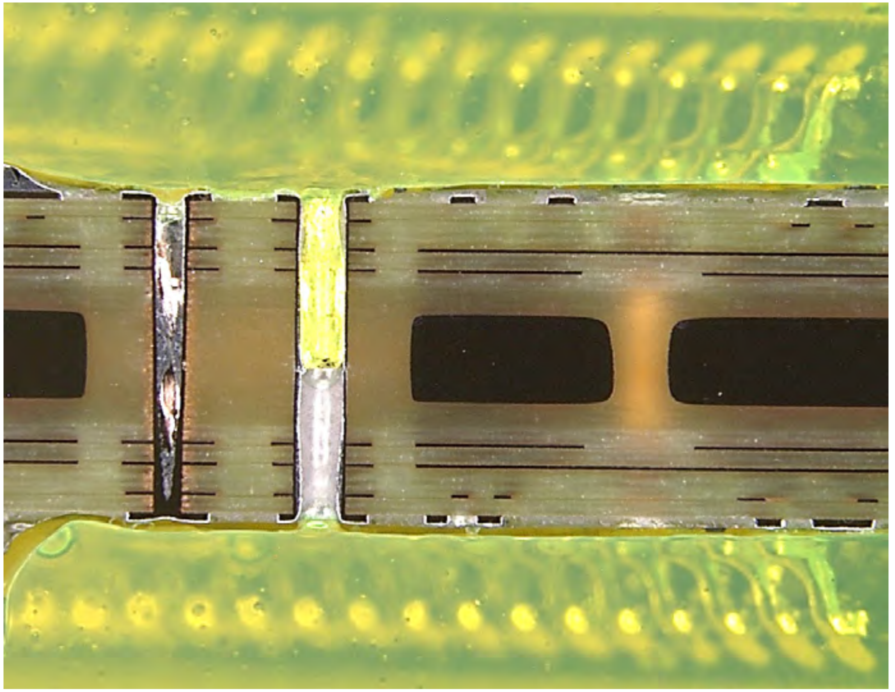
Case study – open circuit failure

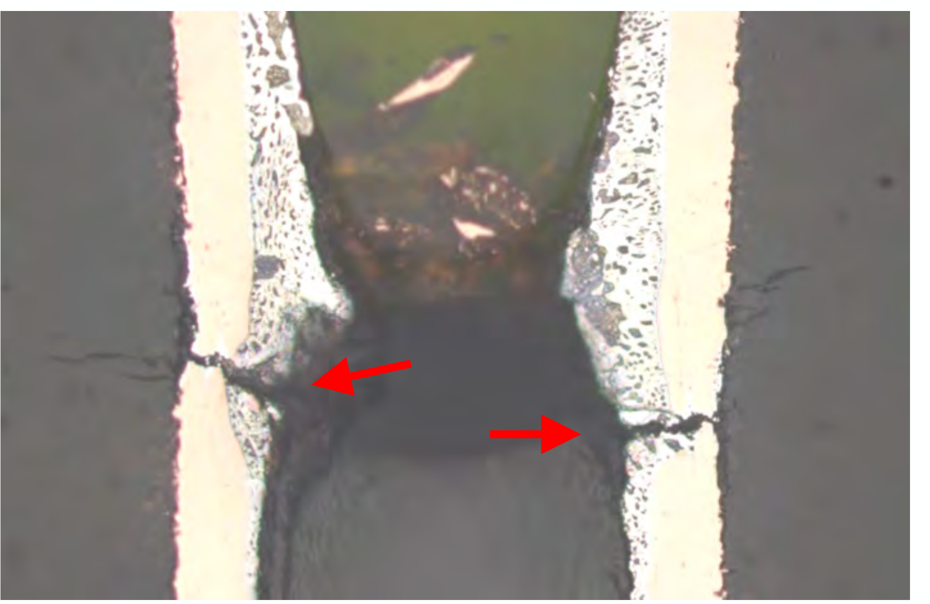
Latent open circuit failures

- Stressful design with Invar core
- Plating voids
- Skip plating









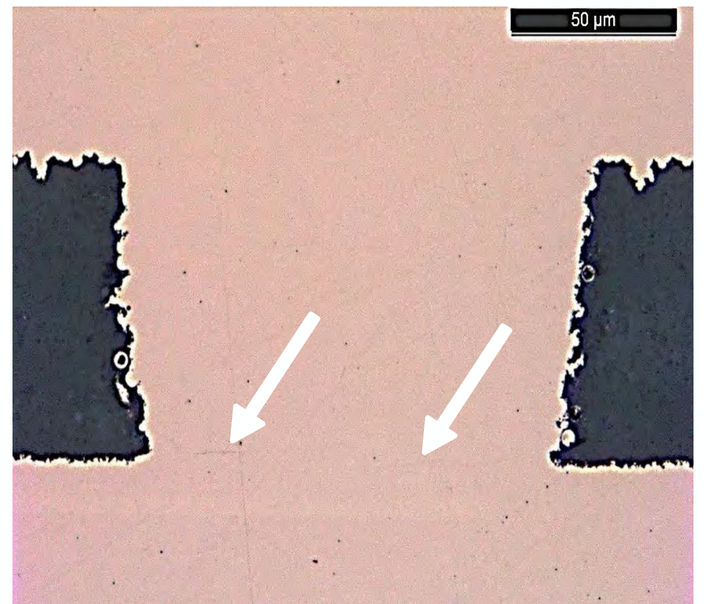
Case study – open circuit failure - microvias

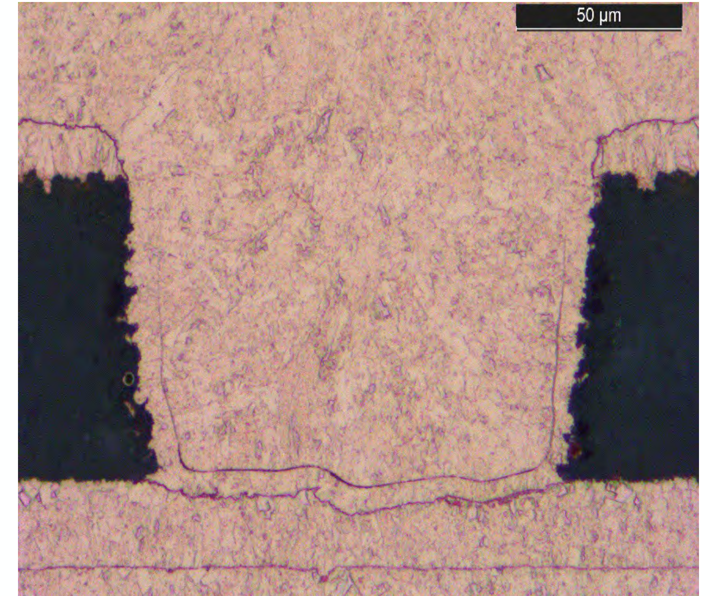
2x EU space industry alerts, global industry alert: “the hidden reliability threat”

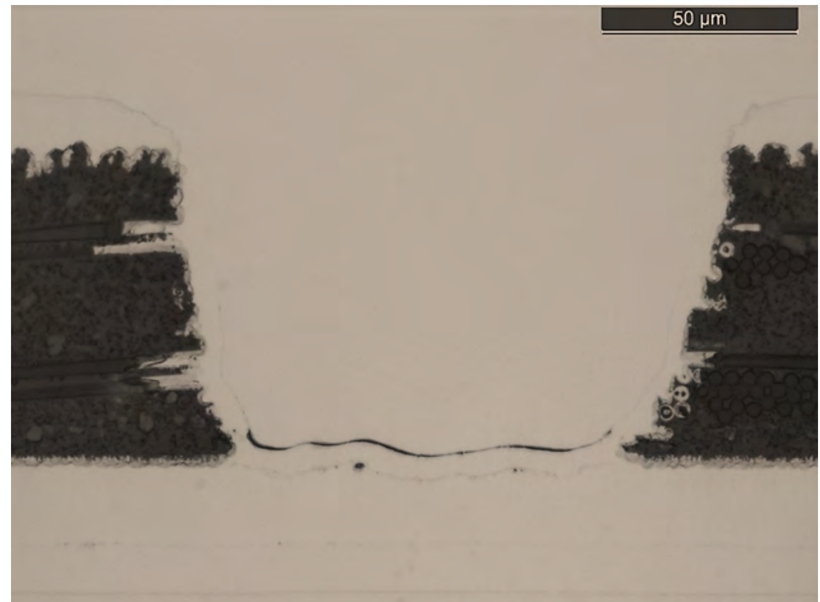
Polishing smears Cu, which can mask cracks.

Chemical micro-etch removes smear, but shows plating boundaries and does not allow to evaluate presence of cracks.

Ion beam polish is capable to reveal cracks.







EU IPC UVIA WG - background

Microvias can fail for one or more of the following reasons:

1. non-optimised materials and processes, causing general weak microvias
2. stressful design
3. inhomogeneous processes, causing an incidental weak microvia

The hidden reliability threat triggered IPC-V-TLS-WG.

In addition, a European IPC working group on microvia reliability has been raised.

- Gather PCB experts from EU high-rel electronics manufacturing industry,
- Execute a specific first work proposal, as well as to identify future work proposals,
- Strengthen EU industry presence in IPC standardization (on microvias).

EU IPC UVIA WG – test panel

Coupon
IST
HATS2
D-Coupon
CITC

MMCAT TV 175 v03
imec / ESA - 2022

EU IPC UVIA WG – test methods

<table>
<tr><th>Coupon</th><th>Test method</th><th>Precon</th><th>Cycling</th><th>2nd test</th></tr>
<tr><td>IST</td><td>ECSS-Q-ST-70-60
&
2.6.26A(A)</td><td rowspan="3">6x 245°C
IPC reflow profile</td><td>RT / 210°C
< 1000 x</td><td rowspan="4">RT / 245°C
< 100 x</td></tr>
<tr><td>HATS2</td><td rowspan="2">2.6.27B
&
2.6.7.2C</td><td>-55°C / +210°C
< 1000 x</td></tr>
<tr><td>D-Coupon</td><td>-55°C / +210°C
< 1000 x</td></tr>
<tr><td>CITC</td><td>2.6.26A(B)</td><td>none</td><td>RT / 245°C
< 100 x</td></tr>
</table>

EU IPC UVIA WG – build-up

4x uvia diameters

The smallest diameter is deliberately out of comfort zone.

First test round focuses on polyimide.

Second test round includes high speed laminate.

100 um dielectric thickness + Cu foil

diameter [um]	aspect ratio
175	0.6
150	0.8
125	0.9
100	1.2

First work proposal - objectives

Secure PCB supply chain

Request test panels from EU PCB supply chain for high-rel industry.

In addition, request panels from global state-of-the-art manufacturers for **benchmarking**.

Industry commonly specifies test regimes for qualification and lot conformance.

This test proposal goes beyond normal effort, by using **all** available accelerated coupon tests, which allows for the **most robust assessment** of microvia technology.

First work proposal - objectives

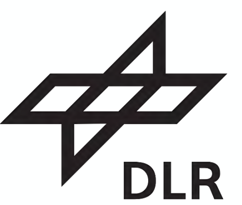
Validate test methodology

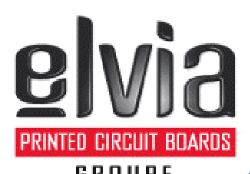
Correlation of accelerated coupon tests has never been done.
Only a single test has been introduced in 3.10.15 of IPC-6012E since 2020.
This is undesirable, as other test methods have been successfully used
(e.g. ESA standardized IST in 2014).

The test method validation can be input to setting common standards.

- It is not an objective to determine a single 'smoking gun' process flaw, as it is widely recognized this does not exist.
- Reliability is tightly correlated with design (complexity), which is a well-known and intuitive dependency. Design is not the driving parameter for the experimental work.

EU IPC UVIA WG – Customers, RTI, PCB manufacturers





UVIA manufacturing process review

Microvia process guidelines ESA-TECMSP-TN-19672:

- Recommendations to processes
- Tests for qualification, lot conformance and in-process verification
- Lessons-learned
- Suitable level of detail

Laser drilling, pre-etching, desmear, electroless copper, flash plating, via fill plating;

Pre-etching, micro-etch after desmear, prior to electroless copper, prior to via fill plating;

Rinses, pre-dip and post dip baths included in most processes.

Conclusion

Thank you for your attention !

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https://technology.esa.int/lab/materials-electrical-components-laboratory

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