Electronic assemblies and ECSS-Q-ST-70-61C

TEC-MSP Electronics Assembly Team

10/11/2023

Meet the ESA team

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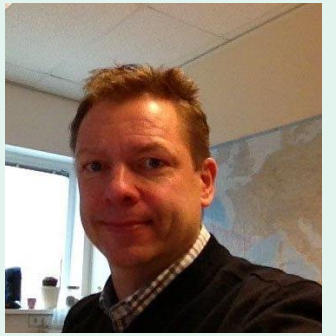


QR code to the questionnaire for PCB & EA training course.

Alternatively, access to the survey may be obtained using this simple URL:

https://qrco.de/pcbea

Presentation Outline

- Basics of electronic assembly

- Assembly reliability

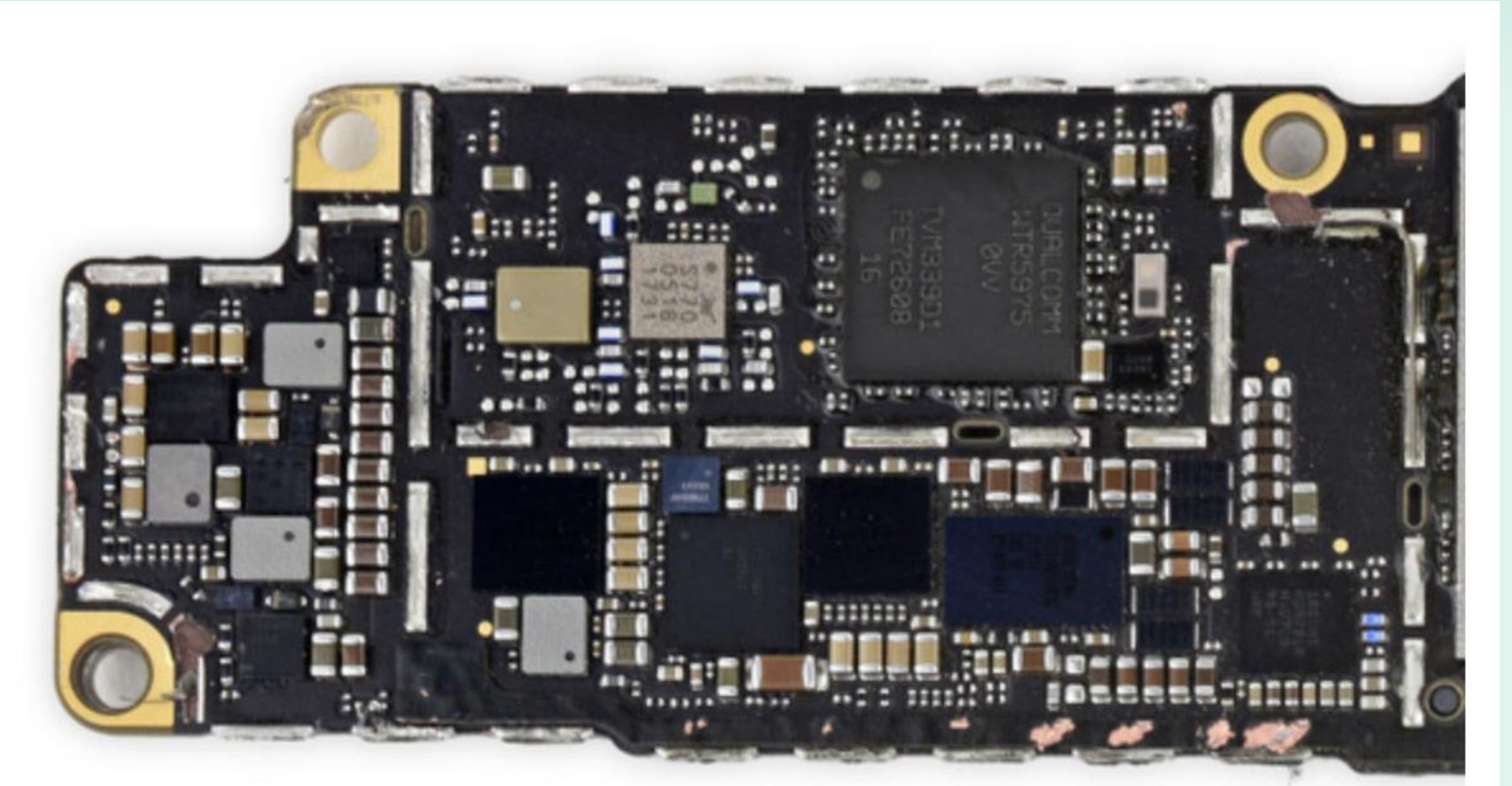
- What the standards says?

- MPCB: How does it work?

- What’s next?

Basics of Electronic Assemblies

Connections made using solder



Basics of Electronic Assemblies

Solder is used as mean to provide electrical and mechanical connection of different items:

- Printed Circuit Board plating:	- Component termination: See ESCC23500	- Wires
• Copper (Cu) with Tin Lead (Sn60Pb40) • Copper with lead free finish (RoHs compliant): ENIG/ ENEPIG/ Gold	• Tin Lead • Gold plating: degolding and pretining prior assembly using tin/lead solder • Silver plating: • COTS (pure tin,…)	• Silver • Copper (Cu) with Tin lead (Sn60Pb40) • Pure Tin

Basics of soldering

Connection made using solder: Printed Circuit Board

Rigid PCB

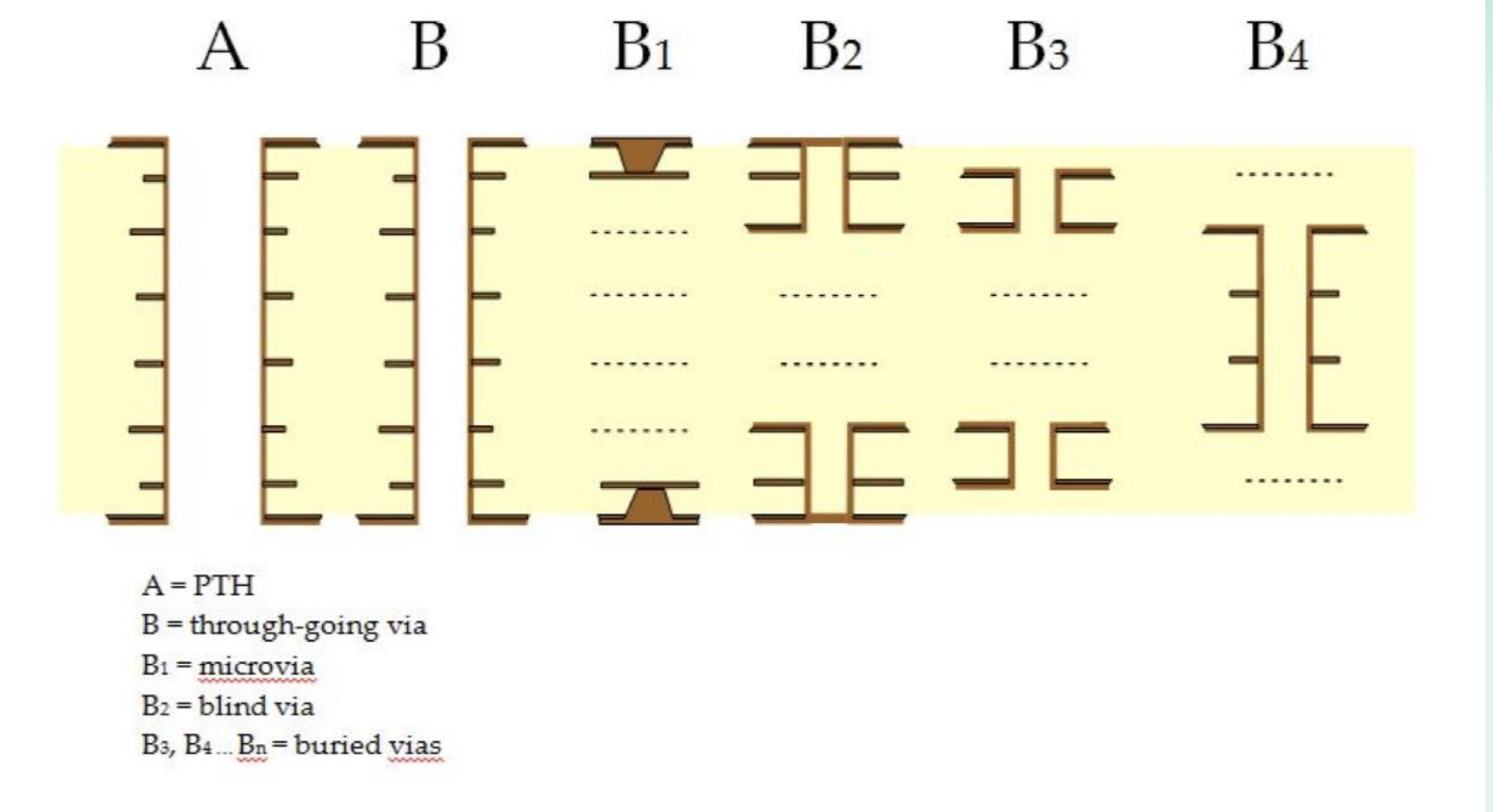
-Single sided

-Double sided

-Multilayer (A/B)

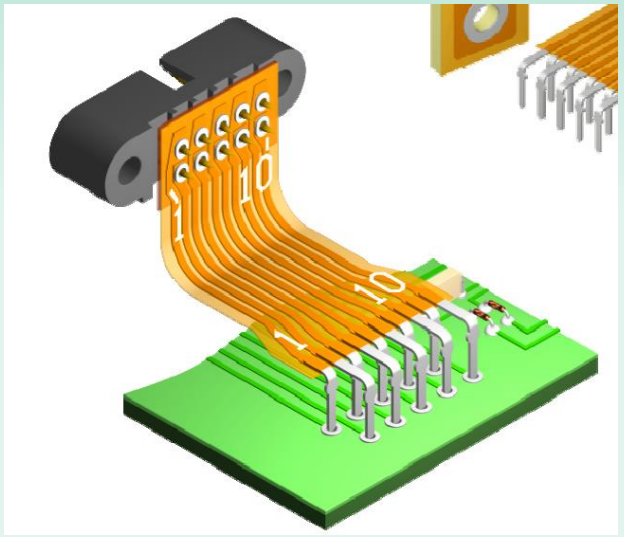
-Sequential (A/B/B2/B3/B4)

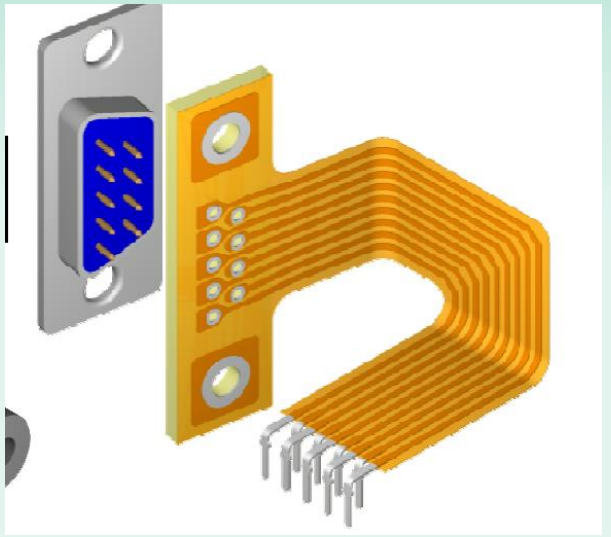
-Micro vias (A/B/B1/B3/B4)

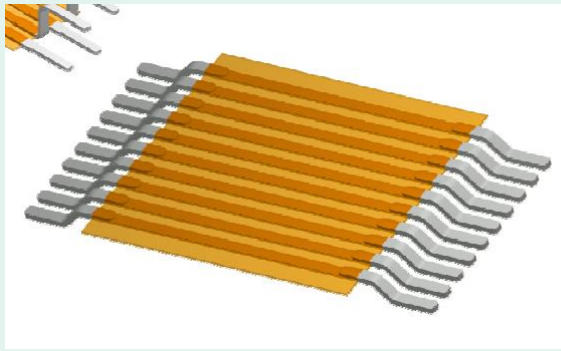


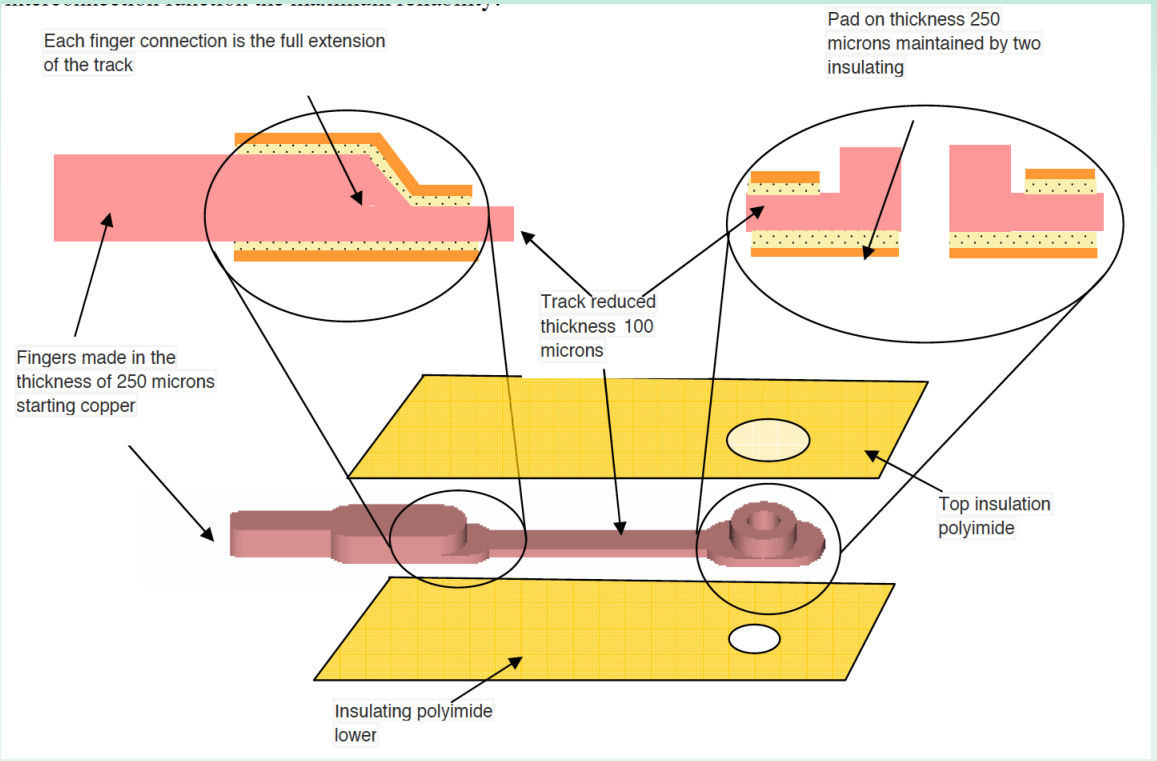
Basics of soldering

Rigid Flex and Sculptured Flex PCB



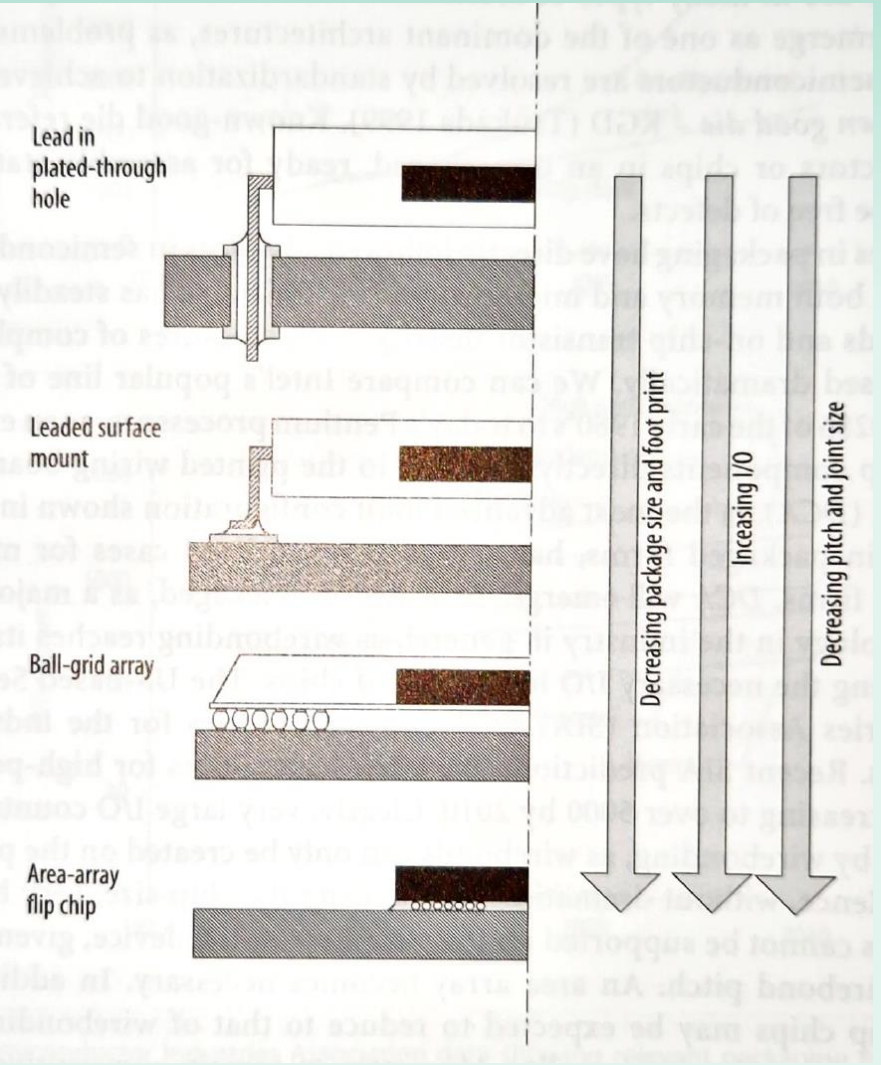






Basics of soldering

Evolution of solder joints in relation to packaging architecture overtime



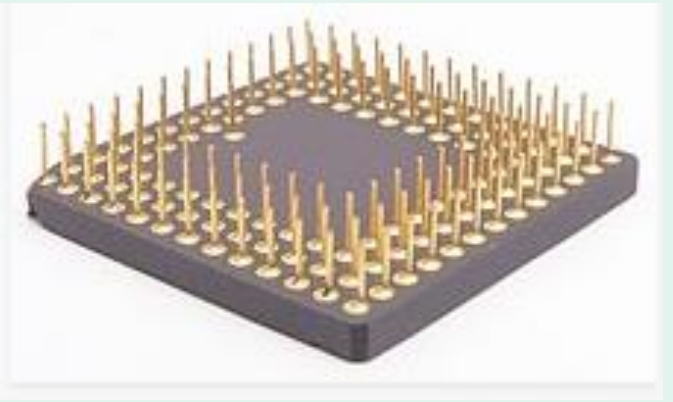
Source: J. W Evans A guide to lead free solders Springer

Basics of Electronic Assemblies

Through hole type of devices

With Stress relief

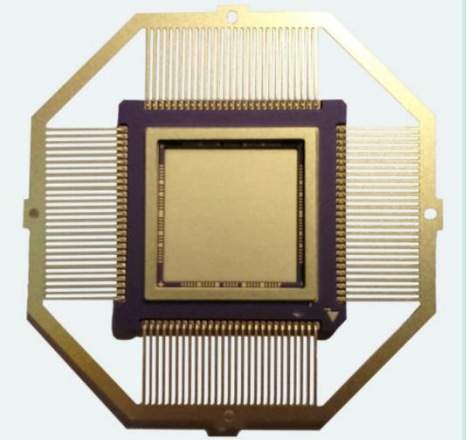
Without Stress relief



Basics of soldering

Surface Mount Devices: Leaded Devices

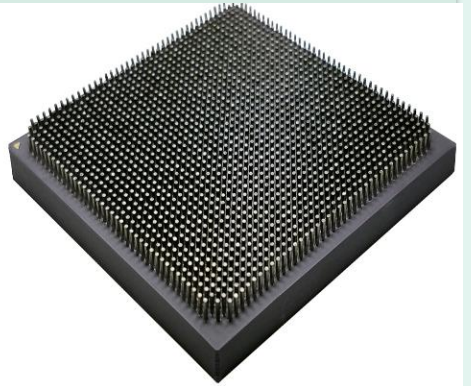
Flat pack



Gull wing

J leads

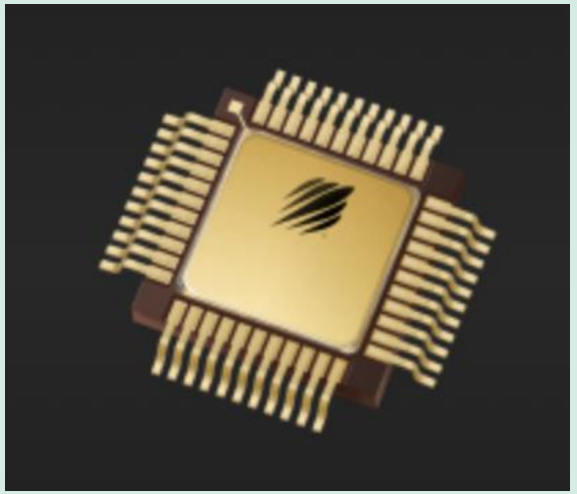
Area Array Device



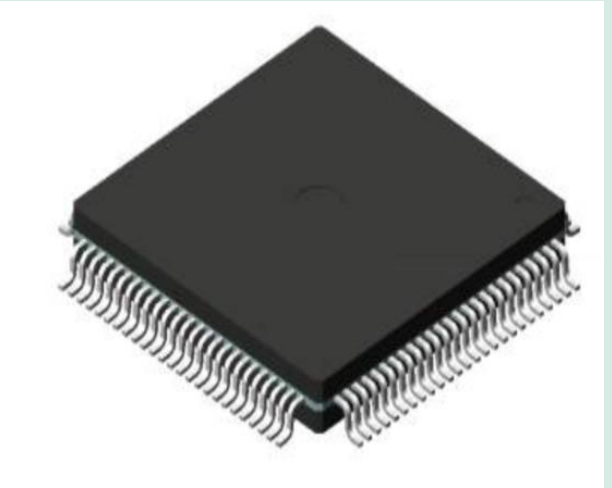
Basics of soldering

Surface Mount Devices: Leaded Devices

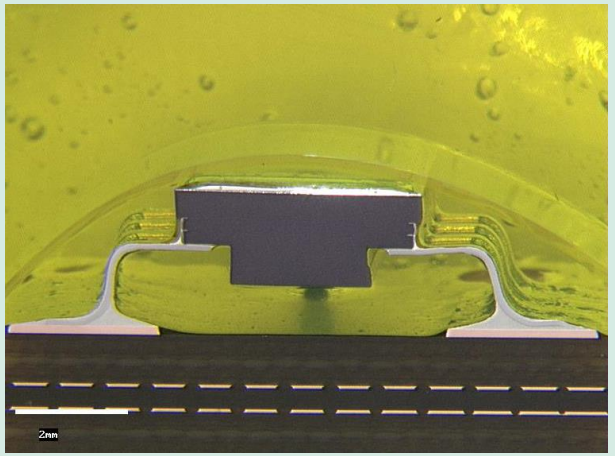
Top attachment



Middle attachment



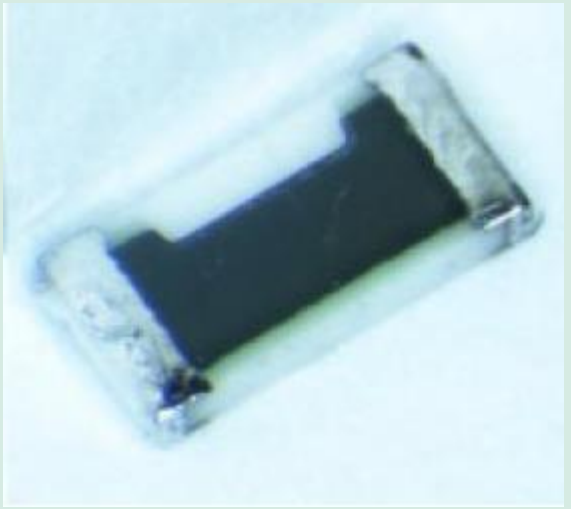
Bottom attachment



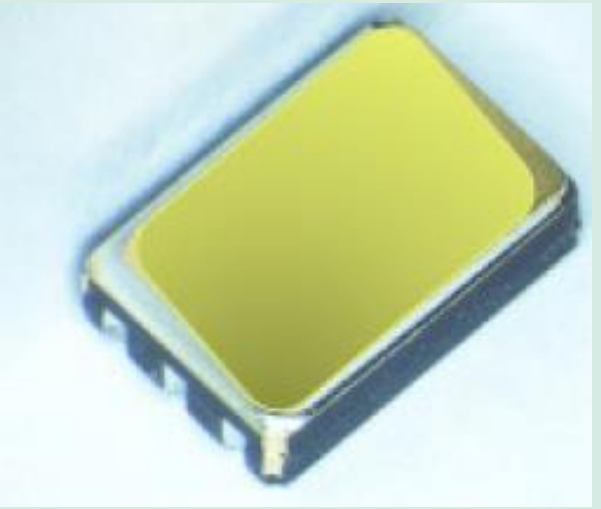
Basics of soldering

Surface Mount Devices: Leadless Devices

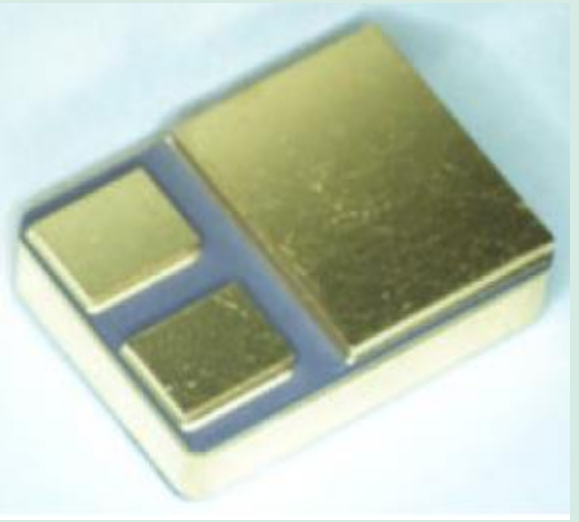
Chips



Castellated



Bottom terminations



Solderless Connections

Advantage: Possible to mate and demate with reduced damaged on the PCB.

Drawback: Limited experience on such assemblies

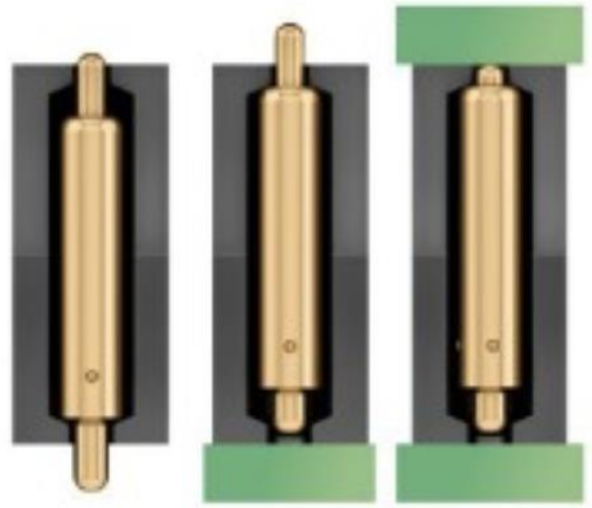
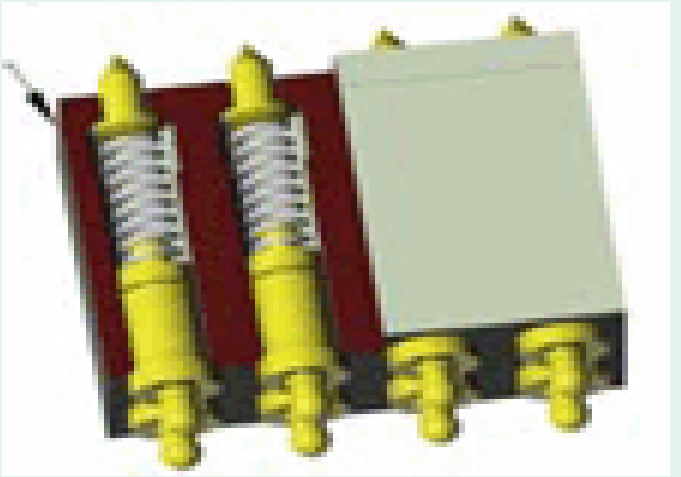


Figure 2a: Cross Section of Two-Piece Housing with Floating Probe



Stacking Connectors

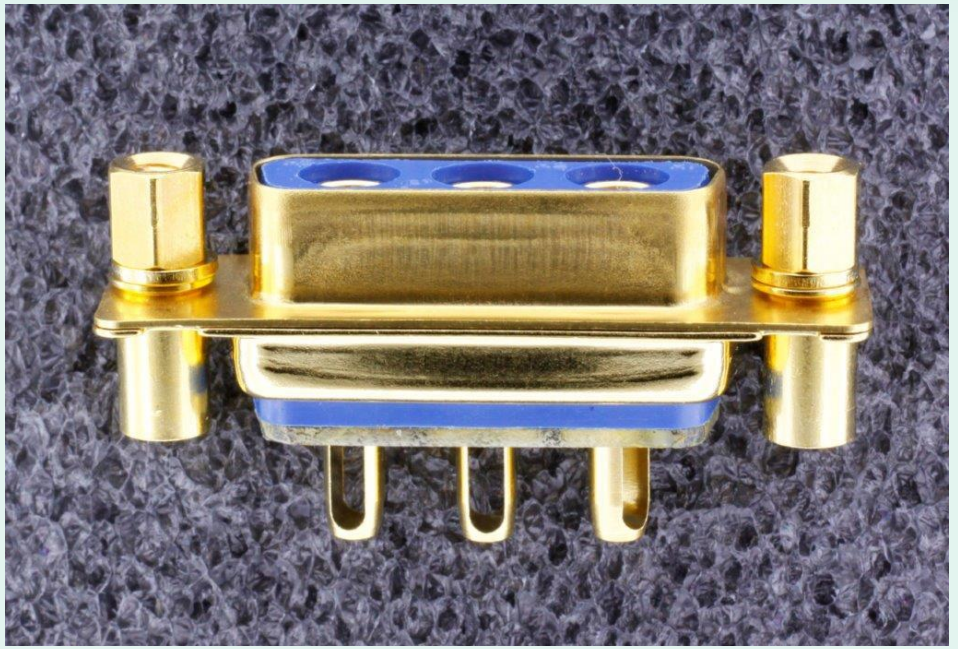
Spring Probe Interposers

- ESCC 3401/076 approved
- Z-Axis interconnects with solderless contacts
- High density button contact
- Design flexibility

Solderless Connections

Press fit connection

Not yet qualified for ESA programms that requires high reliability but under evaluation



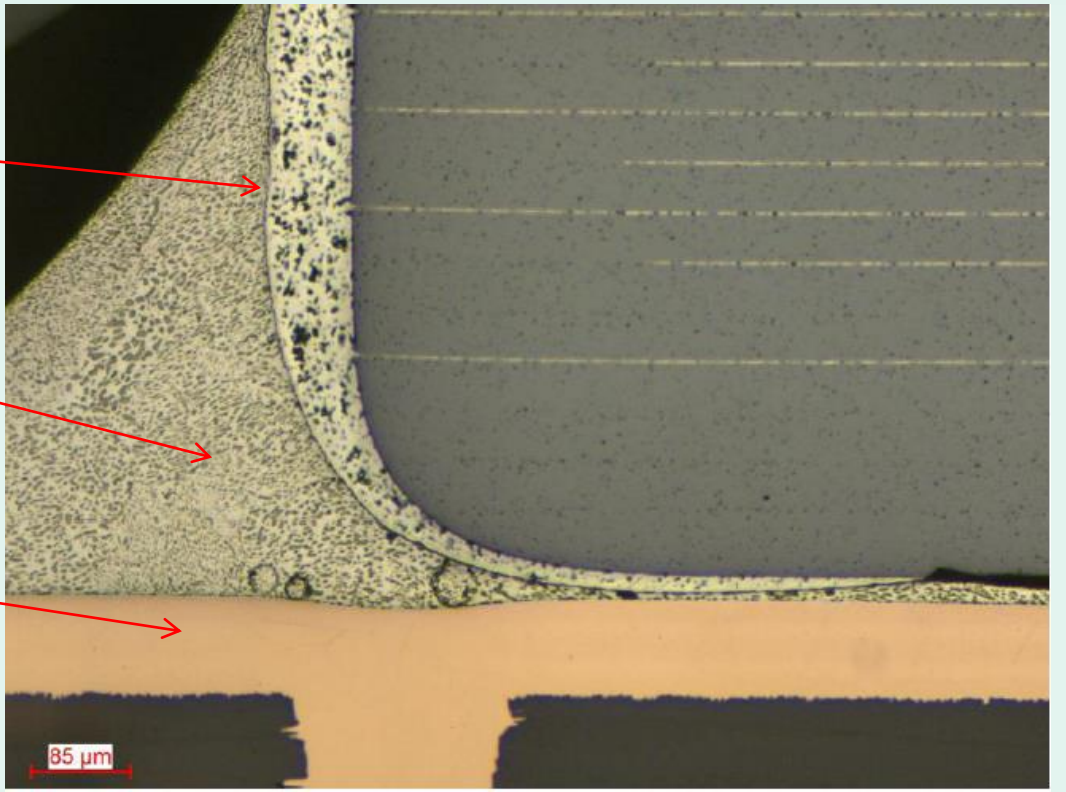
Basics of Electronic Assemblies

Soldering is a process in which two or more items are joined using a filler metals which is molten and form a joint. The filler metal has a lower melting point of the materials is joining and the process is performed at a temperature lower than the melting points of the materials to be joined.

Ni barrier melting point:1455 ° C

Sn63Pb37 solder melting point 183° C

Cu pad melting point: 1085° C

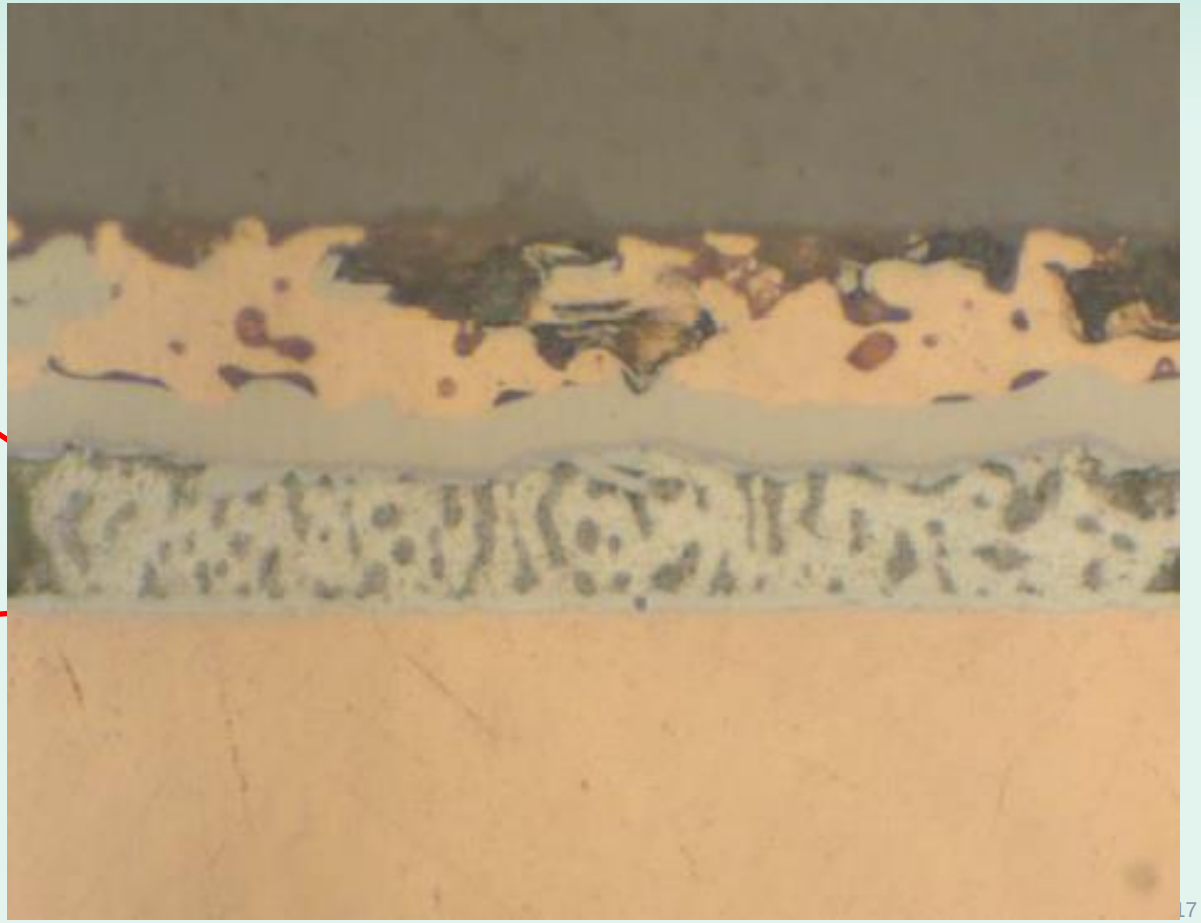


Basics of Electronic Assemblies

The bond between solder and the surface is to be joined is realized through the formation of intermetallic compounds at interface solder/substrate.

NixSny

Cu3Sn Cu6Sn3



Basics of Electronic Assemblies

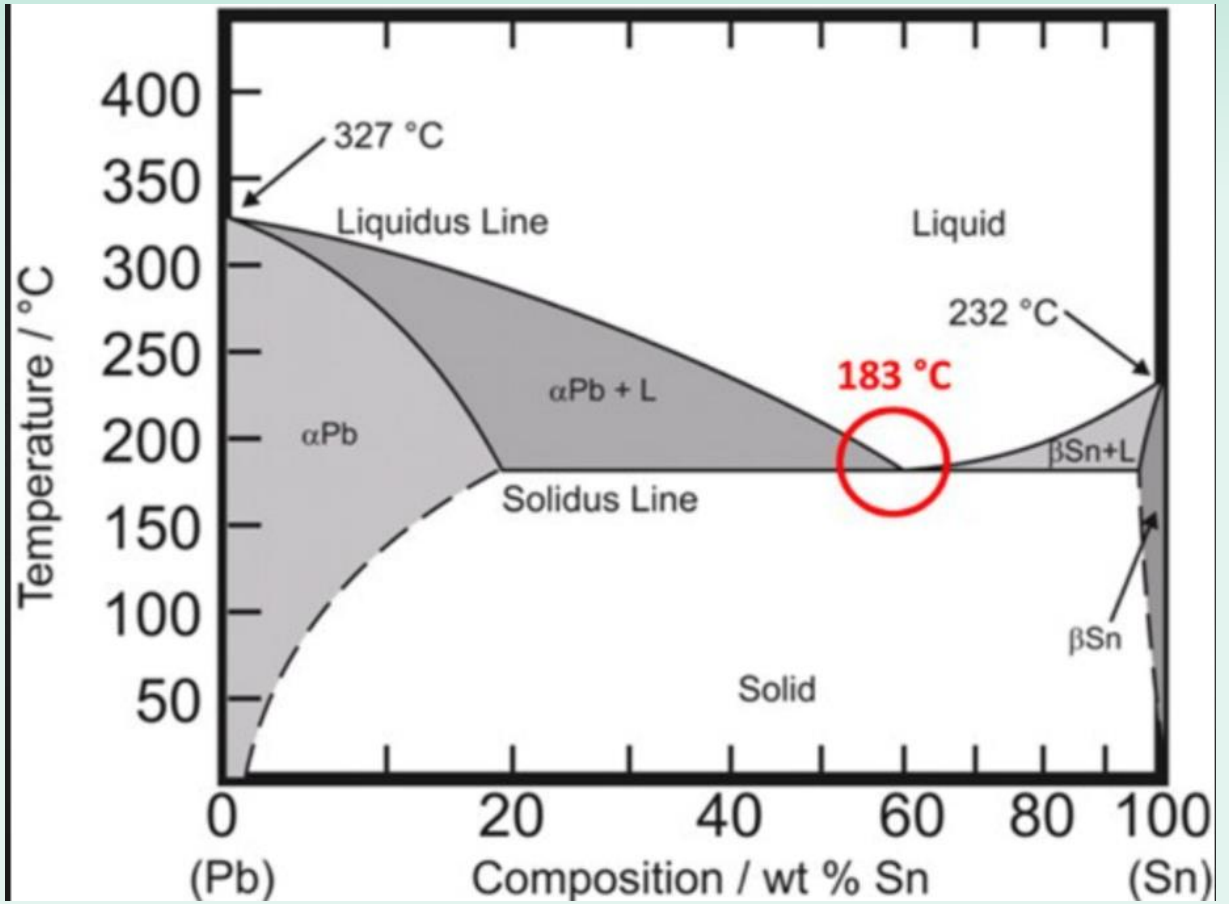
Type of solders:

Commonly used: Sn63Pb37

Alternative: Sn62Pb36 Ag2

High temperature solder: Tin/silver alloy Sn96Ag4

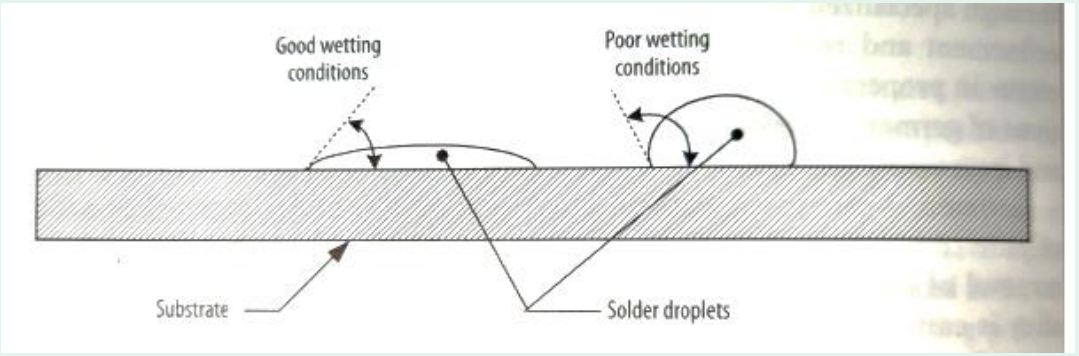
Low temperature solder: Indium/Lead: In/Pb



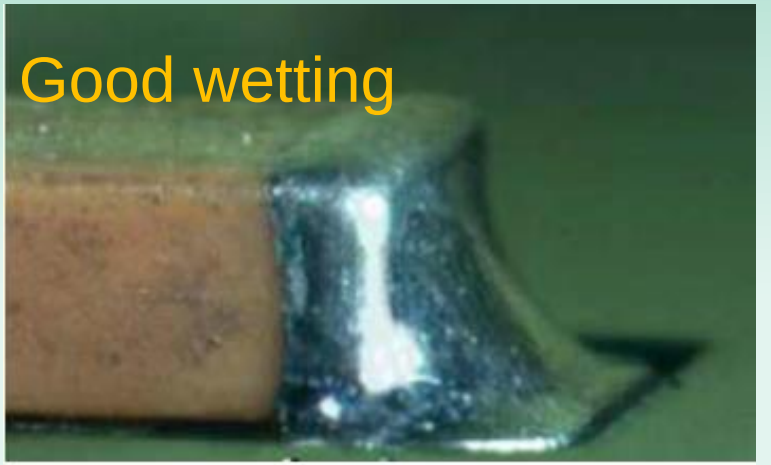
Basics of Electronic Assemblies

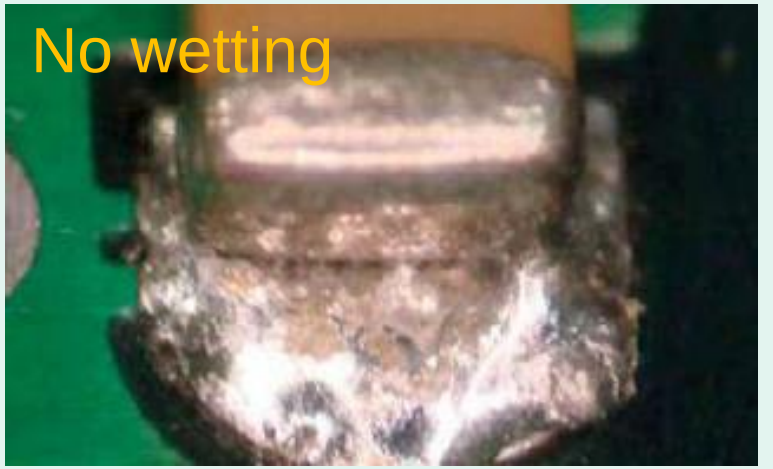
Wetting

In soldering, wetting is the phenomena describing the spreading of the molten solder and the formation of a bond with the surface on which the solder is applied.



Source: Ewans A guide to Lead-Free solders- Springer





Basics of Electronic Assemblies

Fluxes

The function of the flux in soldering is the breakdown and removal of oxides and impurities from the surfaces to be joined promoting the wetting of the surfaces by the solder.

Flux cover the molten alloy during soldering preventing the oxidation of the joint.

ECSS-Q-ST-70-61_1510153

Table 6-2: Fluxes

	IPC J-STD-004B-AM1 (2011) designation	Equivalent designation from ISO 9454-1:2016	Nature	Max composition* (Weight %)
Pretinning				
Normal wetting	ROL0	1111	Rosin	< 0,05 % halide
	ROL1	1122	Rosin	< 0,5 % halide
Difficult wetting	ROM1	1123	Rosin	0,5 % - 2 % halides
Difficult wetting	ROH1	1124	Rosin	≥ 2,0 % halides
Soldering				
Preferred	ROL0	1111	Rosin	< 0,05 % halide
Requiring cleanliness testing	ROL1	1122	Rosin	< 0,5 % halide

* Maximum values of halide contents are based on IPC, which have higher limits than ISO

NOTE: Cleaning is mandatory in any case

Basics of soldering

Assembly technologies:

Automatic assembly (Collective soldering)

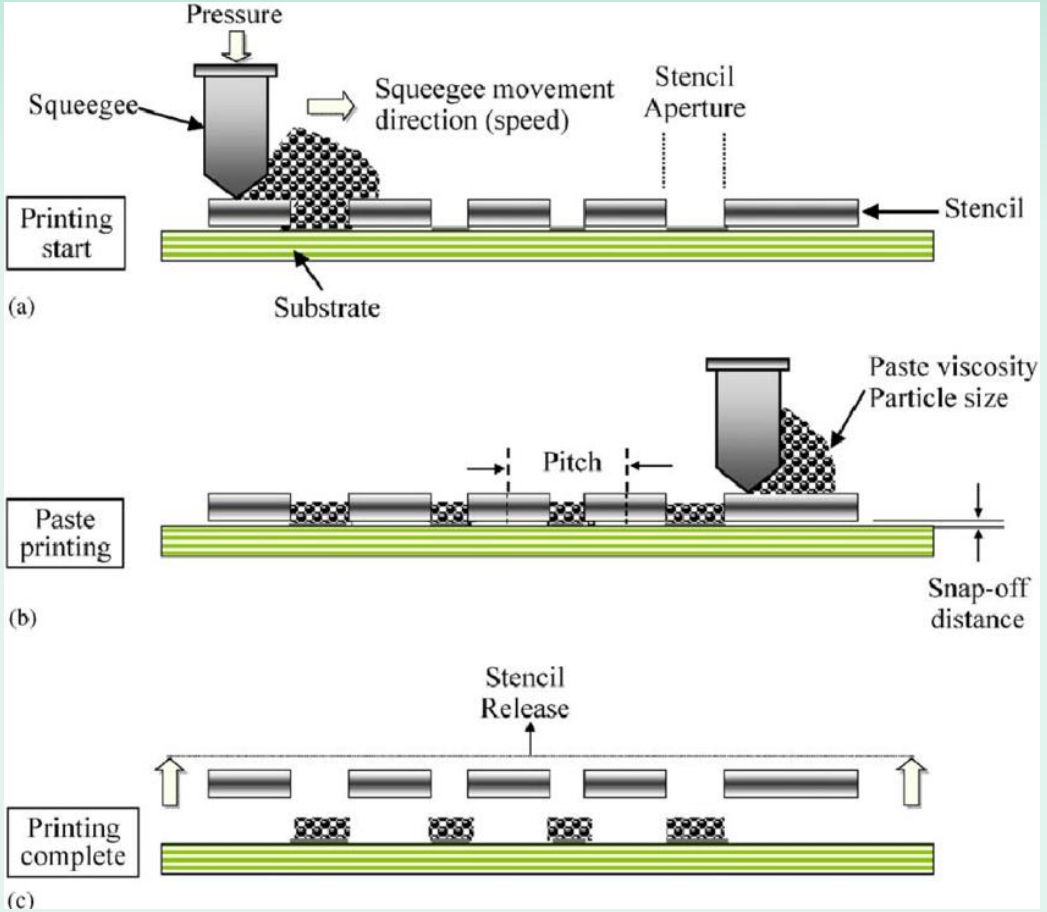
- **Vapour Phase (usually 215C)**
- **Convection reflow (min 12 degree above solder melting point)**
- **Wave soldering (235 ° C to 275 ° C)**

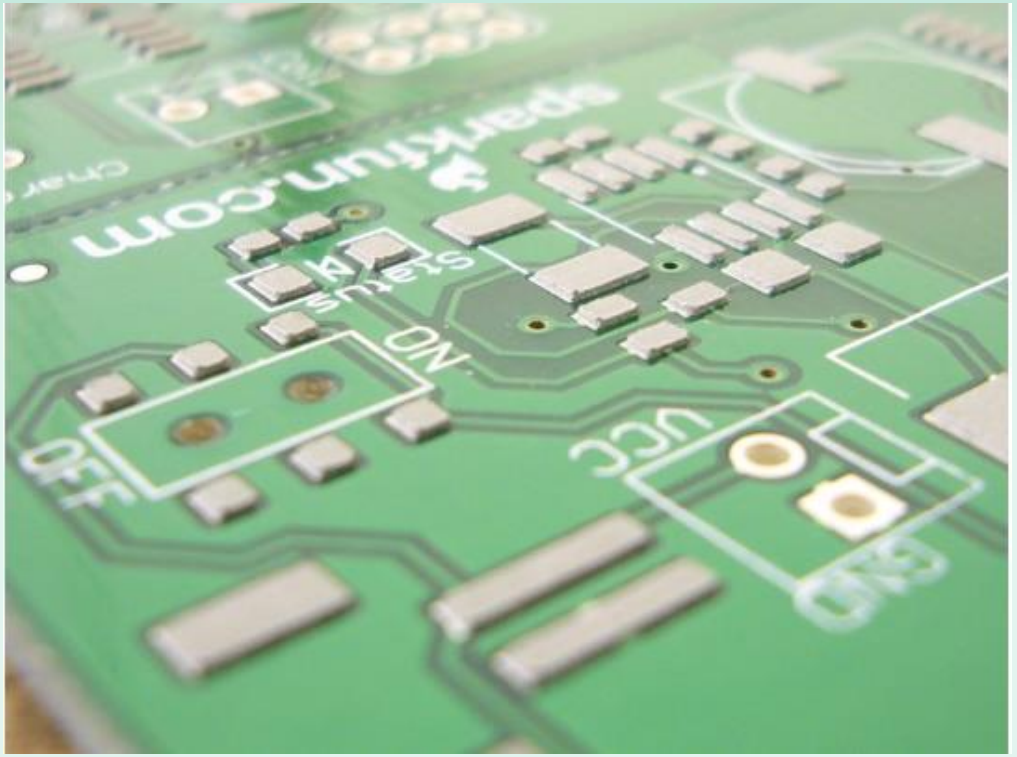
Local assembly

- **Assembly by hand (max 350 C)**
- **Selective wave soldering (max 300C)**
- **Local hot air (Repair station)**

Basics of soldering

Collective soldering (SMT): screen printing of the solder paste





Source https://saferfq.com/

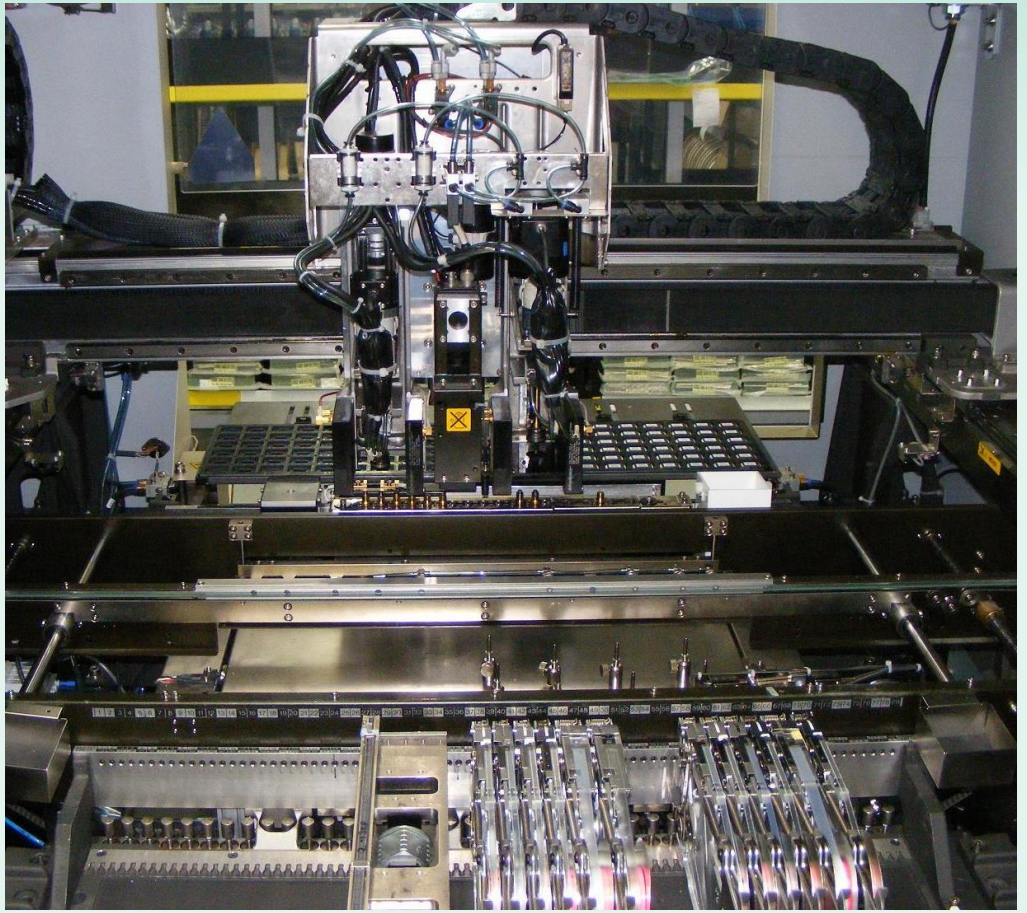
Source Pan, J., Tonkay, G.L., Storer, R.H., Sallade, R.M., Leandri, D.J., 1999. Critical variables of solder paste stencil printing for microBGA and fine pitch QFP. Proceedings of IEEE/CPMT International Electronics Manufacturing Technology Symposium, pp. 94–101

Basics of soldering

Collective soldering: components placement

Semiautomatic and automatic pick and place

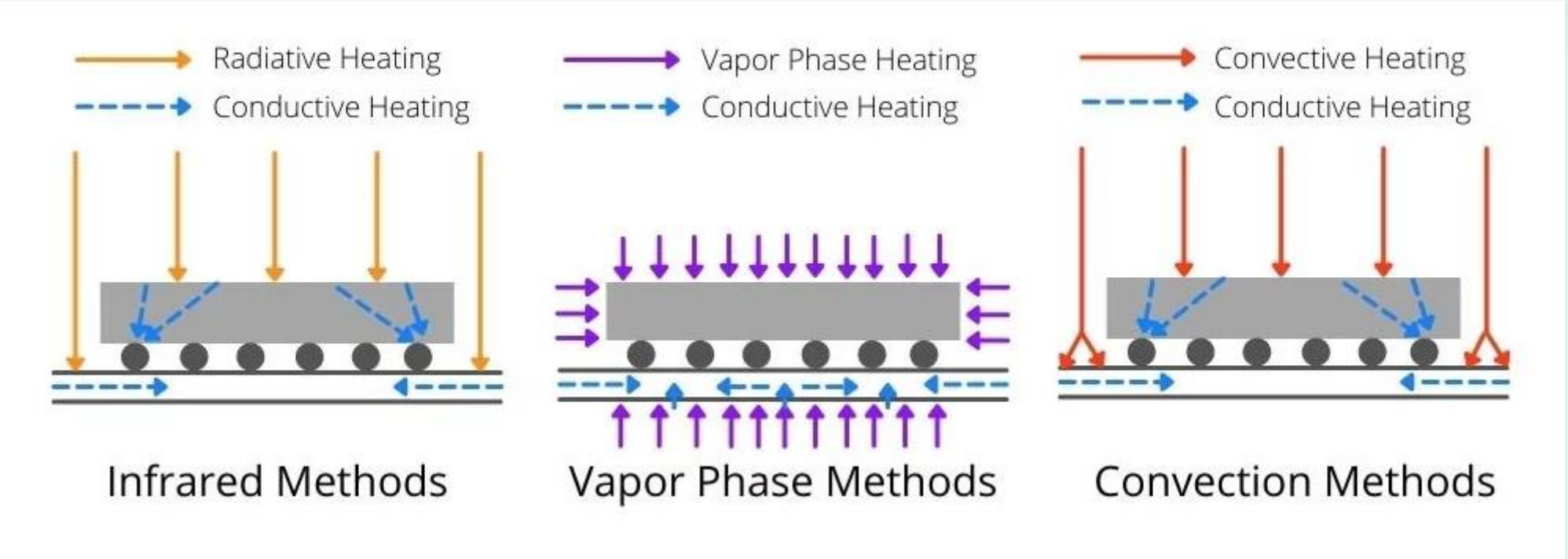
Source https://Fritsch.com/



Source https://wikipedia.com/

Basics of soldering

Collective soldering processes:



Source [Vapor Phase Reflow Soldering Process | Ninja Circuits]

Basics of soldering

Collective soldering processes:

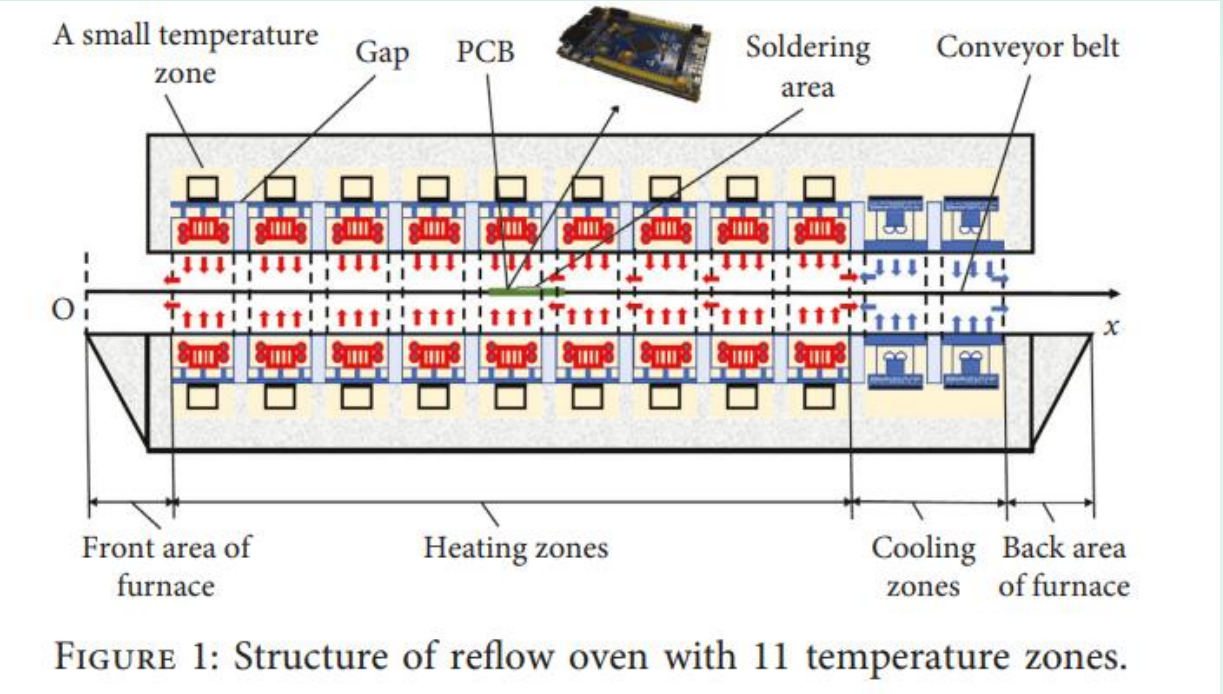


FIGURE 1: Structure of reflow oven with 11 temperature zones.

Source Hindawi Discrete Dynamics in Nature and Society
Volume 2021, Article ID 9955967, 19 pages
https://doi.org/10.1155/2021/9955967

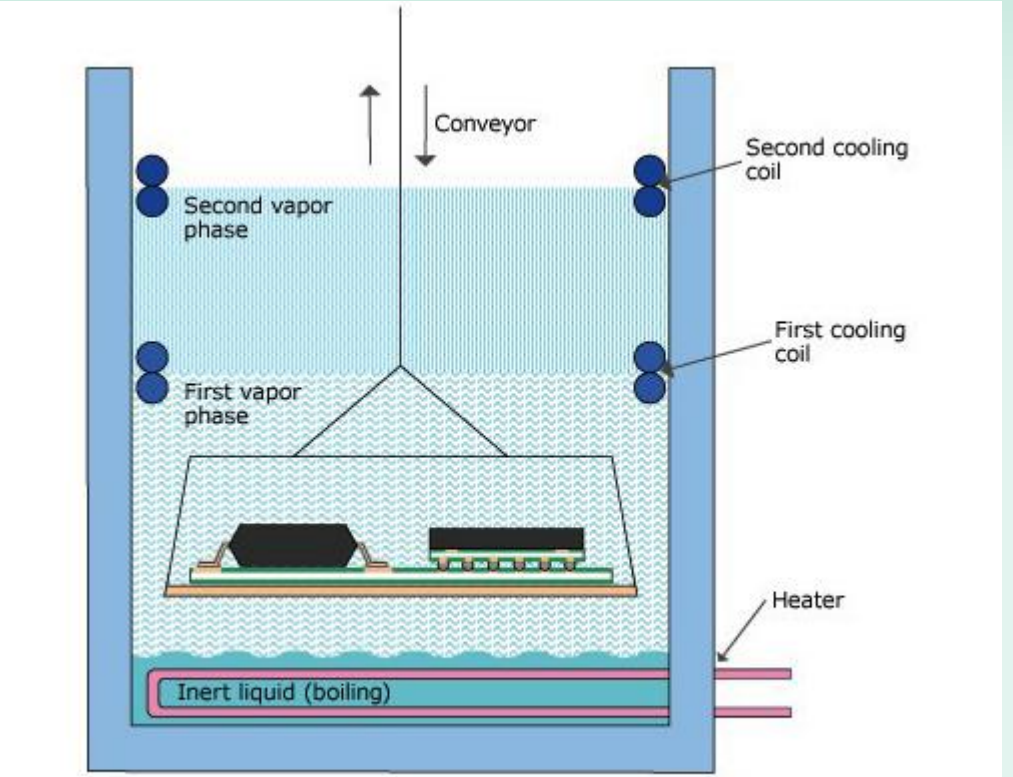
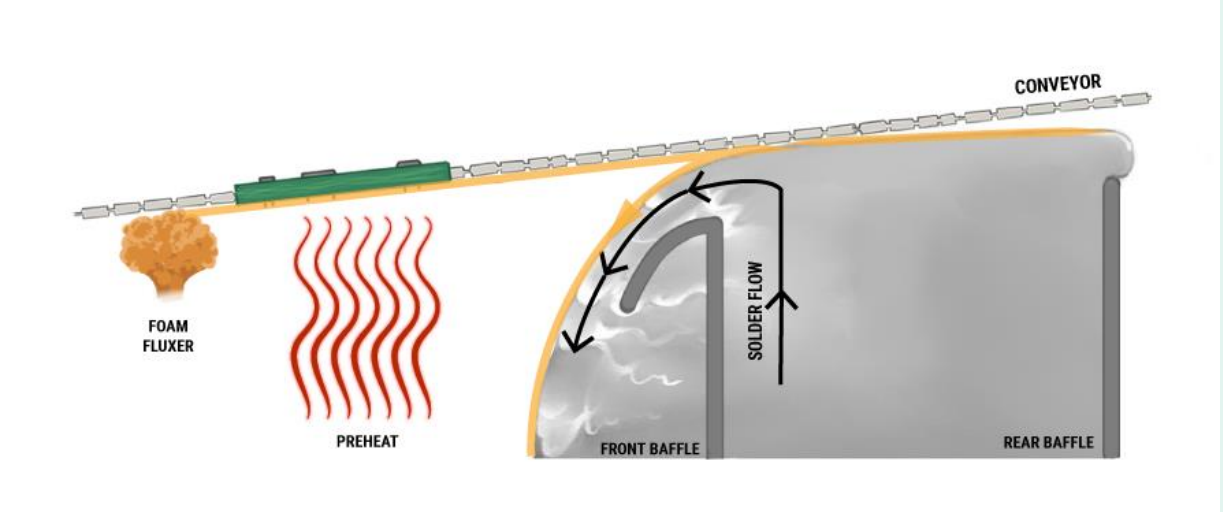


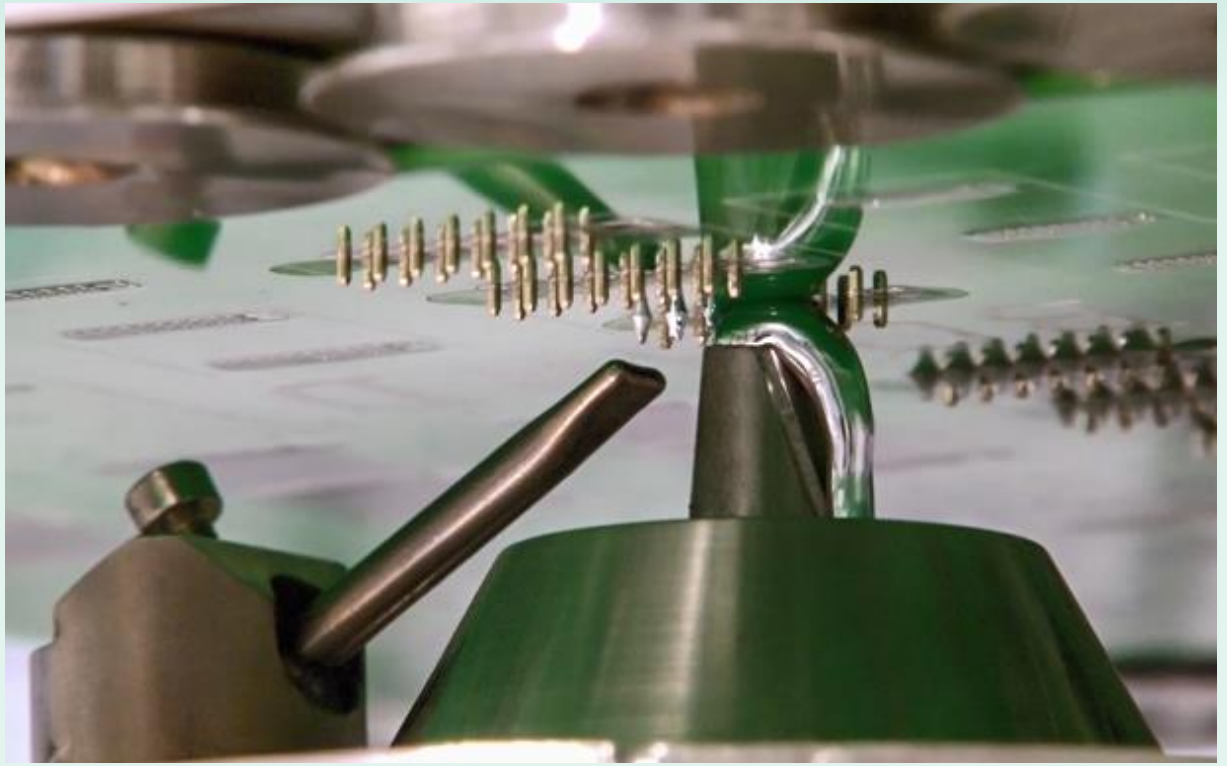
Figure 1: Vapor phase soldering method

Source [Vapor Phase Soldering :: Total Materia Article]

Basics of soldering

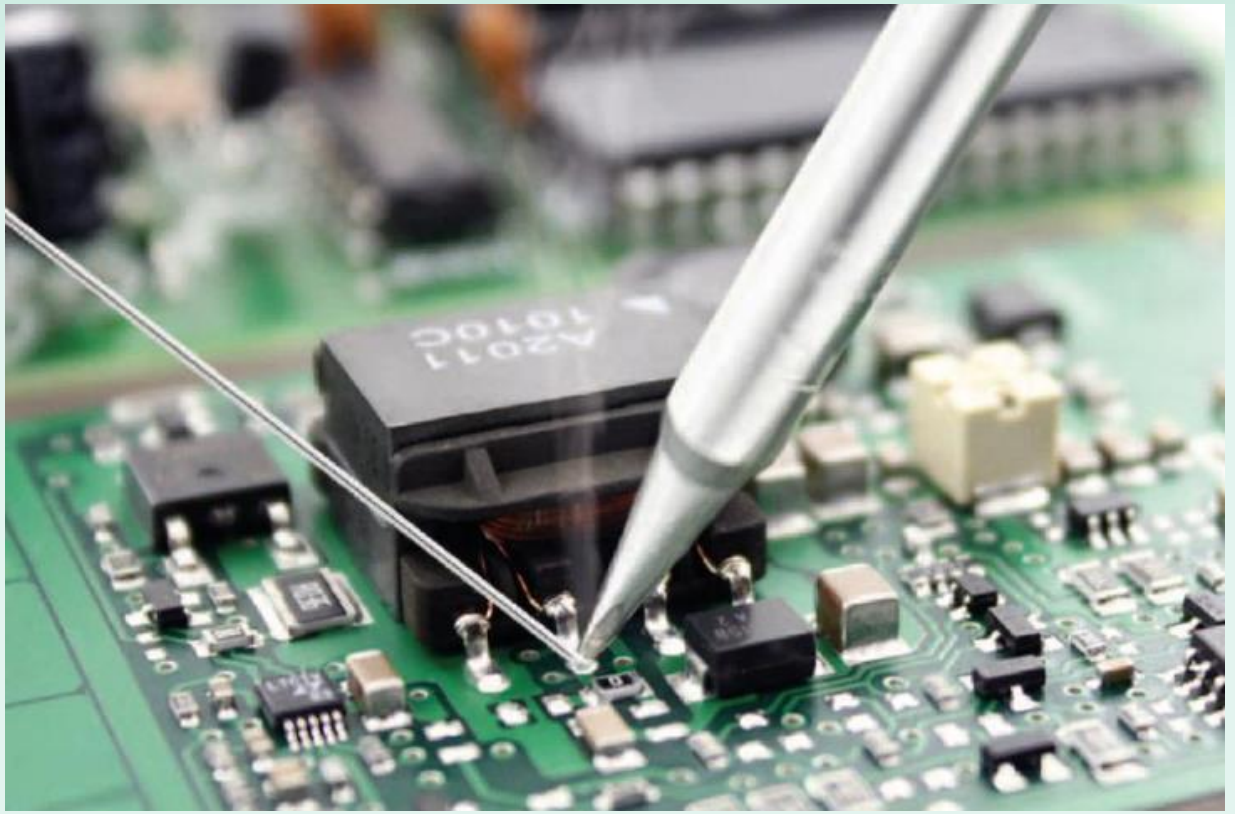
Collective soldering processes: Wave soldering





Source https://www.itweae.com/

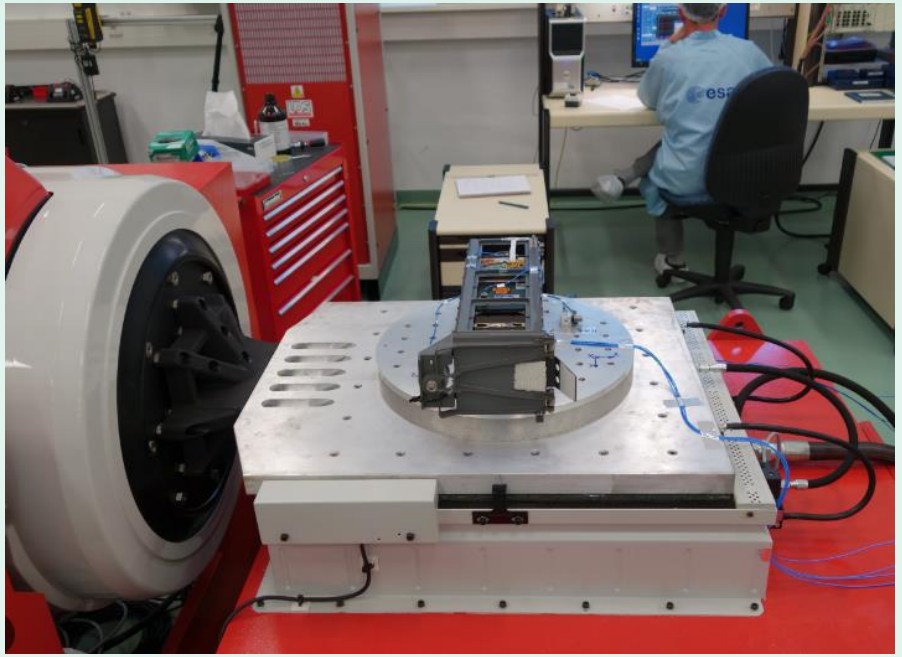
Basics of soldering

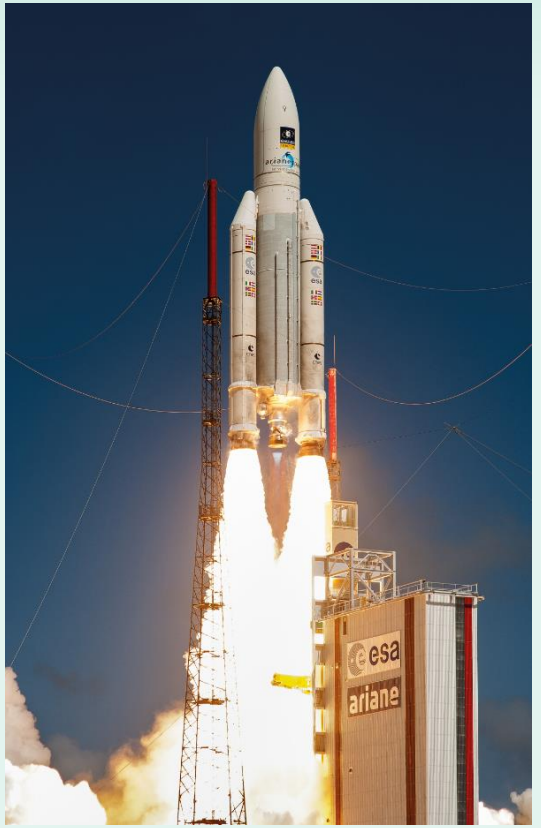


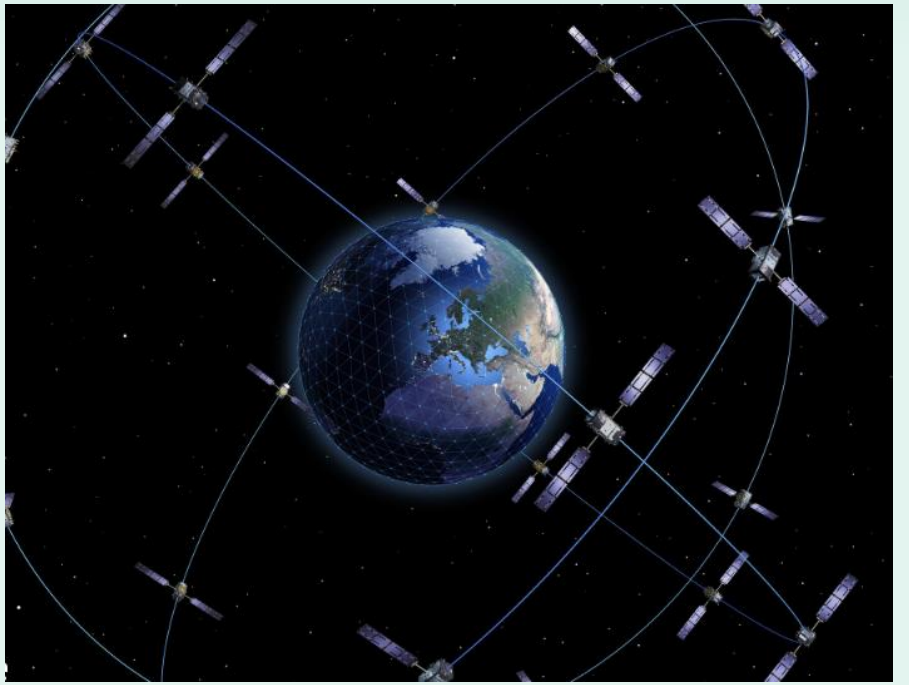
Source https://www.soselectronic.com/

Source https://www.kurtzersa.com/

Assembly reliability

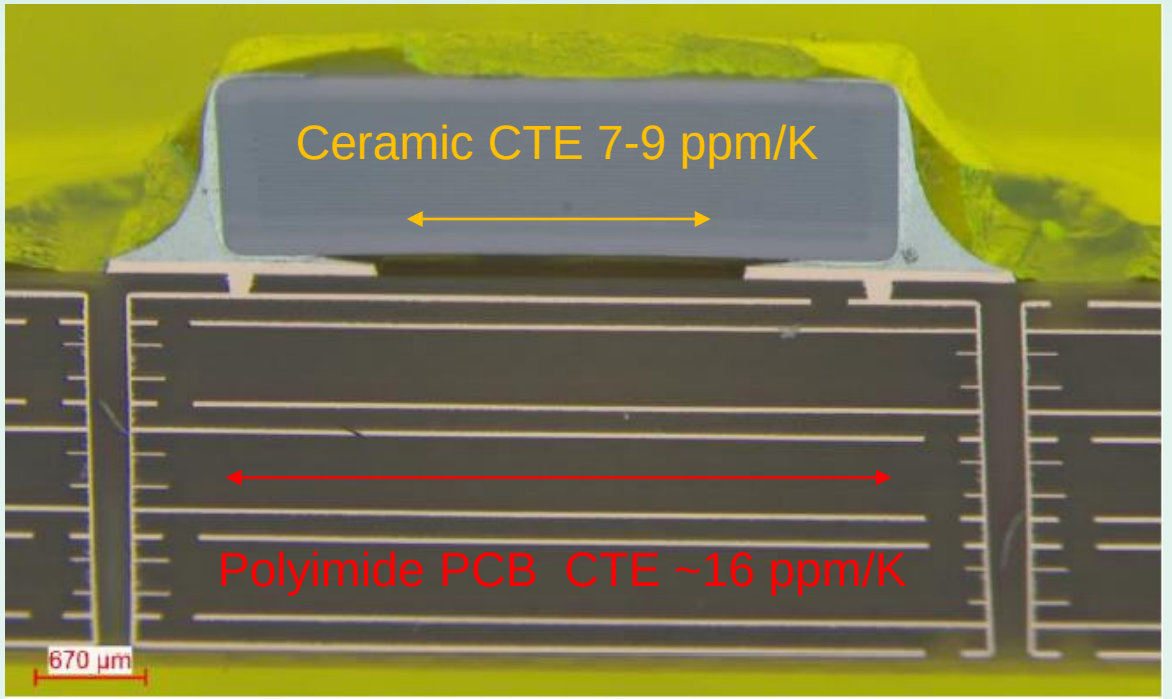




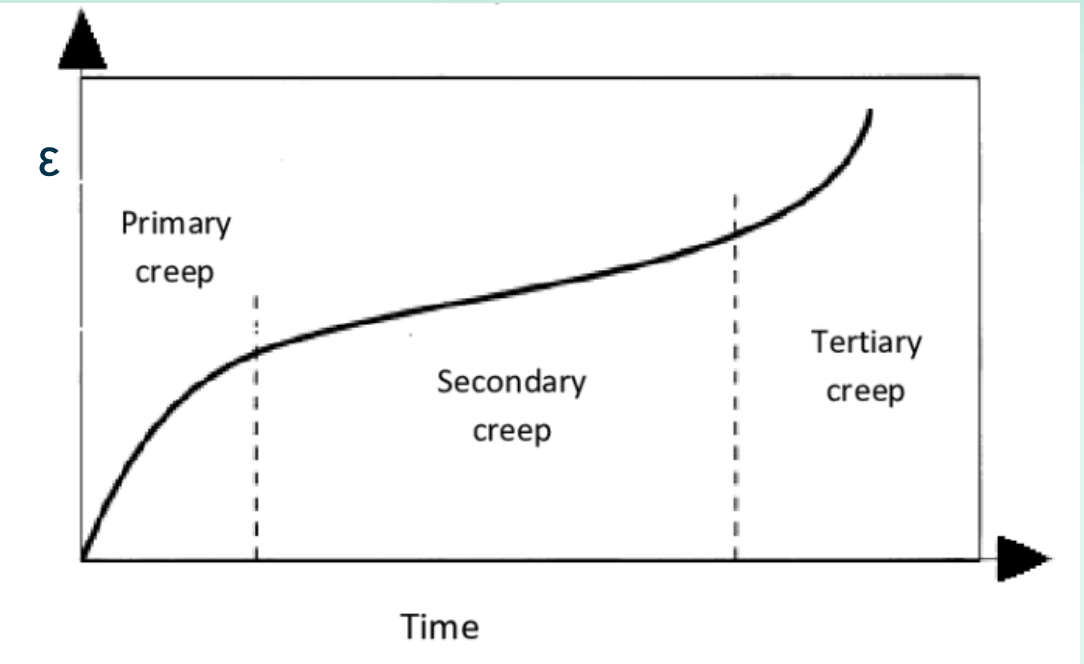


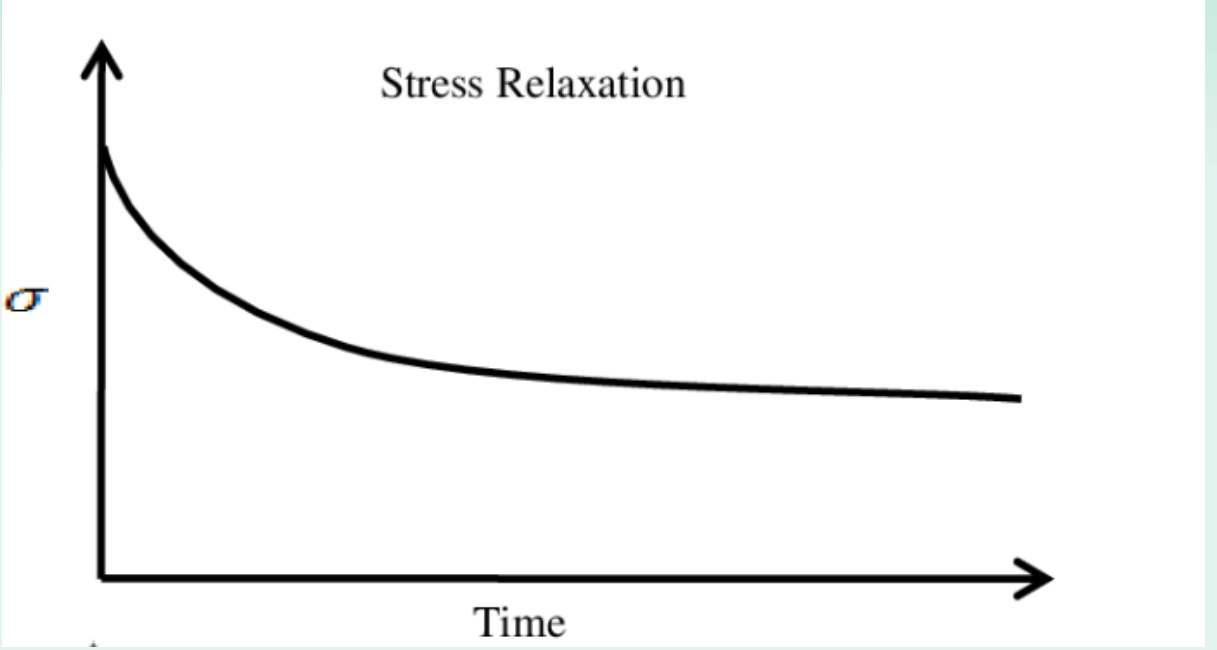
Assembly reliability

Thermal stresses : Differences in the CTE between the package of the devices and the PCB resulting in stresses in the solder joints when the assembly experiences variation of temperature.



Assembly reliability





Assembly reliability

Creep and stress relaxation

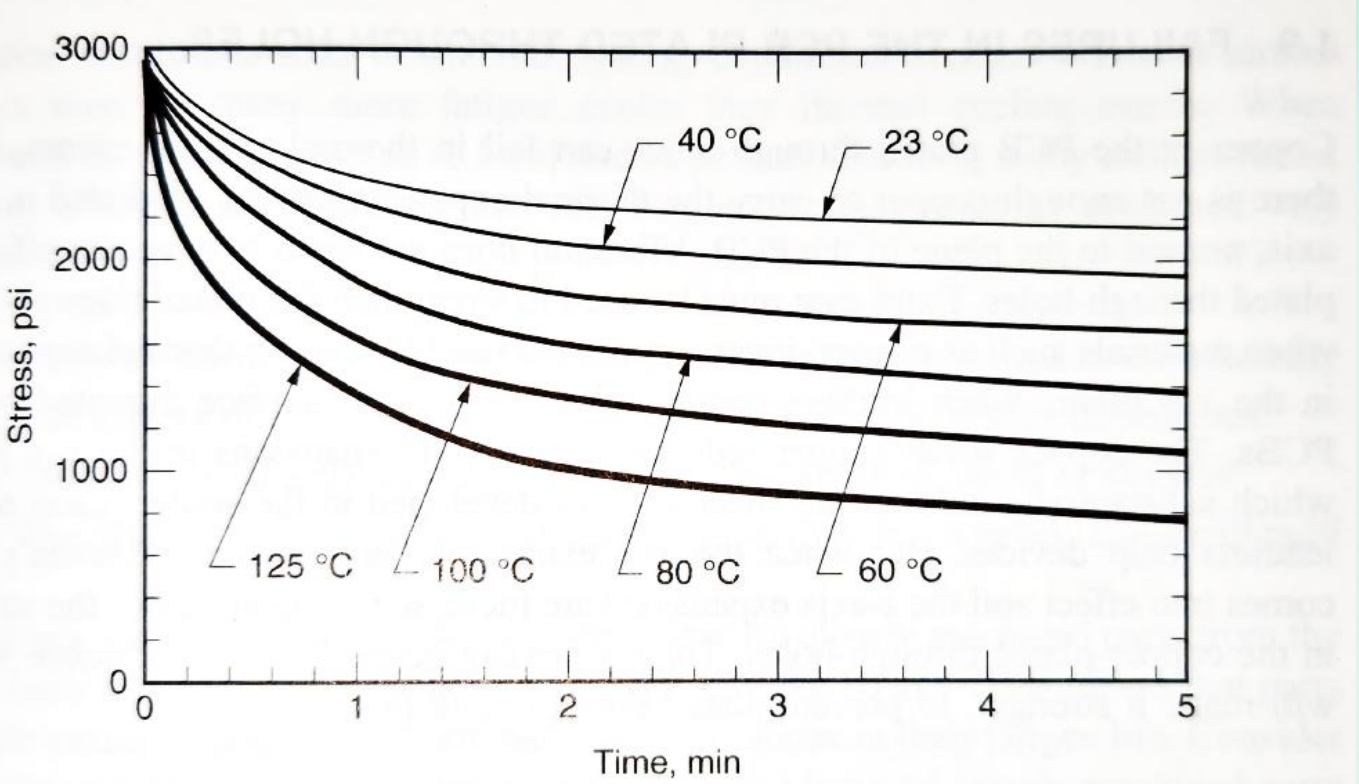


FIGURE 1.6 Rate of solder creep and stress relaxing depend on the temperature and stress level.

Source D.S.Steinberg Preventing Thermal Cycling and vibration failures in Electronic equipment Wiley Interscience

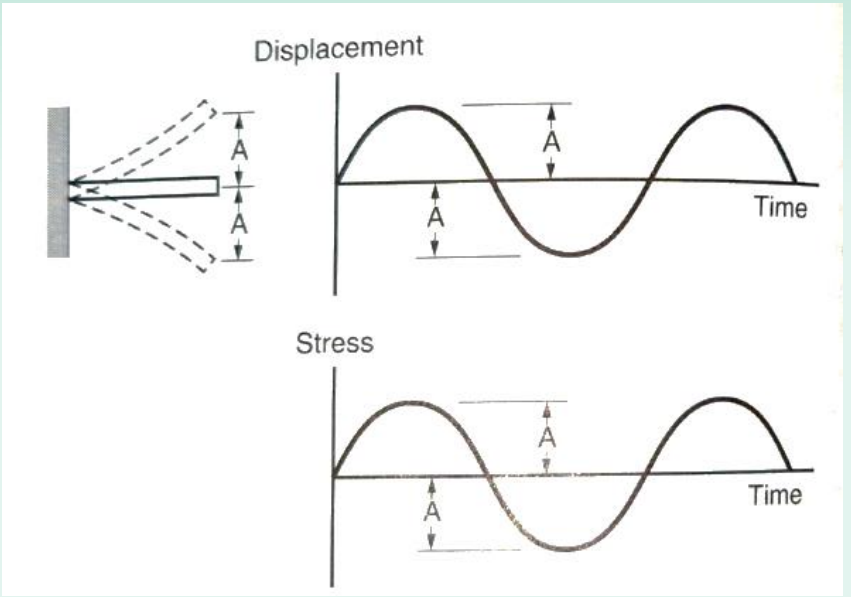
Creep/stress relaxation are in general taking place in materials at temperature >0.5 Tm.

for Eutectic Sn Pb:

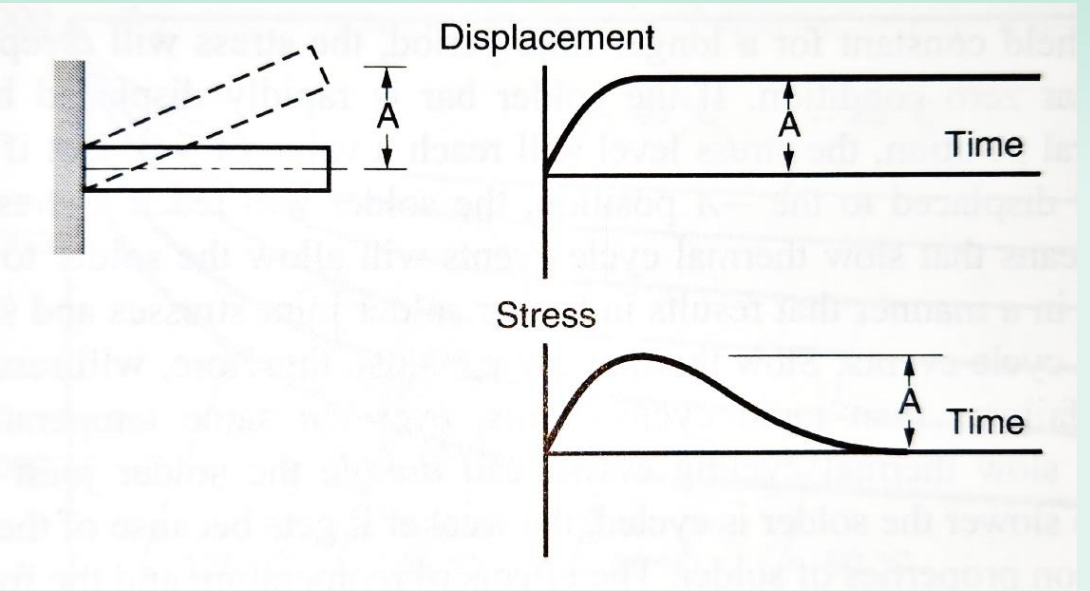
0.5Tm is 228K (-45 ° C)

Assembly reliability

Creep and stress relaxation



Linear systems: no creep

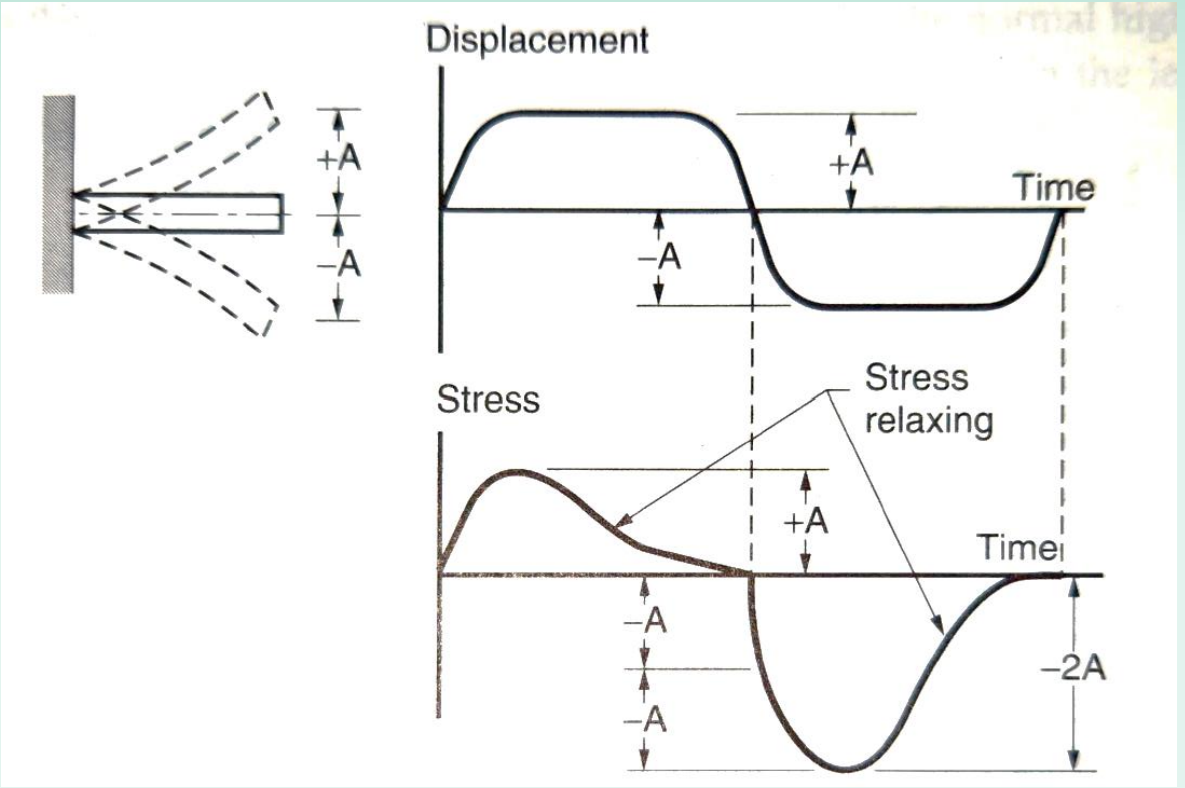


Solder can creep at elevated temperatures and relax stresses when displacement is held constant

Source D.S.Steinberg Preventing Thermal Cycling and vibration failures in Electronic equipment Wiley Interscience

Assembly reliability

Creep and stress relaxation



Solder can creep elevated temperatures and relax stresses can induce an increase in the solder stresses during slow thermal cycling where displacement is held constant for long period of time

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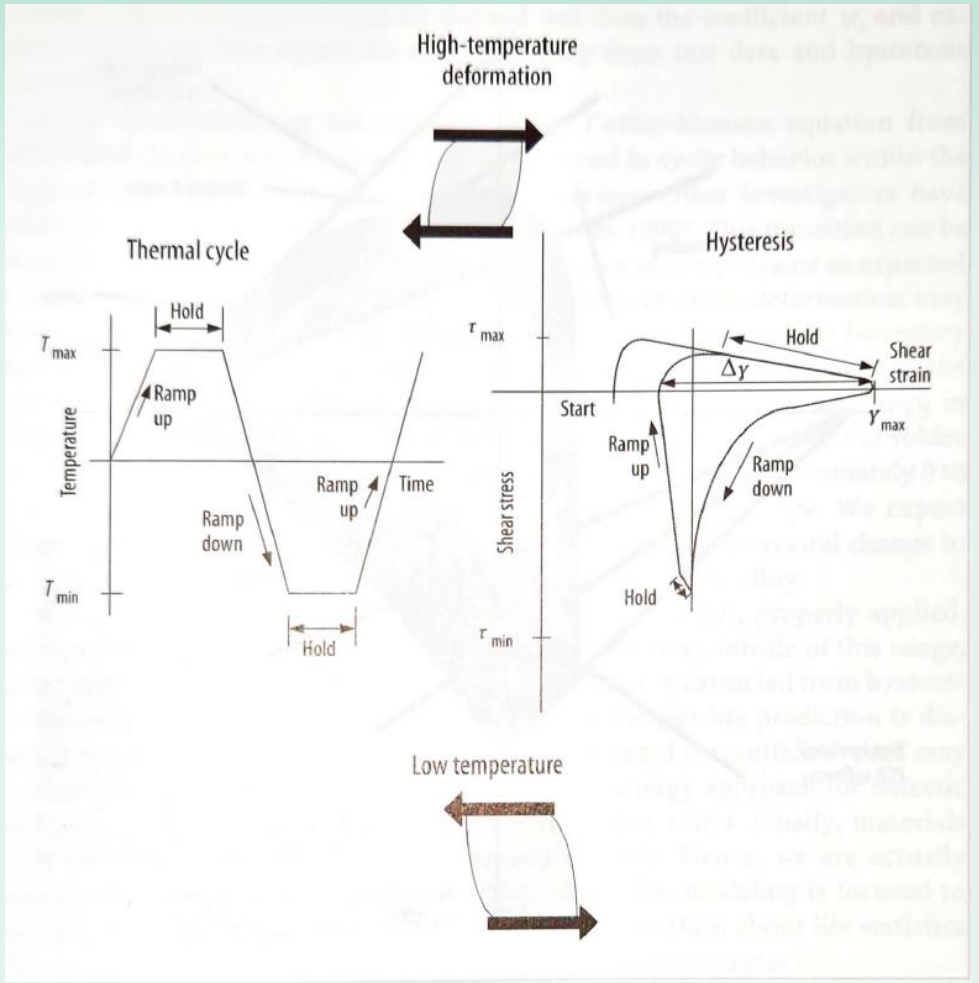
Assembly reliability

Creep and stress relaxation



Source J.W Evans A guide to Lead Free solders Springer

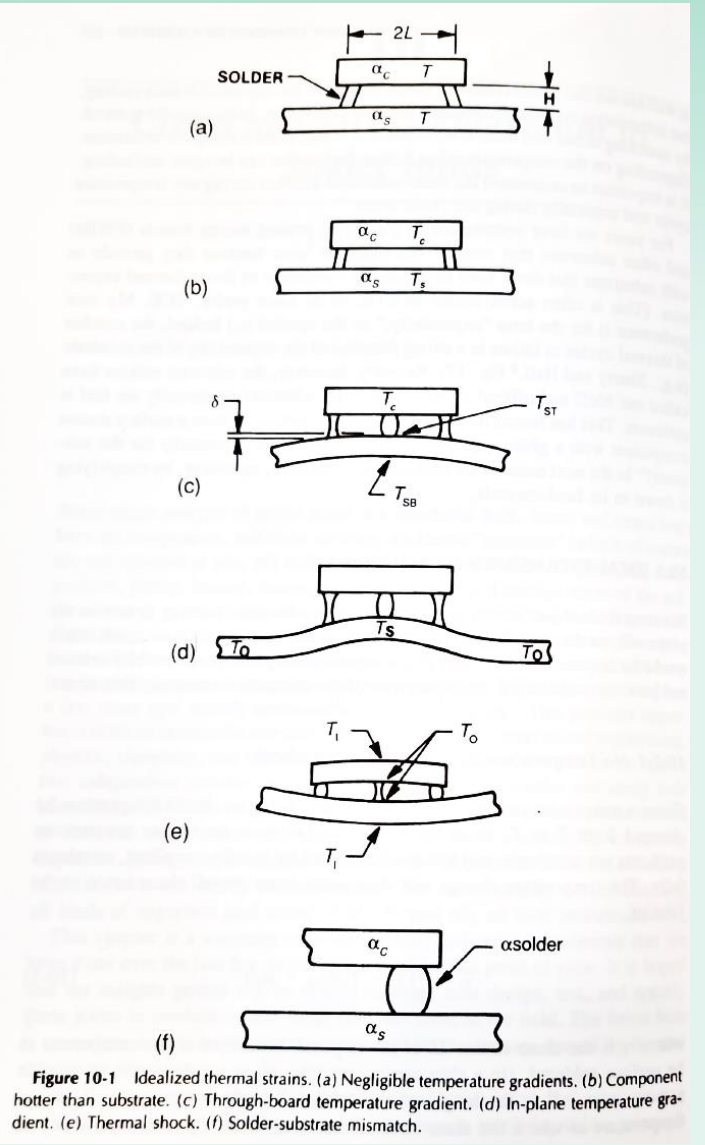
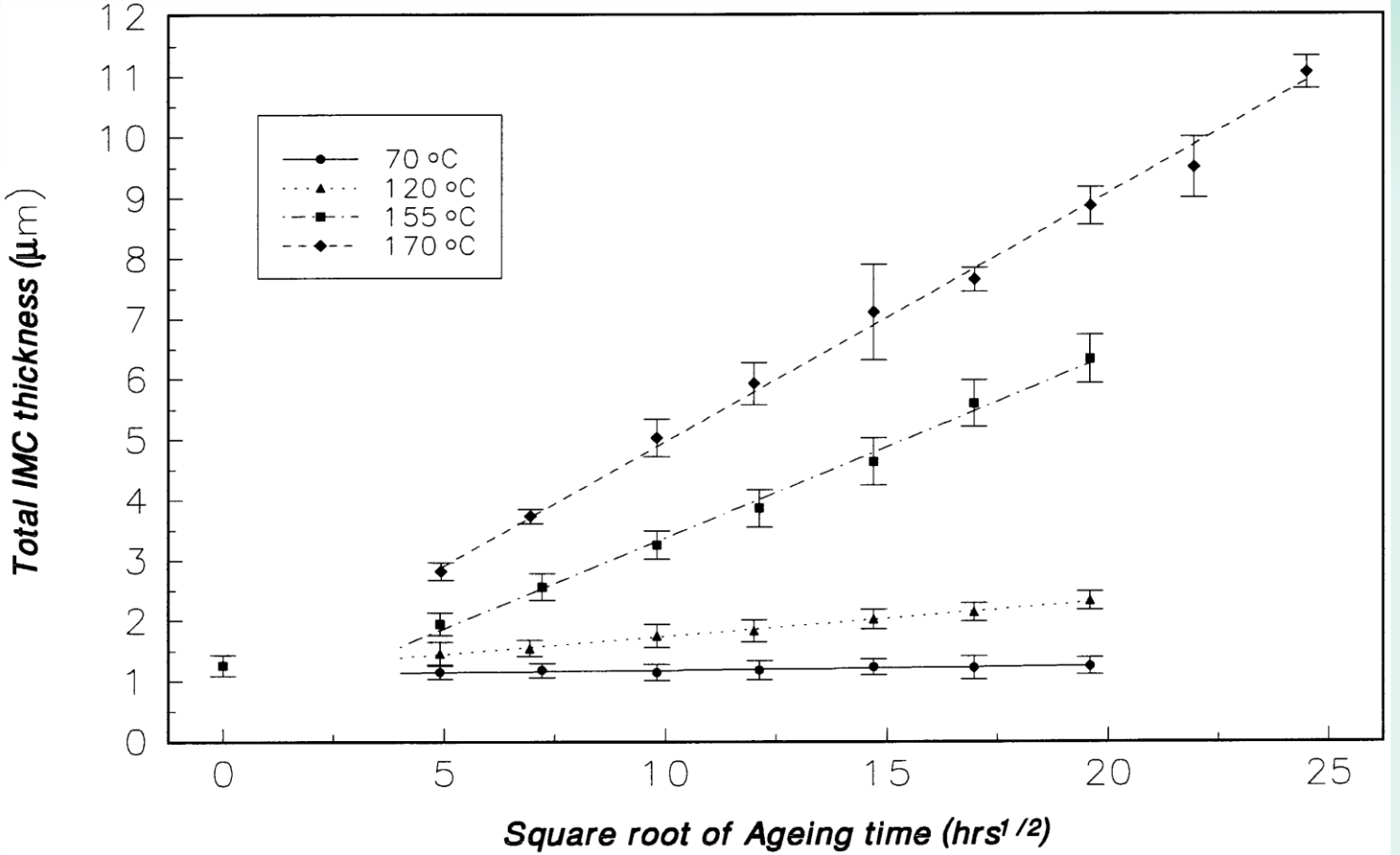


Figure 10-1 Idealized thermal strains. (*a*) Negligible temperature gradients. (*b*) Component hotter than substrate. (*c*) Through-board temperature gradient. (*d*) In-plane temperature gradient. (*e*) Thermal shock. (*f*) Solder-substrate mismatch.

Source J.h. Lau Solder joints reliability. Van Nostrand Reinold

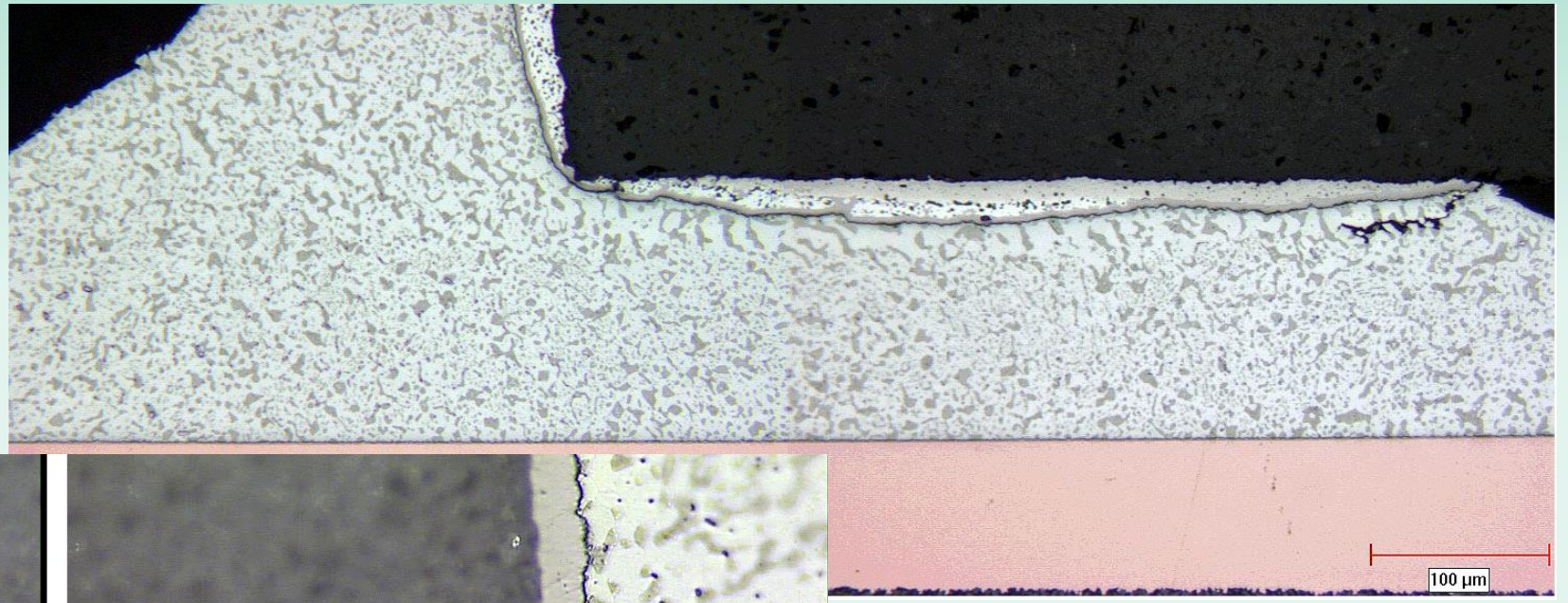
Assembly reliability

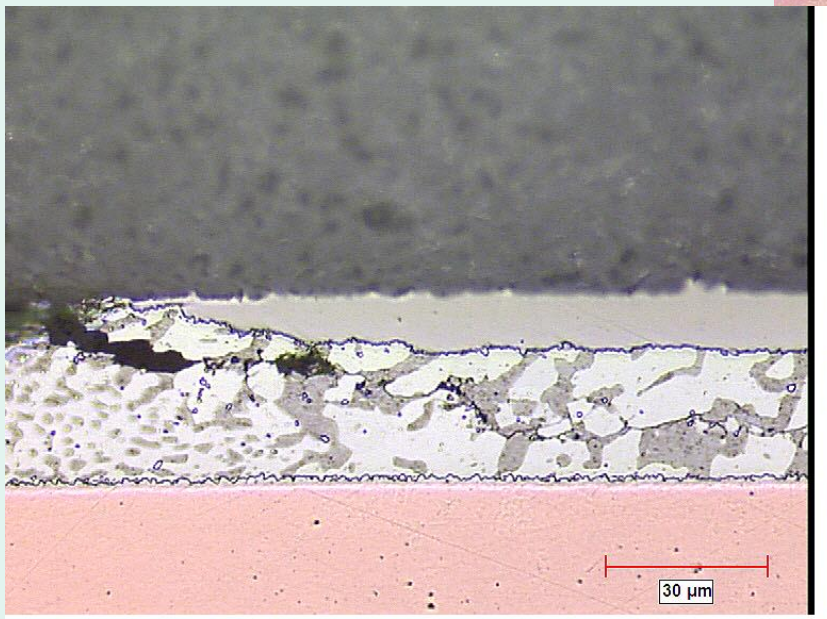
Intermetallic growth

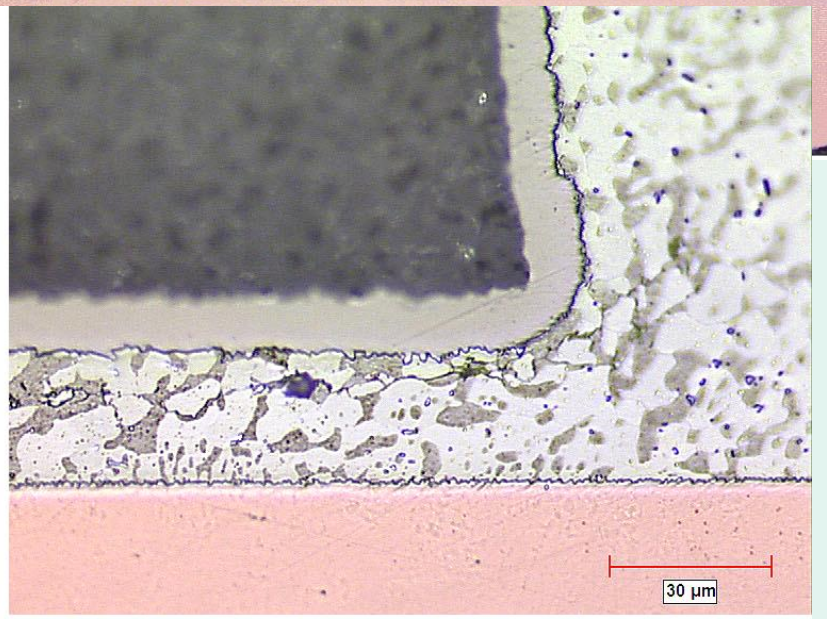


Assembly reliability

Impact on microstructure







Assembly reliability

Vibration and stresses in the connections:

Stresses are due to bending of the PCB as results of the applied load and/or movement of not supported device as results of the applied accelerations

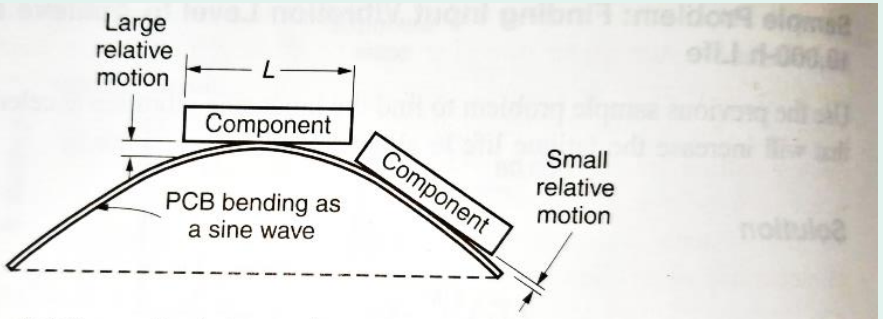


FIGURE 8.11 Relative motion between a long component and a supported PCB, bending in vibration, is reduced when the component is mounted near the PCB edge so the lead wire stresses are also reduced.

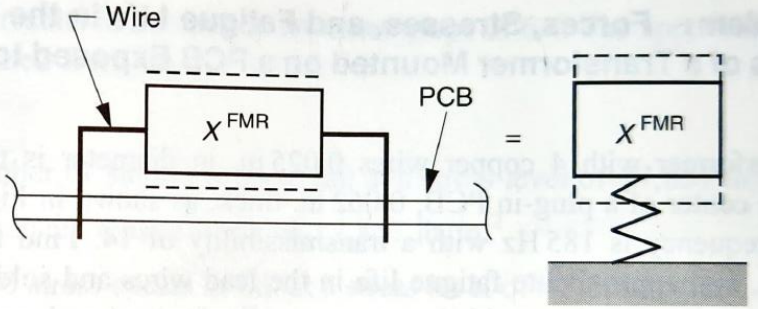


FIGURE 12.4 Large and heavy components with a few thin wires will often bounce up and down in severe vibration and shock conditions when the components are not properly secured.

Source D.S.Steinberg Preventing Thermal Cycling and vibration failures in Electronic equipment Wiley Interscience

Assembly reliability

Thermal induced stress due to:

- **Curing, Bake-out on ground**
- **Thermal testing on ground (Acceptance testing)**
- **Functional testing on ground (AIT, Power dissipation)**
- **Temperature variation on orbit**
- **On-Off cycles**
- **Safe modes**

Mechanical loading: vibrations and shock:

Acceptance testing

Ground testing at system level

Launch

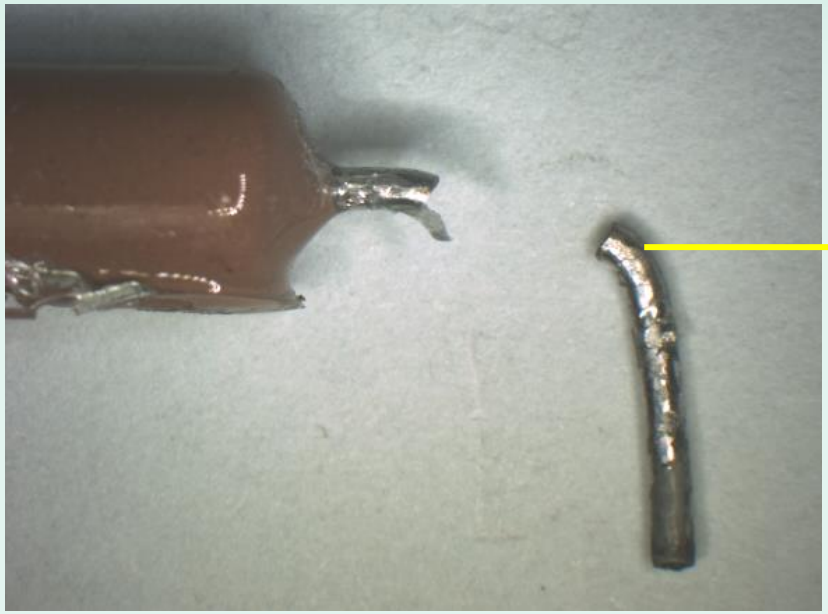
Separation events

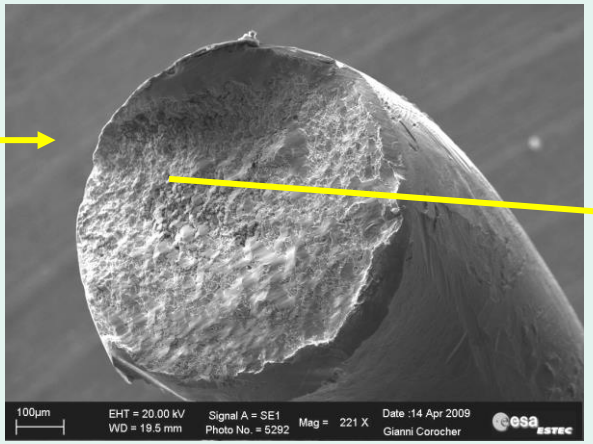
Re-entry

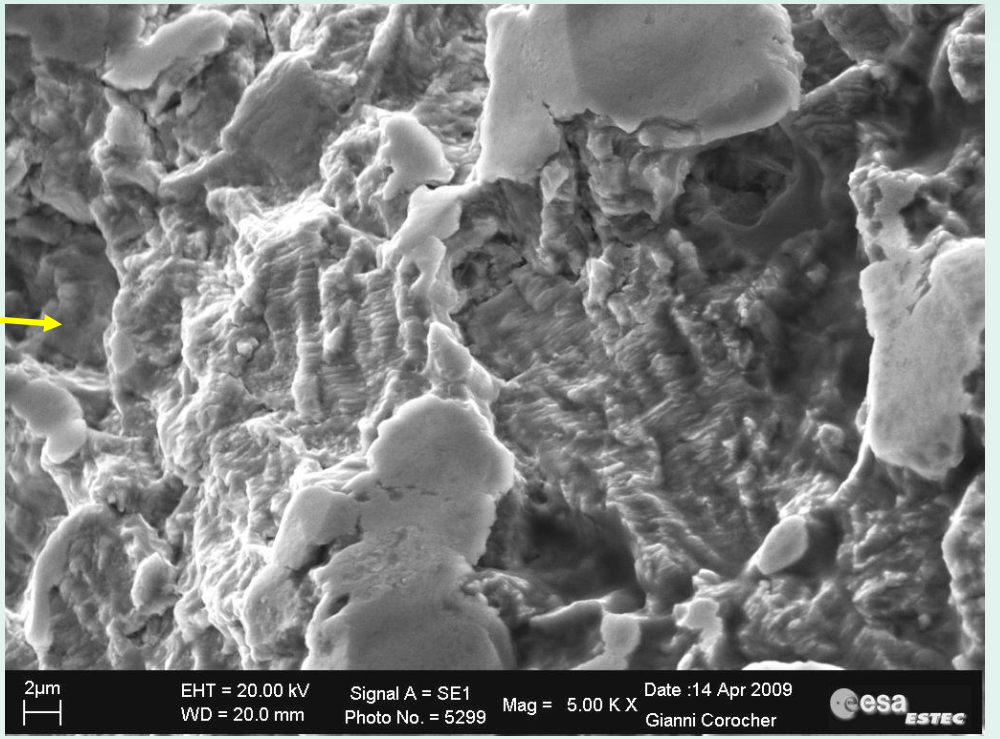
Assembly reliability

Failure of the lead of a THT mounted component after QM testing:

Failure is due to the vibration loading



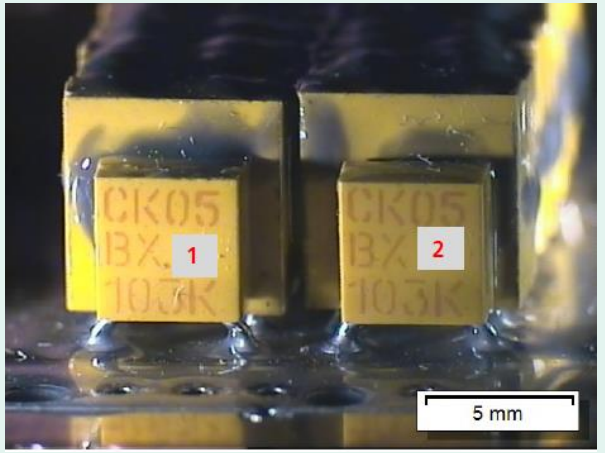


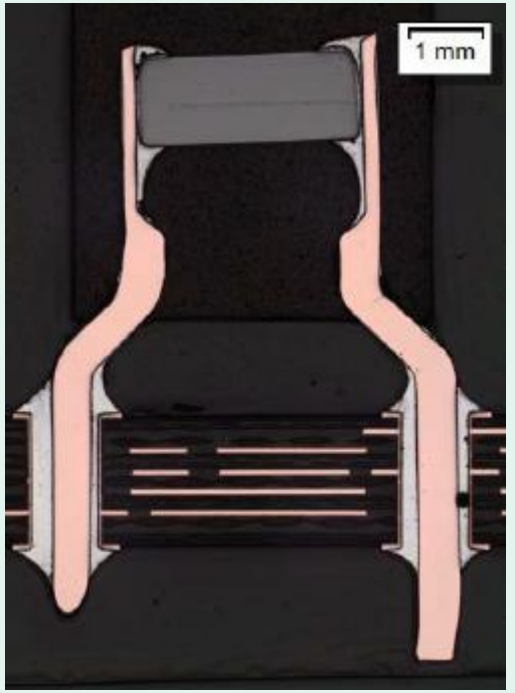


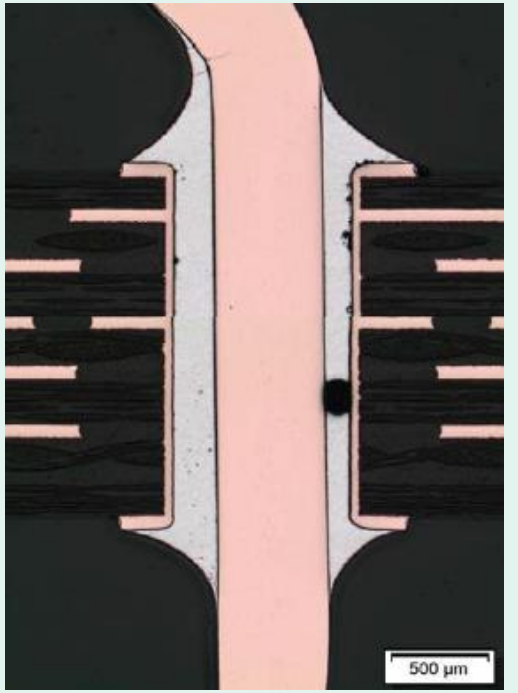
Assembly reliability

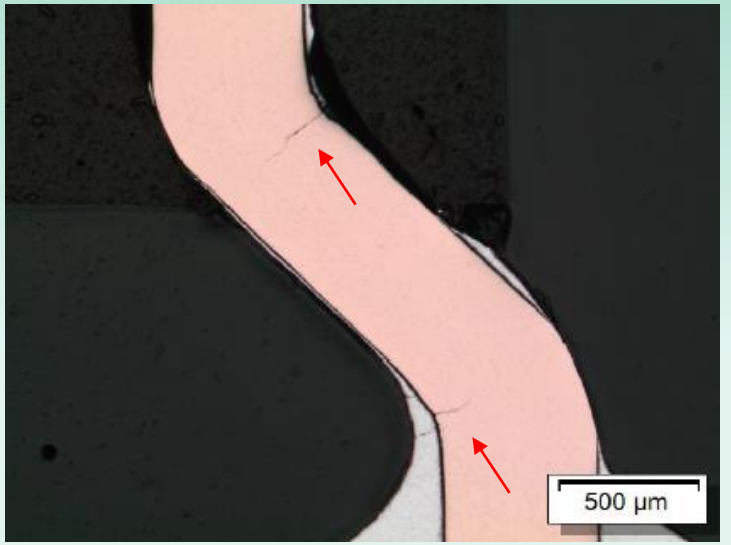
Damage to leads and solder joints as result of vibration and thermal cycling (THT mounted component)

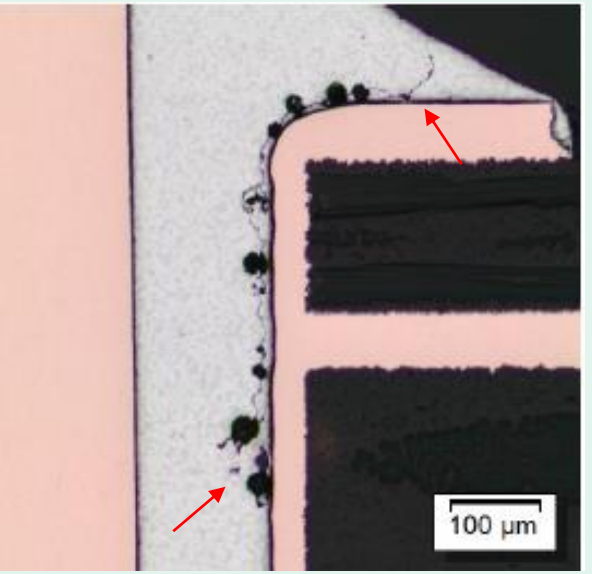
Failure is due to incorrect staking :





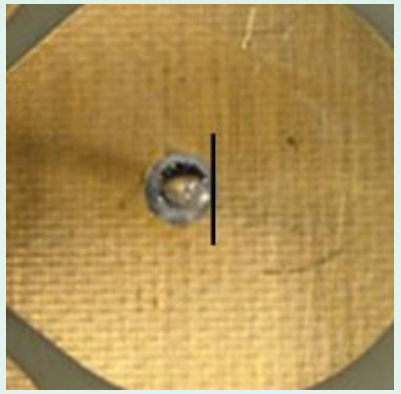


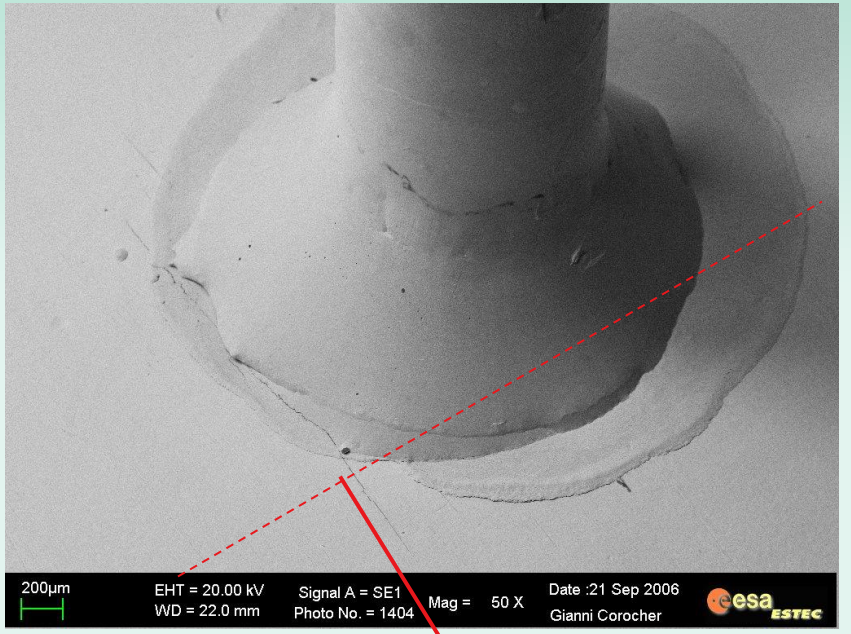


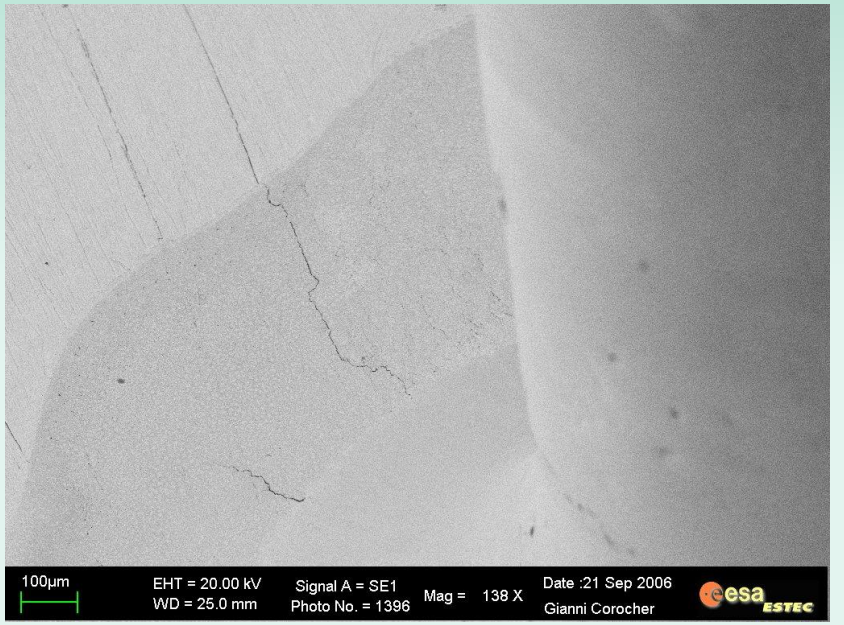


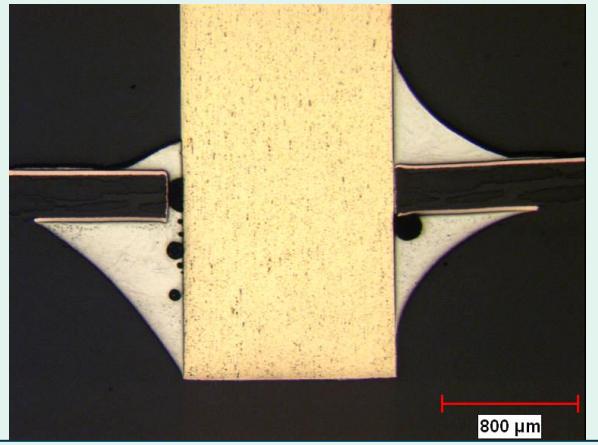
Assembly reliability

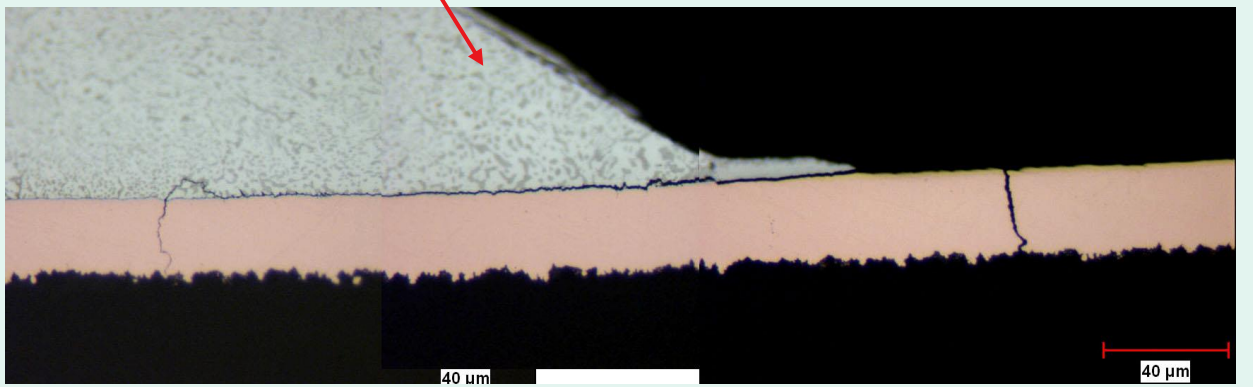
Failure of a thin PCB in vibration





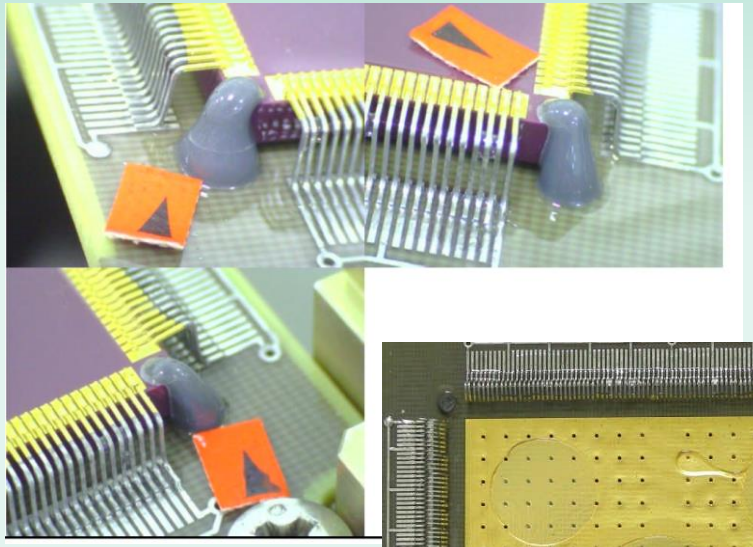


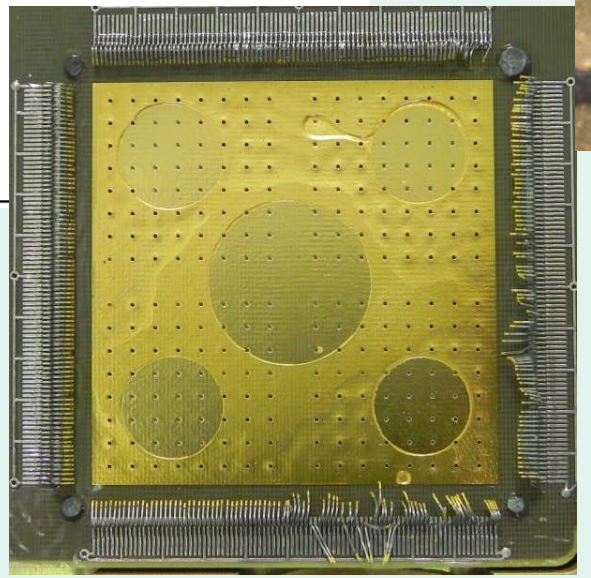


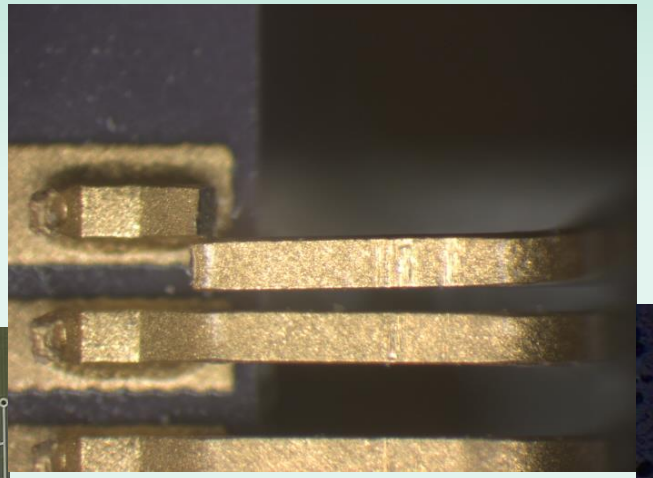


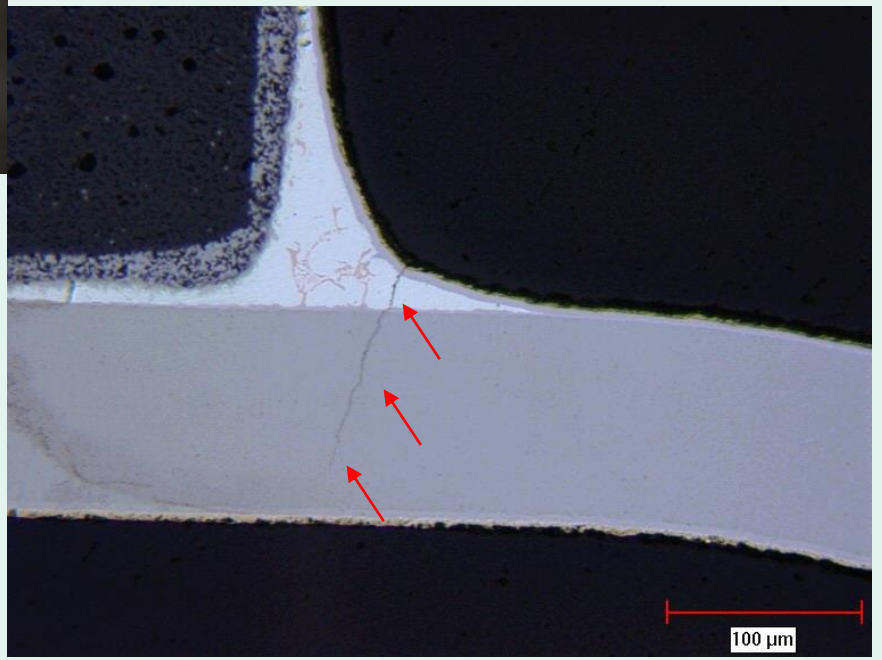
Assembly reliability

Failures of the leads of surface mounted FP during vibration testing



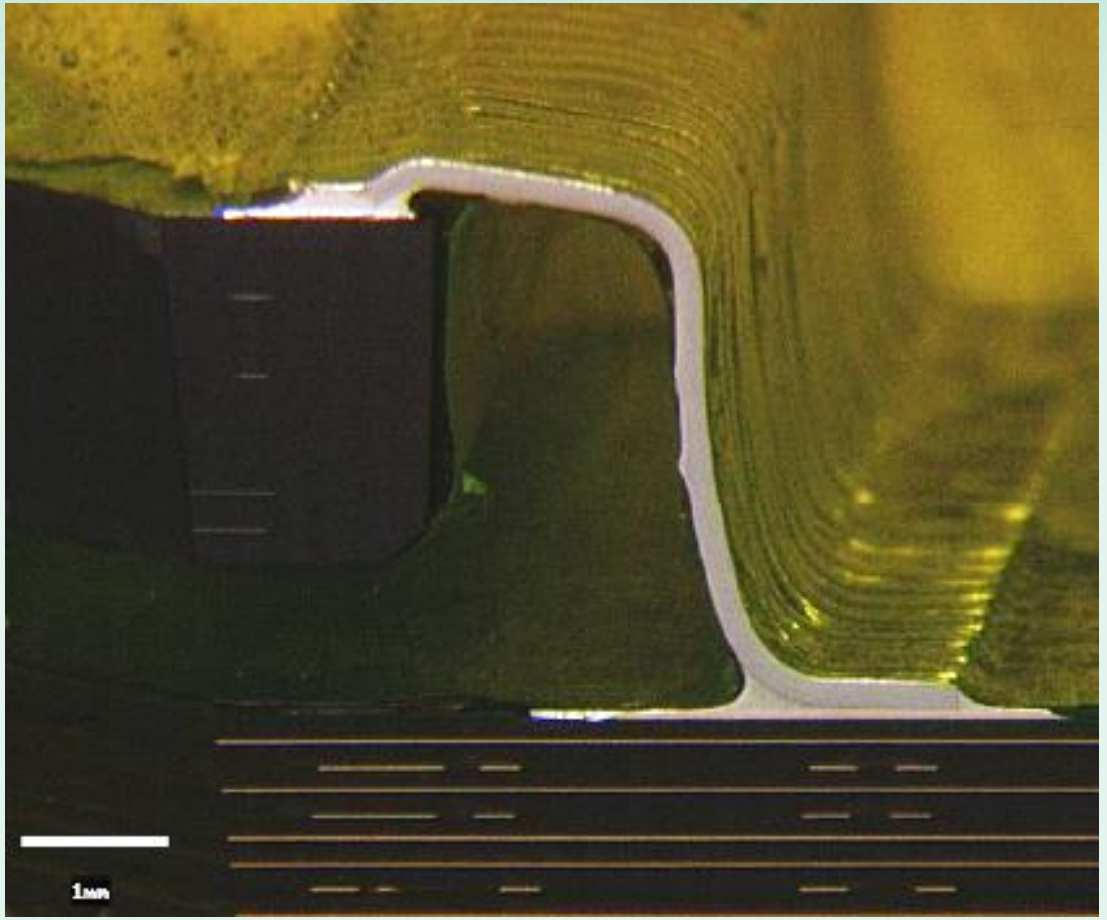


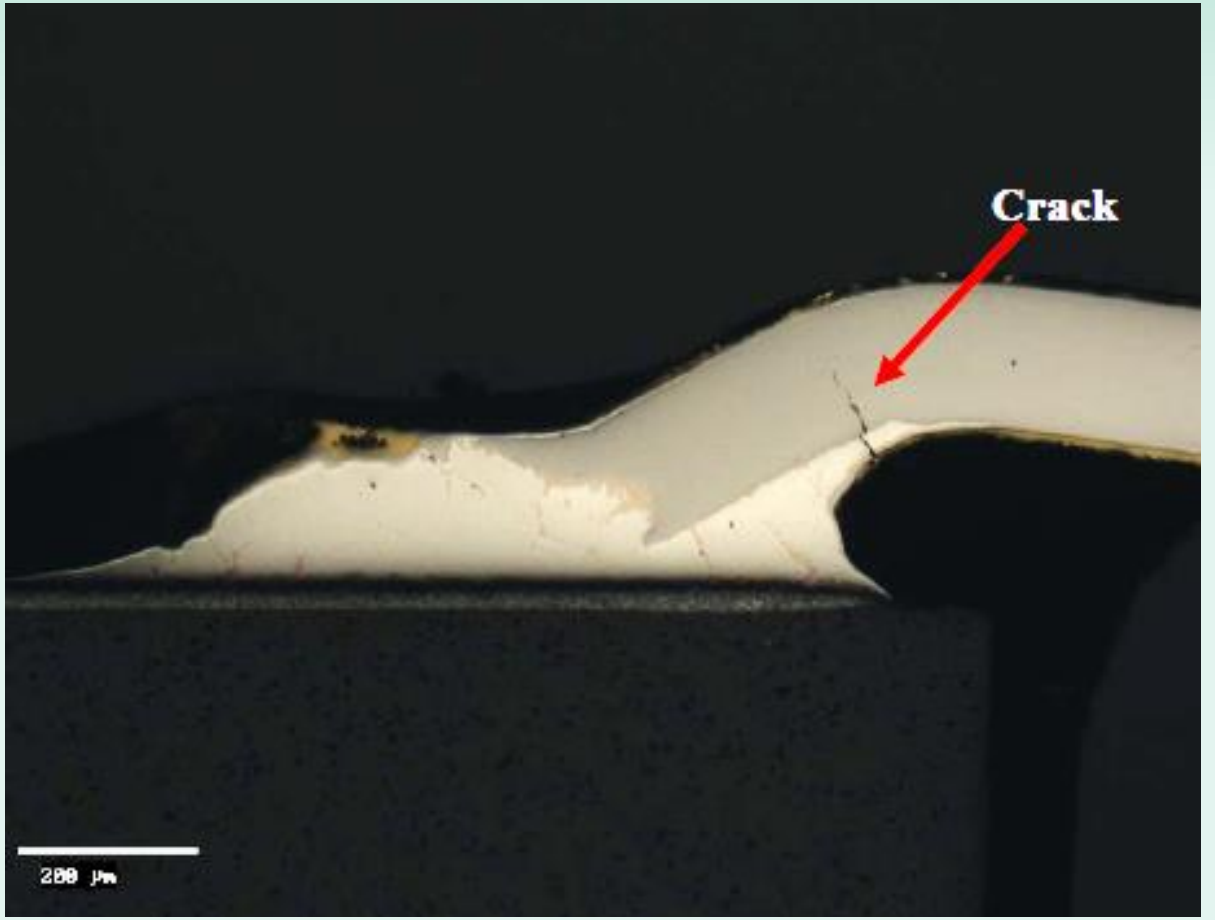




Assembly reliability

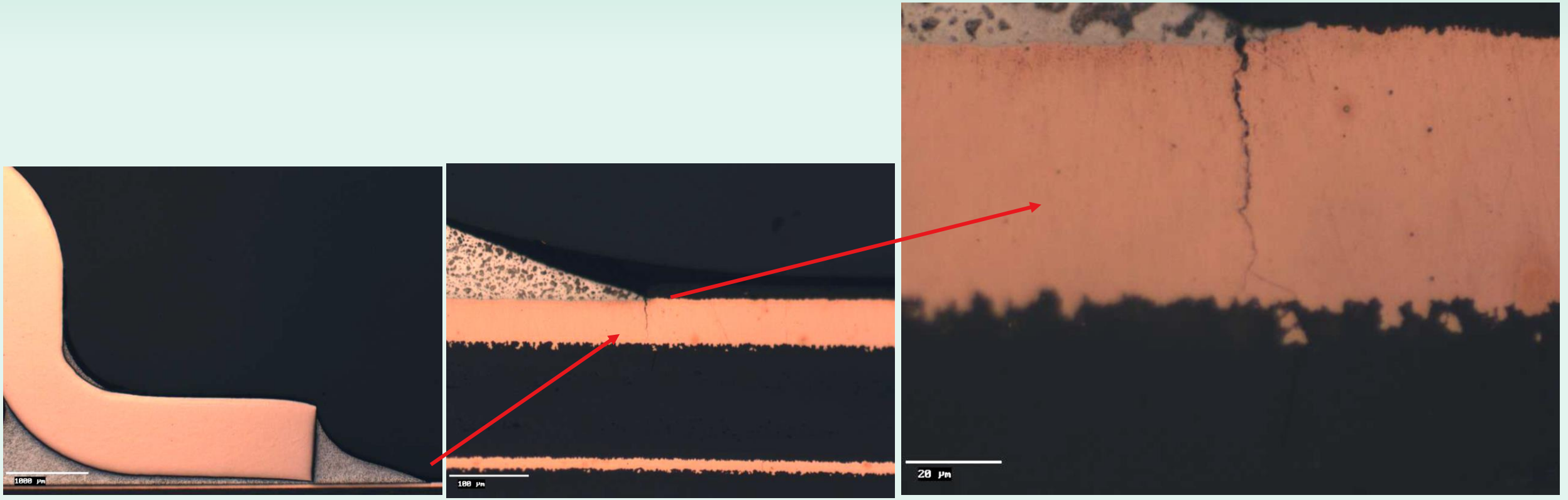
Failures of the leads of surface mounted FP during vibration testing





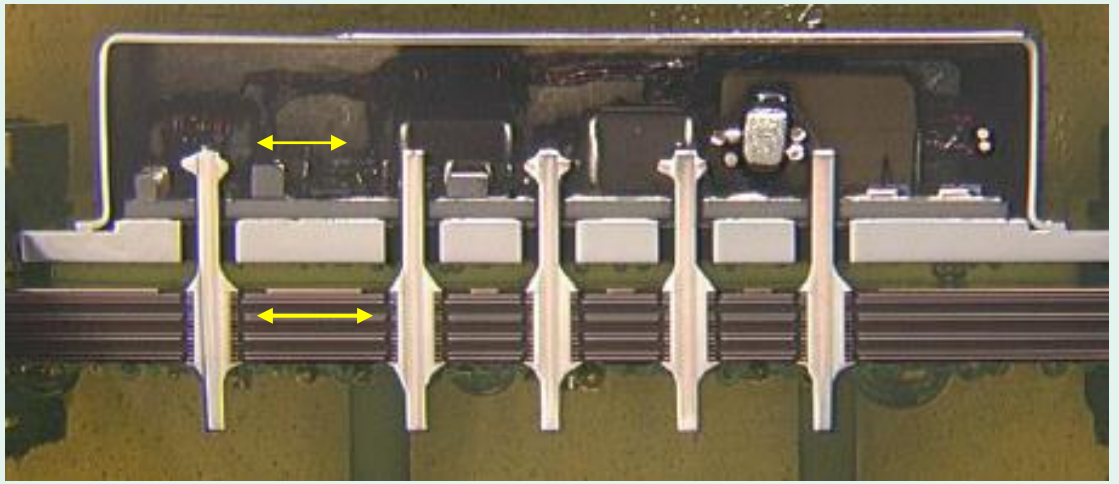
Assembly reliability

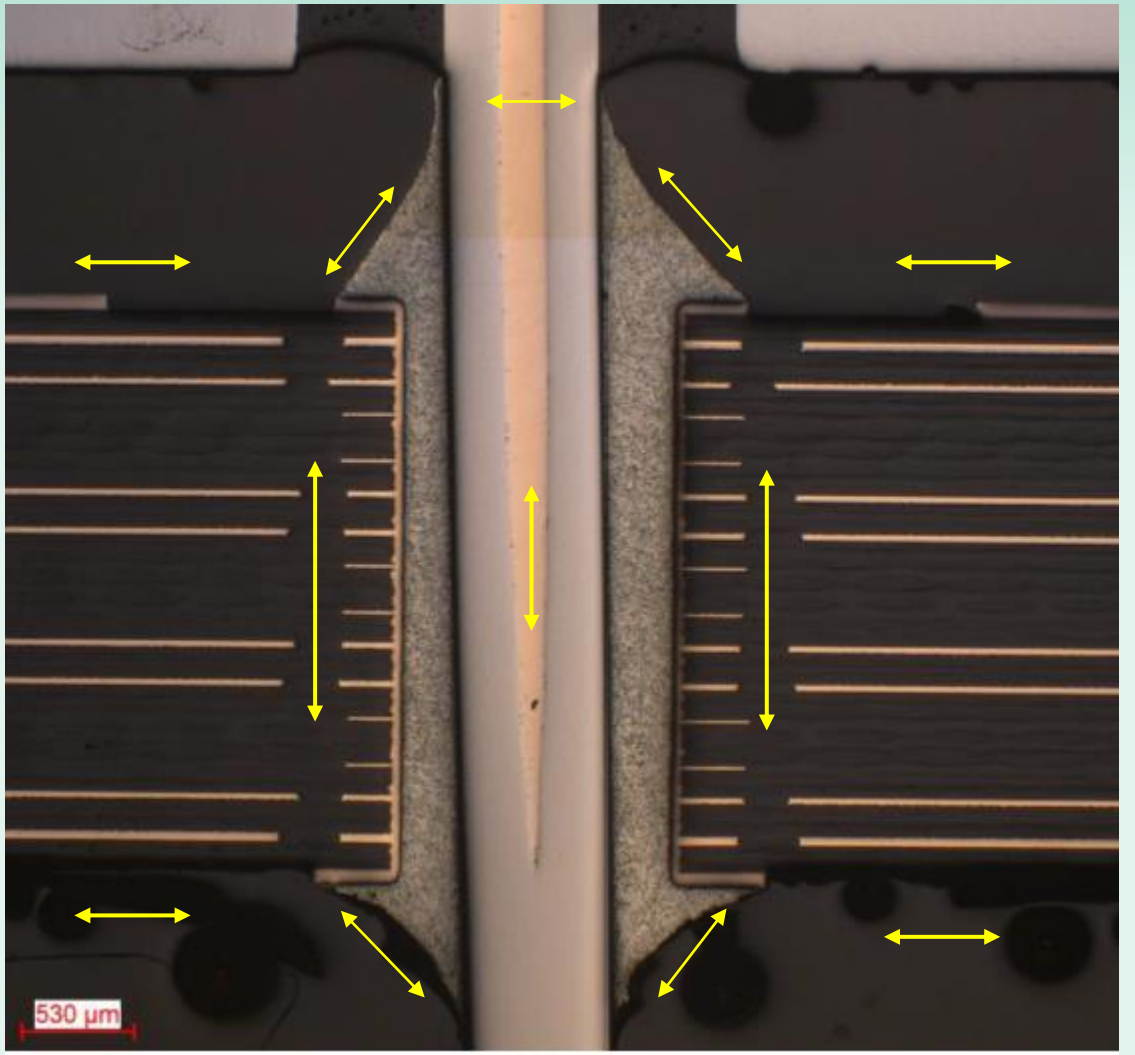
Crack in PCB as result of vibration testing:
Mechanical support of the board not compatible with the applied input levels



Assembly reliability

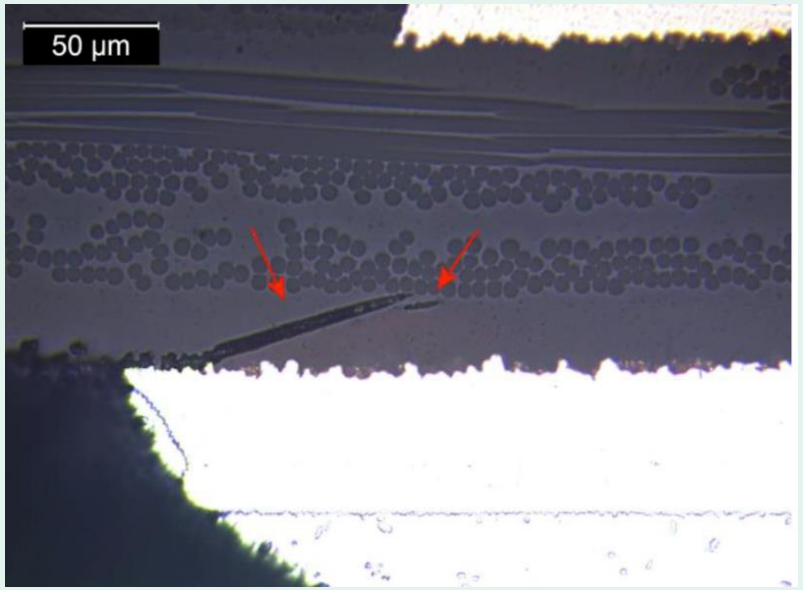
Stress in a THT connection during thermal cycling

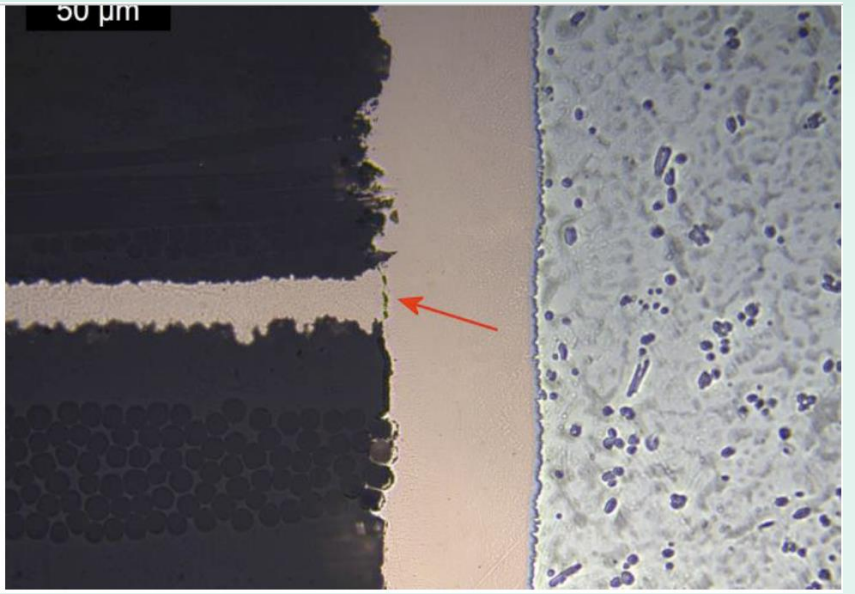


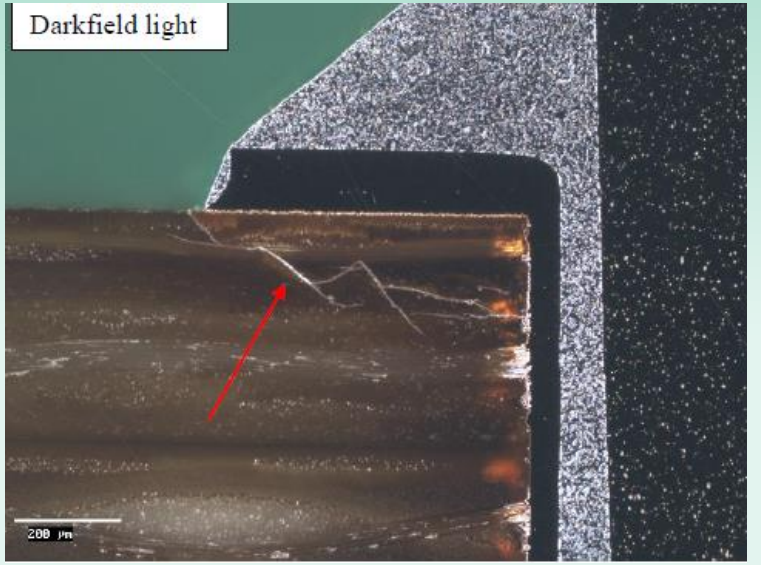


Assembly reliability

THT Defect induced in PCB







Assembly reliability

Possible defects in PCB (ECSS-Q-ST-70-60)

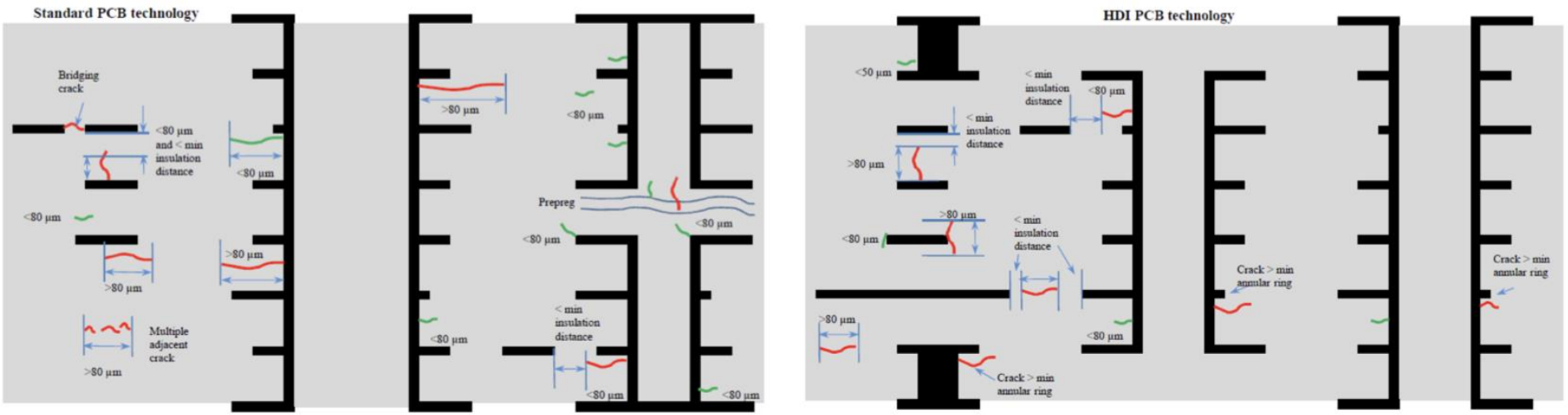


Figure 10-47: Acceptable (green) and non-acceptable (red) dielectric cracks

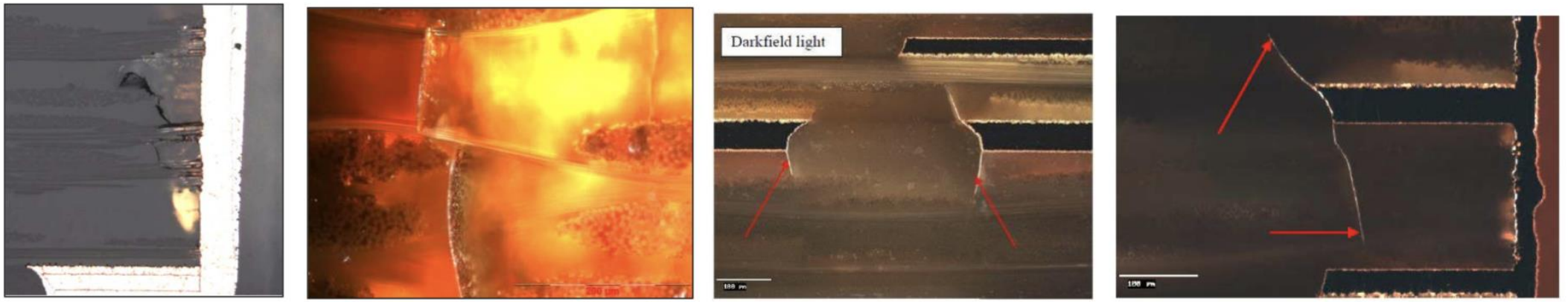
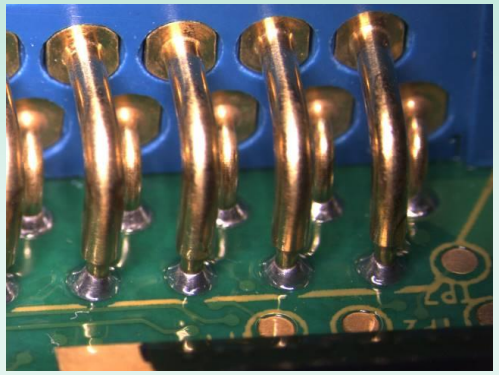
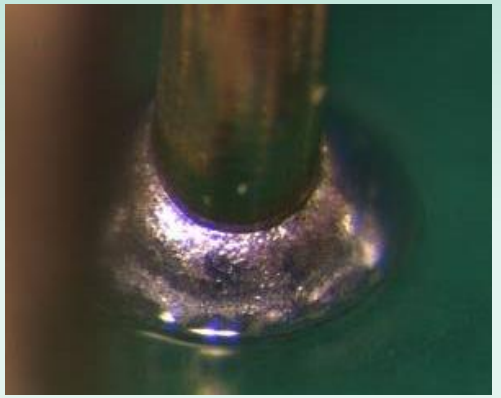


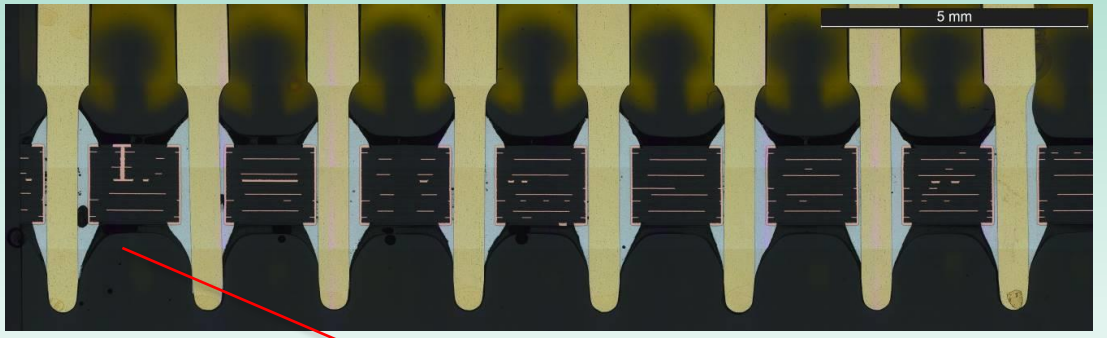
Figure 10-48: Examples of laminate cracks

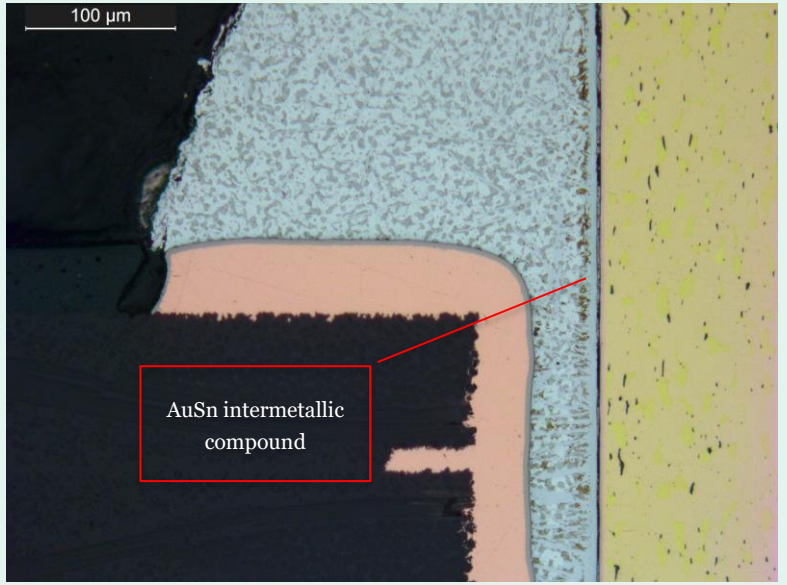
Assembly reliability

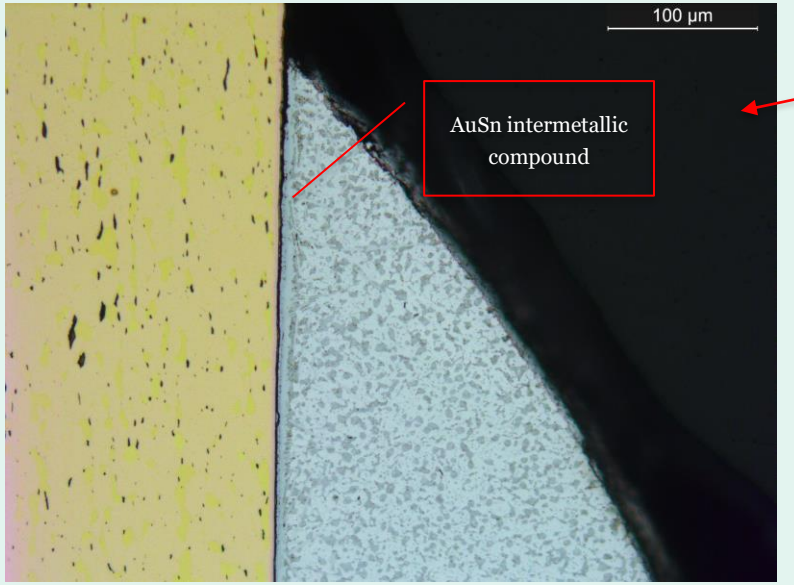
Soldering on Au finished surfaces

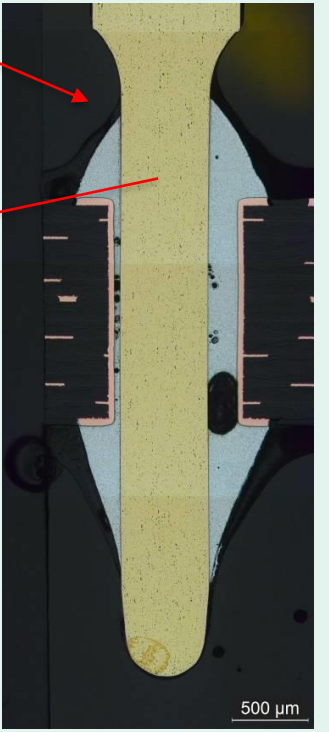






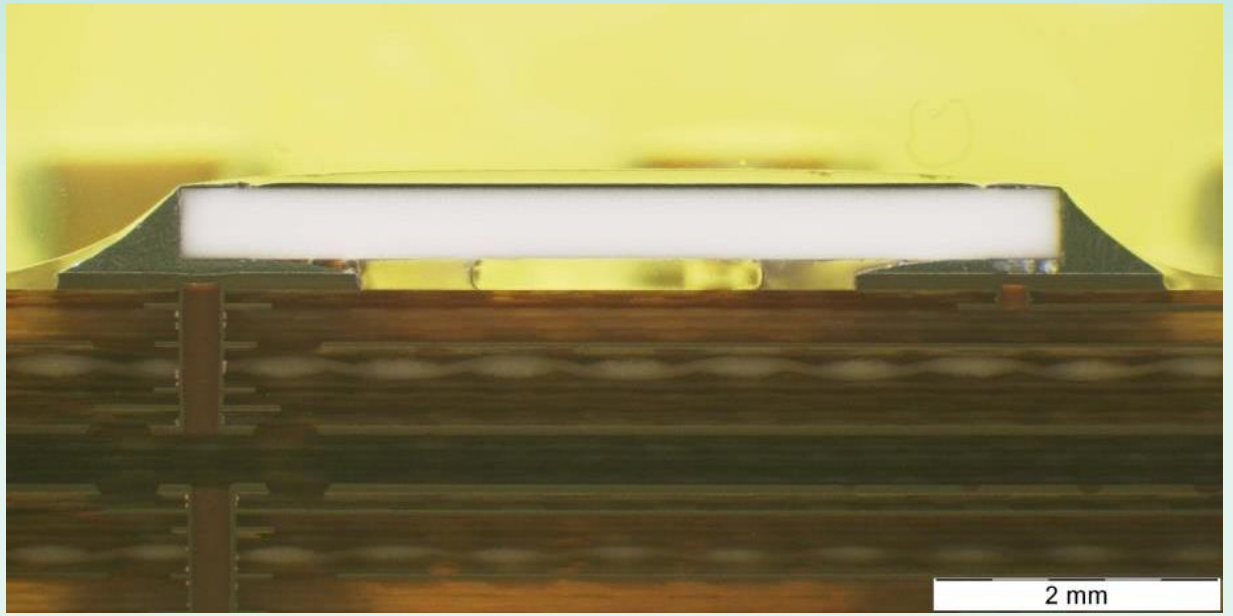


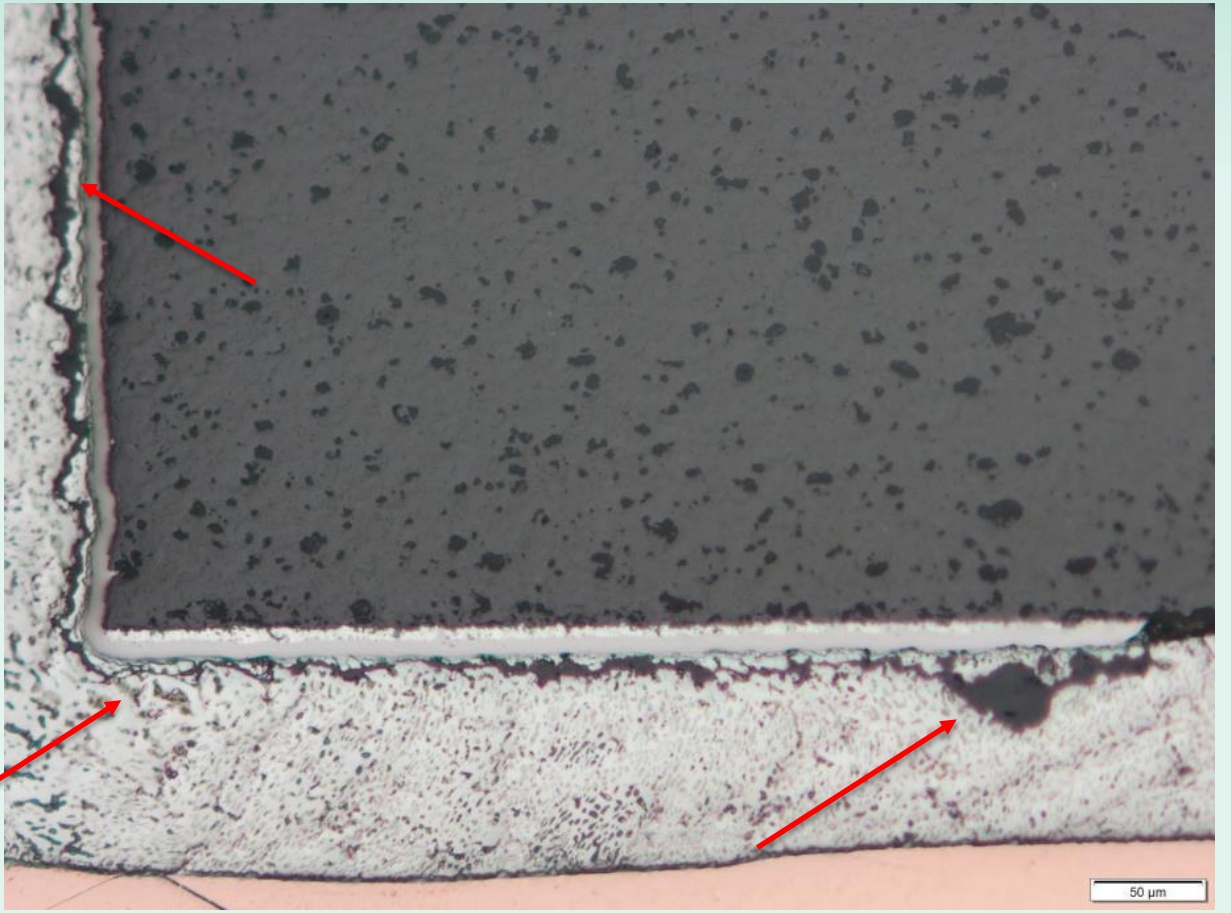




Assembly reliability

Cracks in solder joints due to thermal cycling

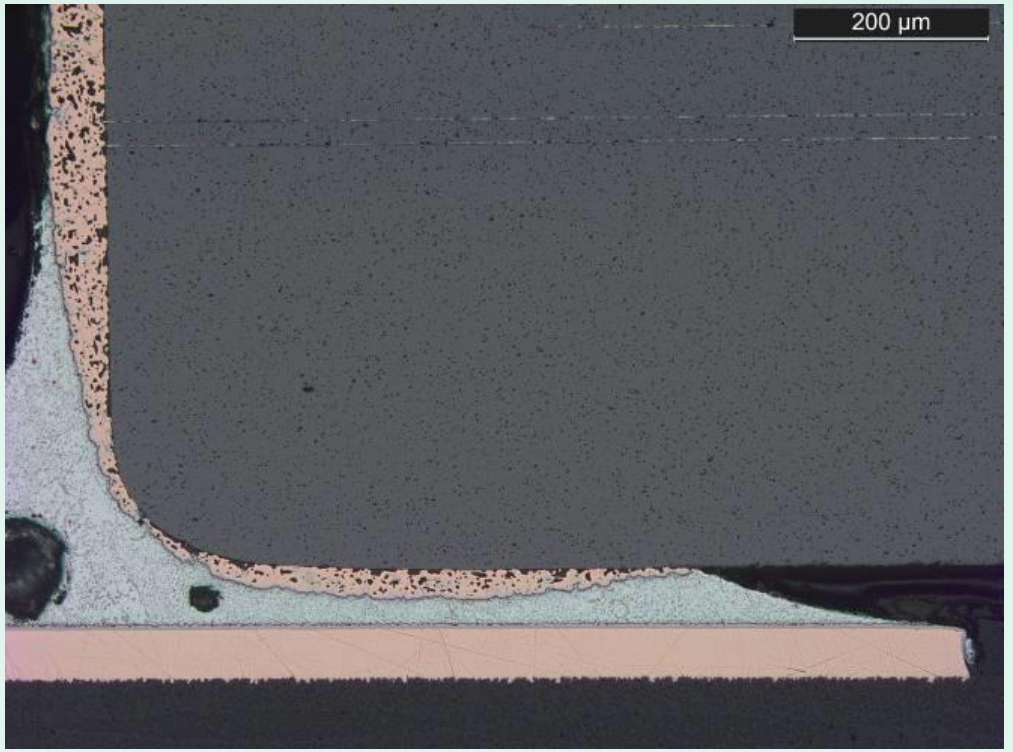


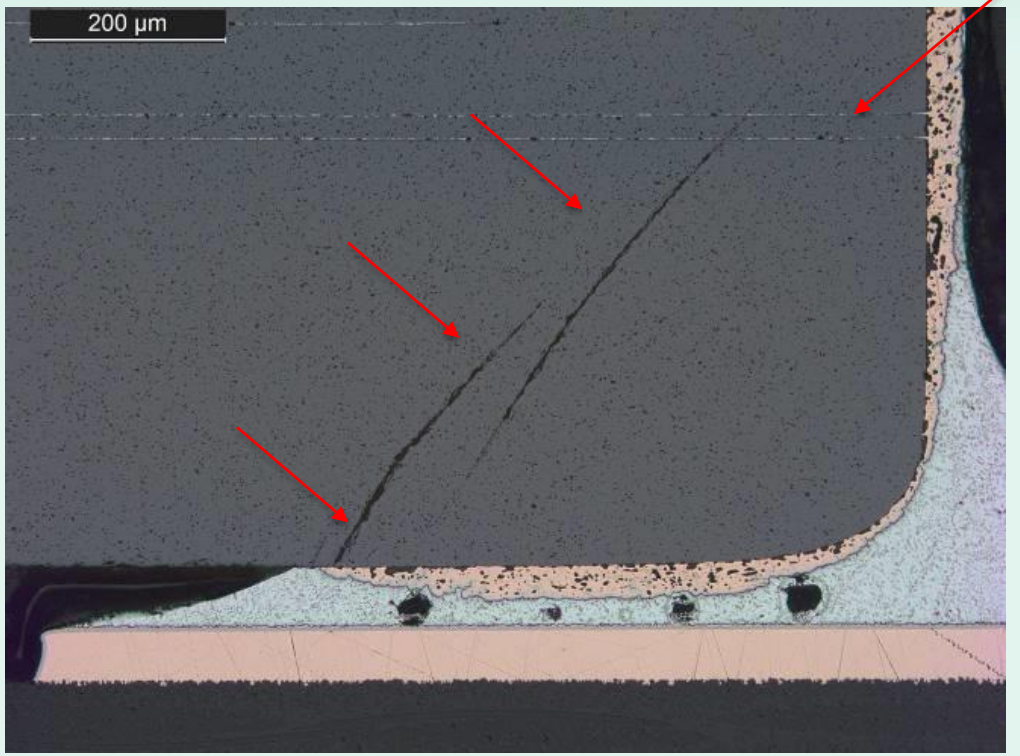


Chip resistor R2512

Assembly reliability

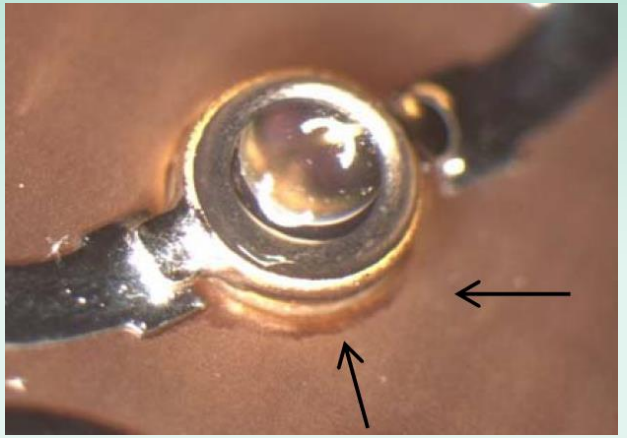
Cracks in ceramic capacitors: Thermal shock

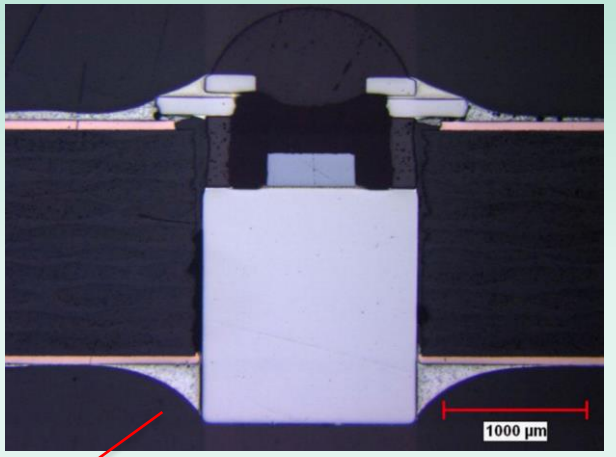


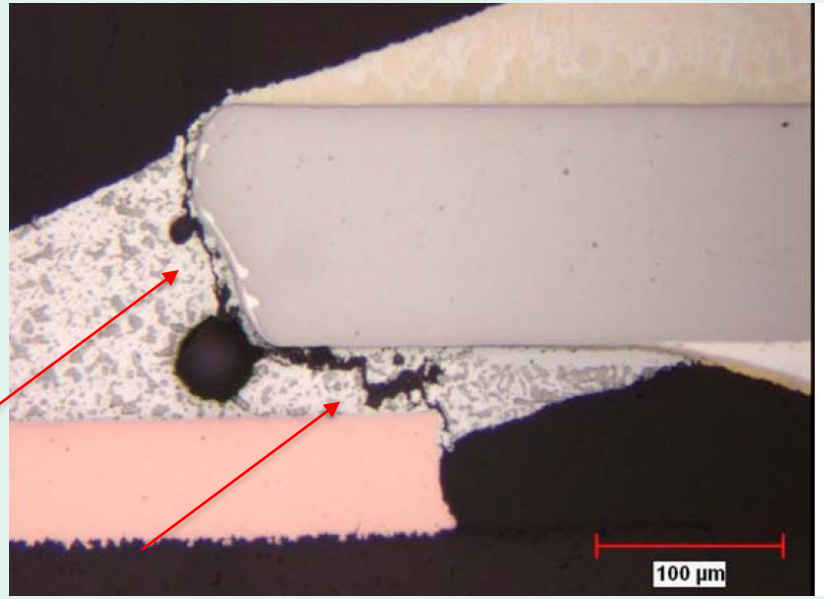


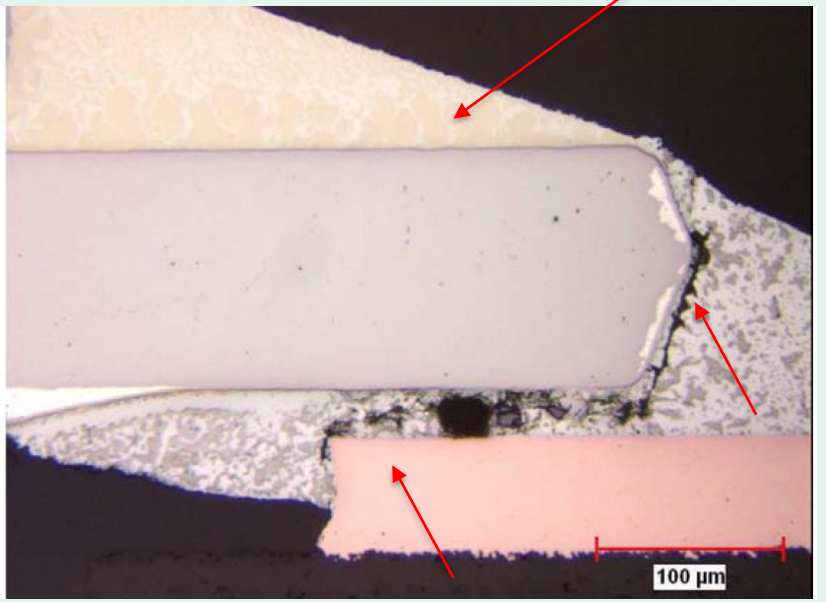
Assembly reliability

Poor design of assembly configuration (lack of stress relief)



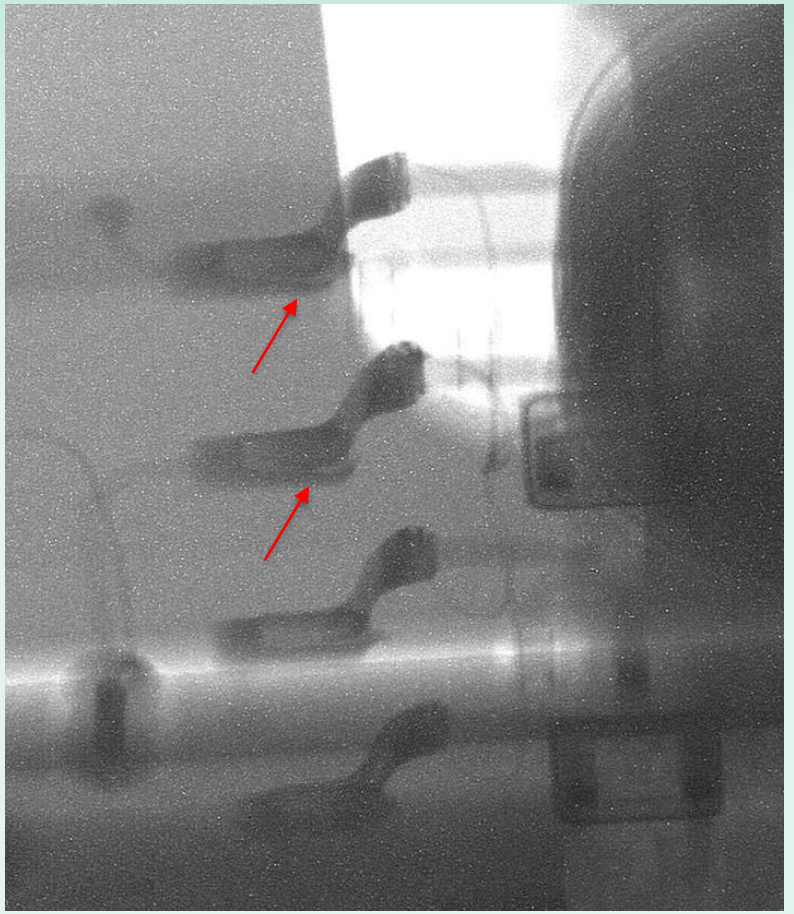


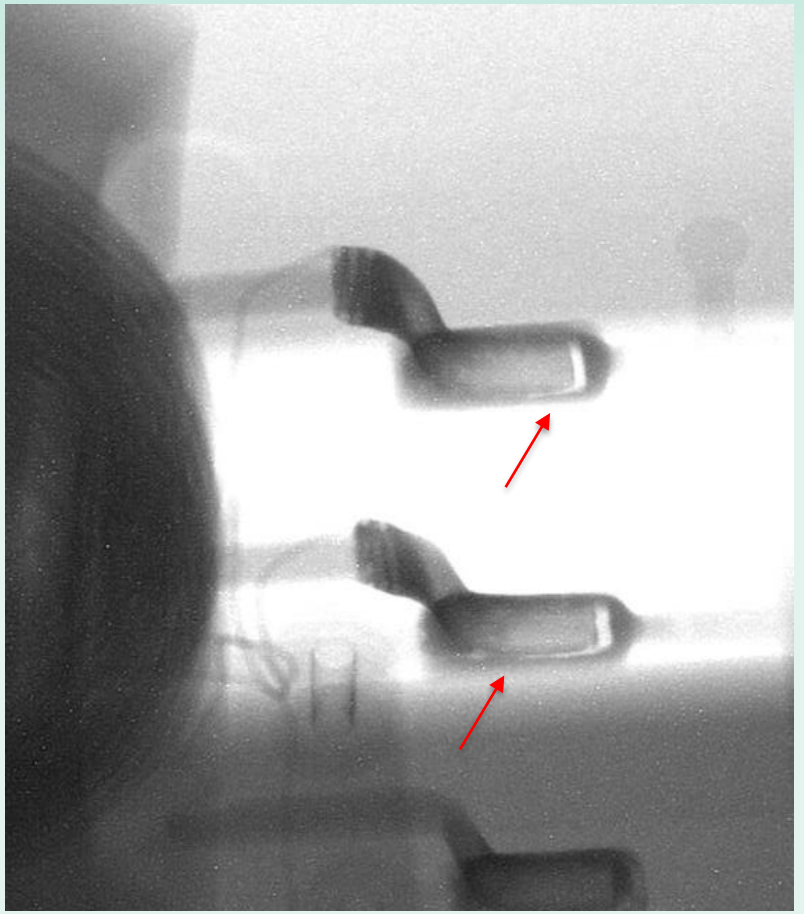




Assembly reliability

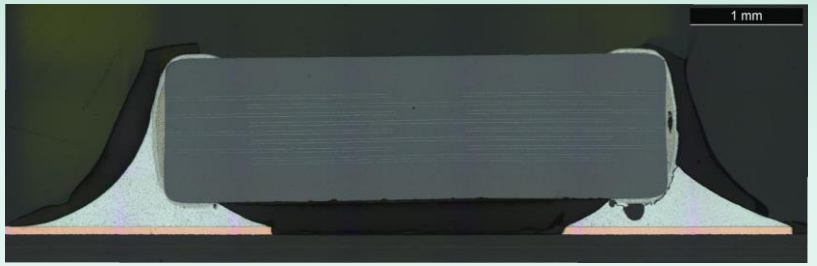
High voltage potting or excess of coating negating stress relief

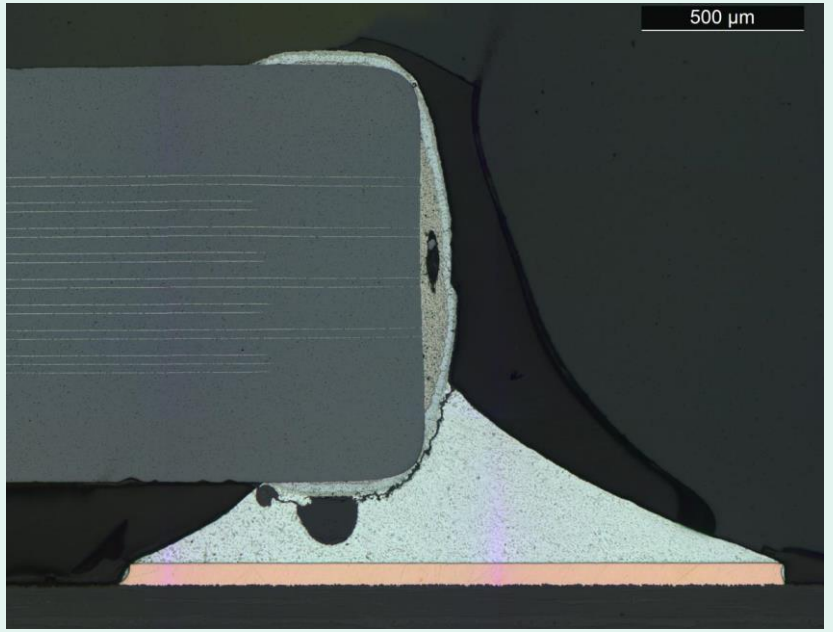


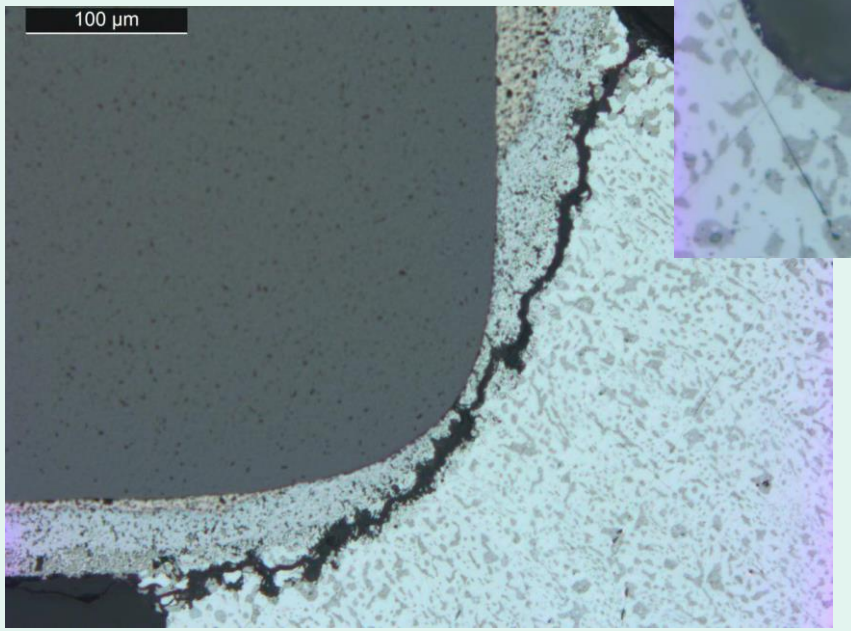


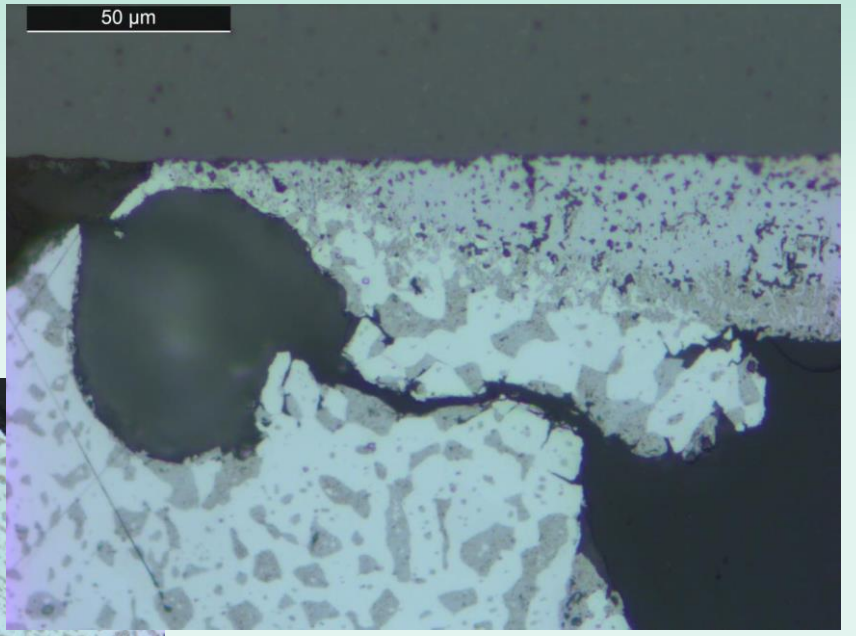
Assembly reliability

Incorrect selection of the finish of a device: use of capacitors without Ni barrier in the termination.



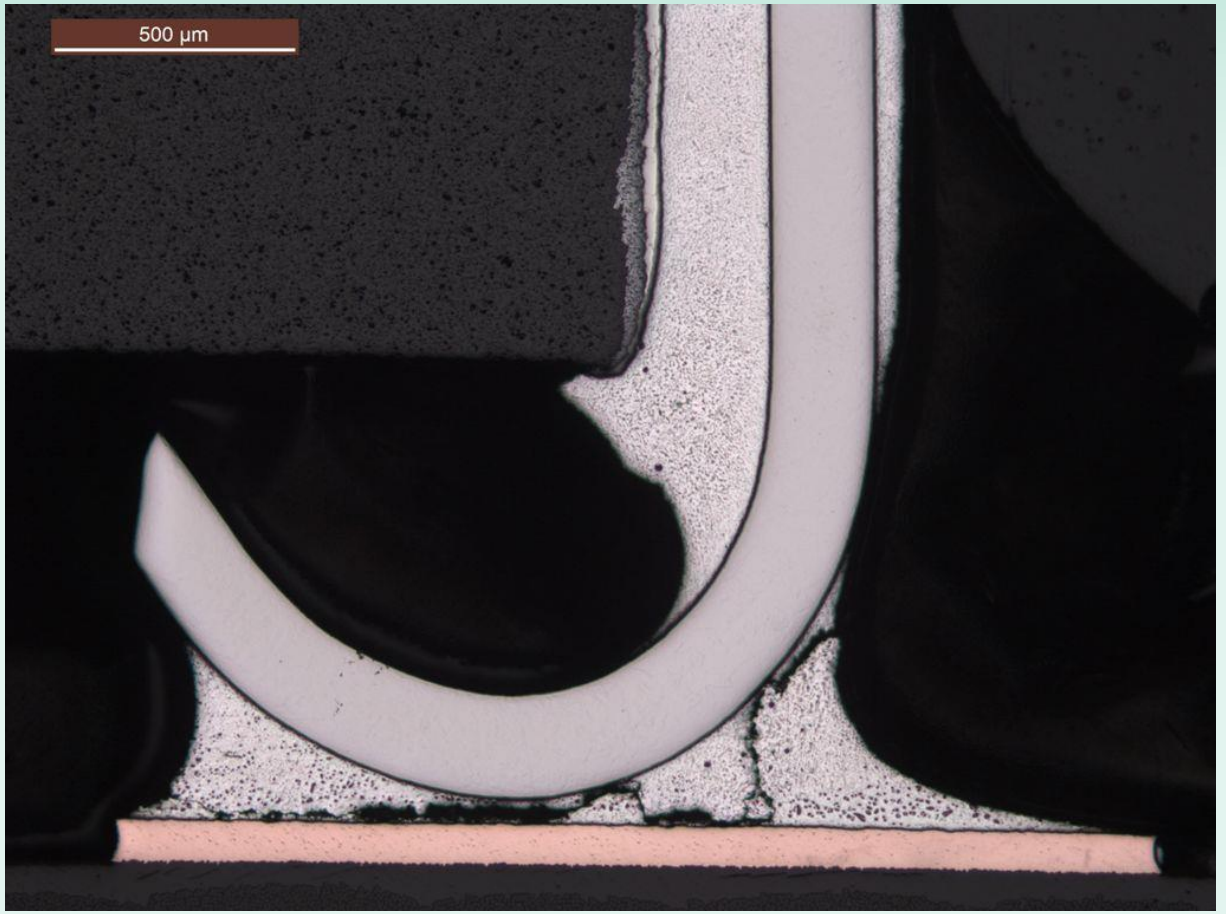


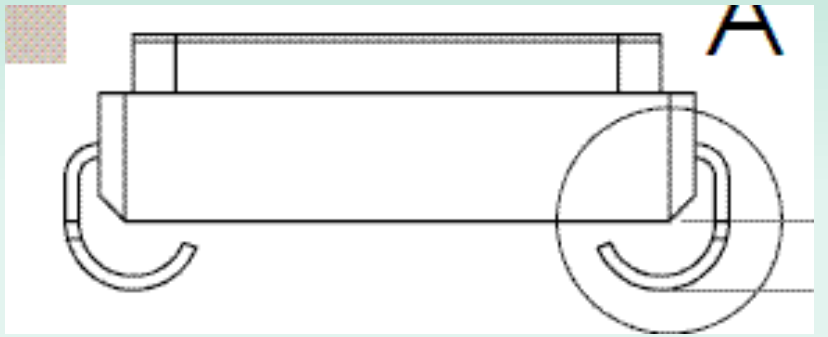




Assembly reliability

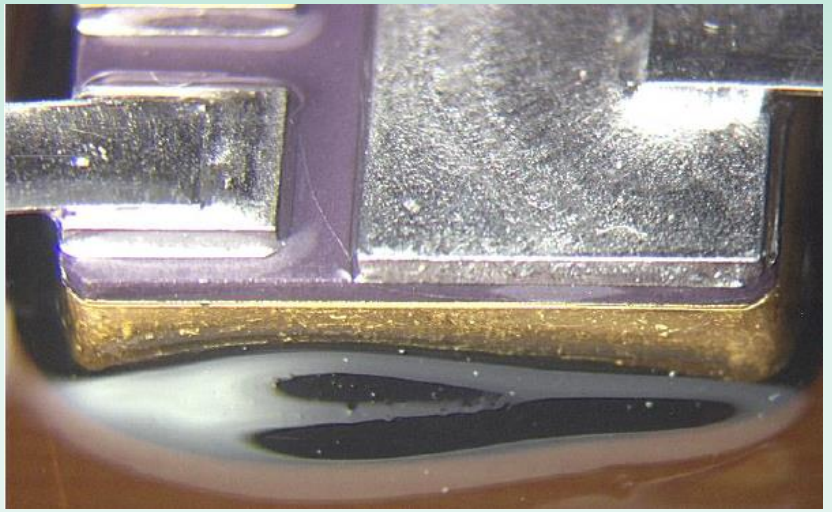
Cracks in solder joints due to negation of the stress relief

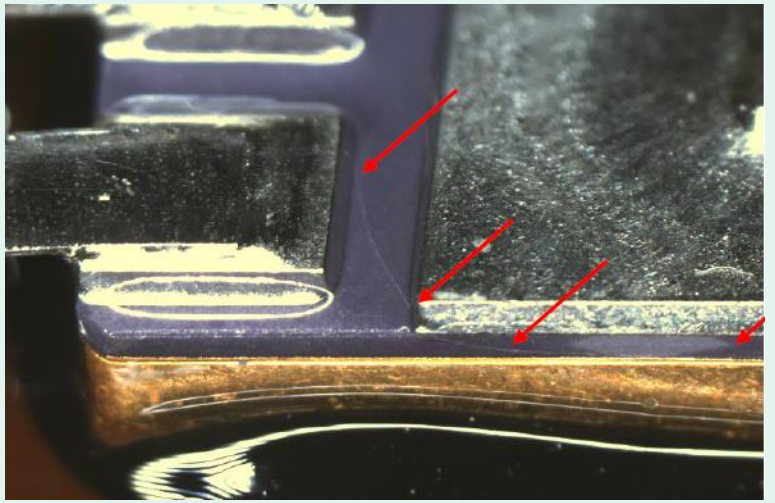


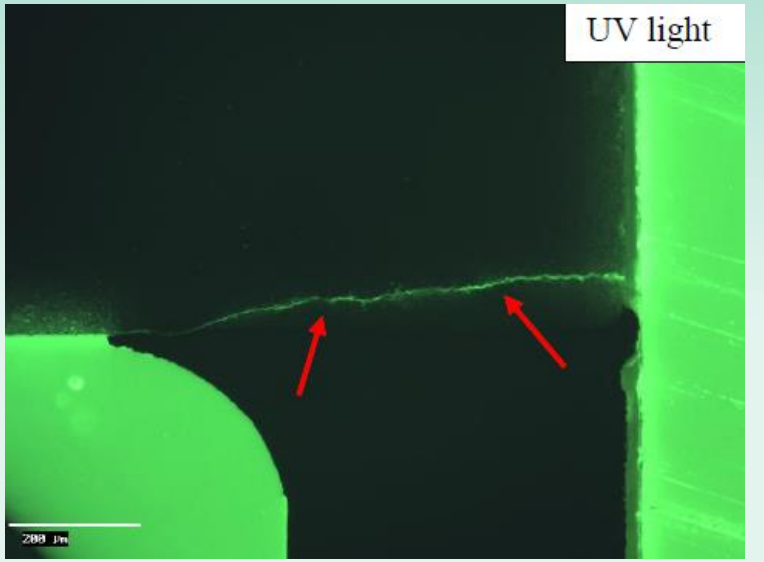


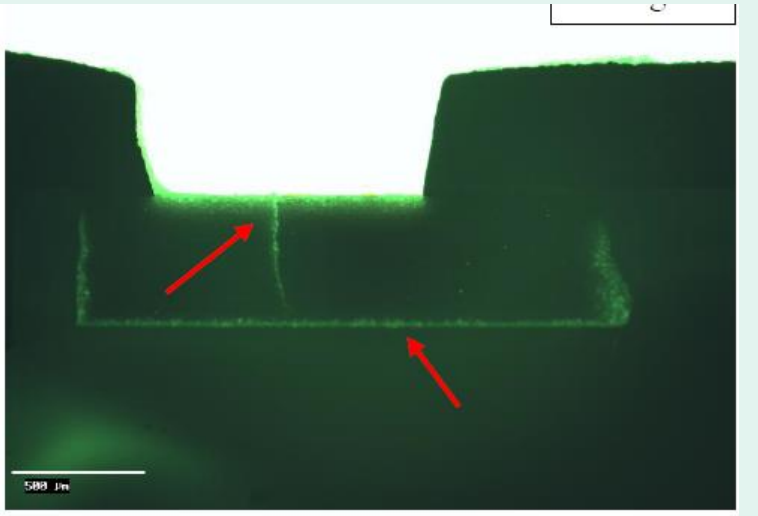
Assembly reliability

Cracks in ceramic of SMD packages



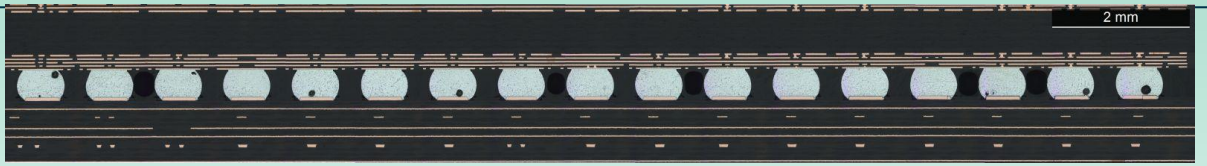


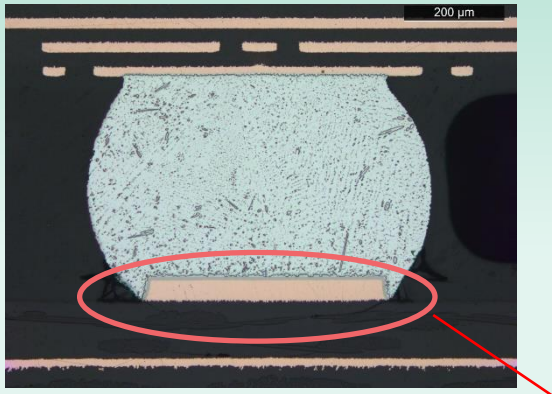


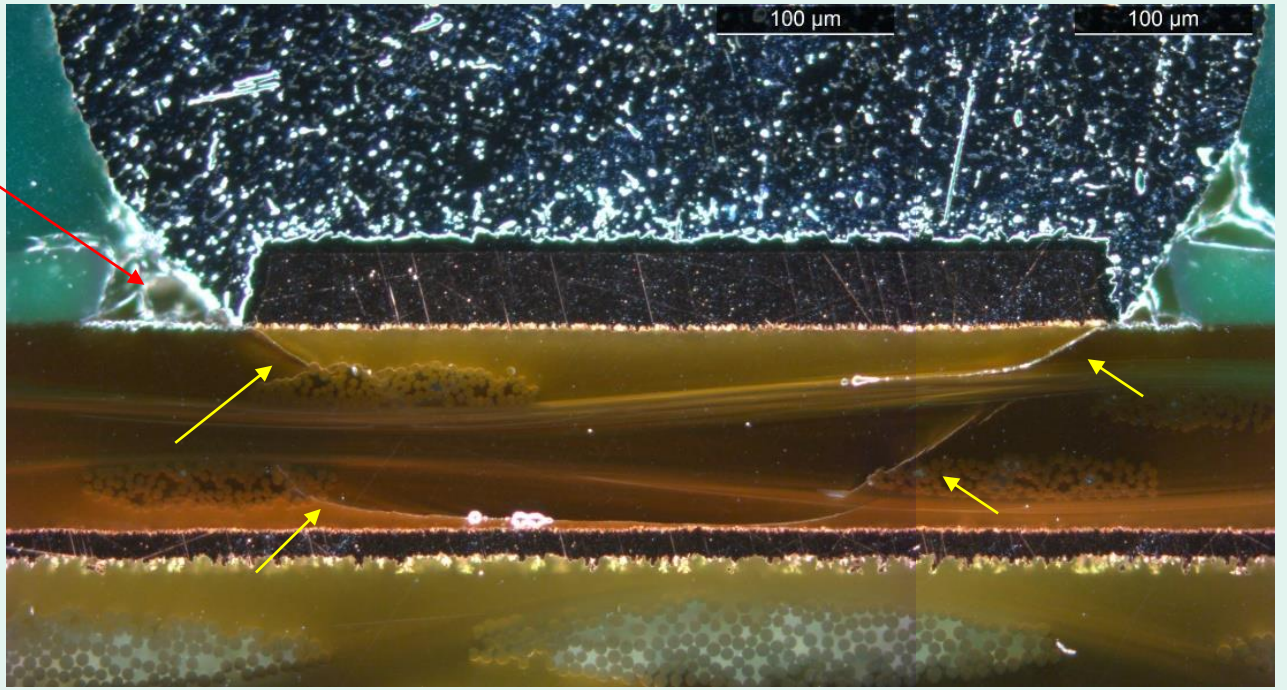


Assembly reliability

Failure of BGA: pad cratering

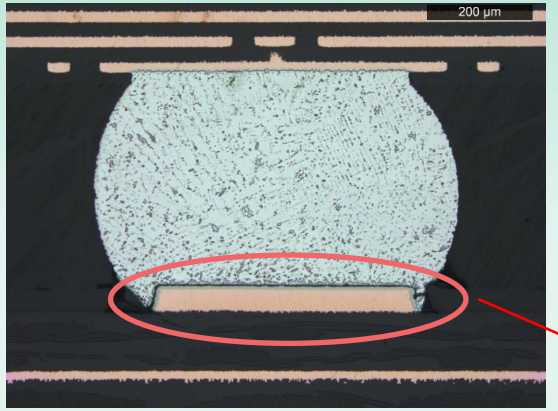


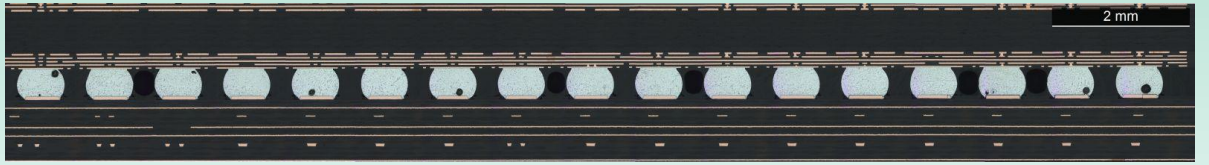


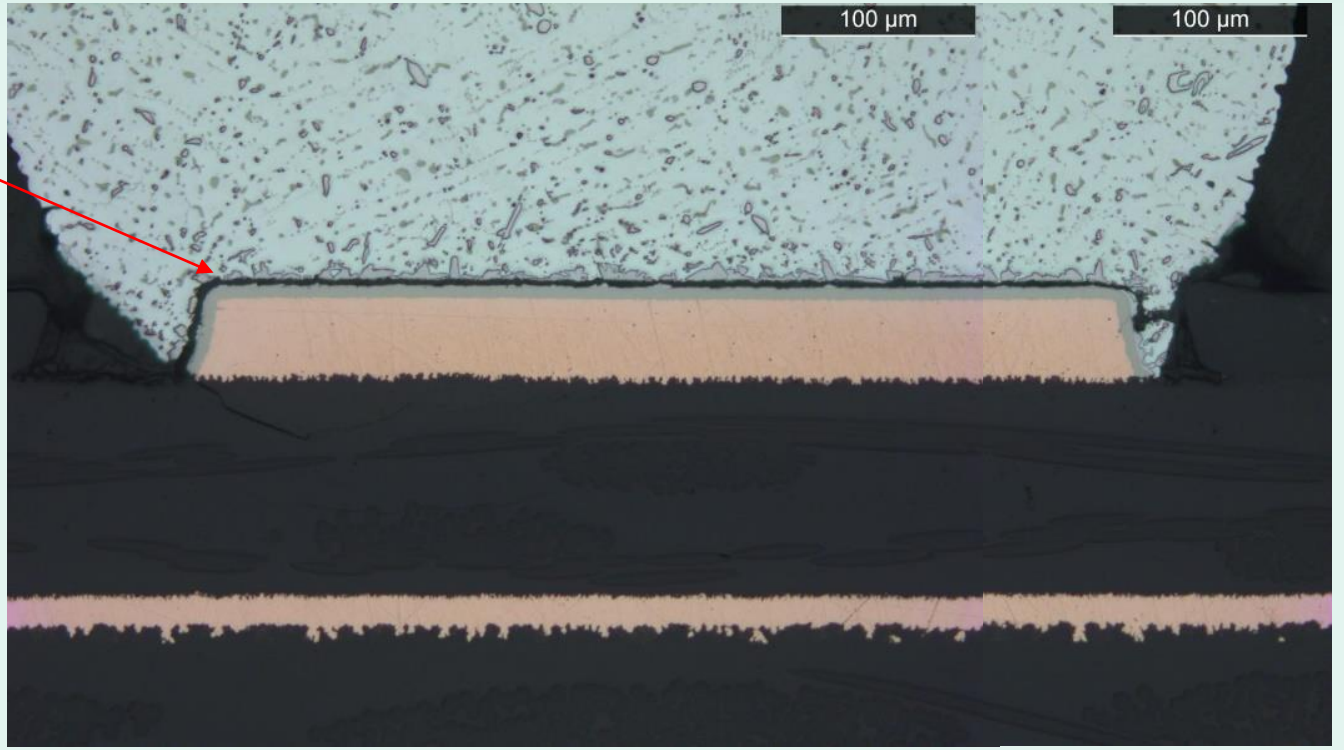


Assembly reliability

Failure of BGA: crack at solder/pad interface

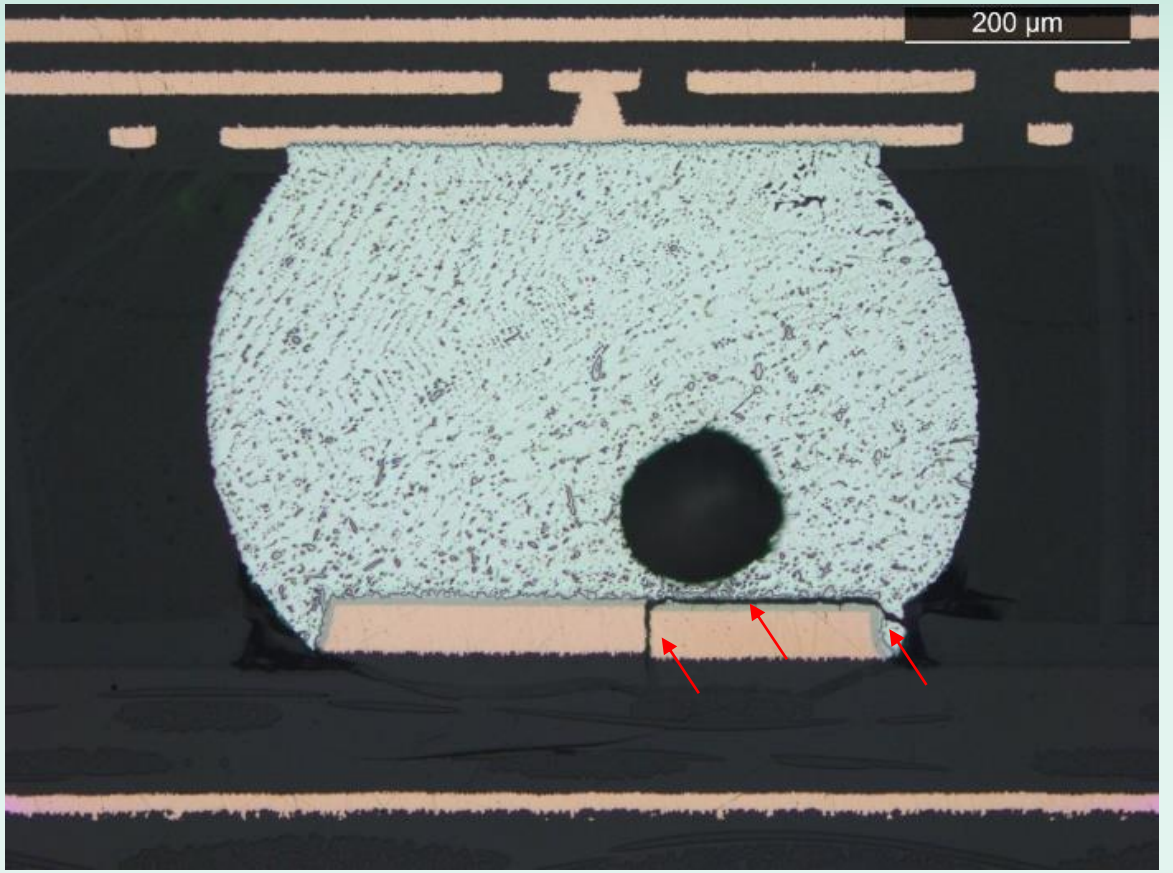






Assembly reliability

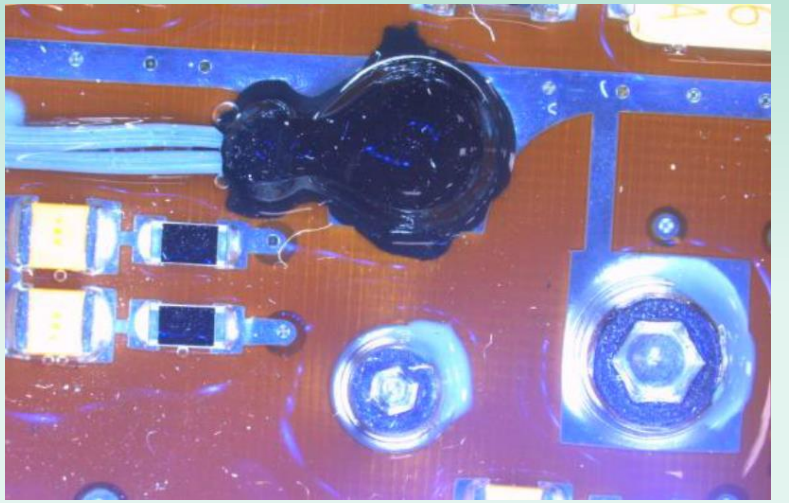
Failure of BGA: mixed failure propagation
Device was submitted to thermal cycling + vibration + thermal cycling

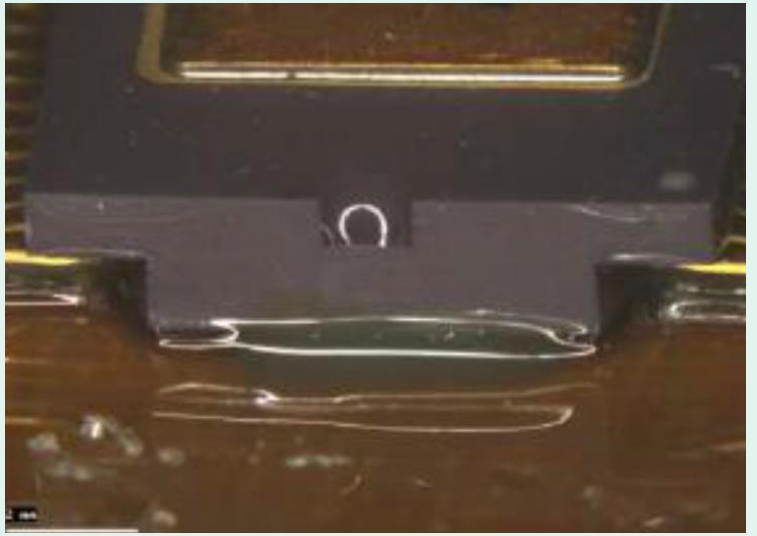


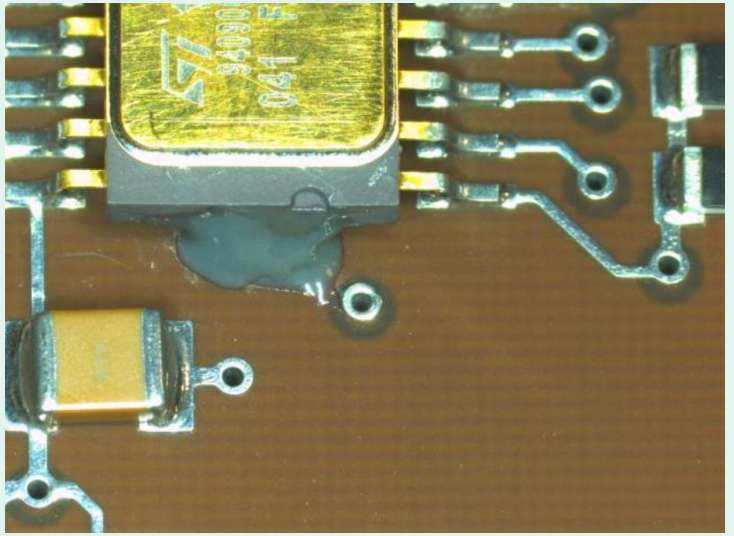
Assembly reliability

Poor control of the staking/bonding process,

Bonding on SnPb finished surfaces. These non compliance have resulted in failures during unit qualification or acceptance test

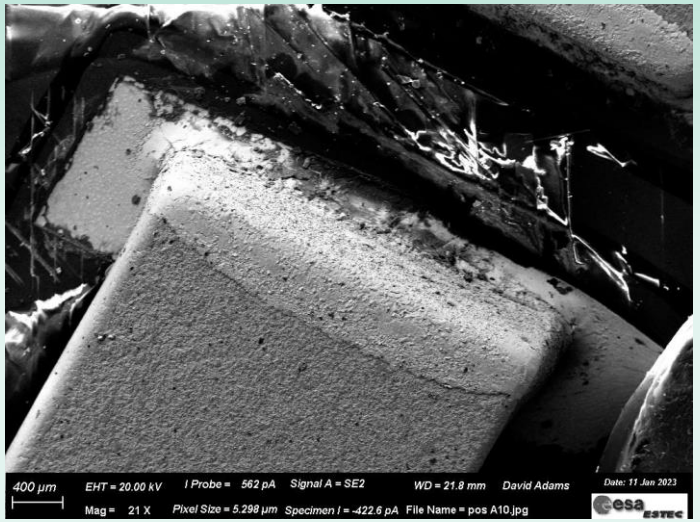






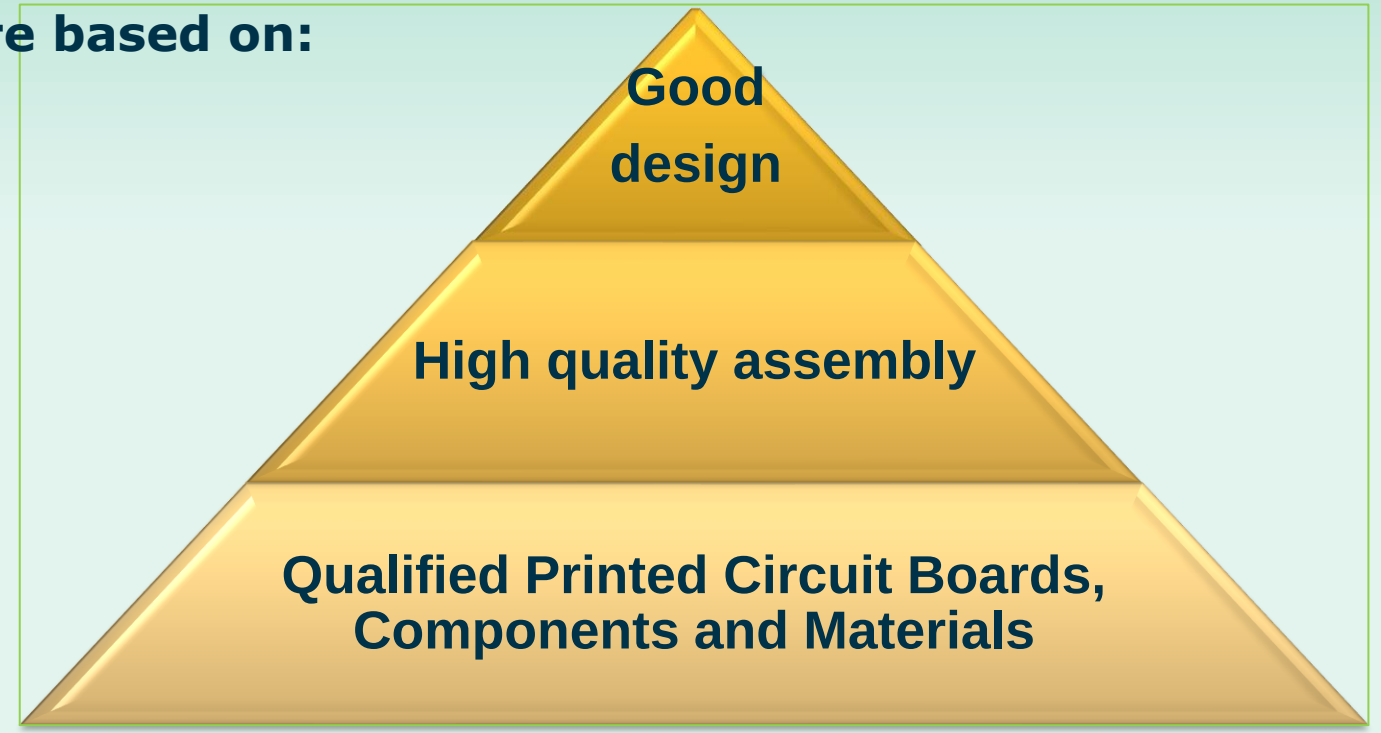
Assembly reliability

Sn Whiskers



Assembly reliability

Reliable electronic assemblies are based on:



This is achieved through the application of dedicated standards

ECSS Standards

ECSS-Q-ST-70-07: Wave soldering replaced by ECSS-Q-ST-70-61C

ECSS-Q-ST-70-08: Hand soldering of through hole connection replaced by ECSS-Q-ST-70-61C

ECSS-Q-ST-70-18: RF cables assemblies

ECSS-Q-ST-70-26: Crimping

ECSS-Q-ST-70-28: Repair and modification on PCBs

ECSS-Q-ST-70-30C: Wire wrap

ECSS-Q-ST-70-38C Rev 1: SMT soldering replaced by ECSS-Q-ST-70-61C

ECSS-Q-ST-70-61C: High reliability assembly for surface mount and through hole connection

ECSS: European Cooperation for Space Standardization

ECSS-Q-ST-70-61C

SCOPE

- This Standard defines the technical requirements and quality assurance provisions for the manufacture and verification of high-reliability electronic circuits of surface mount, through hole, solderless assemblies and soldering of harness and wire interconnection.

- The Standard defines workmanship requirements, the acceptance and rejection criteria for high-reliability assemblies intended to withstand ground testing conditions including LTS (long term storage) and the environment imposed by space flight and launchers.

- The mounting and supporting of components, terminals and conductors specified in this standard applies only to assemblies designed to continuously operate over the mission within the temperature limits of -55 ° C to +85 ° C at solder joint level.

ECSS-Q-ST-70-61C

SCOPE

- Requirements related to printed circuit boards are contained in ECSS-Q-ST-70-60 and ECSS-Q-ST-70-12.
- This standard does not cover lead-free soldering and associated requirements.
- This Standard does not cover the qualification and acceptance of the EQM and FM equipment with high-reliability electronic circuits of surface mount, through hole and solderless assemblies.
- This Standard does not cover verification of thermal properties for component assembly.
- This Standard does not cover pressfit connectors due to the possible damage in the PCB that is not evaluated within this test requirement.
- The qualification and acceptance tests of equipment manufactured in accordance with this Standard are covered by ECSS-E-ST-10-03.
- This standard may be tailored for the specific characteristics and constraints of a space project, in accordance with ECSS-S-ST-00.

Which topics are covered by the standard

- Normative references
- Terms, definitions and abbreviated terms
- Principles of reliable soldered connections
- Preparatory conditions
- Material selection
- Preparations prior to mounting and soldering
- Components mounting requirements prior to soldering
- Attachment of conductors to terminals, solder cups and cables
- Assembly to terminals and to PCBs
- Post soldering process requirements
- Final Inspection

What is covered by the standard

- Verification procedure
- Environmental tests conditions
- Outsourcing
- Process identification document (PID)
- Quality assurance

"The following are the general principles to provide reliable soldered connections:

• Reliable soldered connections are the result of proper design, control of tools, materials, processes work environments and workmanship performed in accordance to verified and approved procedures, inspection control and precautions.

• The basic design concepts to provide reliable connections and to avoid solder joint failure are as follows:

– Stress relief is an inherent part of the design which reduces detrimental thermal and mechanical stresses on the solder connections.

– Where adequate stress relief is not possible materials are so selected that the mismatch of thermal expansion coefficients is a minimum at the constraint points in the component mounting configuration.

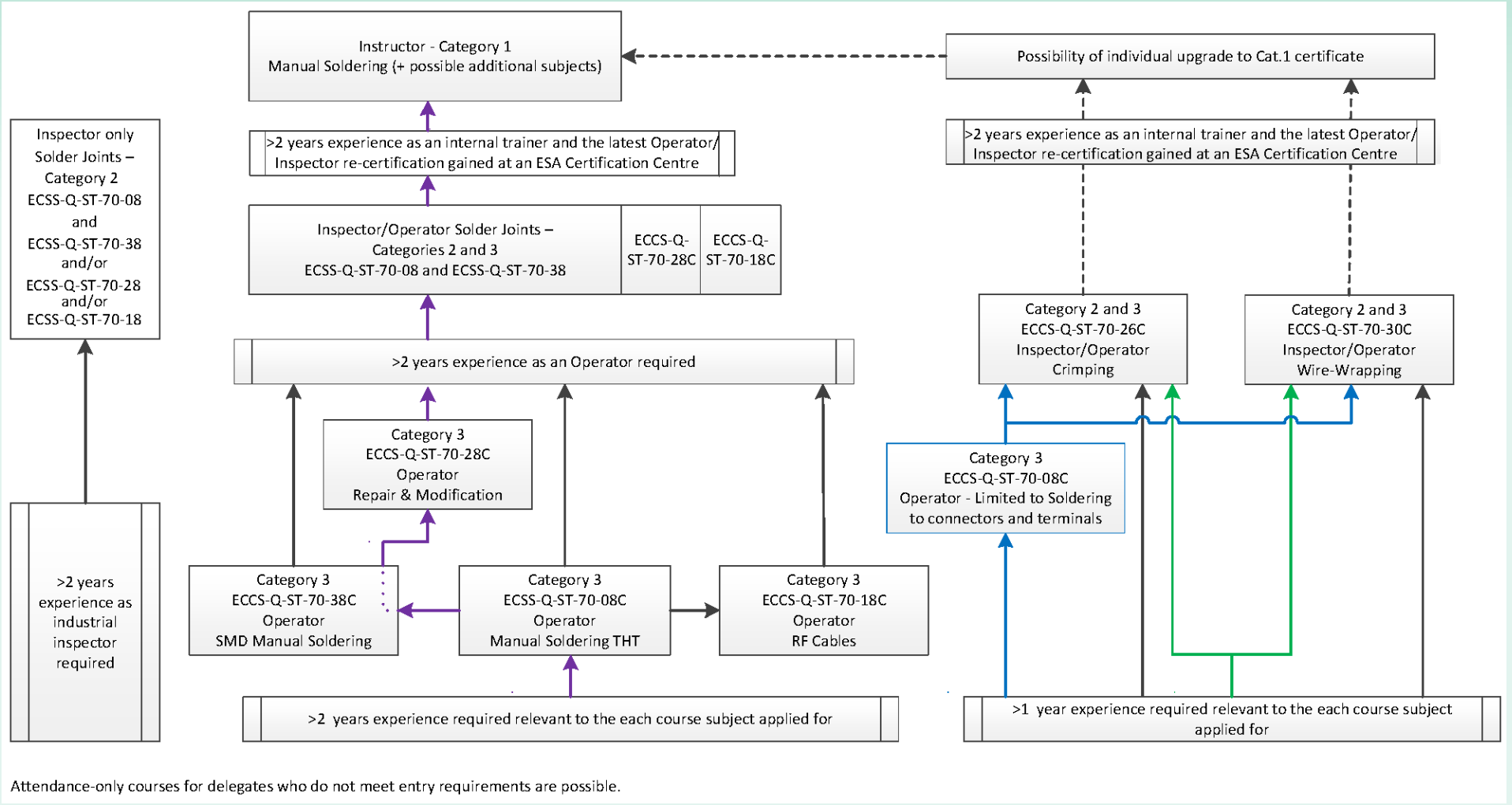
• The assembled substrates are designed to allow easy inspection, rework, and repair.

• The electrical and mechanical integrity of components and assemblies are retained after exposure to processes employed during manufacture and assembly, as handling, baking, fluxing, soldering, cleaning depanelization, electrical test and PCB integration.

• Soldering to gold using tin-lead alloy can cause failure. "

ECSS-Q-ST-70-61 Workmanship

Certification of personnel (STR-258 is.2)



Attendance-only courses for delegates who do not meet entry requirements are possible.

ESA skills certification centers

-ASTA in UK

-IFE in Germany

-ZVE in Germany

-IIS in Italy

-IS in France

-Hytek in Denmark

-SWI in Switzerland

Renex in Poland under evaluation

High quality assemblies:

- ✓ Assembly verification
- ✓ Audit of the assembly line (See ESA Approved Summary Tables)
- ✓ Approved PID

- ✓ Assembly of sensitive devices (see ESA-TECQTM-MO-1143 issue 2)
- ✓ Review of the assembly process as part of the MPCB (see ESA-TEQTM-MO-1931 iss.3)

ESA memo are available at:
https://escies.org/webdocument/showArticle?id=981

Process approval per ECSS-Q-ST-70-61C

Some definitions:

3.2.1 Approval Authority

entity that reviews and accepts the verification programme, evaluating the test results and grants the final approval

3.2.2 assembly sensitive component

component prone to have cracks in solder joint exceeding 75 % of acceptance criteria of solder cracks or showing nonconformance outside the component manufacturer limit, due to assembly.

NOTE 1 The ESA list of assembly sensitive components is regularly updated and published on ESCIES for information, see www.escies.org, Technologies - ESA SMT Verification. ESA-TECMSP-MO-018961.

NOTE 2 Each company maintains its own list of assembly sensitive components in the PID.

PID: Process Identification Document

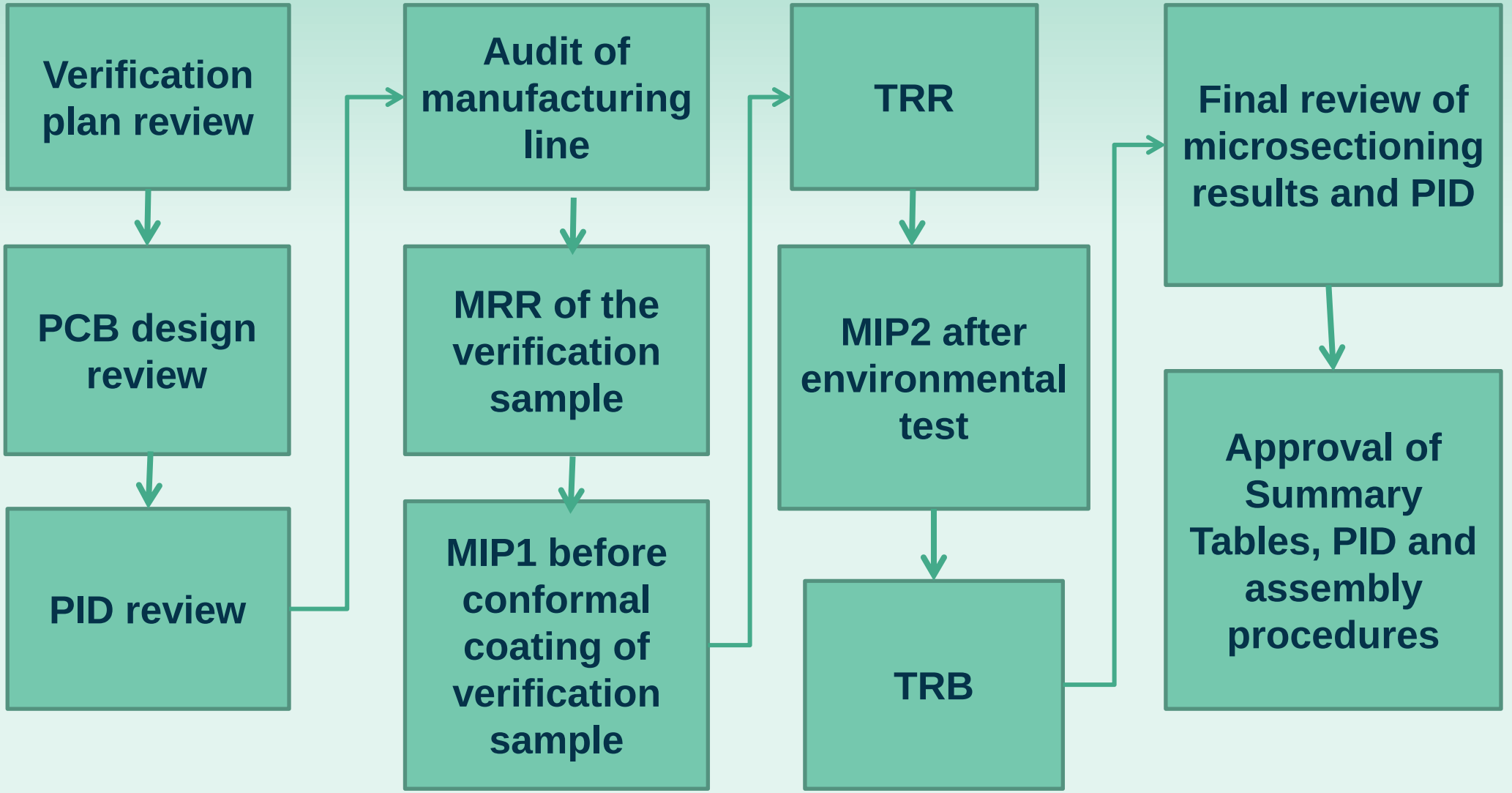
The purpose of the PID is to consolidate the overall management, process and facilities utilised during the manufacturing and verification of the assembly.

Assembly Summary Table:

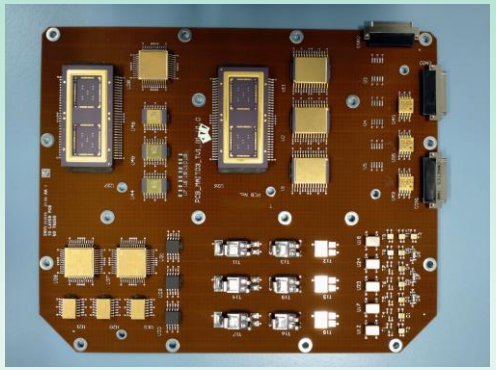
The purpose of the assembly summary table is to consolidate the approval status of the boundary conditions for the verification activity.

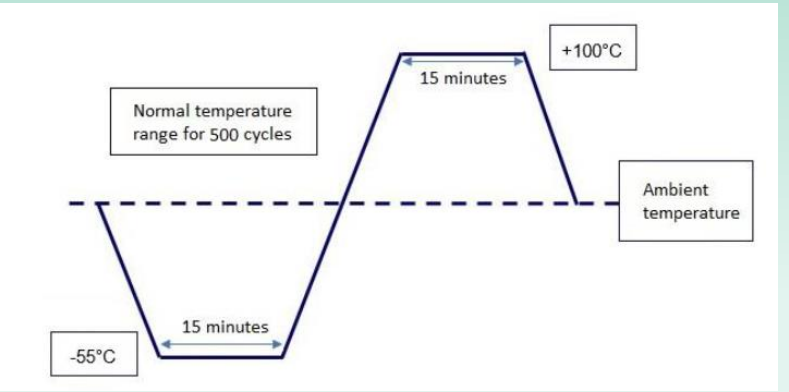
An assembly summary table is issued for each assembly process.

Process approval per ECSS-Q-ST-70-61C

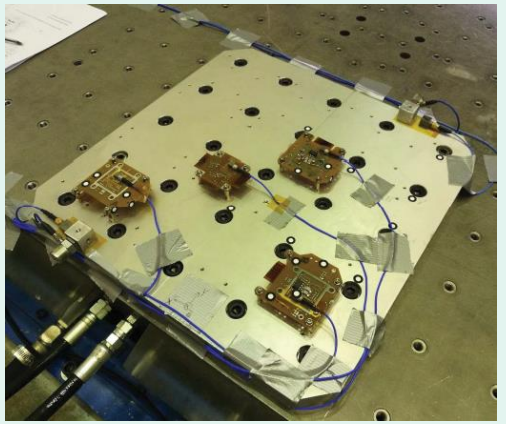


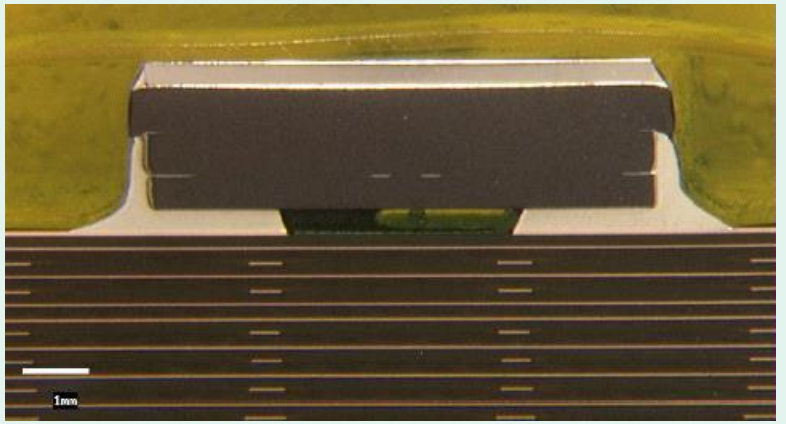
Assembly verification per ECSS-Q-ST-70-61C





Test vehicles manufacturing and inspection ⇨ **Vibration (shock) test** ⇨ **Thermal cycling** ⇨ **Microsectioning**



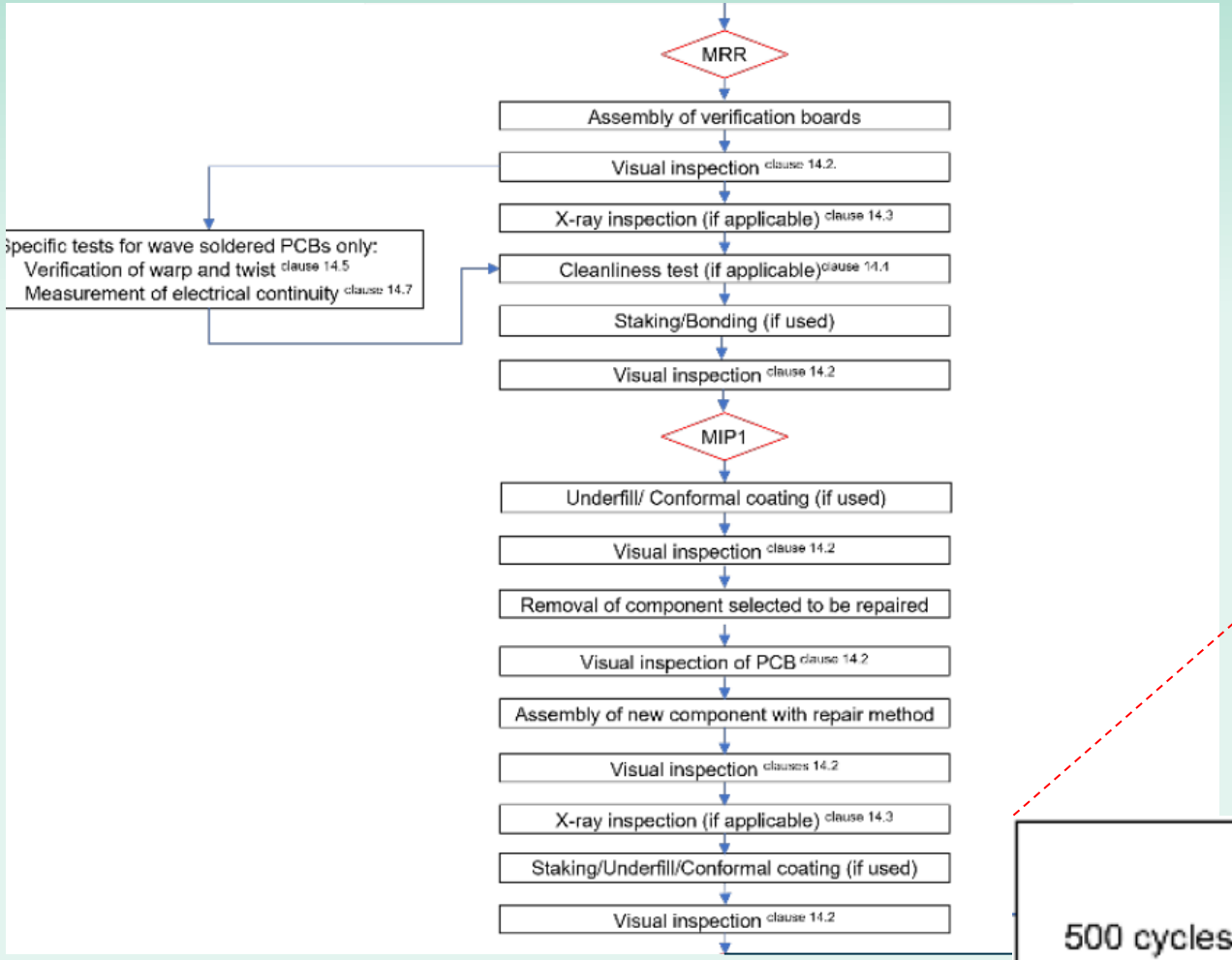


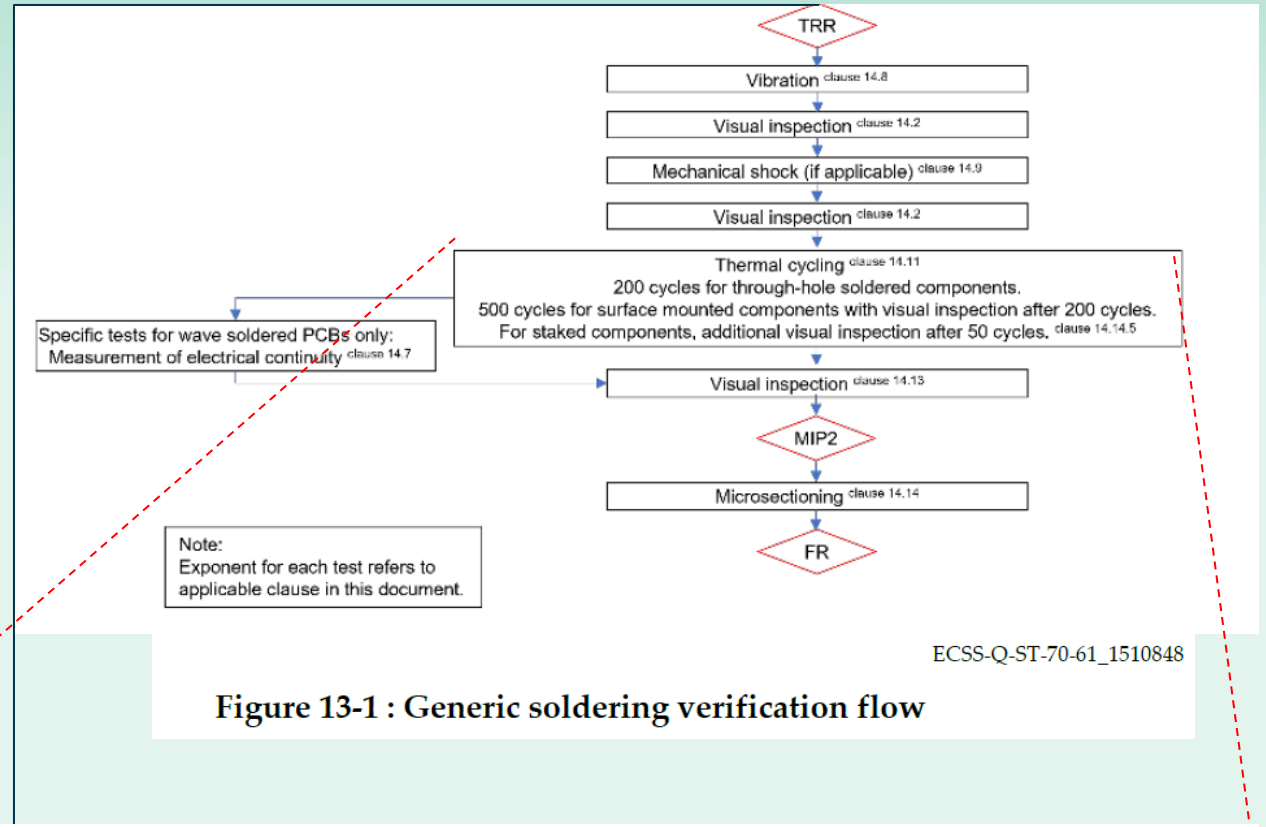
Assembly verification per ECSS-Q-ST-70-61C

Generic flow: test vehicles

COLLECTIVE PROCESSES		NON COLLECTIVE PROCESSES	
Wave soldering	**Reflow soldering**	**Selective wave soldering**	**Manual soldering**
Number of test samples: - 3 identical PCBs; 2 assembled and 1 bare for reference - 3 non assembly sensitive components/board, of which 1 repaired (i.e. 4 components needed in total) - 5 assembly sensitive components/board, of which 1 repaired (i.e. 6 components needed in total)	Number of test samples: - 3 non assembly sensitive components - 5 assembly sensitive components Note: Repair is covered by the verification flow for manual soldering.	Number of test samples: - 3 non assembly sensitive components, of which 1 repaired (i.e. 4 components needed in total) - 5 assembly sensitive components, of which 1 repaired (i.e. 6 components needed in total)	Number of test samples: - 3 non assembly sensitive components, of which 1 repaired (i.e. 4 components needed in total) - 5 assembly sensitive components, of which 1 repaired (i.e. 6 components needed in total)

Assembly verification per ECSS-Q-ST-70-61C





ECSS-Q-ST-70-61_1510848

Figure 13-1 : Generic soldering verification flow

Thermal cycling clause 14.11
200 cycles for through-hole soldered components.
500 cycles for surface mounted components with visual inspection after 200 cycles.
For staked components, additional visual inspection after 50 cycles. clause 14.14.5

Assembly verification per ECSS-Q-ST-70-61C

Vibration testing

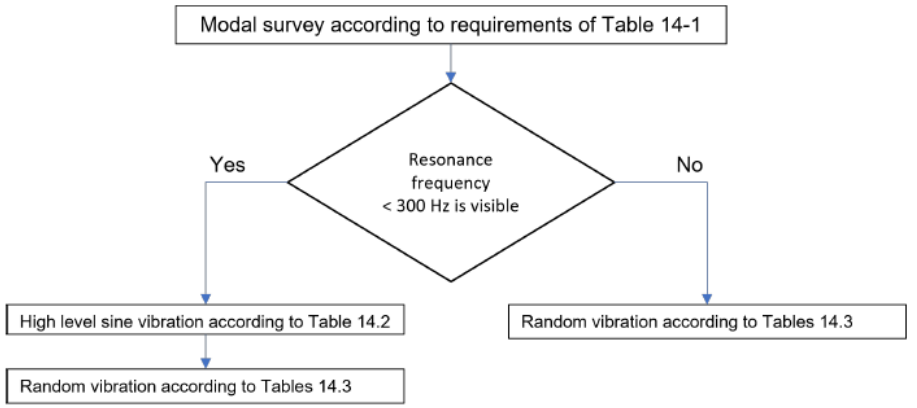


Figure 14-1:Vibration test flow chart

Table 14-1: Modal survey conditions

Table 14-1a - Sine survey		Table 14-1b - Random survey	
Amplitude	0,5 g (zero to peak)	Range (Hz)	Level
Frequency range	10 Hz to 2000 Hz	10 Hz- 2000 Hz	5,10⁻⁴ g²/Hz
Sweep rate	2 octaves/minute	Global levels: 1 g r.m.s.	
Direction	X, Y and Z axis	X, Y and Z axis	1 min/axis
		Frequency sampling = 2 Hz	

ECSS-Q-ST-70-61_1510983

Table 14-2: Minimum severity for sine vibration testing

	Axis	Frequency range [Hz]	PSD level (zero to peak)	Sweep rate [oct/min]
Spacecraft	All	25 - 100	25 g	1
		100 - 200	15 g	1
	Duration: 1 cycle up from 25 Hz to 200 Hz			
Launchers	All	10 - 16	10 mm	1/3
		16 - 60	10 g	1/3
		60 - 70	22,5 g	1/3
		70 - 200	22,5 g	2
		200 - 2000	10 g	2
	Duration: 1 cycle up from 10 Hz to 2000 Hz			

ECSS-Q-ST-70-61_1510984

Table 14-3: Minimum severity for random vibration testing

	Axis	Frequency range [Hz]	PSD level	Global level [g r.m.s.]
Spacecraft	Parallel to PCB	20 - 100	+ 6 dB/oct.	27,1 g r.m.s.
		100 - 800	0,5 g²/Hz	
		800 - 2000	- 3 dB/oct.	
	Perpendicular to PCB	20 - 100	+ 6 dB/oct.	28,5 g r.m.s.
		100 - 500	1,0 g²/Hz	
		500 - 2000	- 6 dB/oct.	
	Duration: 5 minutes per axis			
Launchers	All	20 - 60	+ 3 dB/oct.	20,0 g r.m.s.
		60 - 1000	0,27 g²/Hz	
		1000 - 2000	- 6 dB/oct.	
	Duration: 5 minutes per axis			

Assembly verification per ECSS-Q-ST-70-61C

14.9 Mechanical shock

ECSS-Q-ST-70-61_1510985

Mechanical shock test shall be performed in assembly verification for area array components in accordance with requirements in clause 13.3, for solderless assemblies in accordance with requirements in clause 13.6 and for the following components: 1. Relay
2. Quartz
3. Magnetic components (RM)
4. Transformer and self
5. Hybrid
6. Tantalum capacitor
7. Heavy or large component
8. Optical components
9. Low insertion force DIP socket
10. Semiconductors (IC) components, Hybrid components, relays, capacitors with cavities

NOTE The list of components is taken from Table 17-1 of ECSS-E-HB-32-25A (14July2015) that is reproduced in this Standard as Table 14-4.

ECSS-Q-ST-70-61_1510986

For components listed in requirement 14.9a, assembly verification shall be made with functional testing to be capable to identify degradation due to shock tests.

ECSS-Q-ST-70-61_1510987

The levels and duration of the shock shall be provided in the verification report.

Assembly verification per ECSS-Q-ST-70-61C

13.3 Special verification testing for ceramic area array components

ECSS-Q-ST-70-61_1510860

The assembly verification of ceramic AADs shall be divided in the following 2 (two) steps, as shown in Figure 13-3. 1. Demonstration of capability in accordance with clause 13.3.2, and

2. Demonstration of electrical integrity in accordance with clause 13.3.3.

NOTE 1 Once the capability samples show a satisfactory result the verification of AAD can commence.

NOTE 2 Capability samples can be excluded from the programme if the supplier can demonstrate previous verification heritage.

ECSS-Q-ST-70-61_1510861

The capability and verification samples shall be representative of the FM hardware.

NOTE For example, PCB build-up and size, mechanical fixation, component packages.

NOTE It is recommended to have a successful IST test on PCB to avoid failing the assembly verification due to damaged PCB.

Assembly verification per ECSS-Q-ST-70-61C

13.3 Special verification testing for ceramic area array components

ECSS-Q-ST-70-61_1510862

The PCB material, footprint, via technology used for the capability and verification samples shall be the same and interconnection similar as the ones used for the FM hardware.

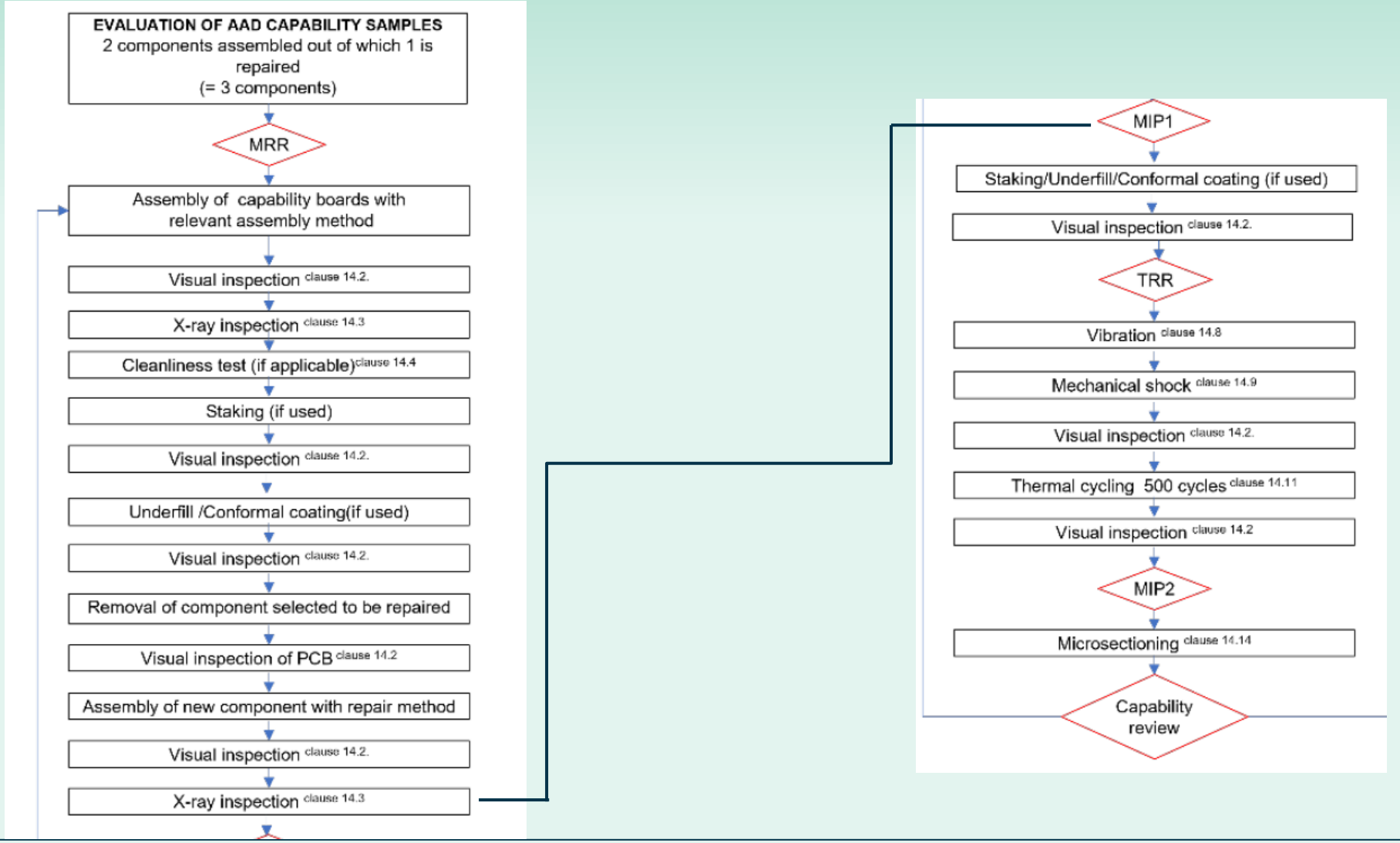
NOTE HDI, blind via and buried via are different types of via technologies.

ECSS-Q-ST-70-61_1510863

The verification shall be performed with daisy chain components to demonstrate a reliable electrical function of the PCB and the package interface throughout the environmental test campaign.

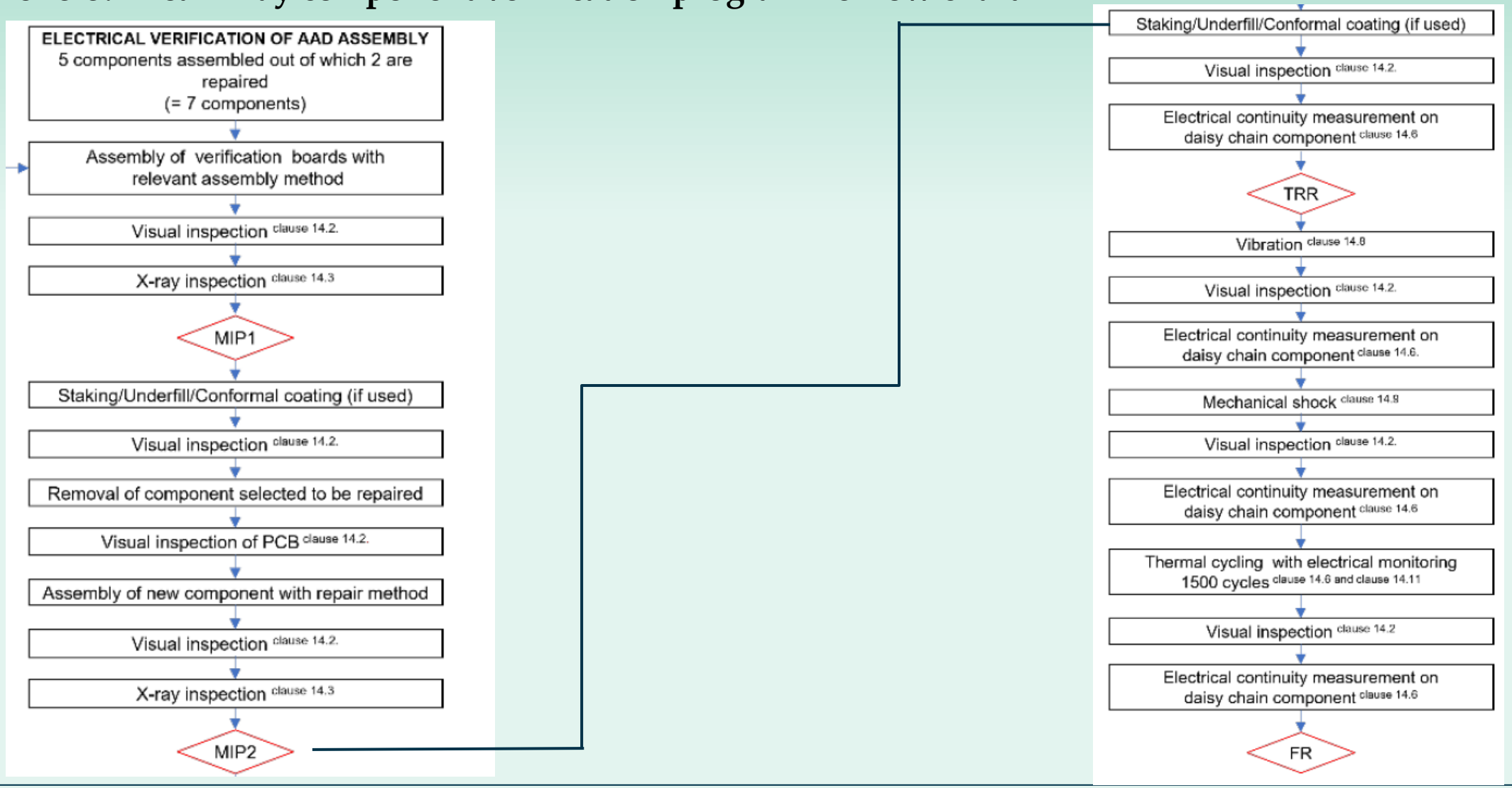
Assembly verification per ECSS-Q-ST-70-61C

Figure 13-3: Area Array component verification programme flow chart



Assembly verification per ECSS-Q-ST-70-61C

Figure 13-3: Area Array component verification programme flow chart



Assembly verification per ECSS-Q-ST-70-61C

13.6 Verification for solderless process

ECSS-Q-ST-70-61_1510906

The verification of solderless process shall be performed on flight representative assembly configuration in accordance with Figure 13-5.

NOTE Representative assembly configuration includes elements for thermal dissipation configuration.

ECSS-Q-ST-70-61_1510907

The verification tests shall be performed to show absence of degradation within the solderless interconnection part, PCB and component during all ground and in-orbit mission.

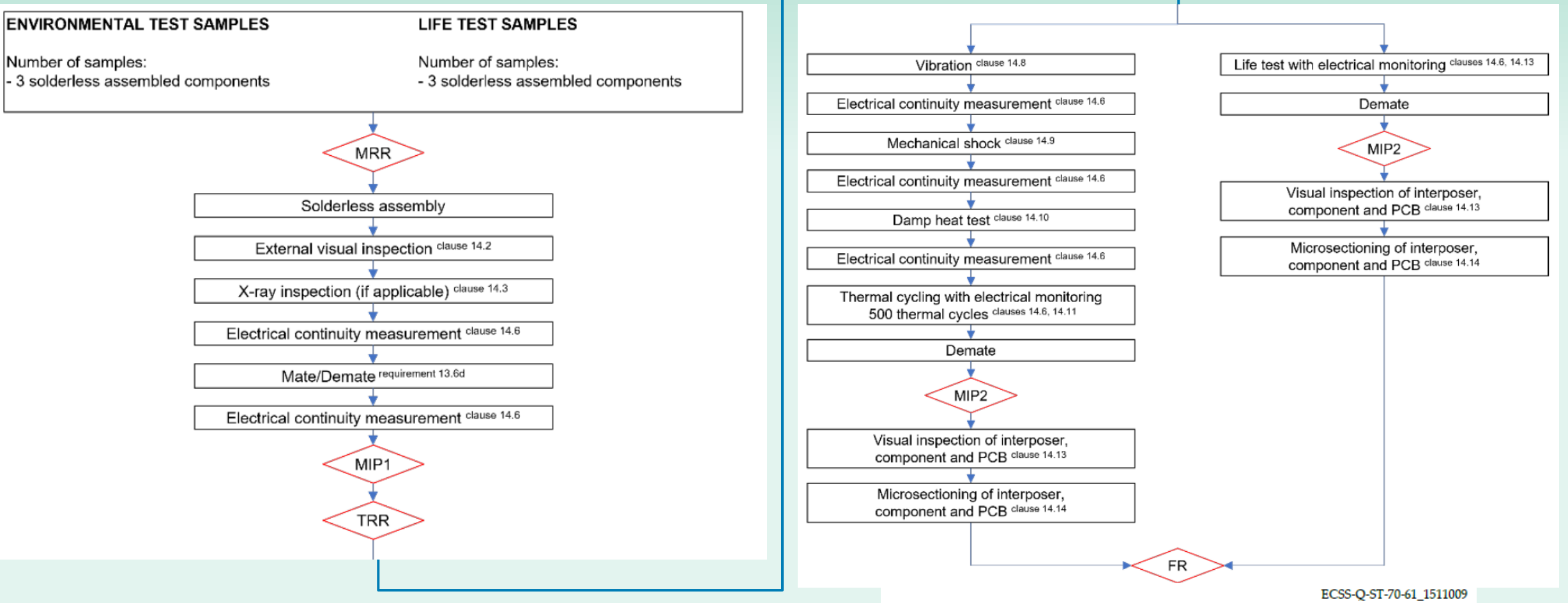
NOTE Possible degradations can be creeping of the spring, fretting degradation of the contact.

ECSS-Q-ST-70-61_1510908

6 (six) components shall be assembled with the same mechanical configuration as flight model.

Assembly verification per ECSS-Q-ST-70-61C

Figure 13-5: Verification procedure for solderless technology



ECSS-Q-ST-70-61_1511009

b. Life test conditions shall be 2000 hours at 125 °C or at maximal operational temperature during flight mission.

Assembly verification per ECSS-Q-ST-70-61C

14.15.1 Microsection facilities

The Approval Authority shall make available a list of laboratories available to perform microsection.

NOTE The list of available laboratories is on ESCIES website, see www.escies.org, Technologies - ESA SMT Verification: ESA-TECMSP-MO-013165 “ESA recommended microsectioning facilities”.

ECSS-Q-ST-70-61_1511018

Microsections shall be performed by a laboratory specified in 14.15.1a except the case specified in the requirement 14.15.1c.

Paragraph 14.15.3 details the Microsection acceptance criteria

The integrity of the assembly shall be assessed by microsectioning.

NOTE Integrity covers PCB, solder joints, adhesives and packages.

ESA recommended microsectionig facilities

-SPUR in UK

-Serma in France

-ZVE in Germany

-IIS in Italy

-Elemca in France

-Hytek in Denmark

-Alter in Spain

-ASP in Germany

ITR in Poland under evaluation

Assembly verification per ECSS-Q-ST-70-61C

Approved Summary Table

Component family	Package	Manufacturer	Package dimensions	Bonding material (under component)	Staking material (edge or corner)	Termination material	Lead finish	Pitch (mm)	Nominal Termination thickness (mm)/ Nominal width	In-House degolding / pretinning	In-house lead forming Yes/No/NA	Artificial stand-off Yes/No	Final report
Ceramic chip	C0603 Type I		Length, width	NA	NA		Sn/Pb	NA	NA	No	N/A	No	
Ceramic	C0603 Type II										N/A		
Ceramic resistor	R0805			NA	NA		Sn/Pb	NA	NA	No	N/A	No	
Diode	D5-B										N/A		
Tantalum capacitors													
IC	FP10 Bottom brazed			yes	One the side	Alloy42	Gold	1,27	0,25	yes	yes	NA	
CQFP	CQFP196 top brazed					Kovar					No		

Electronic assembly MPCB

Scope :

To check if the assembly processes and assembly configurations are verified for the mission environment

The memo ESA-TEQTM-MO-1931 iss.3 provides a checklist to be covered in this assessment

SMT Verification | ESCIES (European Space Components Information Exchange System)

To have an efficient meeting the supplier shall provide the relevant datapack in advance of the MPCB

Electronic assembly MPCB

Assessment of the vibration environment

To check that the testing of Assembly verification test vehicles envelops the response of the QM PCB(s) when subjected to the vibration loads.

This is needed not only to ensure that no undertesting was performed in evaluating past test results for a new mission environment but also to prevent the risk of overtesting when test vehicle and test level for a new verification test campaign are chosen.

Accelerated testing Norris-Landzberg

$$AF = \left(\frac{f_0}{f_t}\right)^m \left(\frac{\Delta T_t}{\Delta T_0}\right)^n e^{1414\left(\frac{1}{T_0}-\frac{1}{T_t}\right)}$$

deg C per minute
lower test temperature °C
T_t = upper temperature at test (C)
dwell time (at either extreme) mins.
total time per cycle (mins)
f_0 = frequency of cycles in operation (number per day)
f_t = frequency of cycle at test (number per day)
ΔT_t = temperature excursion at test (C)
ΔT_0 = temperature excursion at operating (C)
m = 1/3
n = 1.9
T_0 = upper temperature at operating (C)
Exponent factor = 1414 (activation energy = 0.12eV)
T_t = upper temperature at test (Kelvin)
T_0 = upper temperature at operating (Kelvin)
AF = acceleration factor

input to formula (only numbers no text) | Results

	MISSION (input from project/instrument)						Mission			Testing				
PHASE	Ext. condiitions	Unit condition	Baseplate Temperature range	PCB temp range margins included (1)	Number of cycles	Duration	MAX T (K)	Delta T	Frequency (Cycles per day	Max T (K)	Delta T	Frequency (Cycles per day	Acceleration factor	Number of test cycles
Ground ops	air	ON	+20 / +45	+20 / +70	130	24 h each cycle	343	50	1	373	155	23	4.204113851	30.92209312
Unit ground test (Acceptance)	vacuum	OFF	-35 / + 65	-35 / + 65	1	2 h dwell at max and min temp.	338	100	4	373	155	23	1.900591179	0.526152079
Unit ground test (Acceptance)	vacuum	ON	-25 / + 55	-20 / + 90	3	2 h dwell at max and min temp.	363	110	4	373	155	23	1.18881914	2.523512534
S/C ground test (non-op)	vacuum	OFF	-30 / +50	-30 / +50	1	24 hours each cycle	323	80	1	373	155	23	2.221797688	0.450085985
S/C ground test (op)	vacuum	ON	-20 / +50	-20 / +85	3	24 hours each cycle	358	105	1	373	155	23	0.86385899	3.472789004
Flight, orbit cycles (op)	vacuum	ON	-20 / +50	-20 / +85	16	30 days at max temp, six months each cycle	358	105	0.005495	373	155	23	0.152435362	104.9625214
Flight, orbit cycles (op)	vacuum	ON	-20 / +50	76 / +85	20	1 day duration (0.5days ON (HT), 0.5 day OFF (LT))	358	9	1	373	155	23	91.96906205	0.217464434
Flight, switch off, hibernation	vacuum	OFF	-30 / -20	-30 / -20	26000	6 months in total 10minutes per cycle	253	10	144	373	155	23	2032.625991	12.79133501
Cruise Phase	vacuum	OFF>ON>OFF	-30 > +20	-30 > +55	3	1 day at max, 6 months duration	328	85	0.5	373	155	23	1.470124994	2.040642811
Flight, switch off	vacuum	ON > OFF>ON	+50 > -30	+85 > -30	4	TBC (24 hours)	358	115	1	373	155	23	0.726735924	5.504062575
													Total	163.410659
													Margin	2
													To be perfromed	245.1159885

Thank You for your attention

Questions?

QR code to the questionnaire for PCB & EA training course.

Alternatively, access to the survey may be obtained using this simple URL:

https://qrco.de/pcbea

SCAN ME

Gianni.Corocher@esa.int

SCAN ME

QR code to the questionnaire for PCB & EA training course.

Alternatively, access to the survey may be obtained using this simple URL:

https://qrco.de/pcbea

SCAN ME

QR code to the survey for feedback on EMPS.

Alternatively, access to the survey may be obtained using this simple URL:

https://qrco.de/emps

What’’s next

Pb free

COTS

Modelling

Pb Free status

2018: Pb was included in the Reach Candidate list of Substance of Very High Concern for Authorization.

This event and the increase in market pressure due to the transition to Pb free already implemented by the Commercial Electronics Industry prompted the ESCC SCSB to launch a joint task force in 2019.

The task force was participated by members of the CTB and MPTB.

For electronic domain the goal of the task force was to establish a road map for the transition to Pb free.

Pb Free status

- **The Road map for the lead –free Transition of the European Space sector was issued by the task force in April 2020**

- **The Transition Roadmap is divided into 4 independent roadmaps:**
  - ***Roadmap for using COTs with the standard SnPb Assembly Process on standard leaded PCBs*. This is very urgent to allow a widespread introduction of COTs in Space Programmes.**
  - ***Roadmap for using lead-free PCBs with the standard SnPb Assembly Process*. This is also urgent since related to the use of high pin-count ICs**

Pb Free status

- ***Roadmap for the introduction of lead-free solder alloys***. **For this Roadmap it has been assessed that:**
  - ***In the short term (< 5 years): no risk associated with regulation or obsolescence of SnPb solder***
  - ***In the medium term (< 10 years): very low risk from Regulation and very low risk associated with SnPb solder obsolescence***
  - ***In the long term (> 10 years): low risk from the Regulatory side and potential risk associated with SnPb materials obsolescence***

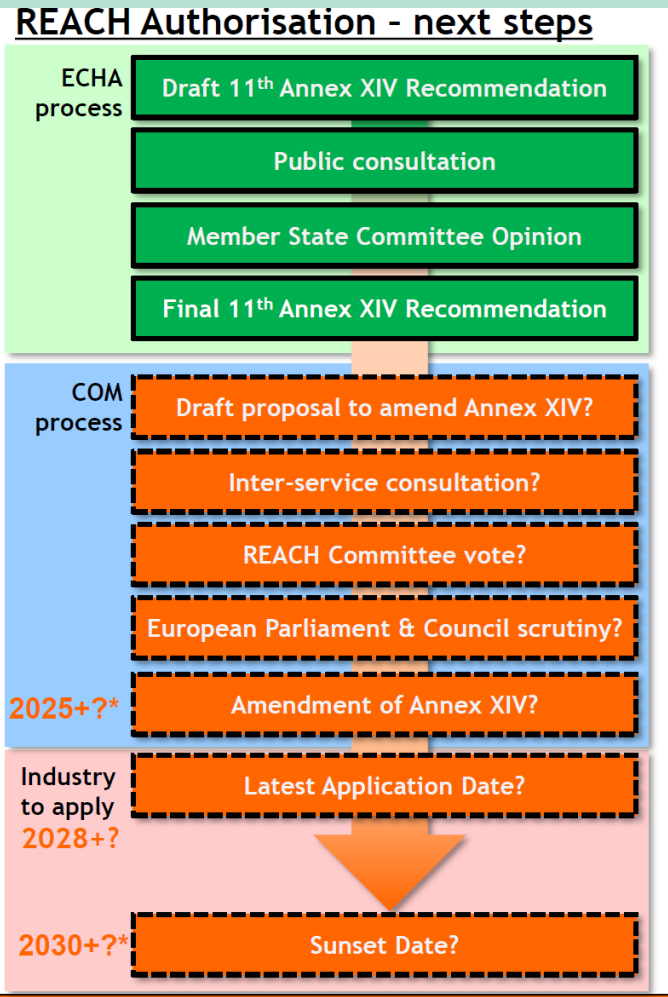
- ***Roadmap for assessment of Sn whiskers mitigation approach.***

Lead metal: Regulatory Update
Outlook of future regulation of Lead

- Current baseline: OEL revision (*COM proposal of 13.2.2023 available*) and specific REACH Restrictions

- Likelihood of REACH Annex XIV inclusion?
  - Numerous steps ahead (see diagram) - No automatism! Opposition of some key Member States, DG GROW message, ongoing baseline activities (see above)
  - Further uncertainties mainly due to REACH Revision (incl. Authorisation & Restriction Reform)

- *In case* of Annex XIV inclusion w/o exemption: Good case for authorisation of space applications without alternatives could be made, but **disproportionate impact and efforts expected** (up to 200+ AfAs for soldering only)

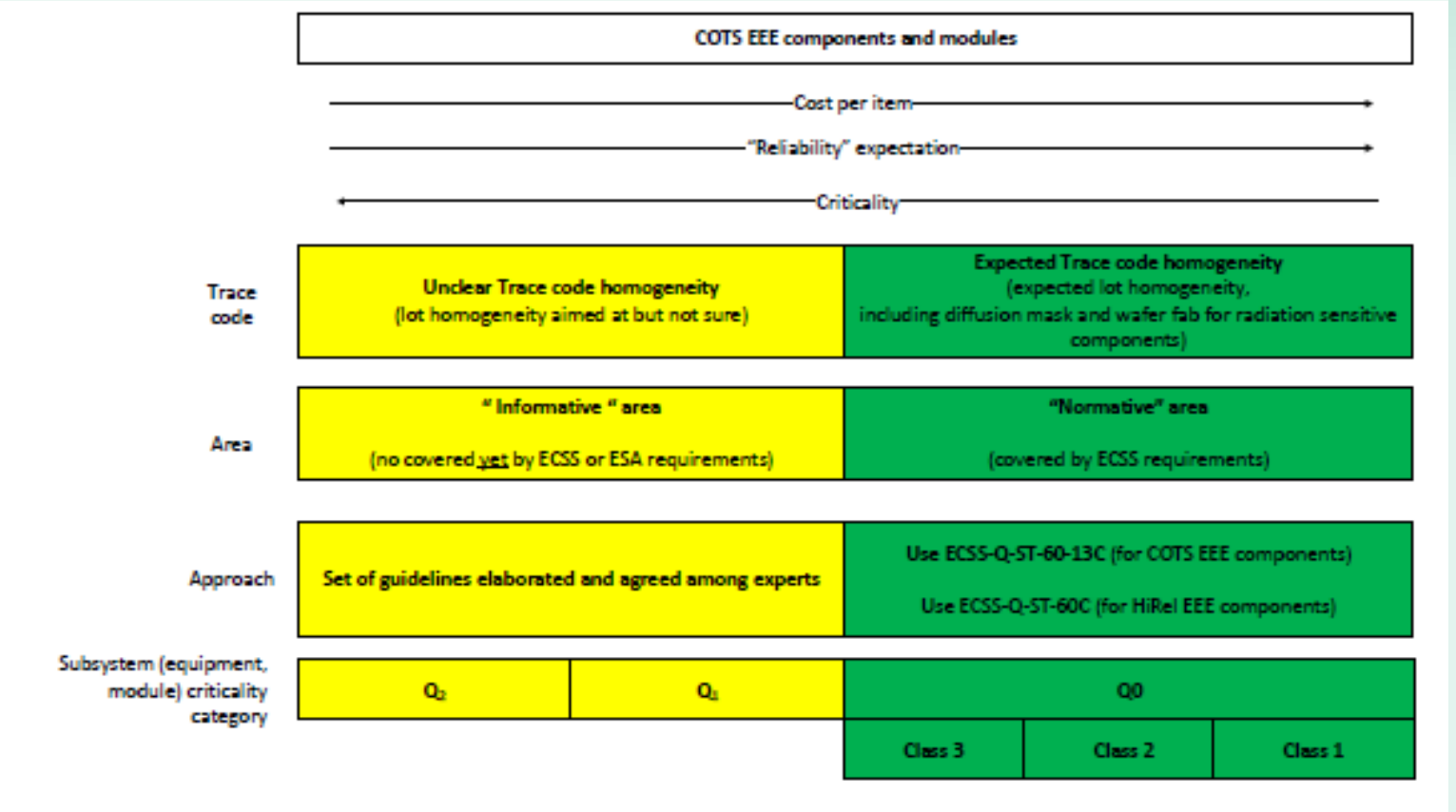


COTS

How the use of COTS is addressed in ESA?

- **Internal Working Group established in 2019 which involved different disciplines and assess possible approach to use of COTS:**
- **Technical Note ESA-TEC-TN-021473 Guideline document issued in 2022:**
- **“Guidelines for the utilization of COTS components and modules in ESA”**
- **OSIP campaign started in 2020**

COTS


COTS EEE components and modules
Cost per item
"Reliability" expectation
Criticality
Trace code
Unclear Trace code homogeneity
(lot homogeneity aimed at but not sure)
Expected Trace code homogeneity
(expected lot homogeneity,
including diffusion mask and wafer fab for radiation sensitive components)
Area
" Informative " area
(no covered yet by ECSS or ESA requirements)
"Normative" area
(covered by ECSS requirements)
Approach
Set of guidelines elaborated and agreed among experts
Use ECSS-Q-ST-60-13C (for COTS EEE components)
Use ECSS-Q-ST-60C (for HiRel EEE components)
Subsystem (equipment, module) criticality category
Q3
Q1
Q0
Class 3
Class 2
Class 1

Recommendations for PCBs assessment for COTS modules:

ANNEX 5, RECOMMENDATIONS FOR PCBS FOR CATEGORY Q1

The approach for assessment of PCBs used for COTS module of category Q1 is given by the following recommendations.

1. Printed Circuit Boards (PCB) should be procured as per IPC-6012ES, or ECSS-Q-ST-70-60.
   a. Any proposal that this quality class can be further lowered to IPC-6012E class 3 should be submitted for approval by ESA.
2. PCB manufacturers should be listed on the IPC QML or, alternatively, PCB manufacturers may hold a qualification from its customer as per IPC-6012ES, of from ECSS or NADCAP. This should be reviewed by the Satellite or Instrument Prime and their supplier during the equipment selection process (EQSR).
3. The design of the PCB and coupons should be compliant to IPC-2221B.
4. RF PCBs should be as per IPC6018CS.
5. The surface finish should be reflowed SnPb, ENIG or ENEPIG/ENIPIG. Solder mask may be used when this is technically required.
6. Hypercorrosion of ENIG should be evaluated to be in compliance with level 0 or level 1 as per IPC-4552. It is recommended that the PCB customer assesses the compliance of the PCB manufacturer to individual requirements from IPC-4552 for ENIG and IPC-4556 for ENEPIG/ENIPIG and that the compliance is reviewed by the Satellite or Instrument Prime. Note that "ESA-TECMSP-MX-11320 Checklist for ENIG ENEPIG ENIPIG finish" is available on www.escies.org/pcb/ to support such review.
7. The shelf-life of ENIG should be a maximum 6 months, otherwise a re-life test should be performed.
8. Particular care should be paid if state-of-the-art PCB technology is used. Examples are rigid-flex, microvias,back-drilling, metal core, 3-ounce (75 micron) copper foil or thicker, embedded film passives. It is recommended to use an aspect ratio for vias of max 7. In case microvias are used, it is recommended to use an aspect ratio of max 0.7 and not to stack them.
   An assessment of any possible use of state-of-the-art PCB technology and risk mitigations (such as test, inspection) should be submitted to ESA for review and approval.
9. It is recommended NOT to use tented vias (covered with solder mask) or blind vias with depth-controlled drilling (however, depth-controlled back-drilling for RF purpose is acceptable).
   Any use of the non-recommended technology should be described and submitted to ESA for review and approval.
10. It is recommended to use polyimide materials for the PCB. When using epoxy/FR4 laminate materials, they should have high temperature of glass transition (HTg FR4).
11. It is recommended that the PCB customer and the PCB manufacturer hold an MRR for the review of build-up, lay-out, panelisation, coupons, risk factors, compliance to release standard and compliance to capability.
12. All materials (PCB dielectric, solder mask, conformal coating, etc) should meet outgassing requirements.
13. IST coupons should be implemented for rigid-flex and micro-vias, back-drilling and high aspect ratio and should be tested in accordance with section 9.5.5 of ECSS-Q-ST-70-60.
14. All technology covered and not covered by IST should be specified and submitted to ESA for review and approval.
15. The PCB customer should perform incoming inspection of each batch covering the following:
    i. Review of CoC,
    ii. Microscopic inspection on coupons and
    iii. Visual inspection of all PCBs.
16. It is recommended to perform third-party evaluation of microsectioned coupons by an independent, IPC certified test lab.
17. The aspects of the incoming inspection of bare PCBs should be described in the appropriate documentation, including an assignment of the responsible institutes for these tasks, and submitted to ESA for review and approval.
18. High resistance electrical test with 1GOhm threshold is recommended and signature comparison should not be done
19. It is recommended to use 3x thermal shock (solder bath float at 280degC) for evaluation of coupons, instead of 1x.
20. In case microsectioning is already performed for evaluation of the assembly, as described in the table from annex 6, the evaluation of such microsectioning should also cover for an assessment of the quality of the PCB after test.

COTS

For electronic assembly the assessment depends on the category and on:

Designed modules: custom design for a specific (space) application

vs

Procured modules: already existing design and series production for high Rel application (defense, aeronautic)

And

Single use on a specific project: one batch of manufacturing

vs

Serial use (Constellation): series manufacturing

Annex 6: Guidelines for Electronic Assembly

The approach for assembly processes of COTS is provided by the following recommendations:

1. Use of Pb free solder alloys for category Q1 is not recommended. In case Pb free assembly processes are used the verification activities defined in Table 2 might be different. A dedicated Pb free assembly plan should be provided by the supplier.
2. Use of Pb free solder alloys for category Qo is not allowed .
3. For categories Q1 and Qo class3: companies which have assembly processes compliant to ECSS standards should apply the ECSS workmanship standards.
4. For categories Q1 and Qo class3: workmanship standards per J-STD-001G Space addendum should be applied for companies with assembly processes not in compliance with ECSS standards.
5. Assembly on SnPb finished PCB is preferred, assembly on ENIG or ENIPIG/ENEPIG finishes is allowed
6. GEIA-STD-0005-02 should be applied for managing the risk associated with pure Sn finish.(for Q1 control level 2B may be applied, for Qo control level 2C)
7. Verification of the assembly reliability should be demonstrated as follow (tailoring being possible based on criticality of the unit considered):

    a. Review of procedures for compliance to the declared standard (ECSS or J-STD-001+ Space Addendum)
    b. Visit of manufacturing line by customers
    c. Inspection of available HW (recurrent unit already in manufacturing) to identify possible "show stoppers" (lack of de-golding on components, "risky" assembly configuration....)
    d. Review/definition of manufacturing process parameter control (statistical process control)
    e. For procured modules review of the failures and return from the field data.
    f. The assessment of the reliability of the assembly using SnPb solder alloys is based on functional testing at module level following one of the approaches described in Table 2.
    g. Assessment of results of the verification testing
    h. Identification of corrective action/improvement when necessary
    i. Review/Update of the statistical process control strategy
    j. MIP of test vehicles and of Flight Models to be attended.

Verification activities might be invalidated and require repetition in case of changes of design, processes, materials or changes in the components manufacturing/procurement
For modules of category Qo Class 1 and 2 the requirements of ECSS-Q-ST-70-38C ([32]) are applicable.

COTS

Application	Class	Designed modules	Procured modules (large volume of manufacturing)
One use single batch of procurement	Q2	No reliability testing of assembly	No reliability testing of assembly
	Q1	Annex 6 par. 7a,7b,7c,7d, 7f: vibration, shock, thermal cycling **3x mission time or equivalent to 200 thermal cycles** (-55/+100C) whichever is the maximum. Test vehicle to include repair configuration for selected type of devices. **Assessment by full functional test at RT, hot and cold.** Microsectioning may be applied to assembly sensitive devices or parts tested in a statistically non significative amount. Annex 6 par. 7g,7h,7i,7j,	Annex 6 par. 7b,7c,7d,7e 7f: vibration, shock, thermal cycling **3x mission time or equivalent to 200 thermal cycles** (-55/+100C) whichever is the maximum. Test vehicle to include repair configuration for selected type of devices. **Assessment by full functional test at RT, hot and cold.** Microsectioning may be applied to assembly critical devices or parts tested in a statistically non significative amount. Annex 6 par. 7g,7h,7i,7j,
	Qo cl.3	Annex 6 par. 7a,7b,7c,7d, 7f: vibration, shock, thermal cycling **3x mission time or equivalent to 200 thermal cycles** (-55/+100C) whichever is the maximum. **Assessment by full functional test at RT, hot and cold.** Microsectioning to be applied to assembly sensitive devices, parts with heat dissipation pads underneath, and parts tested in a statistically non significative amount (**<10 for chip devices <3 for other packages**). For critical devices 2 microsections. pass fail criteria for cracks in solder joints: **75%** of critical area. Annex 6 par. 7g,7h,7i,7j,	Annex 6 par. 7a,7b,7c,7d,7e 7f: vibration, shock, thermal cycling **3x mission time or equivalent to 200 thermal cycles** (-55/+100C) whichever is the maximum. **Assessment by full functional test at RT, hot and cold.** Microsectioning to be applied to critical devices and parts tested in a statistically non significative amount (**<5 for chip devices <3 for other packages**). For critical devices 1 microsections. pass fail criteria for cracks in solder joints: **75%** of critical area. Annex 6 par. 7g,7h,7i,7j,

Application	Class	Designed modules	Procured modules (large volume of manufacturing)
Series manufacturing (use in constellation)	Q2	No reliability testing of assembly	No reliability testing of assembly
	Q1	Annex 6 par. 7a,7b,7c,7d, 6f: vibration, shock, thermal cycling **3x mission time or equivalent to 200 thermal cycles** (-55/+100C) whichever is the maximum. Test vehicle to include repair configuration for selected type of devices. **Assessment by full functional test at RT, hot and cold.** Microsectioning to be applied to assembly sensitive devices (2), parts with heat dissipation pads underneath, and parts tested in a statistically non significative amount **(<10 for chip devices <3 for other packages).** pass fail criteria for cracks in solder joints: **85%** of critical area. Annex 6 par. 7g,7h,7i,7j,	Annex 6 par. 7b,7c,7d,7e 7f: vibration, shock, thermal cycling **3x mission time or equivalent to 200 thermal cycles** (-55/+100C) whichever is the maximum. Test vehicle to include repair configuration for selected type of devices. **Assessment by full functional test at RT, hot and cold.** Microsectioning to be applied to assembly sensitive devices (2), parts with heat dissipation pads underneath, and parts tested in a statistically non significative amount **(<10 for chip devices <3 for other packages).** pass fail criteria for cracks in solder joints: **85%** of critical area Annex 6 par. 7g,7h,7i,7j,
	Qo cl.3	Annex 6 par. 7a,7b,7c,7d,	Annex 6 par. 7a,7b,7c,7d,7e
		7f: vibration, shock, thermal cycling **4x mission time or equivalent to 250 thermal cycles** (-55/+100C) whichever is the maximum. Test vehicle to include rework and repair configurations. **Assessment by full functional test at RT, hot and cold.** Microsectioning to be applied to assembly sensitive devices, parts with heat dissipation pads underneath, and parts tested in a statistically non significative amount **(<15 for chip devices <3 for other packages).** For assembly sensitive devices **3** microsections pass fail criteria for cracks in solder joints: **75%** of critical area. Annex 6 par. 7g,7h,7i,7j,	7f: vibration, shock, thermal cycling **4x mission time or equivalent to 250 thermal cycles** (-55/+100C) whichever is the maximum. Test vehicle to include rework and repair configurations. **Assessment by full functional test at RT, hot and cold.** Microsectioning to be applied to assembly sensitive devices, parts with heat dissipation pads underneath, and parts tested in a statistically non significative amount **(<10 for chip devices <3 for other packages).** For assembly sensitive devices **2** microsections. pass fail criteria for cracks in solder joints: **75%** of critical area. Annex 6 par. 7g,7h,7i,7j,