Abstract of Capability Domain

Technology Specification for a Mixed Signal ASIC Based on Rad-Hard XH018 IP Library

Document No.: 7000/SPAC/IMST_RD_020, Version 1.5

Confidentiality: Public

Author: Jan Steinkamp

IMST GmbH

Carl-Friedrich-Gauss-Str. 2-4

47475 Kamp-Lintfort

Germany

Document Information

File Name	IMST_RD_020_Abstract_Capability_Domain_1V5.docx
Created	14.11.2014
Total pages	11

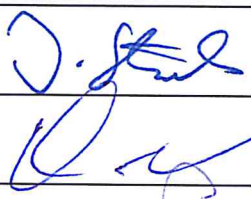
Distribution

Receiver	**Note**
ESCC Executive	DLR, Deutsches Zentrum für Luft und Raumfahrt
TESAT Spacecom	Dr. Ralf Symanczyk, Volker Lück
IMST GmbH	Internal distribution: PM, CI, QA, Commercial Manager

Version

Date	**Version**	**Author**	**Note**
06.08.2018	1.0	Johannes Borkes	Final Review and editorial corrections
17.12.2018	1.1	Jan Steinkamp	Edited after PID release
28.02.2019	1.2	Jan Steinkamp	Edited after review from ESCC Executive
20.03.2019	1.3	Jan Steinkamp	Edited after review from ESCC Executive
29.07.2020	1.4	Jan Steinkamp	Edited after review from ESCC Executive
24.01.2024	1.5	Jan Steinkamp	Changed information on LVDS speed

Release

Name	**Function**	**Date**	**Signature**
Jan Steinkamp	Programme Manager	24.01.2024	
Tobias Kleinfeld	QA (Design)	24.01.2024	
Johannes Borkes	Chief Inspector	24.01.2024	
Burak Gökgöz	ESCC Executive		

Change History

Version	**Chapter / Pages**	**Description of Changes**
0.1	All	Digital library updated and PDK update
1.2	1, 2, 3.4, 5.1	Reference to PID added, flow-chart updated, added new, addresses added
1.3	All	Editorial changes
1.4	3.6	Added more information

1.5	3.1	LVDS speed information changed to 40 MHz as tested and qualified. A note is given for a possible requalification at higher speed on demand

Contents

1 SCOPE

Scope of the capability domain is the supply chain for a RF/Mixed-Signal ASIC, based on an IP library, specially designed against radiation effects. This library is called HARD Library, derived from Hard Against Radiation by Design Library.

The capability domain is described in terms of:

- The HARD Library, which is an IMST developed IP library specially designed for products for space applications on the XH018 Process from XFAB
- The system design of the ASIC based on the HARD Library elements
- Digital circuit design based on standard library elements from XFAB tripled by an TMR script which is also part of the capability domain
- The manufacturing processes of the ASIC.
- The quality assurance procedures during design and manufacturing using the ESCC system
- The control and tests procedures which are followed in every step of the supply chain.

This supply chain begins with the customer specification and finishes with the delivery of qualified ASIC with flight module status.

Specification that details the ratings, physical and electrical characteristics and test and inspection data for an ASIC developed, fabricated and delivered within the respective Capability Domain can be found in the respective Process Identification Document (PID). The document ID is IMST_RD_000.

2 Supply Chain

Figure 2-1 shows the flow chart of the supply chain starting with the definition phase of the ASIC, followed by the different design, manufacturing and screening phases.

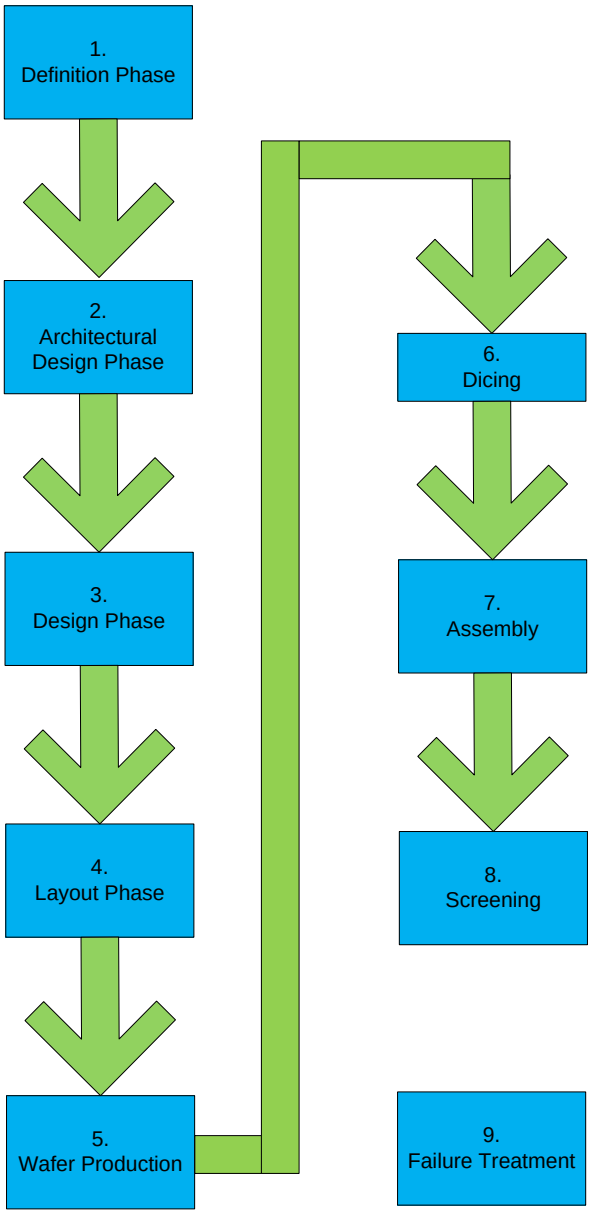


Figure 2-1: Supply Chain Flow – Overview

3 Technology Boundaries

3.1 IP Library

**Tested and thereby qualified is 40 MHz. By simulation the max. frequency is 622 MHz. A requalification is possible on demand*

Table 3-1 summarizes all IP elements provided by the HARD library with a short description of performance and the provided radiation level letter.

IP Block	Main Characteristics	Radiation level: A=300 kRad R=100 kRad
4-Wire SPI Interface	1.8V, extendible register bank with 8 register and 16 bit, each. Refresh logic for SEE mitigation implemented	A
I/O Cells	3.3V & 5.0V digital + Analog I/O, TMR In/Out	A, 5V I/O = R
LVDS Driver	1.8V, Fmax=40 MHz*	A
LVDS Receiver	1.8V and 3.3V, Fmax=40 MHz*	A
Reconfigurable Multifunctional Operational Amplifier	• Inverting OpAmp, variable gain: -10 dB…+30 dB; 1 dB step size • Non inverting OpAmp, variable gain: -10 dB…+30 dB; 1 dB step size • LPF; 3 different cut off frequencies • I/U Converter with different input ranges • Schmitt Trigger • Voltage buffer • Open Loop configuration	A
Bandgaps	1.8V & 3.3V trimable	A
Reference Bias Generators	1.8V & 3.3V with PtoPR and constant currents & adjustable voltage references	A
Temperature sensor	1.8V, temperature range from -40°C…+150°C	A
POR Generator	POR delay: 5µs	A
LDO	Input voltage: 3.3V Output Voltage: 1.8V with adjustable short protection, 150mA Imax	A
Level shifter High-Low	input signals with 0V…1.8V output signals with -5V…-3.2V	A
Level shifter Low- High	input signals with -5V…-3.2V output signals with 0V…1.8V	A
Digital Level shifter High-Low	3.3V-1.8V	A
Digital Level shifter Low- High	1.8V-3.3V	A
16bit MUX	Max. signal frequency: 800 MHz	A
12bit ADC	charge-scaling SAR ADC fast mode: 200 KSamples/sec.	A
12bit DAC	segmented current steering DAC	A
Trim Cell	64 bit OTP	R
Clock PLL	16 bit 2nd order SDM fractional-N divider period jitter: 50ps (PK-PK)	R
DCXO	Supports 5 MHz … 50 MHz crystals	A
VCO with frequency divider bank	VCO frequency from 80 MHz – 600 MHz Divider bank ration from 1 to 128	A

**Tested and thereby qualified is 40 MHz. By simulation the max. frequency is 622 MHz. A requalification is possible on demand*

Table 3-1: IP Library Summary Table

3.2 Standard cells

The Capability Domain makes use of the standard digital libraries from XFAB with the names: D_CELLS_JI and D_CELLS_JI3V. For digital logic all provided cells are allowed. For SEE mitigation a TMR script will be executed to triple the digital logic. The TMR script is part of the domain.

3.3 Supply voltage range

Standard core voltage is 1.8V and I/O voltage is 3.3V. For special applications 5V I/Os are also provides. The following table lists the allowed voltage range for the different supply domains:

- 1.8 V supply range from 1.62 V to 1.98 V
- 3.3 V supply range from 3.0 V to 3.6 V
- 5.0 V supply range from 4.5 V to 5.5 V

3.4 Semiconductor technology

The baseline of the designed HARD IP Library elements are the junction isolated transistors. Figure 3-1 shows the cross section of these transistors as shown on the web page from XFAB. The metal stack of the XH018 technology is shown in Figure 3-2 and can also be found on the web page from XFAB as public information.

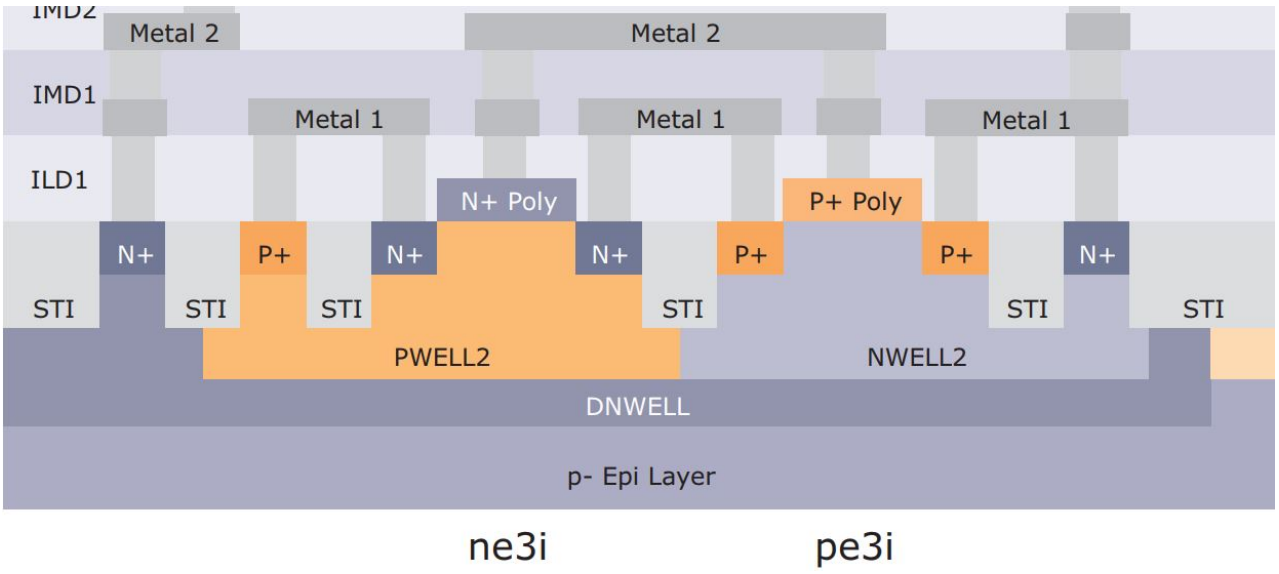


Figure 3-1: Cross section of the junction isolated transistors (Copy from XFAB web page)

XH018 METAL RESISTORS

Device	Name	Available with module	RS [Ω/ □]	Thickness [µm]	Max J/W [mA/µm]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
Metal 1	rm1	LPMOS	0.077	0.555	0.5*	3.4	45
Metal 2	rm2	LPMOS	0.074	0.565	0.5*	3.4	45
Metal 3	rm3	MET3	0.074	0.565	0.5*	3.4	45
Metal 4	rm4	MET4	0.074	0.565	0.5*	3.4	45
Metal 5	rm5	MET5	0.074	0.565	0.5*	3.4	45
Top Metal	rmtp	METMID	0.031	0.98	1.6**	3.2	45
Thick Metal	rmtpl	METTHK	0.0101	3.11	6**	3.8	45

* value quoted at Tj = -40°C ... +175°C; value for Tj = -40°C ... +125°C is 1.0 mA/µm
** value quoted for both Tj = -40°C ... +175°C and Tj = -40°C ... +125°C

Figure 3-2: Metal stack of XH018

3.5 Temperature range

The IP library elements are designed for a junction temperature range from -40°C up to +135°C with the intention to provide an operating temperature range for the packaged ASIC of -40°C up to +125°C. Maximum operating temperature is dependent on the individual power dissipation of the ASIC and the selected package type.

Maximum storage temperature is +150°C.

3.6 Radiation hardness

All IP library elements covered by this Capability Domain have been tested with respect to radiation hardness. Thorough testing was performed both for total ionizing dose (TID) and single event effects (SEE). For that purpose test samples with individual addressable IP library elements were exposed to irradiation of total dose up to 300 krad (Si) and heavy ions up to 88 MeV/mg/cm ^ 2.

TID hardness was tested in accordance with ESCC22900 and low dose rate. Hardness is demonstrated up to 300 krad for most IP elements with limitations to 100 krad for some IP elements. Table 3-1 lists the possible radiation level letter for each IP. If any ASIC will contain IPs with different radiation level letter, the lowest level will determinate the ASIC specification with respect to TID hardness.

Irradiation with heavy ions was performed in accordance with ESCC25100 and using different types of ions up to a maximum LET of 88.4 MeV/mg/cm ^ 2. No destructive SEL or SEU was observed. SETs have been registered and cross sections have been calculated for all individual IP elements.

The results of the radiation testing is documented in test-reports for TID and SEE, respectively. These generic reports are available on request from IMST. Lot specific TID testing will be performed in case of ASICs with radiation hardness letter.

3.7 Package variants

Five different package variants are offered and listed in Table 3-2.

Variant Number	Pin count	Pitch leads [mm]	lead width [mm]	edge length ceramic [mm]	min die size pad limited [mm^2]	min die length	Cavity length [mm]	max die length [mm]	max die size [mm²]
01/06/11	256	0.5	0.2	36	58.4	7.64	11.6	10.1	102.8
02/07/12	208	0.5	0.2	29.21	39.9	6.32	10.3	8.8	77.8
03/08/13	132	0.635	0.2032	24.13	17.9	4.23	8.2	6.7	45.3
04/09/14	64	0.635	0.2032	14.5	5.6	2.36	6.4	4.9	23.6
05/10/15	32	0.635	0.2032	9.5	2.2	1.48	5.5	4.0	15.8

Table 3-2: Package Variants

The packages have dedicated LVDS ports with 100 Ohm controlled impedances for high speed interfaces. If no LVDS is required, these dedicated ports can be used as standard I/Os as well.

4 Design

The HARD library is a property of IMST and the ASIC design is performed usually in IMST premises, using a determined Process Design KIT (PDK) of XFAB. Therefore all design rules are described inside the specification documents for XH018 manufacturing process.

These documents are strictly confidential and are not allowed to be shared without XFABs permission.

The design concept and after that, the design and the layout of the ASIC is done by the department of Chip Design Centre (CDC) at IMST GmbH. All quality assurance and test procedures are included in the Design Flow.

IMST offers a shared design flow, where the customer can provide some digital IP by VHDL code or synthesized gate level netlist.

5 Manufacturing and screening

The capability domain contains the full production flow with wafer manufacturing, packaging and screening. Procurement of ASICs within this domain will follow the ESCC 9000.

5.1 Manufacturing Sites

Service provider	Description / Tasks	Location and Address
X-FAB	Wafer Production	X-FAB Sarawak Sdn. Bhd.1, Silicon Drive, Sama Jaya Free Ind. Zone, 93350 Kuching, Sarawak, Malaysia
X-FAB	Headquater	X-FAB Semiconductor Foundries GmbH Haarbergstr. 67, 99097 Erfurt, Germany
First-Sensor MP	Dicing	First Sensor - Microelectronic Packaging GmbH Grenzstrasse 22, 01109 Dresden, Germany
IMST	Assembly	IMST GmbH Carl-Friedrich-Gauss Str. 2-4, 47475 Kamp-Lintfort, NRW, Germany

RoodMicrotec	Wafer test and parts of the screening tests	RoodMicrotec Oettinger Str. 6, 86720 Nördlingen, Germany
RoodMicrotec	Parts of the screening tests and failure analysis	RoodMicrotec GmbH Motorstrasse 49, 70499 Stuttgart, Germany
First-Sensor Lewicki	Hermetic sealing, leakage test and laser marking	First Sensor - Lewicki GmbH Allee 35, 89610 Oberdischingen, Germany

Table 5-1: Manufacturing Sites