APPLICATION FOR ESCC QUALIFICATION APPROVAL

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Component Title: **Integrated Circuits, Silicon, Monolithic, Radiation-Tolerant 32-bit ARM Cortex-M7 Microcontroller (SAMV71RT)**

Appl. No. 389

Executive Member: CNES Date: 12/07/2024

1 Components (including series and families) submitted for Qualification Approval

ESCC COMPONENT. NO.	VARIANTS	RANGE OF COMPONENTS	BASED ON	TEST VEHICLE / S	COMPONENT SIMILAR
9512/007	01	Integrated Circuits, Silicon Monolithic, Radiation-Tolerant 32-bit ARM Cortex-M7 Microcontroller	SAMV71RT - 65K1 65nm 6 metal layers + top-metal layer Microchip proprietary technology available in UMC Singapore	SAMV71RT CQFP-144	NA

2 Component Manufacturer
MICROCHIP TECHNOLOGY NANTES

3 Location of Manufacturing Plant
LA CHANTRERIE – ROUTE DE GACHET
BP70602
44306 NANTES CEDEX

4 ESCC Specification used for Qualification
Generic: ESCC9000
Issue 11
Detail/s: 9512/007
Issue 2

5 Qualification Report Reference and date:
QP-SAMV71Q21RT.pdf
Date: 01/04/2022

6 **PID** used for manufacturing Qualification Lot
Ref No: PID0042
Issue: 0
Date: 16/05/2024

7 **PID** changes since start of qualification
None ☒
Minor* ☐
Major* ☐
(* Details not published, provided in confidential annex 2.)

8 Current **PID** Verified by D. Dangla, CNES
Name of Executive Representative
Ref No: SAMV71RT PID 0042
Issue 0
Date 16/05/2024

9 Current Manufacturing facilities surveyed by:
CNES (D. Dangla) ESA (S. Hernandez) 04/10/2023
(Name of Executive Responsible) (Date)

Report Reference
DTN QE EC-2024.0000575 CR-ESCC QML survey MCHP-04102023.pdf
Satisfactory: Yes ☒ No ☐ Explain

10 Quality and Reliability Data
Evaluation testing performed Yes ☒ No ☐
Report Ref. No.: Date:
Equivalent Data: Single Phase Qualification applies
Certification:

Failure analysis, DPA, NCCS available Yes ☒ No ☐
(supply data)
Ref Nos. and purpose:
Construction analysis reports done by MCHP/SERMA:
19-0345-100_approved.pdf (February 20th, 2019)
+ 22-2825-100 MICROCHIP_approved.pdf (July 6th, 2022)

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The undersigned hereby certifies on behalf of the ESCC Executive, that the above information is correct; that the appropriate documentation has been evaluated; that full compliance to all ESCC requirements is evidence except as stated in box 13; that the reports and data are available at the ESCC Executive and therefore applies for ESCC qualification status to be given to the component(s) listed herein.

Date: 12/07/2024

Lya Fontaine,CNES

(Signature of the Executive Coordinator)

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Continuation of Boxes above: (Only non-confidential comments)

Qualification Package SAMV71Q21RT Aerospace ARM Microcontroller family - qp-samv71q21rt.pdf
SAMV71RT ESCC QPL - submission 2024-04 rev1.pptx
SAMV71RT 32-bits Flash Microcontroller Radiation Test Report Single Event Effects & Total Ionizing Dose - rad_samv71rt.pdf

Construction analysis reports done by MCHP/SERMA:
- 19-0345-100_approved.pdf (February 20th, 2019)
- 22-2825-100 MICROCHIP_approved.pdf (July 6th, 2022)

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Non compliance to ESCC requirements:

No.:	Specification	Paragraph	Non compliance

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Additional tasks required to achieve full compliance for ESCC qualification or rationale for acceptability of noncompliance:

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Executive Manager Disposition

Application Approval: Yes ☒ No ☐

Action / Remarks:

Date:

B. Schade: Head of the Product Assurance and Safety Department

ANNEX 1: LIST OF TESTS DONE TO SUPPORT QUALIFICATION

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Tests conducted in compliance with:

- ESCC 9000 generic specification; Chart F4 (for ESCC/QPL parts);
- Or PID-TFD [redacted] (for ESCC/QML parts)

Tests vehicle identification/description:

SAMV71RT CQFP-144 ESCC 951200701E	The SAMV71Q21RT, generally named SAMV71RT, is the Radiation Tolerant version of the Microchip SAMV71Q21 Microcontroller based on the ARM® Cortex®-M7 architecture. The embedded dual CAN-FD interface and Ethernet-AVB controller provide state-of-the-art technology for high bandwidth communication. In addition to one of the most powerful Arm cores delivering 600 DMIPS, the SAMV71Q21RT features a flexible bus and memories architecture coupled with a powerful Floating Point Unit (FPU), thus providing advanced DSP and real-time capabilities to serve the most demanding space applications. The SAMV71RT die, in its hermetic CQFP-144 version, is bonded with AlSi wire. Static Burn-in does not apply. No seal test has been performed after Life-Test. Flash memory Write/Erase Endurance Cycling: Up to 10 kcycles over -40°C/125°C.

Detail Specification reference: 9512/007 issue 2

Qualification results – Environmental/Mechanical subgroup

The SAMV71RT is part of the package family "Flat-Substrate CQFP".
Environmental/Mechanical subgroup, required by ESCC every 2-years, is done every 26-weeks per package family (*).

(*) SAMV71RT package family

Flat-substrate CQFP family
- Wires: ultrasonic AlSi 18-25-32µm
- Die attach: JM7000
- Al203 body
- Seam-welded lid
- flat leads
  - min lead pitch: 0.48 mm
  - min lead width: 0.18 mm

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Chart F4	Test	Tick when done	Conditions	Assembly lot datecode	Tested Qty per lot	No. of Rejects	Comments if not performed. Comments on Rejection
Environmental/Mechanical Subgroup	Thermal Shock	☒	MIL-STD-883. Test Method 1011C	A84PNA282P-DC2220 (CQFP-064)	15	0	15 cycles
	Temperature Cycling	☒	MIL-STD-883. Test Method 1010C		(15)	0	100 cycles
	Moisture Resistance	☒	MIL-STD-883, Test Method 1004		(15)	0	
	Intermediate and End-Point Electrical Measurements	☒	3 Temperature Electrical Test		(15)	0	Device specification
	Seal (Fine and Gross Leak)	☒	MIL-STD-883, Test Method 1014		(15)	0	
	Visual Inspection	☒	MIL-STD-883, Test Method 2009	QQFGSA25S9-DC2247 (CQFP-144)	(15)	0	
	Mechanical Shock	☒	MIL-STD-883, Test Method 2002B		15	0	5 pulses
	Vibration	☒	MIL-STD-883, Test Method 2007A		(15)	0	12 sweeps
	Constant Acceleration	☒	MIL-STD-883, Test Method 2001E	A5XHZA2CR9-DC2322 (CQFP-256)	(15)	0	Y1
	Intermediate and End-Point Electrical Measurements	☒	3 Temperature Electrical Test		(15)	0	Device specification
	Seal (Fine and Gross Leak)	☒	MIL-STD-883, Test Method 1014		(15)	0	
	Visual Inspection	☒	MIL-STD-883, Test Method 2009		(15)	0	

Endurance subgroup

Note:

Life test is done on each wafer lot. Three wafer lots have been manufactured since initial qualification.

The 1st wafer lot has been submitted to extended life test, up to 4000 hours/125°C/Vccmax.

No seal test has been performed after life test.

Chart F4	Test	Tick when done	Conditions	Diffusion Lot Assembly lot Date code	Tested Qty per lot	No. of Rejects	Comments if not performed. Comments on Rejection
Endurance Subgroup	Operating Life	☒	MIL-STD-883, Test Method 1005	S8Q72 17Q4	45	0	4000 hrs/Vccmax/125°C
	Intermediate and End-Point Electrical Measurements	☒	Intermediate and End-Point Electrical Measurements in the Detail Specification		(45)	0	
	Operating Life	☒	MIL-STD-883, Test Method 1005	S8NP9 18Q4 - SGM2H 21Q2	45	0	1000 hrs/Vccmax/125°C
	Intermediate and End-Point Electrical Measurements	☒	Intermediate and End-Point Electrical Measurements in the Detail Specification		(45)	0	

Assembly capability group is verified on each assembly lot.

- Solderability test, required by ESCC, is done on each assembly lot

- Terminal strength test, required by ESCC every 2-years, is done every 26-weeks per package family(*)

Chart F4	Test	Tick when done	Conditions	Date Code Diffusion Lot	Tested Qty per lot	No. of Rejects	Comments if not performed. Comments on Rejection
Assembly Capability Subgroup	Permanence of Marking	☒	MIL-STD-883, Test Method 2015	S8Q72A288S DC2225 -- S8Q72A2AHM7 DC2252 -- A5XHQFBTAW DC2327	3#	0	
	Bond Pull test (destructive)	☒	MIL-STD-883, Test Method 2011		4#	0	22 wires
	Substrate attach strength	☒	MIL-STD-883, Test Method 2027		3#	0	
	Internal Visual Inspection	☒	MIL-STD-883 Test Method 2010A		2#	0	
	Solderability test	☒	MIL-STD-883 Test Method 2003		3#	0	22 leads
	Terminal strength test	☒	MIL-STD-883 Test Method 2004 B2	A84PNA282P-DC2220 (CQFP064) QQFGSA25S9-DC2247 (CQFP144) A5XHZA2CRx-DC2322 (CQFP-256)	3#		45 leads

Chart F4	Test	Tick when done	Conditions	Date Code Diffusion Lot	Tested Qty	No. of Rejects	Comments if not performed. Comments on Rejection
Additional Tests	HBM ESD	☒	MIL-STD-883 Test Method 3015	SWMJGAANA3	3#	0	Ok up to 3000V
	CDM ESD	☒	JESD22-C101	SWMJGAANA3	3#	0	Ok up to 750V, Corner pins: up to 2000V, 0/3
	Electrical latch-up	☒	JESD78	S8Q72A22XY	6#	0	Current injection 100mA, Overvoltage 1.5*Vccmax, 125°C
	Flash memory Write/Erase Endurance Cycling	☒	MIL-STD-883 Test Method 1033	S8Q72 (S8Q72A22TZ DC1810)	77# 77# 77# 77# 77# 77#	0 0 0 0 0 0	Step: Endurance 125°C: 10 kcycles Elect. test 3-temp: -40/25/125°C Endurance 25°C: 10 kcycles Elect. test 3-temp: -40/25/125°C Endurance -40°C: 10 kcycles Elect. test 3-temp: -40/25/125°C
	Data Retention	☒	JESD22A117	S8Q72 (S8Q72A22XF DC1833)	77# 77# 77# 77#	0 0 0 0	Step: 700 hours: 250°C Electrical tests: 25/125°C 1000 hours: 250°C Electrical tests: 25/125°C Note: Assuming an activation energy of 0.7 eV, 1000h/250°C is equivalent to a lifetime of 15 years at 125°C or 140 years at 85°C.
	Pre seal & Post seal / Burn-in Die attach strength	☒	MIL-STD-883 Test Method 2027	S8Q72FBT3P S8Q72A2CNF S8Q72A25WS S8Q72A288S S8Q72A2AHM7 A5XHQFBTAW	3# 3# 3# 3# 3# 3#	0 0 0 0 0 0	Ok, all values results from B or C failure modes.
	Pre seal & Post seal / Bond Pull test	☒	MIL-STD-883, Test Method 2011	S8Q72FBT3P S8Q72A2CNF S8Q72A25WS S8Q72A288S S8Q72A2AHM7 A5XHQFBTAW	2+4# 2+4# 2+4# 2+4# 2+4# 2+4#	0 0 0 0 0 0	Since initial qualification, bond pull test is run: At precap inspection step: 2 parts, 100% of wires At Group B: 22 wires over 4 parts Ok, all values results far from limit acceptance, show only failure modes 2-3 or 4: no lift, no fracture
	Bond Pull test results after Life-Test 500hrs/150°C	☒	MIL-STD-883, Test Method 2011	S8Q72FBT3P S8Q72A2CNF S8Q72A25WS S8Q72A288S S8Q72A2AHM7 A5XHQFBTAW	4# 4# 4# 4# 4# 4#	0 0 0 0 0 0	Sampling 100% of wires over 4 parts Ok, all values results far from limit acceptance, show only failure modes 2-3 or 4: no lift, no fracture
	TID	☒	ESCC22900	S8Q72A22ZS (wafer lot S8Q72) (22 biased parts and 5 unbiased parts)	27#	0	30 krad(Si) with NVM in Read mode 25 krad(Si) in write-in-flight operation
	SEL	☒	JESD57, ESCC25100	AF5QB00000 (wafer lot SWMJG)	3#	0	Note: For SEU/SEFI, refer to "rad_samv71rt.pdf" rad test report

NOTES ON THE COMPLETION OF THE APPLICATION FORM FOR ESCC QUALIFICATION APPROVAL

ENTRIES

Form Heading	shall indicate:— the title of the component as given in its detail specification or the name of the series or family; — the entering date; — the serial number and the suffix of the form.
Box 1	shall provide details given in table; in particular there shall be listed - the variants or range of variants; the range of components by using the ESCC code for values tolerances, etc.; the designation given in detail specification as 'based on'; -—under Test Vehicle enter either a cross or the specific characteristic capable to identify the component tested; — under component similar enter a cross.
Box 2 and 3	Manufacturer's name and location of plant where the components were manufactured and tested.
Box 4	Generic and detail specifications used during qualification program.
Box 5	Reference to test report(s) submitted in support of application.
Box 6	Enter details to identify the PID that was applicable at the time the qualification lot was manufactured.
Box 7	If the PID was evolved after qualification lot manufacture, adequate details of such evolution shall be provided together with reasons for changes. Major changes shall be clearly marked.
Box 8	The box serves to identify the current PID and the Executive Representative that has verified it together with the date of this occurrence.
Box 9	This box can be completed only after a physical visit to the plant to confirm that the practices, procedures, materials, etc. used in manufacturing the components are as described in the PID. This survey shall be carried out in accordance with the requirements of ESCC Basic Specification No. 20200 and its findings shall be recorded.
Box 10	Details entered shall be sufficient to evidence that an evaluation program according to ESCC Basic Specification No. 22600 has been performed and that the results thereof are summarized in the survey and test reports. If the evaluation program has not been carried out according to established ESCC documents, the applicant Executive Representative shall provide alternative data and declare its assessed degree of satisfactory compliance with the ESCC basic requirements. Reference shall be made to the reports on Destructive Physical Analysis (DPA), Failure Analysis and Non conformance (NCCS) issued during the Evaluation and/or Qualification Phase.
Box 11	Enter the name of the Executive Coordinator and the signature.
Box 12	To be used when there is a need to expand any of the boxes from 1 through 10. Identify box affected and reference the Box 12 in the relevant Box. Box 12 can be broken into 12a, 12b, etc. if several Boxes have to be expanded.
Box 13	Fill table as requested.
Box 14	Fill in any additional tasks required to achieve full compliance.
Box 15	All Executive recommendations on the application itself, special conditions or restrictions, modifications of the QPL or ESCC QML entry, letters to the manufacturer, etc. shall be entered clearly in Box 15, signed by the ESA Representative.
Box 16	Fill in Table as requested.
Box 17	Confidential details of PID changes shall be provided.
Box 18	State noncompliance with reference to specification(s) and paragraph(s). To simplify reference in Box 18 each nonconformance shall be sequentially numbered. If relevant state 'None'
Box 19	Any additional action deemed necessary by the Executive Representative to bring the submitted data to a standard likely to be accepted by the ESCC Executive should be listed herein or the reason(s) to accept the nonconformance.
Box 20	Additional Comments