		APPLICATION FOR EXTENSION OF ESCC TECHNOLOGY FLOW APPROVAL			Page 1 Appl. No. 381A	
Component Title: Integrated Circuits, Silicon, Monolithic, CMOS Radiation Hardened 65nm ASIC Platform, based on type C65Space		Executive Member: CNES		Date: 19/02/2025		
Technology Flow submitted for Extension of Qualification Approval: 1						
SUMMARY DESCRIPTION		TEST STRUCTURES		COMPONENTS PROPOSED FOR QUALIFICATION		
ST C65SPACE ASIC platform technology		NX1H35AS in CQFP-352 package (NG-MEDIUM)		Integrated Circuits, Silicon Monolithic, 35KLUT Radiation-Hardened FPGA based on NanoXplore architecture		
Component Manufacturer STMicroelectronics 2		Location of Manufacturing Plant(s) 3 NanoXplore (design) ST Crolles (foundry) Chipbond Taiwan (OPM (Over Pad Metallization)) ST Rennes (assembly) ST Grenoble (test) ST Grenoble + ST Rennes (space qualification)		Date of original qualification approval: 4 Date: 31/08/2022 Certificate Ref No. 381		
ESCC Specifications used for Maintenance testing: 5 Generic: 9000 Issue: 11 Detail(s): 9202/086 Issue: 2		Deviations to LVT testing and Detail Specification used: 6 No <input checked="" type="checkbox"/> Yes <input type="checkbox"/> (supply details in Box 15) Deviation from current Specifications: No <input checked="" type="checkbox"/> Yes <input type="checkbox"/> (Supply details)		Qualification Extension Report reference and date: 7 "VOQ_2022_2024_C65SPACE_NX1H35AS-v2.pdf" document and associated reports		
Summary of procurement or equivalent test results during current validity period in support of this application (those to ESCC listed first) 8						
Customer	Component	LVT	Date code	Quantity Delivered		
See Qualification Extension report						
		-				
PID changes since last maintenance of qualification 9 None <input type="checkbox"/> Minor* <input checked="" type="checkbox"/> Major* <input type="checkbox"/> *Provide details in box: <div style="border: 1px solid black; padding: 2px; width: 100px; margin-top: 5px;">19</div>		Current PID Verified by: CNES 10 Name of Executive Representative Ref No: ST012008 ESCC PID GENERIQUE (8097046.pdf) Ref No: PID for ASICs C65S WB and FC (DM00508779.pdf) ST Crolles PID (DM00408351.pdf) Chipbond Wafer Specification (DM00593640.pdf) Dice Layout PID (DM00508782.pdf)				
Current Manufacturing facilities surveyed by: ESA and CNES on 12/07/2023 11 (Name of Executive Representative) (Date)						
Satisfactory: Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> Explain MoM Quality Meeting held on the 12th of July 2023 (B2015)						
Report Reference: CR-Activités ST Juillet 2023						

	<p align="center">APPLICATION FOR EXTENSION OF ESCC QUALIFICATION APPROVAL</p> <p>Component title: Integrated Circuits, Silicon, Monolithic, CMOS Radiation Hardened 65nm ASIC Platform, based on type C65Space</p> <p>Executive Member: CNES Date: 19/02/2025</p>	<p align="center">Page 2</p> <p align="center">Appl. No.</p> <p align="center">381A</p>
<p>Failure Analysis, DPA, NCCS available: Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> (Supply data)</p> <p>Ref. No's and purposes: NCCS 2CSTM301 - ESA Logo – CLOSED NCCS 2CSTM401 - TID RAD LETTER MARKING – CLOSED NCCS 2CSTM402 - NG-Medium Qualified Flow Issue – CLOSED</p>		
<p>The undersigned hereby certifies on behalf of the ESCC Executive - that the above information is correct; - that the appropriate documentation has been evaluated; - that full compliance to all ESCC requirements is evidence (except as stated in box 15;) - that the reports and data are available at the ESCC Executive and therefore applies on behalf of CNES as the responsible Executive Member for ESCC qualification status to be extended to the component(s) listed herein.</p> <p>Date: 19/02/2025</p> <div style="display: flex; justify-content: space-between; align-items: center;"> <div data-bbox="883 548 1078 630"> <p>Fontaine Lya</p> <p><small>Signature numérique de Fontaine Lya Date : 2025.02.19 15:23:30 +01'00'</small></p> </div> <div data-bbox="1117 564 1463 619"> <p align="center">L. FONTAINE, CNES</p> <p align="center">(Signature of the Executive Coordinator)</p> </div> </div>		
<p>Continuation of Boxes above:</p> <p>Box 7: "VOQ_2022_2024_C65SPACE_NX1H35AS-v2.pdf" document and associated reports: 8097046.pdf (ESCC PID GENERIQUE) DM00508779.pdf (PID for ASICs C65S WB and FC) DM00408351.pdf (ST Crolles PID) DM00593640.pdf (Chipbond Wafer Specification) DM00508782.pdf (Dice Layout PID) esc9304010iss4.pdf (ESCC Detail Specification No. 9304/010) (NG-Medium Product) esc9202086iss2.pdf (ESCC Detail Specification No. 9202/086) (Technology Flow ST CMOS RH 65nm ASIC PLATFORM) DC2414A_SPCNGFPC532E_33220F0V01_SG1_SG3 - Chart F2 and F3: o 33220F0VRR_Chart_F2_F3.pdf o Electrical data (33229F0VRR): <ul style="list-style-type: none"> ▪ 33229F0VRR_Chart_F3_ElecData_FT1_AMBIANT.csv ▪ 33229F0VRR_Chart_F3_ElecData_FT1_HOT.csv ▪ 33229F0VRR_Chart_F3_ElecData_FT1_COLD.csv ▪ 33229F0VRR_Chart_F3_ElecData_BIA_AMBIANT.csv ▪ 33229F0VRR_Chart_F3_ElecData_BIH_HOT.csv ▪ 33229F0VRR_Chart_F3_ElecData_BIC_COLD.csv ▪ 33229F0VRR_Chart_F3_DriftReport.pdf o 33229F0V01_Chart_F2_F3.pdf o Electrical data: <ul style="list-style-type: none"> ▪ 33229F0V01_Chart_F3_ElecData_FT1_AMBIANT.csv ▪ 33229F0V01_Chart_F3_ElecData_FT1_HOT.csv ▪ 33229F0V01_Chart_F3_ElecData_FT1_COLD.csv ▪ 33229F0V01_Chart_F3_ElecData_BIA_AMBIANT.csv ▪ 33229F0V01_Chart_F3_ElecData_BIH_HOT.csv ▪ 33229F0V01_Chart_F3_ElecData_BIC_COLD.csv ▪ 33229F0V01_Chart_F3_DriftReport.pdf - Chart F4 (SG1 and SG3): o 33229F0V01_Chart_F4_SG1_SG3.pdf o Electrical data: <ul style="list-style-type: none"> ▪ 33229F0V01_Chart_F4_ElecData_SG1_Environmental.csv ▪ 33229F0V01_Chart_F4_ElecData_SG1_Mechanical.csv DC2309A_SPCNGFPC532E_33220F0VZX_SG2 - Chart F2 and F3: o 33220F0VZX_Chart_F2_F3.pdf o Electrical data: <ul style="list-style-type: none"> ▪ 33229F0VZX_Chart_F3_ElecData_FT1_AMBIANT.xlsx ▪ 33229F0VZX_Chart_F3_ElecData_FT1_HOT.xlsx ▪ 33229F0VZX_Chart_F3_ElecData_FT1_COLD.xlsx ▪ 33229F0VZX_Chart_F3_ElecData_BIA_AMBIANT.xlsx ▪ 33229F0VZX_Chart_F3_ElecData_BIH_HOT.xlsx ▪ 33229F0VZX_Chart_F3_ElecData_BIC_COLD.xlsx ▪ 33229F0VZX_Chart_F3_DriftReport.pdf - Chart F4 (SG2): o 33229F0VZX_Chart_F4_SG2.pdf o Electrical data: <ul style="list-style-type: none"> ▪ 33229F0VZX_Chart_F4_ElecData_T0_Amb.csv ▪ 33229F0VZX_Chart_F4_ElecData_T0_Hot.csv ▪ 33229F0VZX_Chart_F4_ElecData_T0_Cold.csv ▪ 33229F0VZX_Chart_F4_ElecData_500h_Amb.csv ▪ 33229F0VZX_Chart_F4_ElecData_500h_Hot.csv ▪ 33229F0VZX_Chart_F4_ElecData_500h_Cold.csv ▪ 33229F0VZX_Chart_F4_ElecData_1000h_Amb.csv ▪ 33229F0VZX_Chart_F4_ElecData_1000h_Hot.csv ▪ 33229F0VZX_Chart_F4_ElecData_1000h_Cold.csv ▪ 33229F0VZX_Chart_F4_ElecData_2000h_Amb.csv ▪ 33229F0VZX_Chart_F4_ElecData_2000h_Hot.csv ▪ 33229F0VZX_Chart_F4_ElecData_2000h_Cold.csv ▪ 33229F0VZX_Chart_F4_DriftReport.pdf Sales listing.xlsx</p>		



APPLICATION FOR EXTENSION OF ESCC QUALIFICATION APPROVAL

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Executive Member: CNES Date: 19/02/2025

Page 3
Appl. No.
381A

Non compliance to ESCC requirements:

15

No.:	Specification	Paragraph	Non compliance

Additional tasks required to achieve full compliance for ESCC qualification or rationale for acceptability of noncompliance:

16

None


Executive Manager Disposition


17

Application Approval: Yes ☒ No ☐

Action / Remarks:

Date: 31-03-2025


A. Zadeh: Head of the Avionics & EEE Division,
Electrical Department

	APPLICATION FOR EXTENSION OF ESCC QUALIFICATION APPROVAL Component Title: Integrated Circuits, Silicon, Monolithic, CMOS Radiation Hardened 65nm ASIC Platform, based on type C65Space Executive Member: CNES Date: 19/02/2025	Page 4 Appl. No. 381A
ANNEX 1: LIST OF TESTS DONE TO SUPPORT EXTENSION OF QUALIFICATION		18
Tests conducted in compliance with: <ul style="list-style-type: none">- ESCC 9000 generic specification; Chart F4 (for ESCC/QPL parts);- or PID-TFD (for ESCC/QML parts) Tests vehicle identification/description:		
<div>NX1H35AS CQFP-352 with Ceramic Tie Bar Gold Wire- Bonded</div>	<div>NX1H35AS has been designed in compliance with ST C65Space libraries and design rules for custom cells. The qualification has been performed with flight models from 1 diffusion lot. See "VOQ_2022_2024_C65SPACE_NX1H35AS-v2.pdf" document and associated reports</div>	
Detail Specification reference: 9202/086		

NX1H35AS in CQFP-352 package :

Subgroup	Test	Tick when done	Conditions	Date Code Diffusion Lot	Tested Qty	No. of Rejects	Comments if not performed. Comments on Rejection
Environmental/Mechanical Subgroup	Thermal Shock	<input checked="" type="checkbox"/>	MIL-STD-883. Test Method 1011	NX1H35AS-CQFP352 Cut 1.2 Diffusion Lot: VQ128380 Assembly Lot: 33229F0VRM Date code: 2414A	15	0	
	Temperature Cycling	<input checked="" type="checkbox"/>	MIL-STD-883 Test Method 1010		15	0	
	Moisture Resistance	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 1004		15	0	
	Seal (Fine and Gross Leak)	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 1014		15	0	
	Intermediate and End-Point Electrical Measurements	<input checked="" type="checkbox"/>	Intermediate and End-Point Electrical Measurements in the Device Specification		12	0	For the Moisture resistance test, we are supposed to do it on components whose leads have been arched. To do this, we have to cut the tie bar of the CQFP352. The problem is that once we have cut the tie-bar, we are no longer able to do the electrical test in socket. So we indicated in §2.1.1.2 in esc9304010iss4.pdf (ESCC Detail Specification No. 9304/010) (NG-Medium Product) to arch the leads on 3 components instead of 15 and to switch to electrical testing only 12 parts with tie bar (same sampling and philosophy as in QML).
	External Visual Inspection	<input checked="" type="checkbox"/>	ESCC Basic Specification No. 20500 / 2059000	NX1H35AS-CQFP352 Cut 1.2 Diffusion Lot: VQ128380 Assembly Lot: 33229F0VRN Date code: 2414A	15	0	MIL-STD-883, Test Method 2009
	Mechanical Shock	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2002		15	0	
	Vibration	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2007		15	0	
	Constant Acceleration	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2001		15	0	
	Seal (Fine and Gross Leak)	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 1014		15	0	
	Intermediate and End-Point Electrical Measurements	<input checked="" type="checkbox"/>	Intermediate and End-Point Electrical Measurements in the Device Specification		15	0	
	External Visual Inspection	<input checked="" type="checkbox"/>	ESCC Basic Specification No. 20500 / 2059000		15	0	MIL-STD-883, Test Method 2009

Subgroup	Test	Tick when done	Conditions	Date Code Diffusion Lot	Tested Qty	No. of Rejects	Comments if not performed. Comments on Rejection
Assembly Capability Subgroup	Permanence of Marking	<input checked="" type="checkbox"/>	ESCC Basic Specification No. 24800	NX1H35AS-CQFP352 Cut 1.2 Diffusion Lot: VQ128380 Assembly Lot: 33229F0VRP Date code: 2414A	NA	NA	Not Applicable on Laser Marking
	Terminal Strength	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 2004 Cond. B2		3	0	As described in §2.1.1.2 (a) in esc9304010iss4.pdf (ESCC Detail Specification No. 9304/010) (NG-Medium Product)
	Internal Visual Inspection	<input checked="" type="checkbox"/>	ESCC Basic Specification No. 2049000		5	0	MIL-STD-883 Test Method 2010A
	Bond Strength	<input checked="" type="checkbox"/>	MIL-STD-883 Test Method 2011		5	0	
	Die Shear	<input checked="" type="checkbox"/>	MIL-STD-883 Test Method 2019		4	0	

Subgroup	Test	Tick when done	Conditions	Date Code Diffusion Lot	Tested Qty	No. of Rejects	Comments if not performed. Comments on Rejection
Endurance Subgroup	Operating Life	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 1005	NX1H35AS-CQFP352 Cut 1.2 Diffusion Lot: VQ128380 Assembly Lot: 33229F0VZQ Date code: 2309A 2000h @125°C @Ta = +25°C @Tj Max = +125°C @Tc = -55°C Vccmax	15	0	
	Intermediate and End-Point Electrical Measurements	<input checked="" type="checkbox"/>	Intermediate and End-Point Electrical Measurements in the Device Specification		15	0	
	Seal (Fine and Gross Leak)	<input checked="" type="checkbox"/>	MIL-STD-883, Test Method 1014		15	0	
	External Visual Inspection	<input checked="" type="checkbox"/>	ESCC Basic Specification No. 2059000		15	0	MIL-STD-883, Test Method 2009

