ARQUIMEA

Online detection and diagnosis for radiation-induced errors in COTS microprocessors

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Outline

- About Arquimea
- Introduction
- TRACER IP
- Validation approach
- Radiation testing results
- Conclusions

ARQUIMEA

We are a technology company operating globally

PASSION FOR TECHNOLOGY

20+

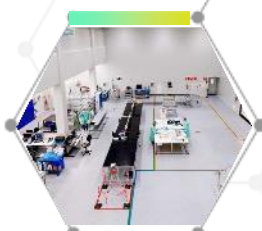
Years of innovation

500+

Professionals

ARQUIMEA

We offer solutions for sectors demanding highly reliable products and technologies.



AEROSPACE & DEFENSE

Parts and systems for all kinds of spacecraft.

Cryptography, drones, pointing control systems for defense and security.

Parts and ground equipment for airplanes.

- **Space**
- **Defense**
- **Aeronautics**

SCIENCE

We build tools, instruments and mechanisms for big telescopes and scientific facilities.

- **Astrophysics**
- **Particle Physics**
- **Nuclear Fusion**

FINTECH

Through KAUDAL INVESTMENT, we fund R&D projects for tech companies in Spain.

- **R&D Financing**

ARQUIMEA

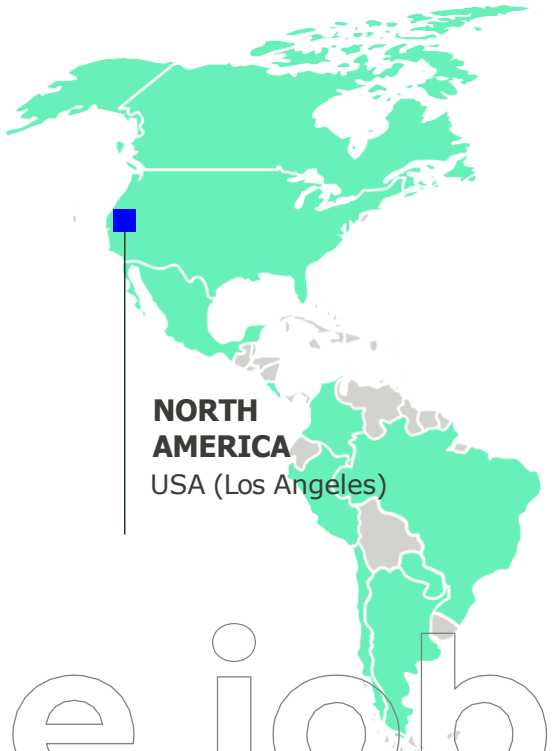
We solve complex and demanding challenges all over the World

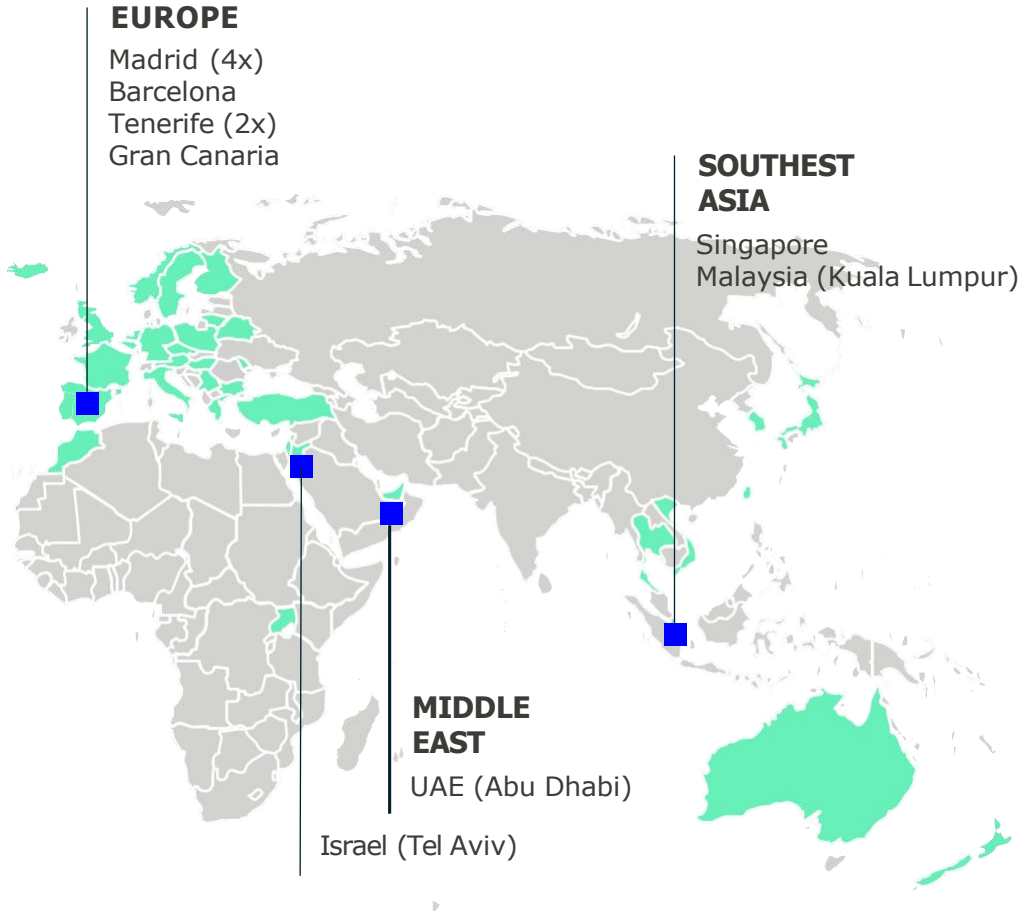
60+

Countries where we operate

12

Offices and facilities





Do the job.

ARQUIMEA

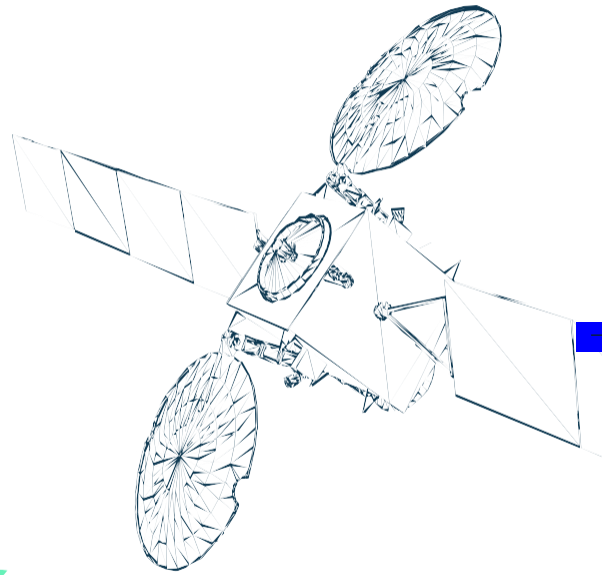
We design and manufacture systems and components over the entire space value chain

THERMAL SYSTEMS AND STRUCTURES

3000+ units delivered of satellite structures and thermal systems for the most relevant space missions worldwide.

AVIONICS AND CAMERAS FOR SATELLITES AND LAUNCHERS

500+ cameras in space for observation, exploration, monitoring and surveillance.



SMALLSATS AND TURNKEY MISSIONS

High-throughput smallsats and LEO missions from definition to operation
3 missions completed.

DEPLOYMENT SYSTEMS AND MECHANISMS

Critical systems for release and deployment of solar panels, antennas, instruments or radars in space. **200+ flight units.**

RAD-HARD MICROELECTRONICS

5000+ chips in satellites. Analog, digital and mixed-signal integrated circuits for space.

180+
Space missions

200+
Clients

8000+
Space parts delivered

AENOR ER Aerospace Quality UNE-EN 9100

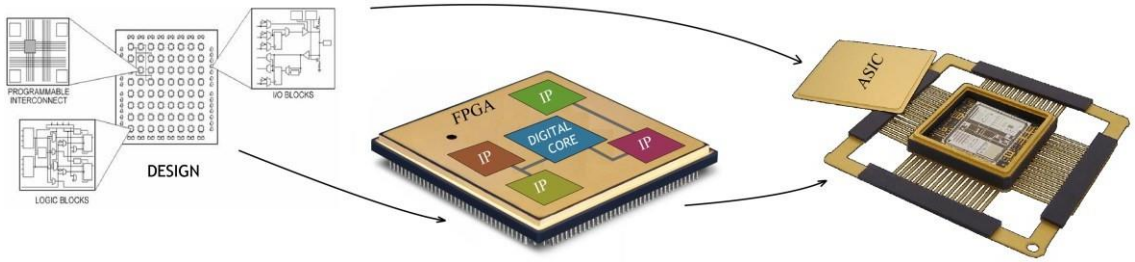
Microelectronics Design & Implementation Services

ASIC and IP Design for space applications

- **Trade-off analysis** for suitable technology selection and procurement flow
- **Turnkey solutions** from specification to space qualification
- **Rad-Hardening** of digital cells and analog IPs of the technology
- **Test Vehicles and internal block** design & characterization (Electrical & Radiation)
- **Technology access** and manufacturing
- **Final design evaluation & qualification** Test campaigns management
- **Product Assurance** based on ESCC/MIL standards

FPGA to ASIC conversion

- **Trade-off analysis** to assess on suitability for FPGA to ASIC conversion based on BOM costs, performances, integration and/or Power consumption requirements.
- **Custom procurement flow** and Long-term supply commitment
- **Design support** for RTL and netlist adaptation as well as SET/SEU mitigation.
- **Design verification and validation** based on ESCC/MIL standards



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LVDS Family

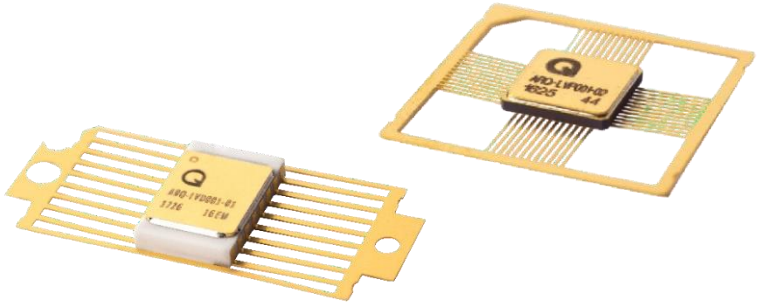
Description

- European alternative for LVDS transceivers – RadHard - ITAR/EAR free
- Improved compatibility with SpaceWire standard
- Specific Features for space (Cold spare, Extended Common Mode, Fail-Safe, etc..)
- High data transfer rate (>500Mbps)
- European Component Initiative program (ESA-ECI)

esa

Product family

- **AQLVD01** LVDS Quad Driver
- **AQLVR02** LVDS Quad Receiver
- **AQLVT01** LVDS Dual Transceiver
- **AQLVP01** LVDS Octal Repeater
- **Embedding** LVDS own Tx & Rx IPs developed under SiGe 250nm technology



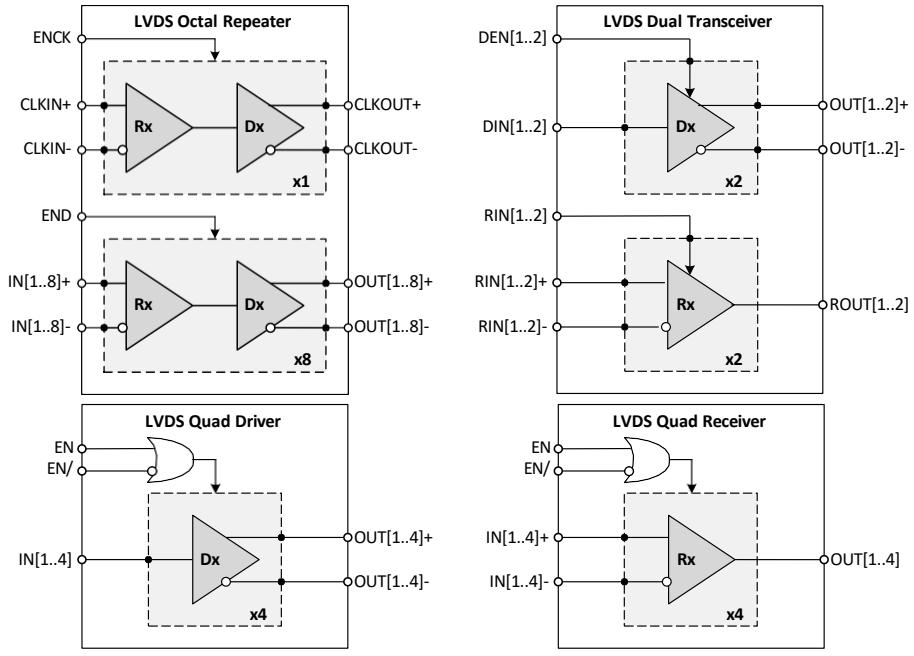
Applications

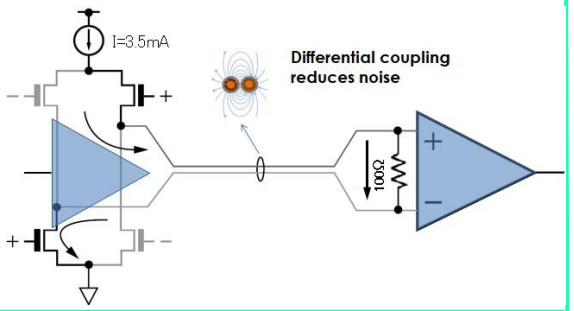
Any spacecraft Equipment that requires:

- Noise tolerant transmission along twisted pair cables at high data-rates (500Mbps)
- Low EMI and low power
- Maturity of LVDS Standard
- Rad-Hardened devices

Typical applications:

- SpaceWire network
- Clock distribution networks
- Coldspare buffer
- Command & Data Handling





Product Features

- ANSI EIA/TIA644A standard
- 500Mbps Channel data rate
- Low Channel skew and jitter
- Extended CMI [-4V to +5V]
- Cold-spare in all pins
- Fail Safe protection
- LVDS Input hysteresis
- TID: 300 kRad(Si)
- SEL immune
- BER $<10^{-13}$ err/bit (GEO Orbit)
- 8kV ESD protection
- [-55 to 125ºC]

Available options

- Soft IP, hard die/wafer
- Space-grade ceramic
- Hi-rel plastic (on-going)

Status

- TRL8 –Qualification test as per ESCC9000
- EPPL Approval for LVDS Driver and Receiver
- Lead time: 12 weeks
- Quote upon request

Competitive advantages

- High performance (speed, cold-spare, extended input common mode, Hysteresis, fail-safe)
- Fully European, ITAR free

ARQUIMEA

16-Bit Analog Multichannel Monitoring & Control IC

Description

- Full-integrated solution to acquire telemetries (thermistors, gauges, magnetometers, star trackers, sun sensors) and generates telecommands (reaction wheels, control moment gyroscopes, magnetorquers, flow control, latch valves, catalytic bed heaters) for spacecraft subsystems
- Reduced BOM to improves integration of satellite RIU/RTU and ICU equipments
- ITAR/EAR free

Part-type

- The **AQTMC01** mixed-signal ASSP is completely configurable and reads telemetries from sensors with up to 54 multiplexed channels and generate the telecommand with a PWM module. Functions with threshold detection and overcurrent alarm are embedded.
- Embedding own 16b, 100KSps ADC IP developed under CMOS 180nm technology

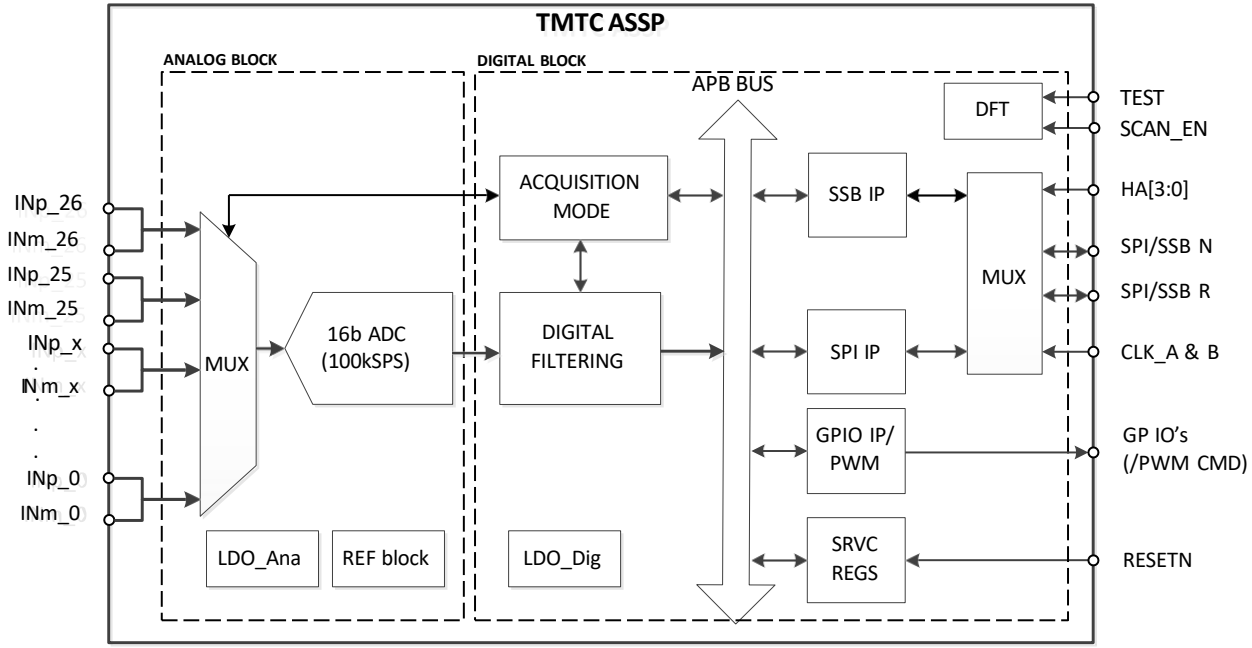
Applications

Any spacecraft equipment, especially concerning:

- Propulsion
- Altitude and Orbit Control System
- Solar Array Drive Electronics

Typical applications:

- Remote Terminal Unit
- Remote Interface Unit
- Instrument Control Unit



Product Features

- 54 s.e./27 diff. Acq. channels
- 10µA /100µA /1mA biasing
- Up to 20V input Voltage range with external resistance network
- Continuous / sweep modes.
- Input common mode control
- Built-in 50 kHz anti-alias & configurable digital filter
- 16-bit res., 100kSps Nom.
- LVCMOS/ LVTTL levels
- PWM & voltage monitoring functions [100Hz to 10MHz].
- 20MHz Dual SPI (N&R).
- Cold-spare & 2kV ESD HBM
- LDO with over-current protect
- TID above 50 krad(Si).
- SEE free >37 MeV·cm²/mg.
- SEL immune

Available options

- CQFP-100 package.

Status

- Silicon proven (Electrically & radiation)
- Fully Qualified by Q2 2025 (TRL8)

Competitive advantages

- High integration
- Low cost compared to other solutions
- Configurability (channel sweep, latency, precision)
- European supply chain, ITAR free

AIRBUS

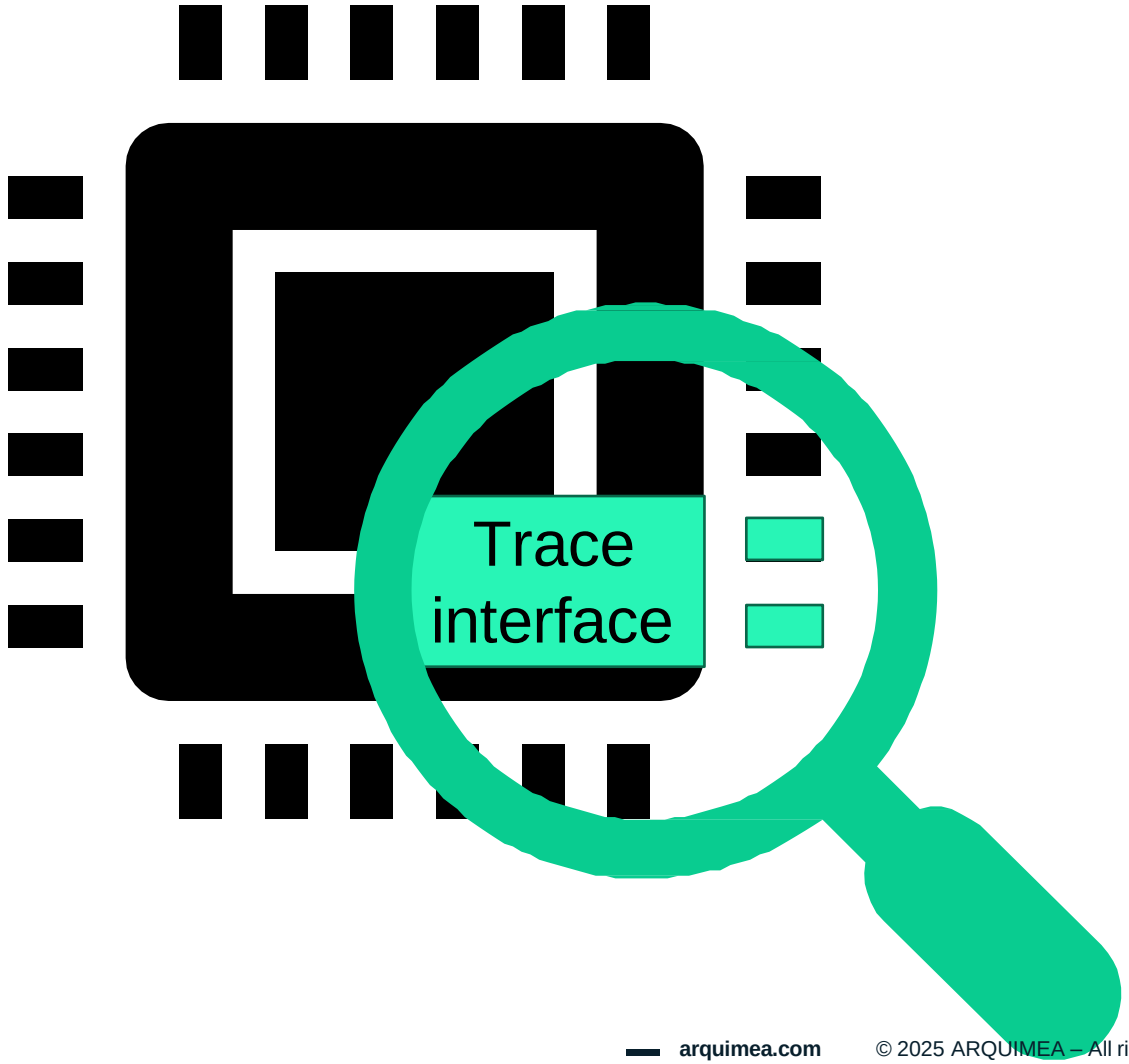
esa

Introduction

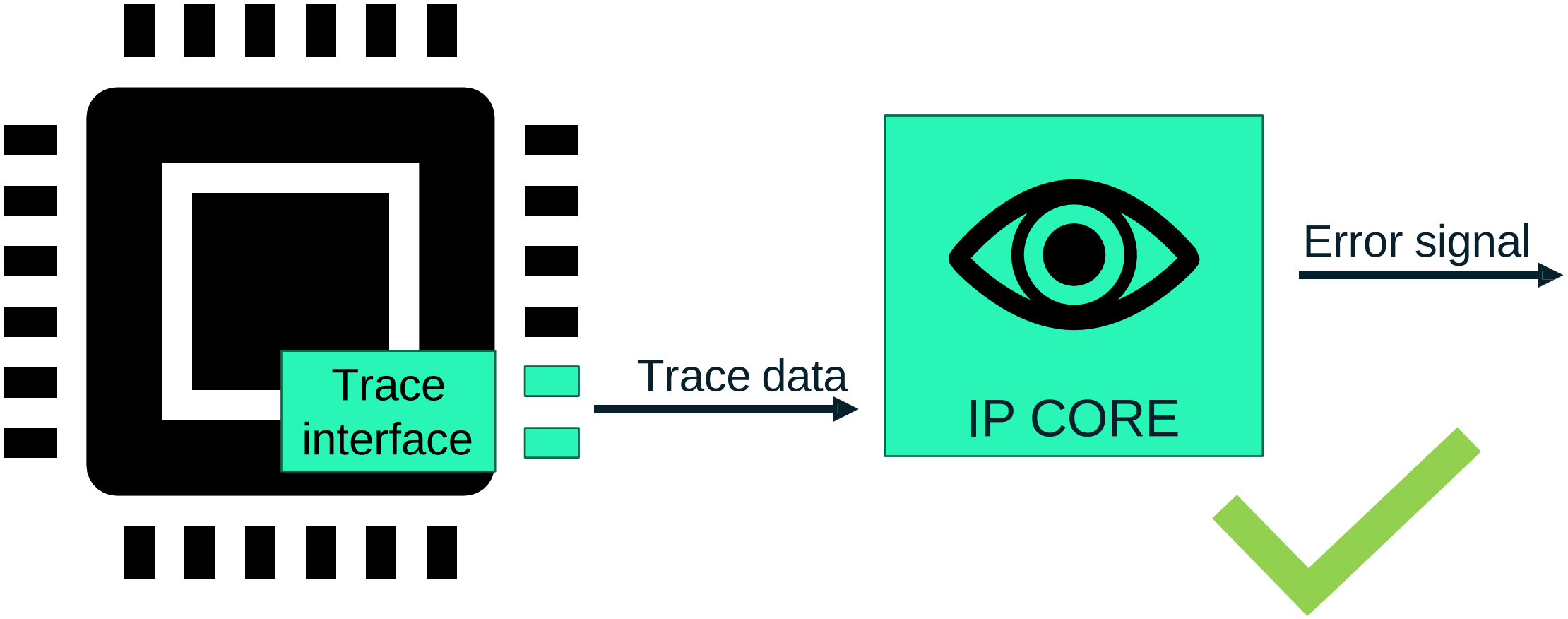
- COTS usage is widespread on New Space missions
- On Board Data Processing (OBDP) capability needs increase
- COTS microprocessors: high performance, low power, small size and weight, low cost…
- Critical key points:
  - Difficult to test complex circuits such as microprocessors
  - Difficult to assure correct circuit behavior under radiation

Introduction

- Trace interface key features:
  - Non-intrusive
  - Online operation
  - Processor observability
- Suitable for:
  - ✓ Processor monitoring
  - ✓ Error detection
  - ✓ Error diagnosis



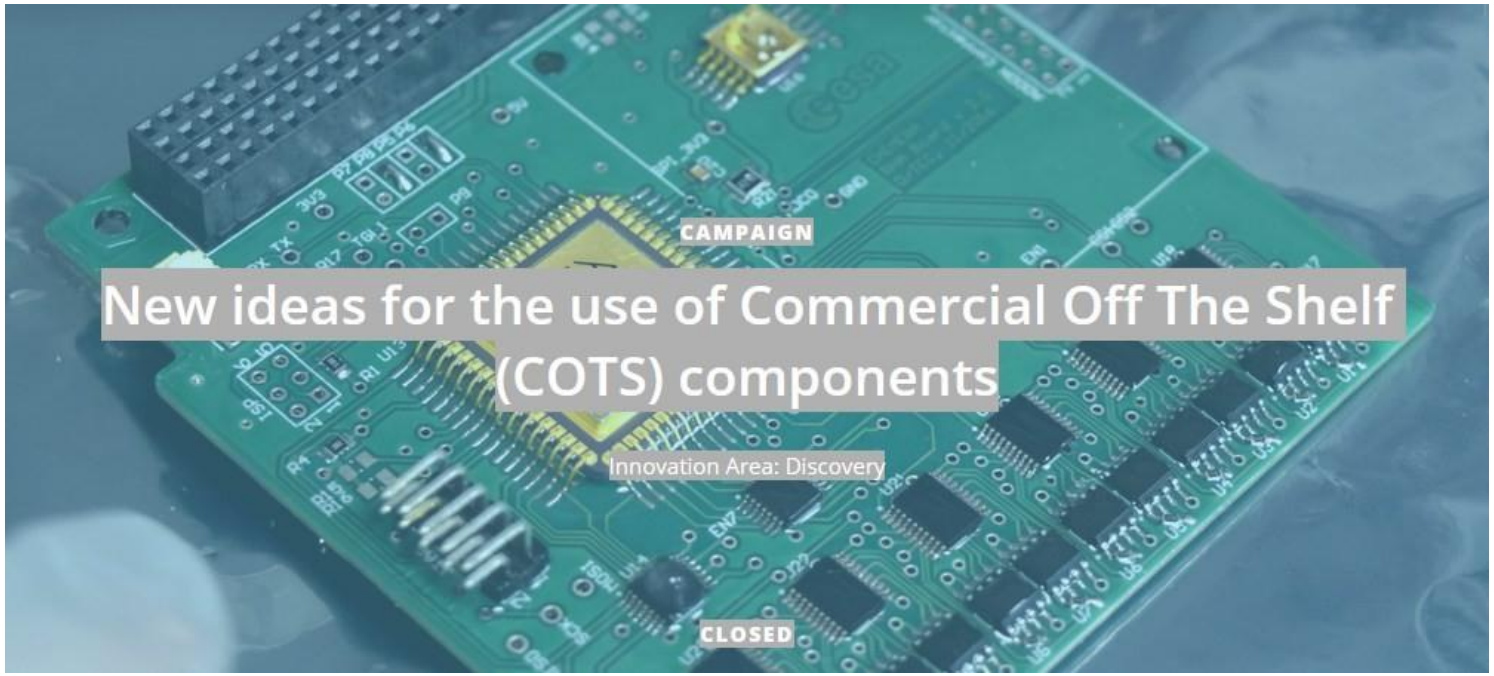
Introduction



- Previous work had validated our approach in ZYNQ-7000 device under proton and neutron irradiation.

Objectives

- Extend to more ARM Architectures (ETMv4)
- Increase maturity of our solution
- Test with heavy ions



TRACER IP

Trace Real-Time Analyzer to Check processor Errors under Radiation (TRACER) IP is devised as a feasible solution for both detecting and diagnosing errors on a microprocessor during execution, including radiation-induced errors.

TRACER IP

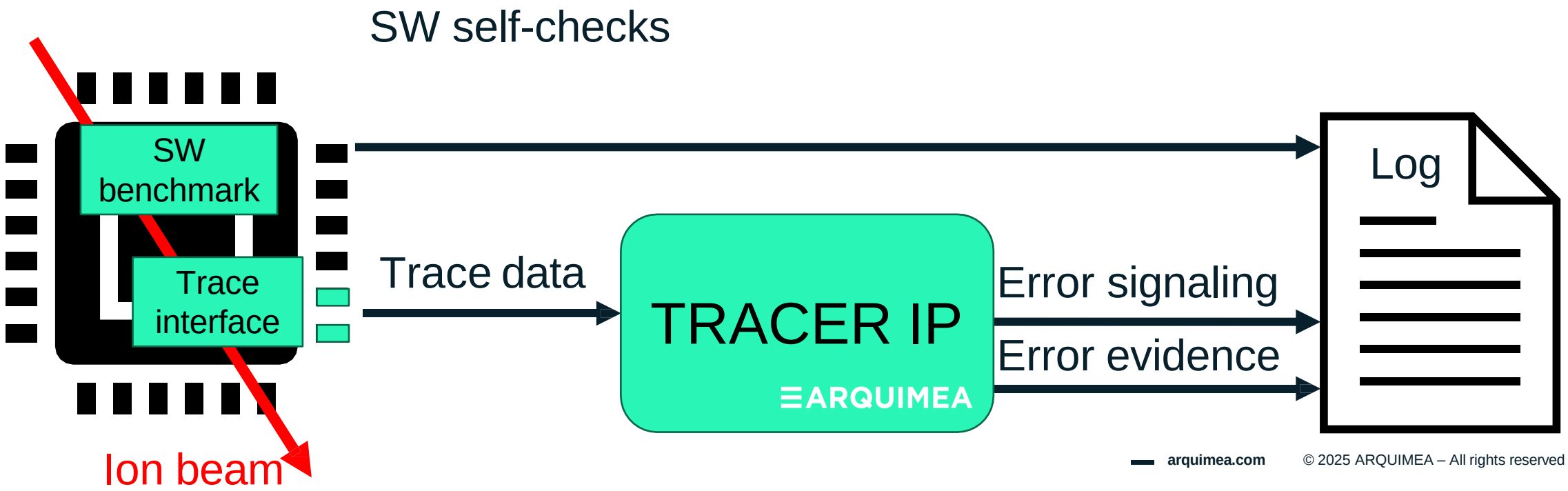
- ✓ User-configurable
- ✓ Real-time operation
- ✓ Low latency
- ✓ Non-intrusive
- ✓ Data monitoring
- ✓ Control-flow monitoring
- ✓ Pure RTL implementation
- ✓ Small footprint

TRACER IP

- Compatibility:
  - ARM processors with CoreSight ™ trace interface
  - Trace protocols: ITM, PTM and ETMv4
- Examples: ARM Cortex-A9, Cortex-M7, Cortex-A53, and more

Validation approach

- Prove that the TRACER IP can detect errors in COTS processors under radiation.
- Low ion energies (C4+ and Ne7+): manageable error rate and minimize destruction risk.
- The processors are executing a certain SW benchmark to represent a computational load.
- The SW benchmark includes a golden reference and reports self checks to external PC.
- Events are logged to check TRACER detection exhaustiveness.

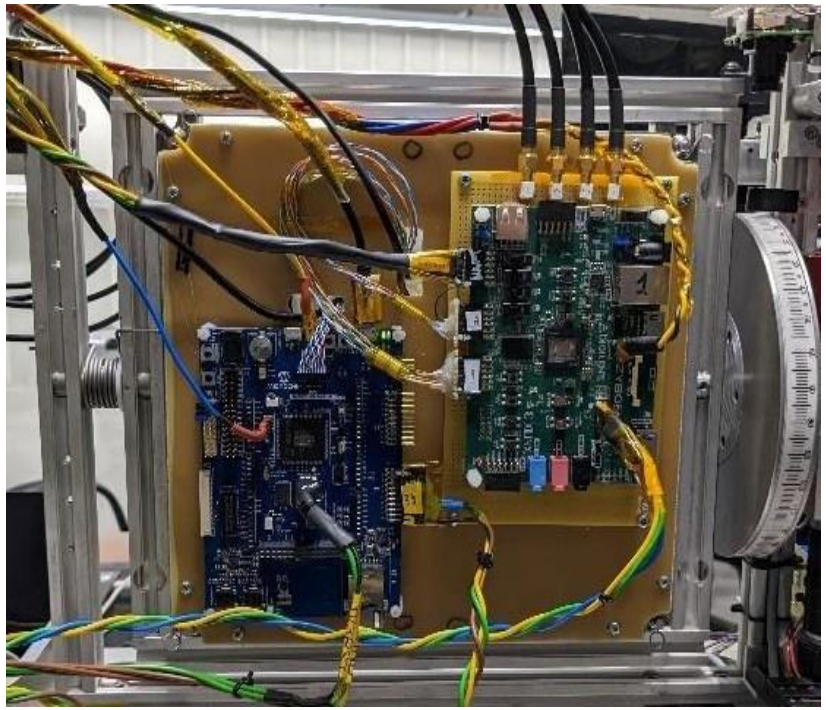


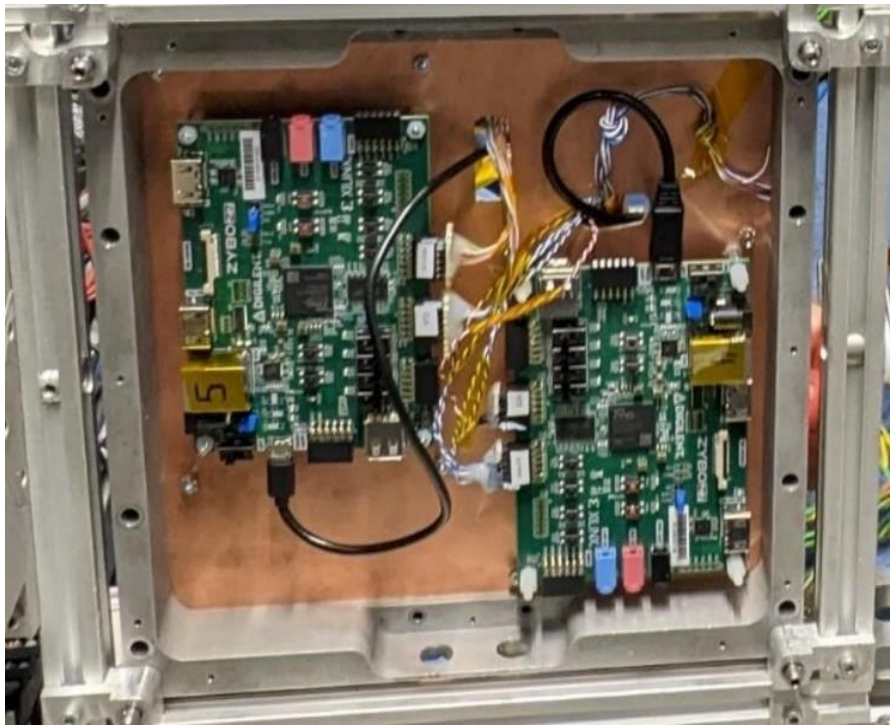
Validation approach

- Target DUT processors
  - ARM Cortex-A9 processor (over a Xilinx Zynq-7000 SoC device) implementing both ITM and PTM trace protocols.
  - ARM Cortex-M7 processor (over a SAMV71Q21RT device) implementing both ITM and ETMv4 trace protocols.
- Target benchmark applications
  - Matrix multiplication.
  - NIR-HAWAII-2RG BM algorithm.

Hardware test setup

- DUT processors:
  - De-lidded
  - Exposed to beam
- TRACER IP:
  - Implemented on FPGA
  - Not exposed to beam





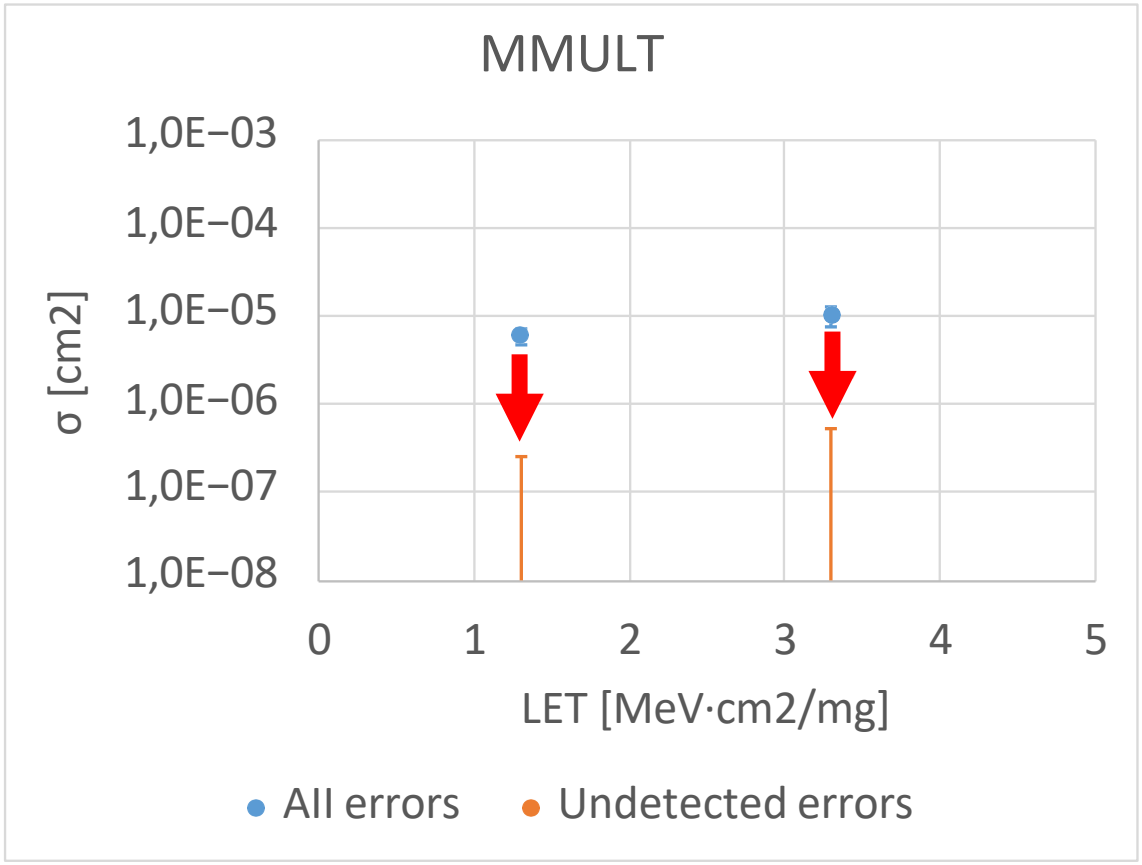
HIF UCL

Validation approach

- SEL monitored via power supply, to avoid device destruction.
- SEU and SEFI effects monitored with TRACER IP:
  - Wrong program instruction address
  - Wrong data output
  - Timeout
- Retrieval of error evidences upon an error is detected.

Experimental results

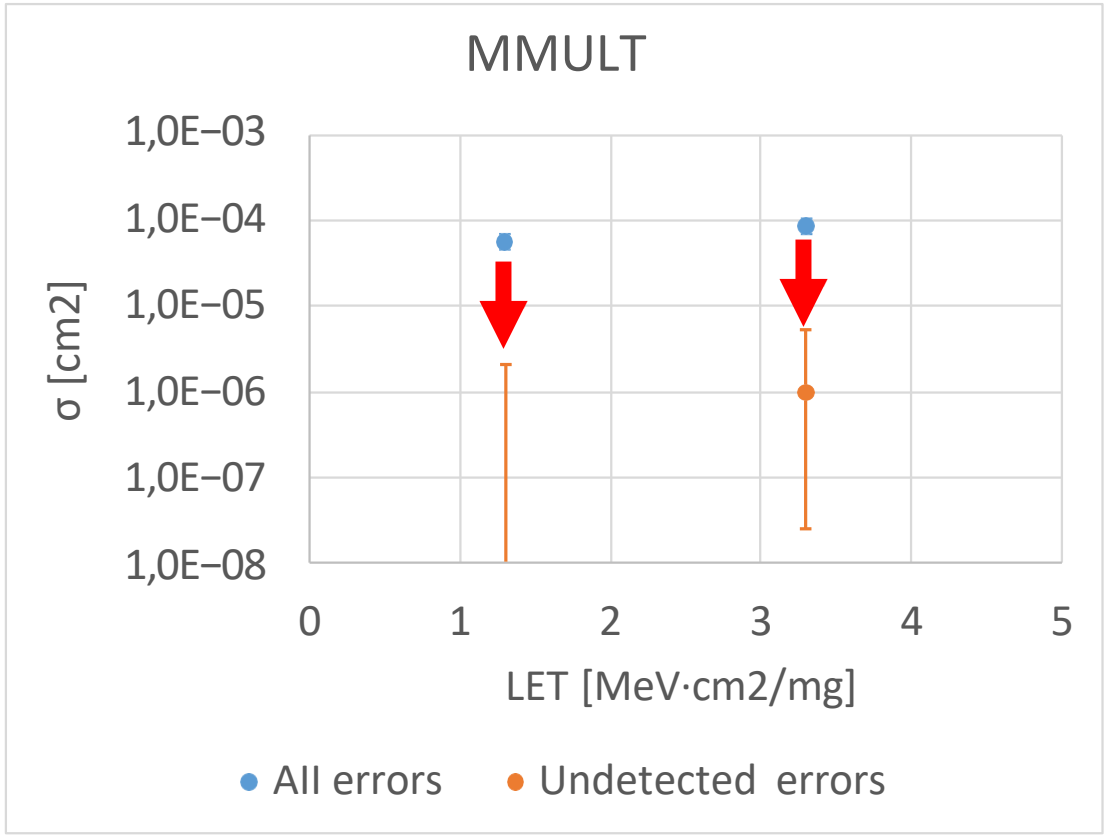
- Cross-section plot for XC7Z010-1CLG400C (ZYNQ) device

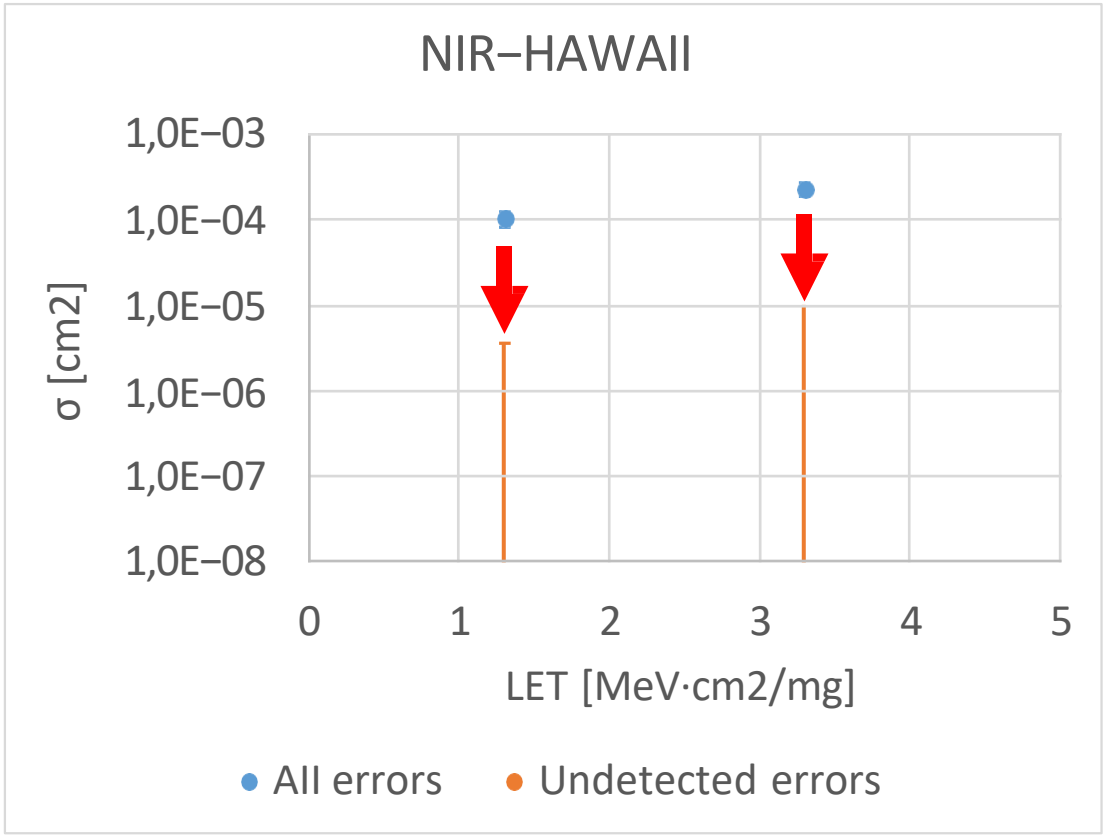


Cross section reduced in more than 1 order of magnitude!

Experimental results

Cross-section plots for SAMV71Q21RT device





Cross section reduced in more than 1 order of magnitude!

Experimental results

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- Error evidences

Errors can be diagnosed!

- Data error

	t-3 …	t-2	t-1	t-0
checksum #1	…	0x1E47A1A4	0x1E47A1A4	0x1FA84524
checksum #2	…	0x1E47A1A4	0x1E47A1A4	0x1E47A1A4

- Control-flow error

	t-3	t-2	t-1	t-0
PC value	0x00015BB0	0x00015BD8	0x00000004	0x000000A0
code region	<generate InputData>	<generate InputData>	<vector table>	<Undefined handler>

Commercial product

- If you are interested in acquiring this IP, please follow contact details at the end of the presentation.
- Deliverables:
  - IP encrypted RTL code
  - IP datasheet

Conclusions

- TRACER IP can successfully monitor ETMv4 instruction, ITM and PTM trace protocols.
- SEU/SEFI effects were detected by TRACER IP as they result in errors in the processor program flow or data access.
- Test environment:
  - Cross section of each device increases when the ion energy is increased but also when the complexity of the executed application is increased.
  - TRACER IP provides the capability of retrieving error evidence to improve design.
- Final application:
  - Cross section of undetected errors is reduced by more than 1 order of magnitude.
  - TRACER IP provides the capability of retrieving error evidence for risk assessment.

Think BIG

DO the job

ENJOY life

Contact:

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Francisco Gutiérrez
fgutierrez@arquimea.com

Experimental results

- SW consistency is dually checked both by the DUT itself and the TRACER IP.
  - Error DAT: each of the duplicated operation branches has output a different result.
  - Error SDC: both operation branches differ from the golden reference.
  - Error TMO: absence of DUT communications for an excessive period of time.
  - Error only IP: corresponds to events that the TRACER IP is alerting on, but DUT does not.
  - Error COM: corresponds to a communication error in any of the serial ports.

Experimental results

- Radiation results over XC7Z010-1CLG400C (ZYNQ) device

DUT #4 & #5	MMULT	
ion	C4+ LET = 1.3 MeV·cm²/mg	Ne7+ LET = 3.3 MeV·cm²/mg
DAT	87	68
Det DAT	87	68
SDC	0	0
TMO	0	1
Det TMO	0	1
Only IP	0	0
COM	1	0
σ (all errors) (cm²)	$5.88 \cdot 10^{-6}$	$9.82 \cdot 10^{-6}$
Δσ (all errors) (cm²)	$[4.71 \cdot 10^{-6}, 7.25 \cdot 10^{-6}]$	$[7.64 \cdot 10^{-6}, 1.24 \cdot 10^{-5}]$
σ (undetected errors) (cm²)	-	-
Δσ (undetected errors) (cm²)	$[0, 2.49 \cdot 10^{-7}]$	$[0, 5.25 \cdot 10^{-7}]$

Experimental results

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- Radiation results over SAMV71Q21RT device

DUT #1 & #2	MMULT		NIR-HAWAII	
ion	C4+ LET = 1.3 MeV·cm²/mg	Ne7+ LET = 3.3 MeV·cm²/mg	C4+ LET = 1.3 MeV·cm²/mg	Ne7+ LET = 3.3 MeV·cm²/mg
DAT	96	89	105	105
Det DAT	96	89	105	105
SDC	0	1	0	0
TMO	0	0	0	1
Det TMO	0	0	0	1
Only IP	4	1	0	0
COM	2	0	1	0
σ (all errors) (cm²)	$5.62 \cdot 10^{-5}$	$8.73 \cdot 10^{-5}$	$1.05 \cdot 10^{-4}$	$2.35 \cdot 10^{-4}$
Δσ (all errors) (cm²)	$[4.57 \cdot 10^{-5}, 6.83 \cdot 10^{-5}]$	$[7.03 \cdot 10^{-5}, 1.07 \cdot 10^{-4}]$	$[8.60 \cdot 10^{-5}, 1.27 \cdot 10^{-4}]$	$[1.92 \cdot 10^{-4}, 2.84 \cdot 10^{-4}]$
σ (undetected errors) (cm²)	-	$9.60 \cdot 10^{-7}$	-	-
Δσ (undetected errors) (cm²)	$[0, 2.07 \cdot 10^{-6}]$	$[2.43 \cdot 10^{-8}, 5.34 \cdot 10^{-6}]$	$[0, 3.69 \cdot 10^{-6}]$	$[0, 8.16 \cdot 10^{-6}]$