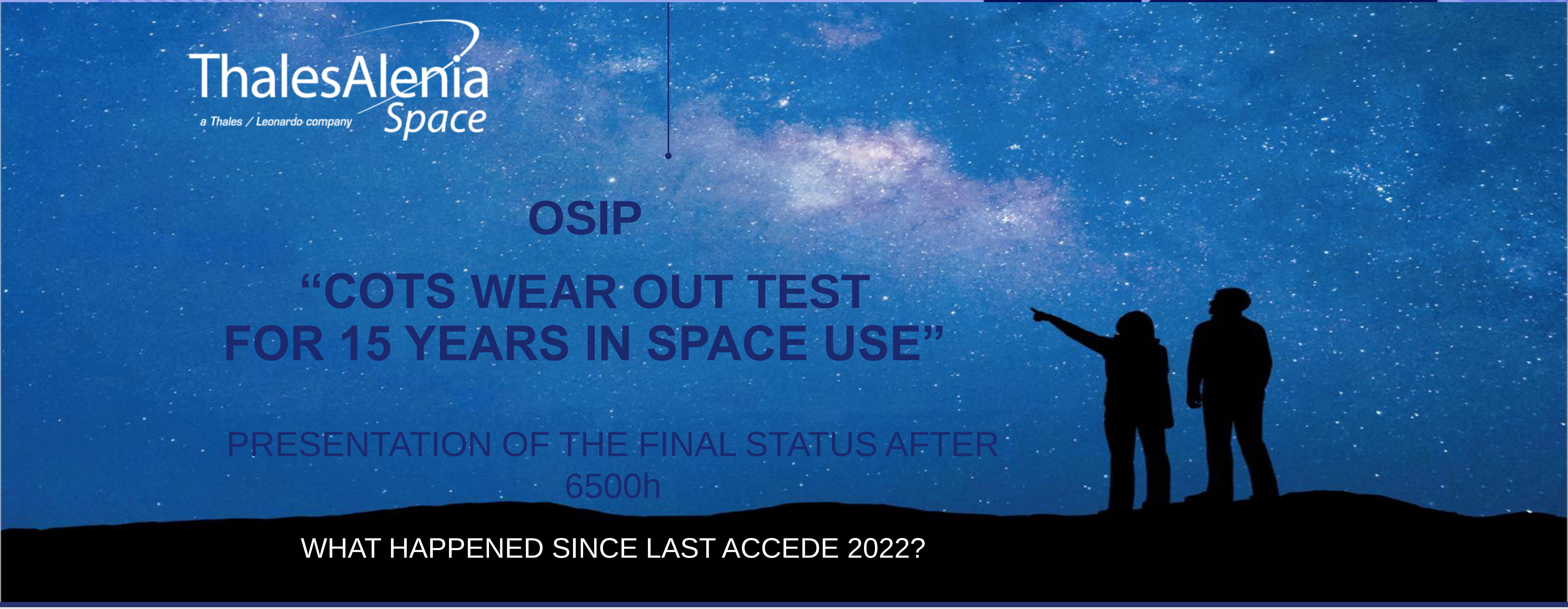
ACCEDE | ESCCON

2025 Seville – Spain
25 to 27th March



OSIP

“COTS WEAR OUT TEST FOR 15 YEARS IN SPACE USE”

PRESENTATION OF THE FINAL STATUS AFTER 6500h

WHAT HAPPENED SINCE LAST ACCEDE 2022?

Part 1 – Stress tests

OSIP STUDY
what is Wear Out?

COMPONENTS FAMILIES
Selection and Tests

RESULTS AFTER 6500 h
Resistor, Ceram Cap, Tant Cap, MOSFET, OAP, DDP2

WEAR OUT SEEN AFTER 6500h

Part 2 – Predictive models

TWO MODELISATION APPROACHES
Failure distribution/Degradation models

PREDICTIVE MODEL TOOL

PREDICTIVE MODEL RESULTS

CONCLUSION
Part 1 stress tests
Part 2 predictive models

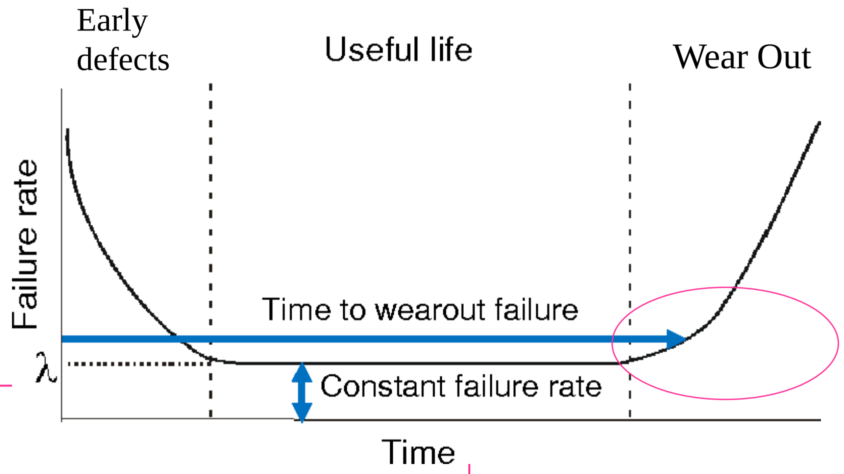
PART 1 : STRESS TESTS

OSIP STUDY – WHAT IS WEAR OUT ?

(OSIP) The Open Space Innovation Platform

Wear Out: The phase in the life of a device during which the mortality function is increasing.

Note: As typically used with the bathtub curve, the Wear Out phase follows the useful life of the device. (JESD122 definition)



In this OSIP study,

- Representative families / technologies are selected (6 families) among Integrated Circuits, Transistors and Passive (resistors, capacitors)
- Dedicated long term "stress test" is performed per family
- At the end of the "stress test" **~6500h** , an estimated life time duration has been done and compared to an objective of 15 Years in Space
- **During the Tests, stresses are applied 1,2 times over the maximum rating of the datasheet in temperature or in power.**
- **So, the electrical behaviour of the components is not guaranteed by manufacturer**

Important

15Y or more

COMPONENTS FAMILIES – SELECTION AND TESTS

- 6 ref. types selected : Parts already passed radiation tests for active components &- Most common used technologies

Family	Details /case	MAX RATING	Qty	T°C Oven	Stress Toven/ P/V/I	Bias	Measured Param.
Resistor (AEC-Q200 tested)	47.5Ohm 1206	25mW 85°C	25 25	Oven 1: 150°C Oven 2: 125°C	Temp 150°C Power +20%	1.09V 2.53V	R, TCR
C0402 T2 100nF 16V Ceramic capacitor (AEC-Q200 qualified)	100nF 16V 0402	16V 125°C	25 25	Oven 1: 150°C Oven 2: 125°C	Temp 150°C Voltage +20%	16,0V 19,2V	C, D, Q, ESR
Solid tantalum capacitor (AEC-Q200 qualified)	4,7UF 50V - D-case	50V 150°C	18 18	Oven 1: 150°C *(only one oven)	Temp 150°C Voltage +20%	25V 30V	C, D, Q, ESR
MOSFET	P channel D PACK	ID@ TCase=100°C 7,6A TCase max : 150°C~ ID 100mA	25 25	Oven 1: 150°C (⇔TCase 150°C) Oven 2: 125°C (⇔TCase 150°C also)	Temp 150°C ID max to have Tcase150°C (with the power dissipation setup)	100mA 2,5A	BVDSS, VGS(th), RDS(on), IDSS
Operational amplifier	Rail to Rail SOIC	12V 125°C	25 25	Oven 1: 150°C Oven 2: 125°C	Temp 150°C Voltage +20%	12V 14.4V	VOS, IB, IOS, VO, IS
1Gb x16 DDR2 SDRAM	Lot1 85°C grade BGA lot2 105°C grade BGA	1.9V 85°C or 105°C	25 (9 lot1, 12 lot2) 25 (9 lot1, 12 lot2)	Oven 1: 150°C Oven 2: 125°C	Temp 150°C Voltage +20%	1.9V * 2.28V * *Dynamic activation	Continuity, Functional (@Vmin, Vnom, Vmax) @Fmax, partial mem. Test& full mem test

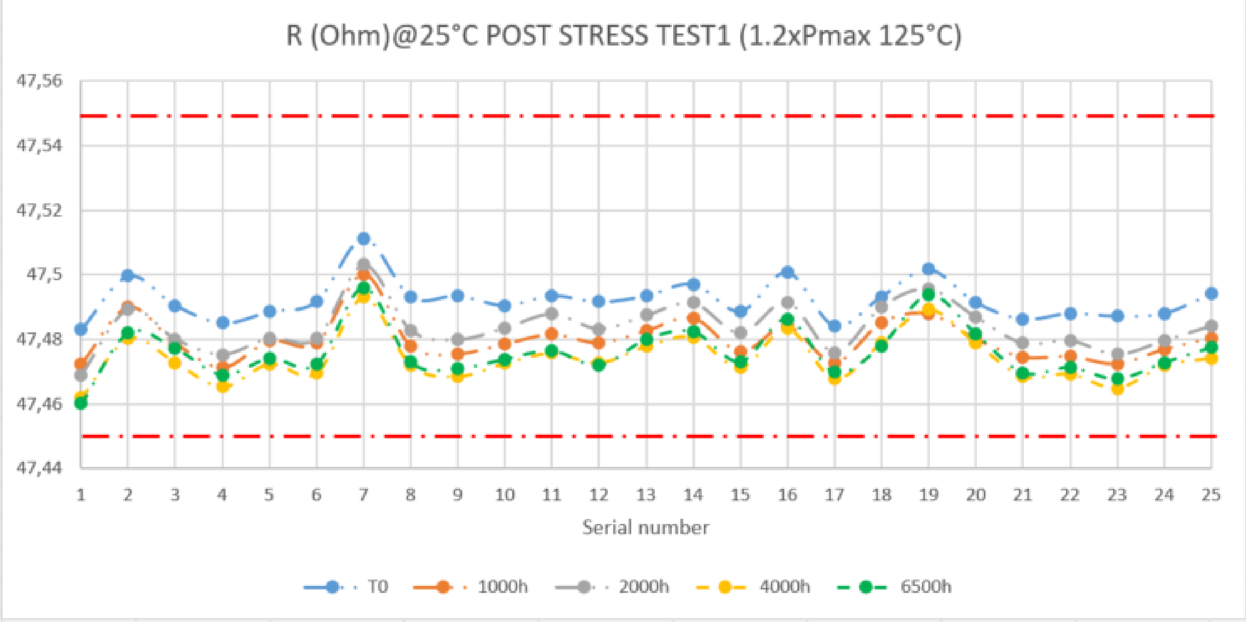
2 stress conditions applied separately: 1 stress in temperature (oven 1) + 1 stress in power supply (oven 2)

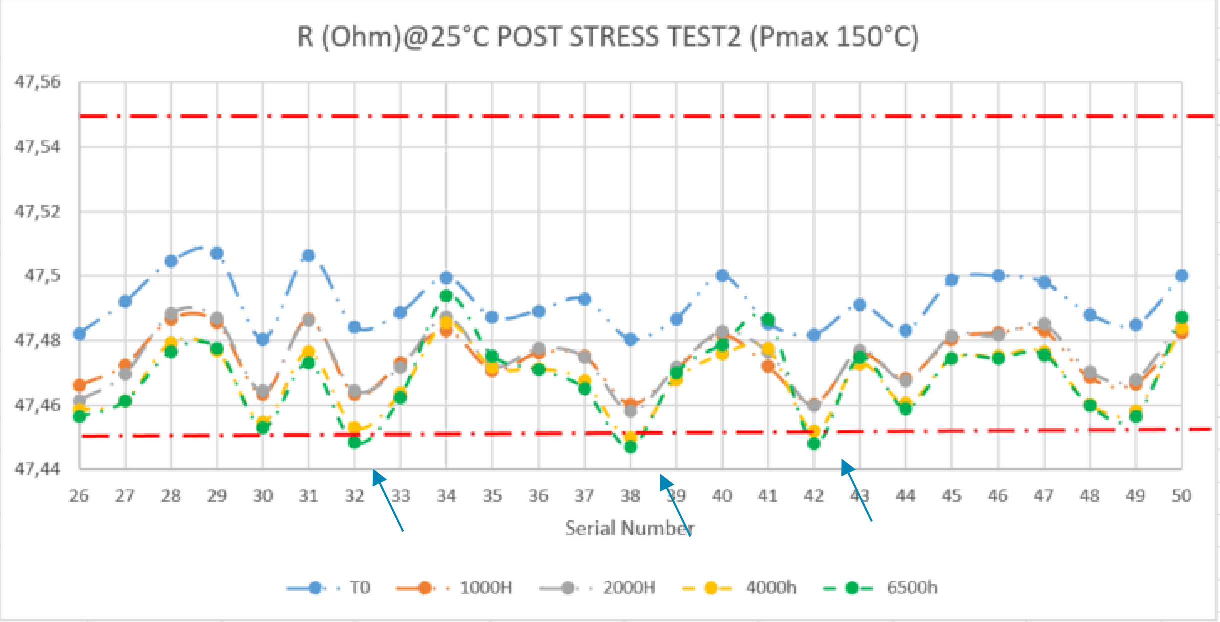
Read&Record at minimum, ambiant and maximum Temp. of the datasheet after 0h, 1000h, 2000h, 4000h, 6500h (~9months)

RESULTS AFTER 6500h

REF1 - RESISTOR (47.5 Ohm)

- No bias monitoring alarm detected & Power consumption is stable
- Read&Record after 0h, 1000h, 2000h, 4000h and 6500h at 25°C :



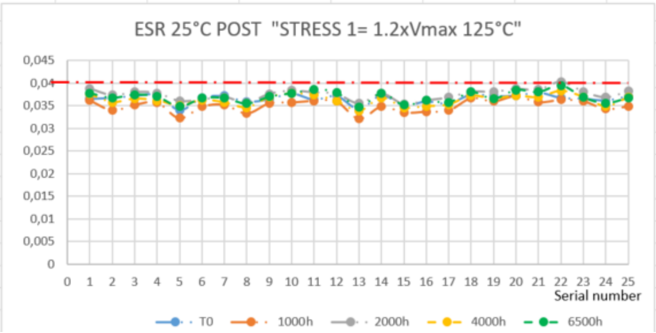


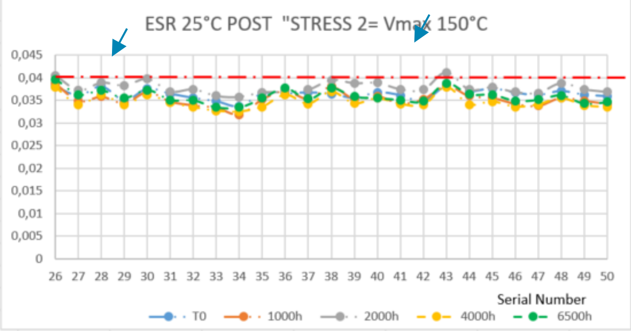
Resistance value decreases but slightly beyond the limit for some parts (aging/Wear Out effect)

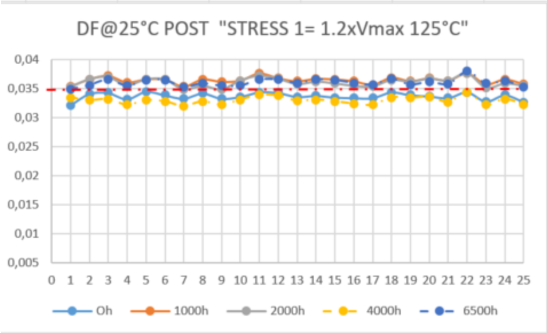
RESULTS AFTER 6500h

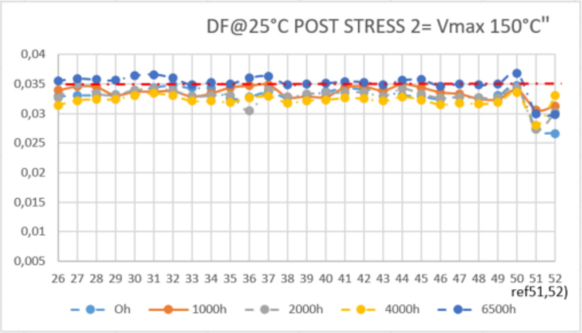
REF2 – CERAMIC CAPACITOR (100nF 16V)

- No bias monitoring alarm detected & Power consumption is stable
- Read&Record after 0h, 1000h, 2000h, 4000h and 6500h at 25°C :

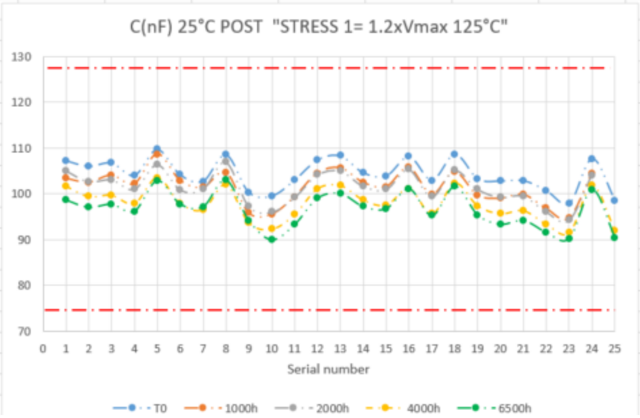


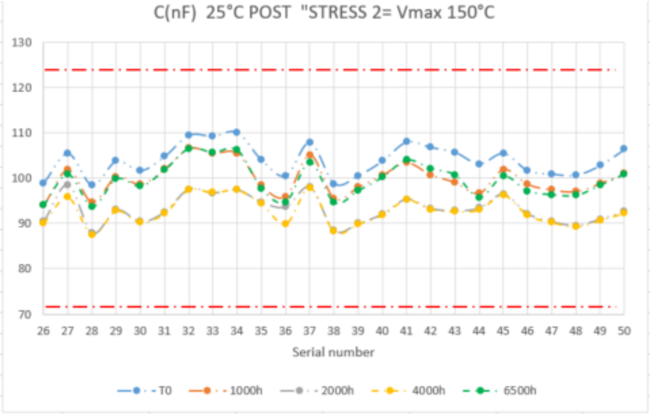


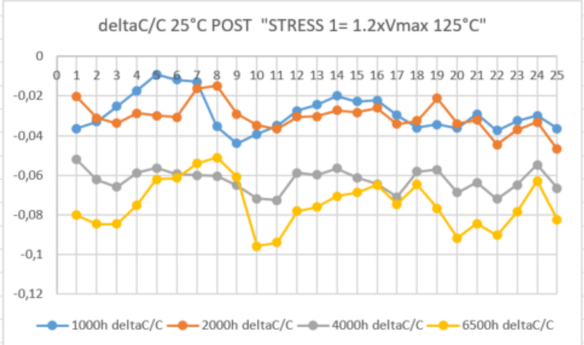


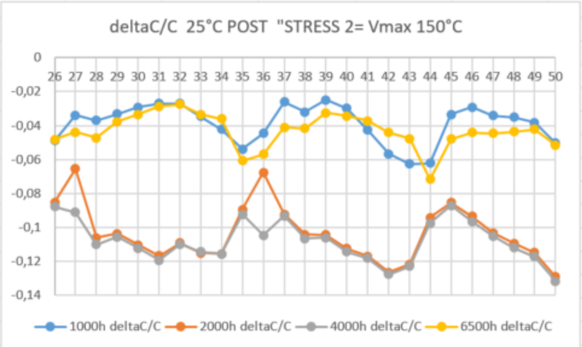


ESR limit slightly beyond the limit for 2 parts, back in then limit after 4000h and 6500h







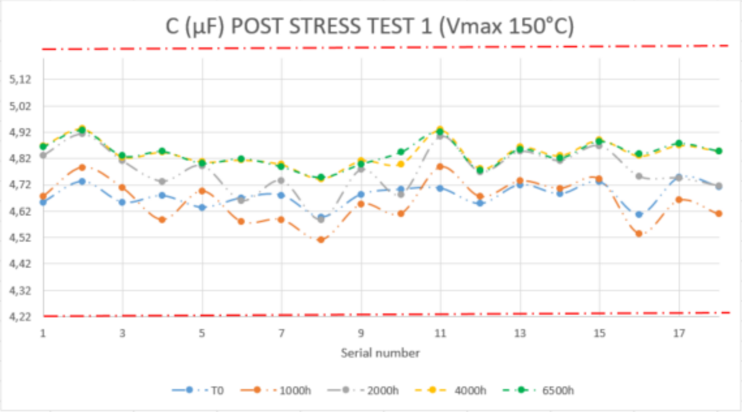


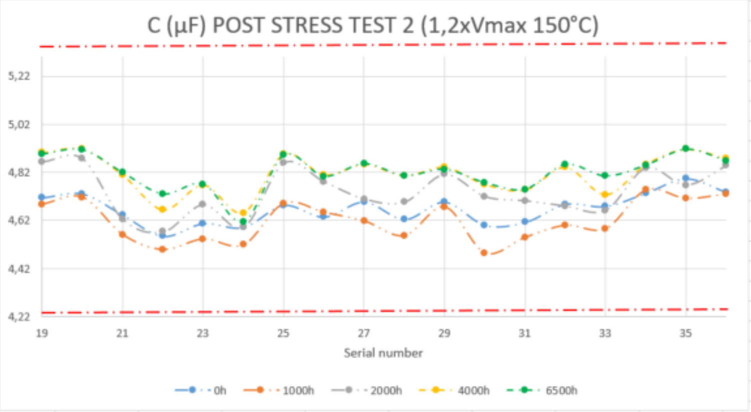
Capacitance value decreases, remains in the limits (aging effect)

RESULTS AFTER 6500h

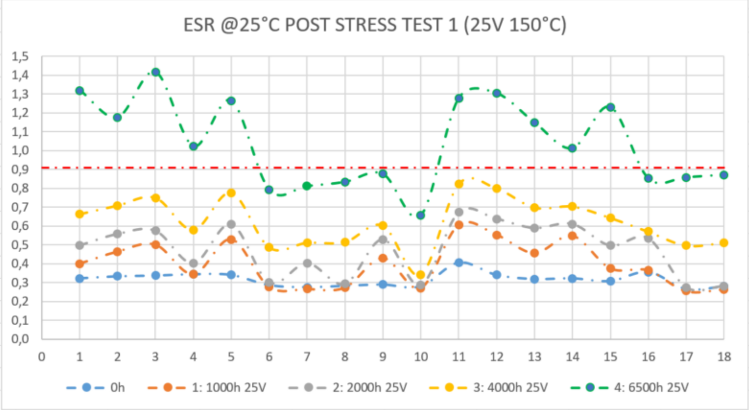
REF3 - TANTALUM CAPACITOR (4,7µF 50V)

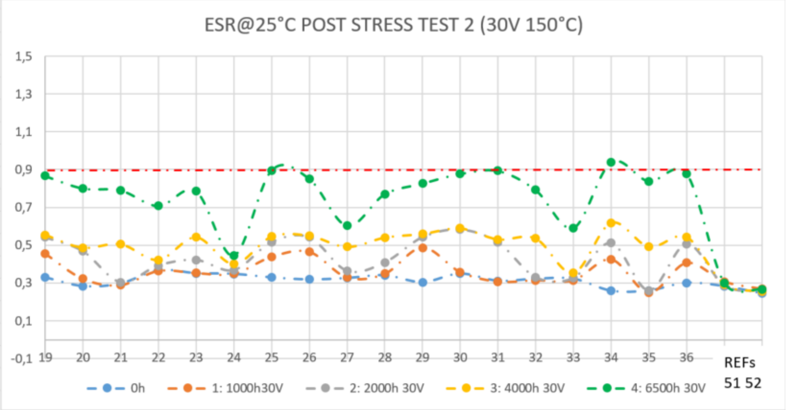
- Bias monitoring current **increase**
- Recovery effect during oven cooling phase for Read&Record
- Read&Record after 0h, 1000h, 2000h, 4000h and 6500h at 25°C :





Capacitance:
remains in the limits





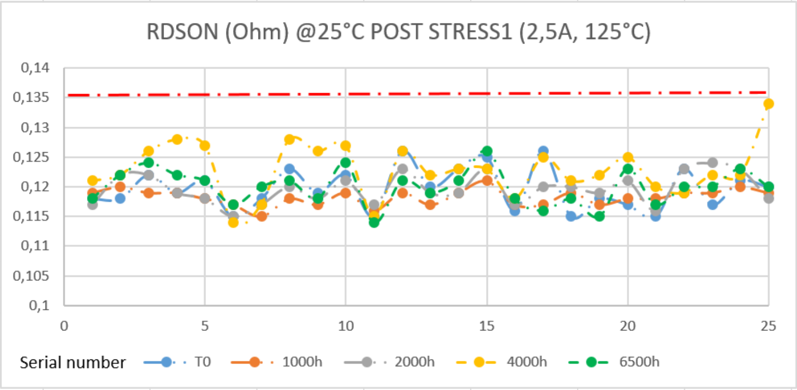
ESR:
Aging effect during the 6500h tests
Wear Out visible after 6500h test 1 (25V@150°C) more than in test 2 (30V 150°C)

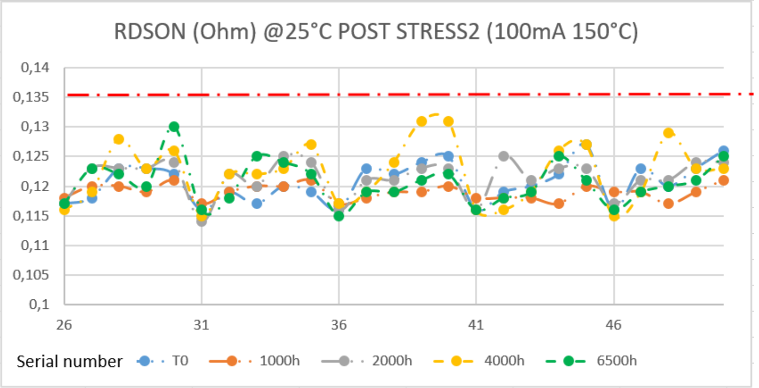
ESR drift more over time with lower voltage

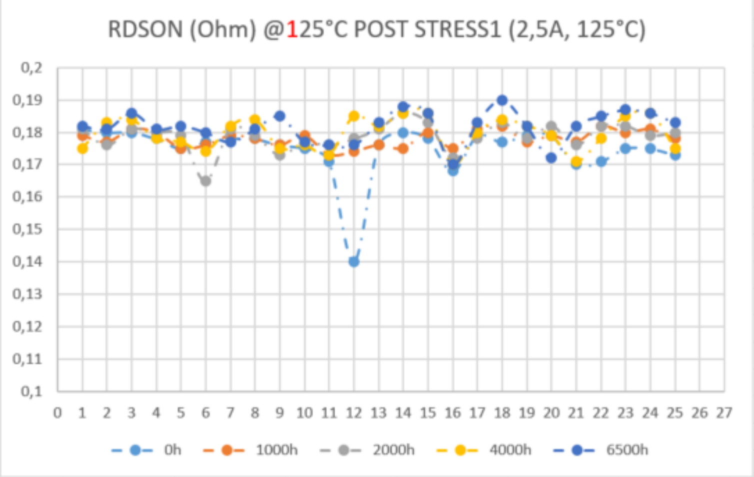
RESULTS AFTER 6500h

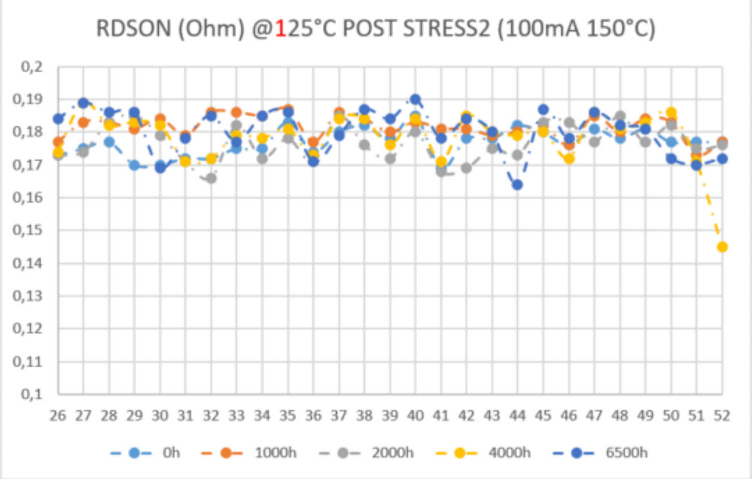
REF4- MOSFET

- No bias monitoring alarm detected & Power consumption is stable
- Read&Record after 0h, 1000h, 2000h, 6500h at 25°C :
- Remains in the limits







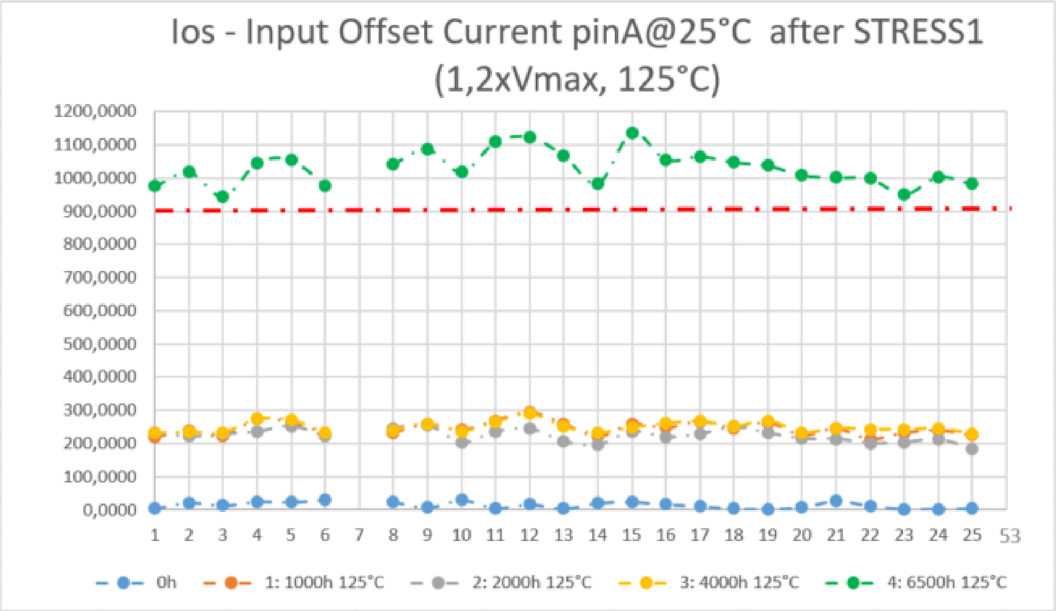


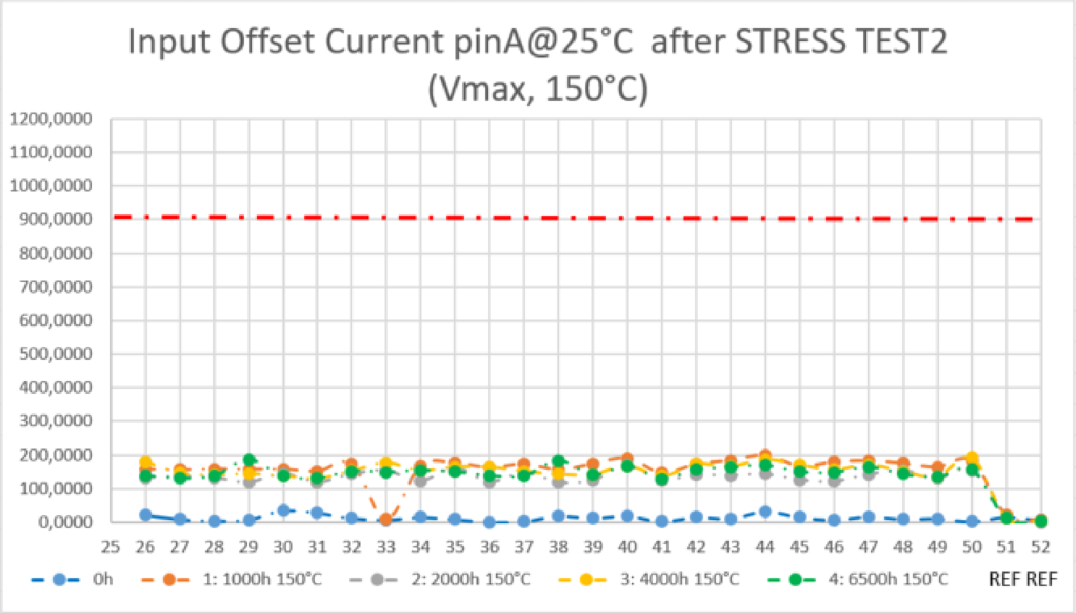
Aging effect : increase of 3% RDS(on) tested at @125°C after both aging conditions after the 6500 hours.

RESULTS AFTER 6500h

REF5- OPERATIONAL AMPLIFIER

- No bias monitoring alarm detected & Power consumption is stable
- Read&Record after 0h, 1000h, 2000h 4000h and 6500h at 25°C :


Ios - Input Offset Current pinA@25°C after STRESS1 (1,2xVmax, 125°C)

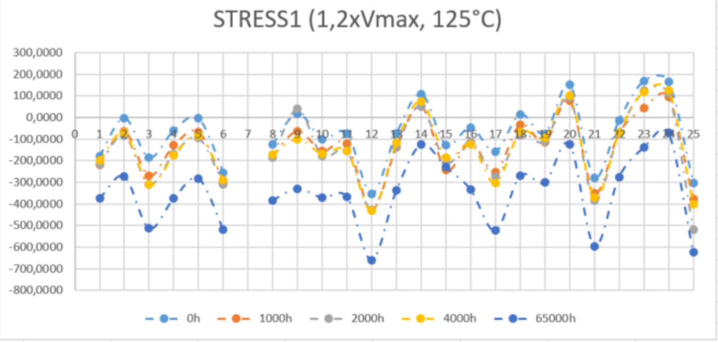

Input Offset Current pinA@25°C after STRESS TEST2 (Vmax, 150°C)

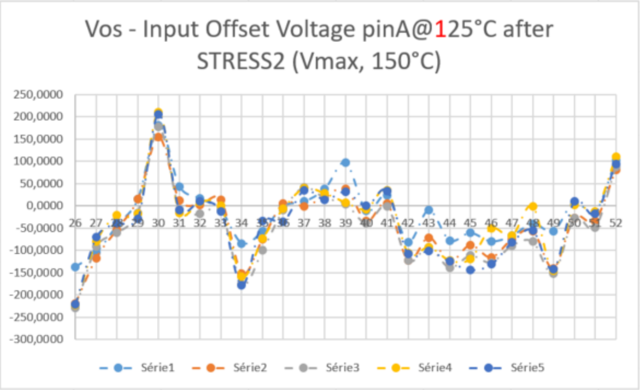
issue suspected position #7 on board (SN7 then SN53 removed)

Wear Out effect after 6500h, all parts (Ios R&R@ 1,2xVmax125°C)

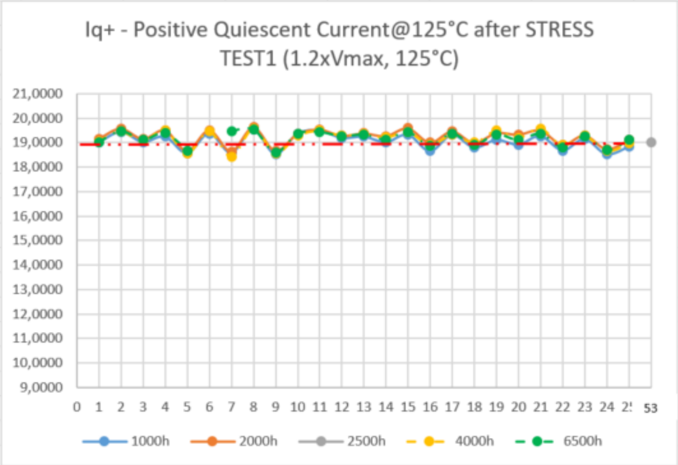
RESULTS AFTER 6500h

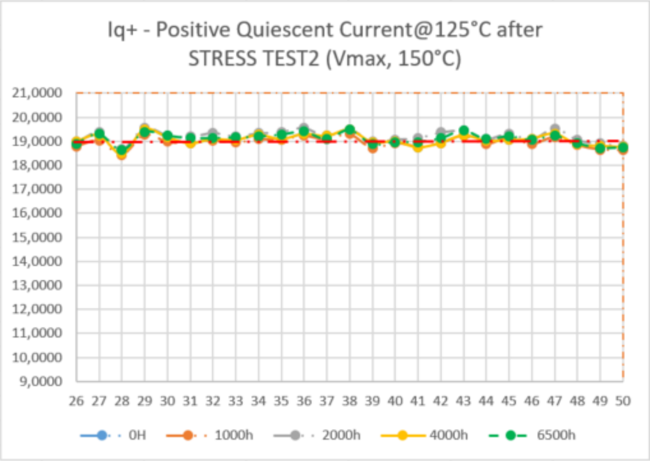
REF5- OPERATIONAL AMPLIFIER (con’t)





Aging effect after 6500h (Stress1 Vos after 1.2xVmax, 125°C)



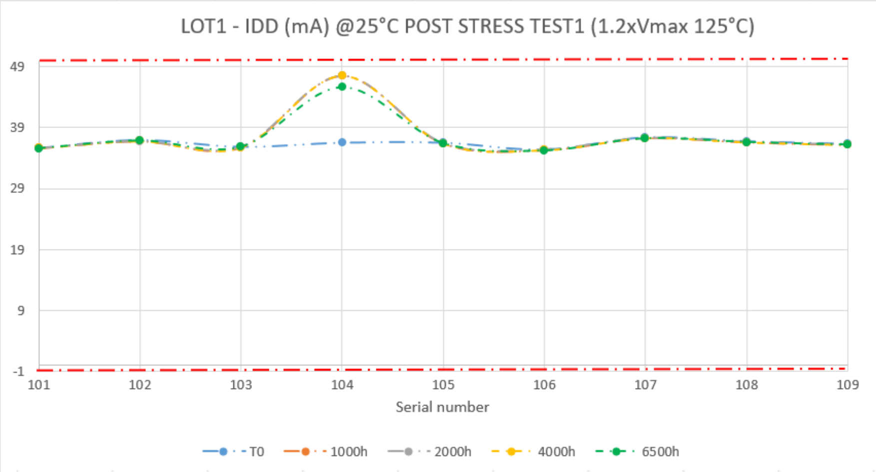


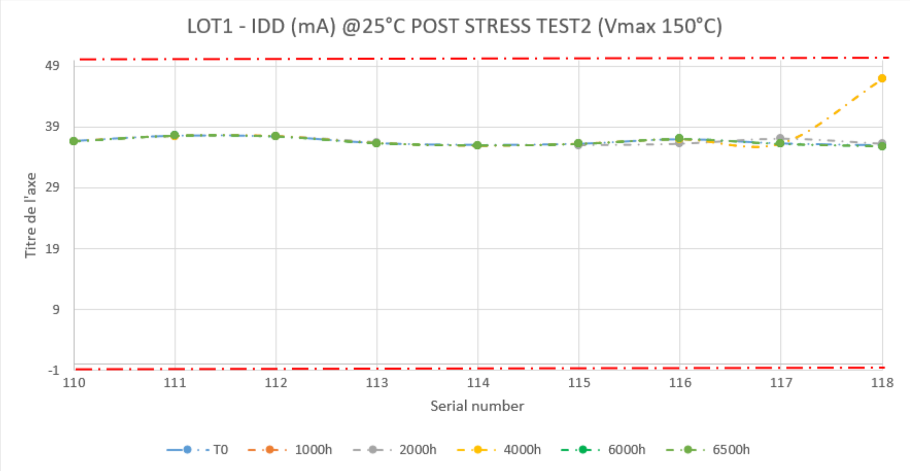
Quiescent current @125°C: At 0h, around the limit and for some parts slightly beyond the limit. Same results after 1000h 2000h 4000h and 6500h. Very stable. Hypothesis: Different between TAS measurement & manufacturer measurement, **not an aging effect**

RESULTS AFTER 6500h

REF6- DDR2

- Read&Record after 0h, 1000h, 2000h, 4000h and 6500h at 25°C :

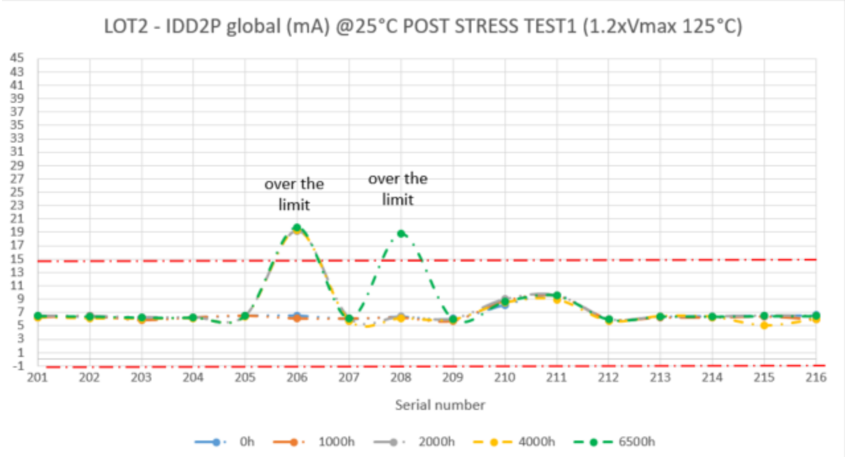


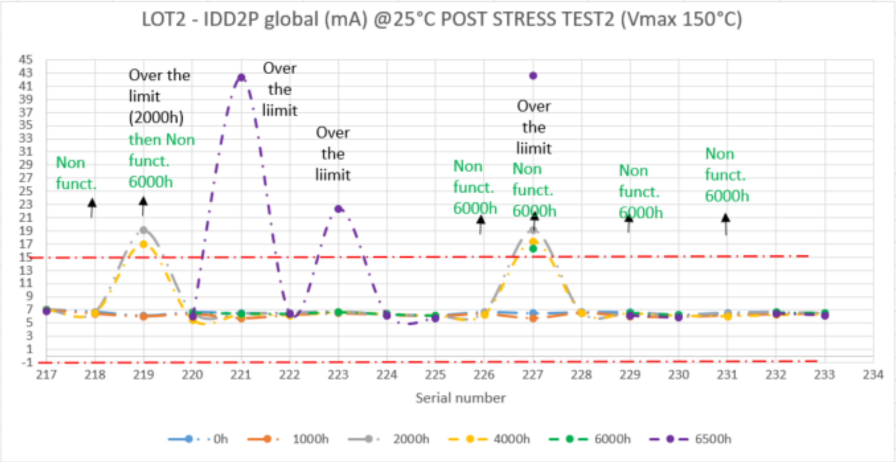


LOT1 (85°C grade)

Stress1 (1,9V@150°C): Only one part, SN104, is slightly over specification in IDD power consumption after 1000h and 2000h back inside the limits after 4000h

Stress2 (2.28V@125°C): 0 fail





LOT2 (105°C grade)

Stress1(1,9V@150°C): 8 parts were non-functional (5 at 5500h, 3 between 6000h and 6500h)

Stress2(2.28V@125°C): : 3 parts beyond the limit in power consumption

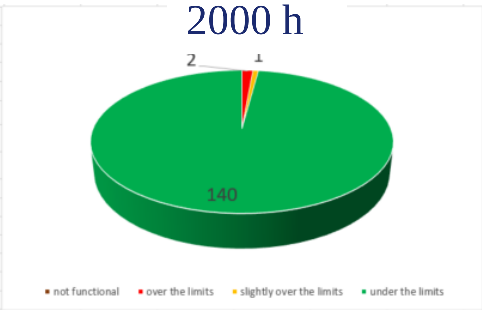
Tests were stopped after 6000 hours due to non-functional parts and maximum power consumption reached.

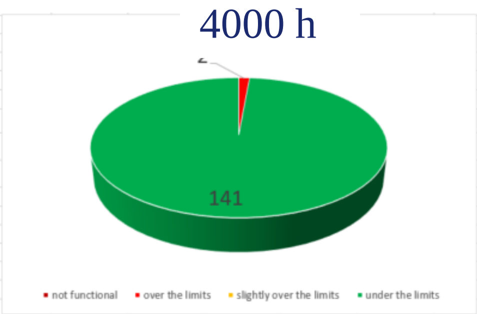
After 6500h: Aging effect Power consumption increase on some parts from both stress tests.

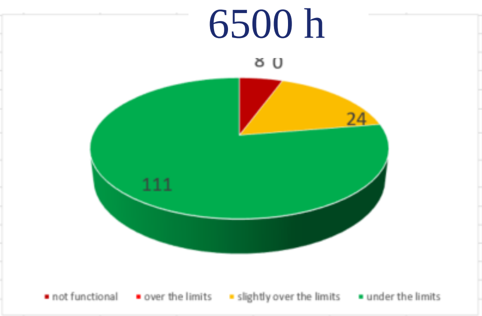
Wear Out: 8 parts non-functional after 6500 h

WEAR OUT SEEN AFTER 6500 h

STRESS 1 VMAX, 150°C

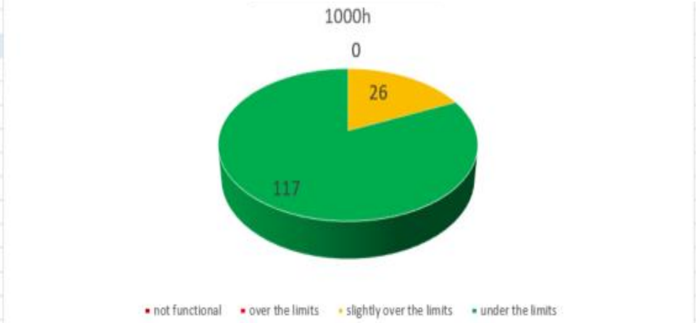


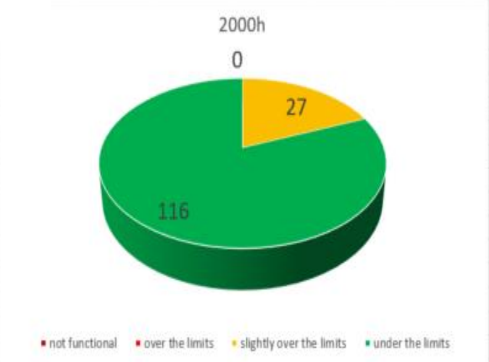




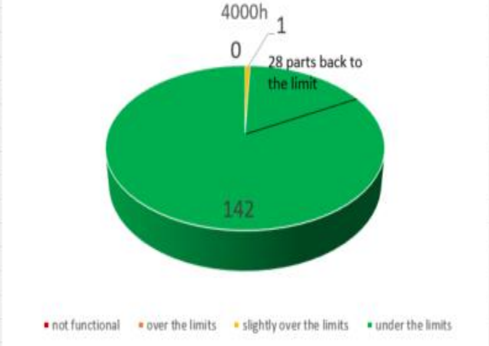
not functional 🟥
over the limits 🟥
slightly over the limits 🟨
inside the limits 🟩

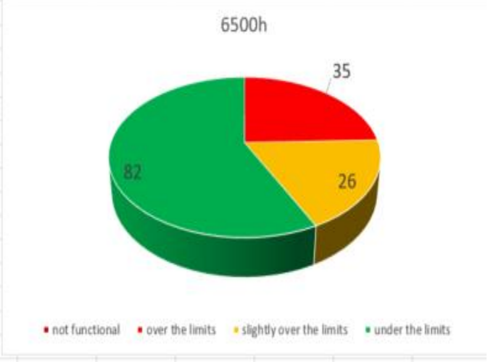
STRESS 2 1,2XVMAX, 125°C





For Ceram Cap DF:





First Wear Out phenomenon between **5500h and 6500h**: **So at the last steps of this study** whatever the stress applied

The 2 observed Failed at 2000h are identified as “stressed early failure” and not Wear Out (as β<1) explained by the overstress applied in temperature on lot1 DDR2 (150°C applied versus 85°C max datasheet)

PART 2 : PREDICTIVE MODELS

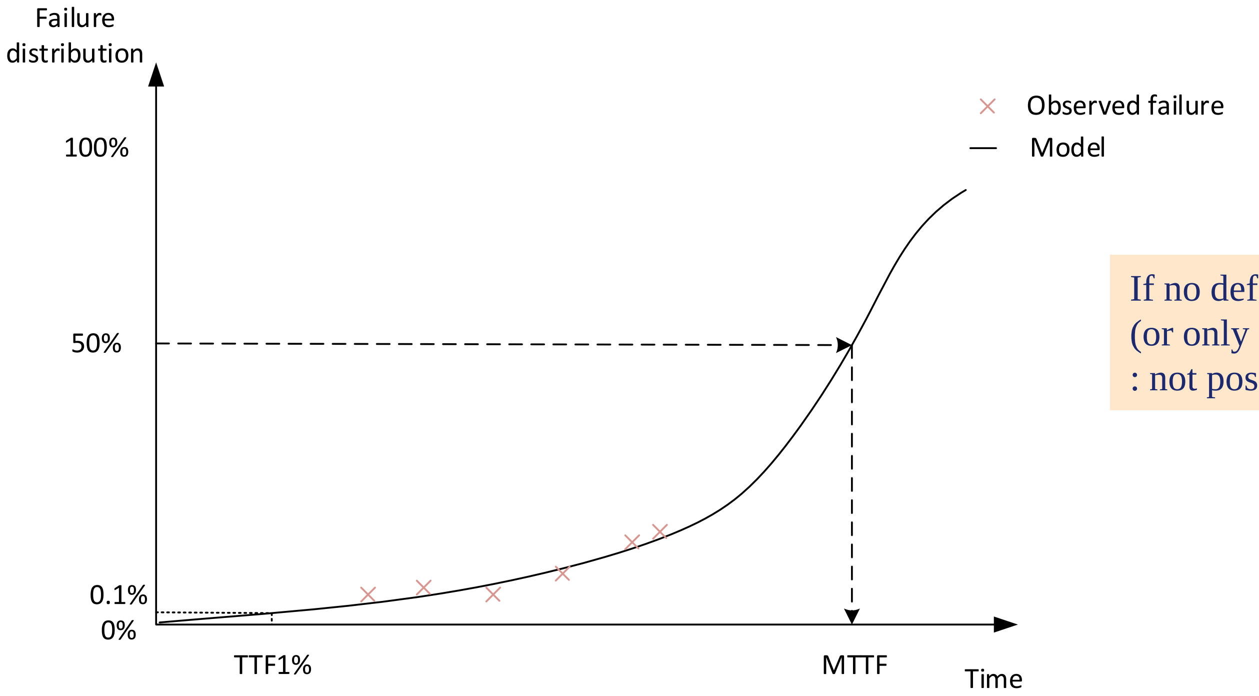
TWO MODELISATION APPROACHES

FAILURE DISTRIBUTION MODEL

Failure can sometime be obvious (part visually destroyed) but most of the time, the identification of a failure relies on a strict criterion for a given parameter.

The manufacturer’s datasheet is the base document to compare measured values with range specification for a given parameter.

As a consequence, when the datasheet shows no maximum or maximum value, no parametric failure can be identified.

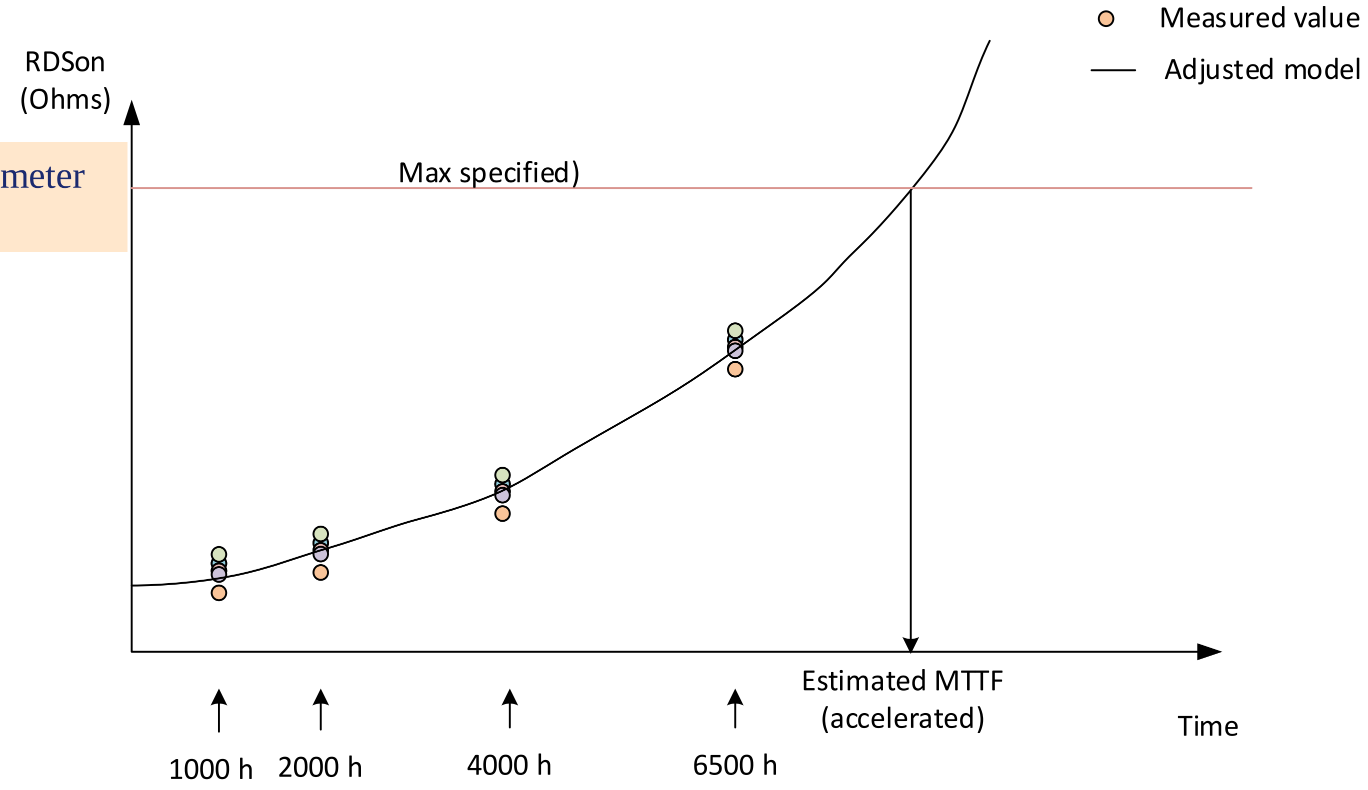


If no defect
(or only few)
: not possible to use

TWO MODELISATION APPROACHES CON'T

DEGRADATION MODEL

Using parameter drifts



The measured values are plotted versus time. The fitted mathematical model can then be extrapolated to the time when the parameter exceeds its specification. This lifetime is not the theoretical MTTF but it is considered a good approximation. An ideally fitted model with a symmetrical distribution of the parameter would lead to the MTTF.

PREDICTIVE MODEL TOOL

SAME TOOL for both models
(failure distribution & degradation)

The same tool is used for both modelling ways. **GENCAB**® tool from Cabinnovation is a powerful optimizing tool based on Microsoft Excel®. This tool allows to select the best set of parameter to optimize the result of an equation.

For failure distribution model the tool will maximize the likelihood of the observed data.

Weibull model is combined with Arrhenius and inverse power laws to account for accelerated stress conditions. GENCAB can process censored and uncensored data with heterogeneous stress conditions.

For degradation model, the tool will use the least square method to issue the best set of parameters that fit the model to the observed measurements for a selected parameter.

PREDICTIVE MODEL RESULTS

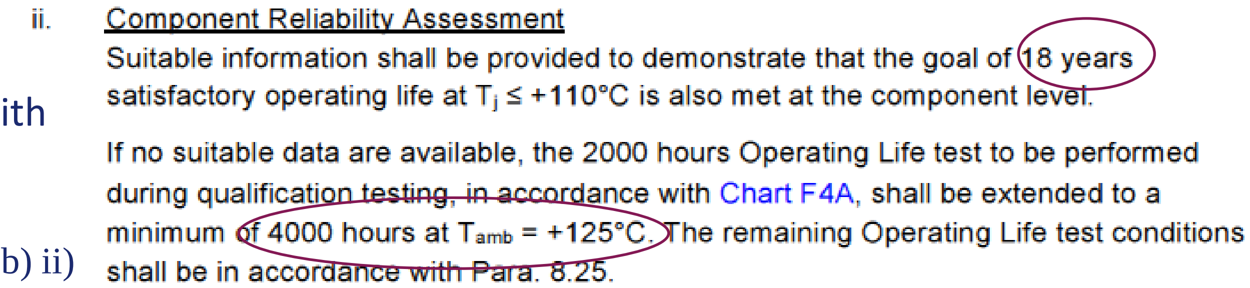
Reference	Extrapolation	Failure distribution model	Degradation model
Resistor (AEC-Q200 tested)	Failure distribution model was altered due to temperature and power stress conditions correlated Degradation model **from publication confirmed with adjusted parameters** Life time calculated for a set of application dependent criteria	Pu = 0.25 W; @60°C, TTF50% = 106000 h (12y), TTF1% = 14000 h (1,5y)	@ 60°C, 0.1% drift: **1525 years**
C0402 T2 100nF 16V Ceramic capacitor (AEC-Q200 qual)	No failure observed : no failure distribution model Degradation model **from publication confirmed with adjusted parameters** Life time calculated for a set of application dependent criteria	**No fail** to issue a distribution model	Fitted model from 125°C Aging tests @60°C 15% drift: **54 years** Using Arrhenius law with an activation energy of 0.1 eV :
tantalum capacitor (AEC-Q200 qual)	Weibull distribution model fitted but with large confidence intervals Little and non-monotonous degradation : no degradation model	Weibull distribution model Eu = 25 V; @60°C), global acceleration factor is 0.064: TF50% = 5300 h TTF1% = 3500 h If all failures occur at the end of the interval, Ea : 0.2: TTF50% = 84000 h (9y) TTF1% = 55000 h (6y) **No fail** to issue a distribution model	There is not enough measurement time and **not enough capacitance variation** to issue a degradation model**.** **Solid tantalum are known for their long term stability**
MOSFET	No failure observed : no failure distribution model Little degradation : no degradation model	**Using Arrhenius** law with an activation energy the equivalent time of the life test is Ea = 0.15eV 6500*3 = 2.22 years @ 60°C for the oven at 150°C 6500*2.34 = 1.7 years @ 60°C for the oven at 125 °C using χ^2 law with a 60% confidence level. Dev.hours = **868000 h (99 y)** with no failure observed. Failure rate = 1054 Fits @ 60°C	**No noticeable drift is observed. No degradation model is possible.** **Power MOSFET are well known for their long term stability.**
operational amplifier	Weibull distribution model fitted but with large confidence intervals Little degradation : no degradation model	Eu = 10 V; Tu = 60°C: TTF50% = 150000 h, TTF1% = 20000 h If all failures occur at the end of the interval, Ea : 0.41: TTF50% = 540000 h **TTF1% = 160000 h (18y)**	**Degradation model is not possible** because measured parameters do not highlight any monotonous drift for any parameter
1Gb x16 DDR2 SDRAM **Lot 1 (85°C grade)** **Lot 2 (105°C grade)**	Weibull distribution model fitted with large confidence intervals but reveals early failures	Lot 1 : Due to SN118 and probably also to SN104. The obtained parameters don't build a wear out model. Lot 2: **The tool algorithm didn't succeed to find a correct wear out model** due to early failures, too large censored intervals and only two stresses combinations	**None**

PART 1 CONCLUSION : STRESS TESTS

WHAT TO SAY SINCE LAST ACCEDE 2022?

1- Resistors
2- Ceramic capa
3- Tantalum capa
4- MOSFET
5- AOP
6- DDR2

Comparison with
ESCC9000
req. for Hirel
(ESCC9000 4.2.1 (b) ii)



ii. Component Reliability Assessment

Suitable information shall be provided to demonstrate that the goal of 18 years satisfactory operating life at $T_j \leq +110°C$ is also met at the component level.

If no suitable data are available, the 2000 hours Operating Life test to be performed during qualification testing, in accordance with Chart F4A, shall be extended to a minimum of 4000 hours at $T_{amb} = +125°C$. The remaining Operating Life test conditions shall be in accordance with Para. 8.25.

OSIP Wear Out project ended after 6500 h in June 2023

Some Wear Out could be seen at the last steps (5500/6500 h) except for Ceramic capacitor and MOSFET

For active **DDR2 :Wear Out test fails** occurred at 5500 h/6500 h @150°C **so it passes** the 4000 h @125°C (compared to ESCC9000 requirements on Hirel for instance)

PART 1 CONCLUSION : STRESS TESTS (con't)

Reference	Tests results - Aging/Wear Out
resistor (AEC-Q200 tested)	Aging effect: R decreases @25°C
	Aging / Wear Out effect for the 3 parts slightly beyond the limit for some parts
Ceramic capacitor (AEC-Q200 qualified)	Aging effect: C decreases (remains in the limits) @25°C. DF is slightly beyond the limit for some parts after 1000h and 2000h but it remains inside the limit after 4000h, slightly passed the limit again after the 6500h.
	No Wear Out
Solid tantalum capacitor (AEC-Q200 qualified)	Aging effect: ESR increases. Also an increase of the current consumption is observed, with a "recovering effects" during Read&Record.
	Wear Out : ESR beyond the limit after 6500h (major parts after stress test 25V@150°C and for some parts after stress tests 30V@150°C).
MOSFET	Aging effect : increases of 3% RDS(on) tested at @125°C after both aging conditions, on the last step after the 6500 hours
	No Wear Out
Rail to Rail operational amplifier	Aging effect : VOS increases@25°C after the stress2 (14.4V@125°C). Still in the limit.
	Wear Out: The input offset Current significantly increased on all parts aged at Vnom+20% and 125°C (above the limit), after the 6500h
1Gb x16 DDR2 SDRAM	Aging effect : Power consumption increases @25°C on some parts from both stress tests
	Wear Out : during the last Read&Record after the 6500h@150°C, 8 parts were non-functional (5 seen during monitoring at 5500h, 3 between 6000h and 6500h)

This study has **successfully shown aging effects for all the 6 families** and **Wear Out on 4 families** (parts beyond the limits or not functional) after 5500/6500h stress tests. It gives **good confidence on the parts chosen from commercial market (COTS) for the use on 15y Space applications**

PART 2 CONCLUSION: PREDICTIVE MODELS

Recommendations

- Manufacturer specification should be thoroughly analyzed to identify parameter limits used as **failed/pass criteria**.
- **Board design should be optimized** to observe failure frequently and isolate a part in case of failure.
- Modelling process needs at **least 50% failure observed** for acceptable confidence intervals.
  - **Increased stress or duration**
- Modelling process needs precise time of failure for acceptable confidence intervals.
  - Instant measurements or **short measurement intervals**
- aging tests should include **more combinations of stress** to allow the optimizing tool to detect the effect of each stress.

Ideas !

More monitoring points on different parameters and one for each serial number (additional cost)
For instance, leakage current on each tantalum capacitors.
Finding beyond the limits have to be studied regarding application to see if it can be acceptable up to the end of the mission.

Casting & Organization

THALES ALENIA SPACE for project management,
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(Nathalie Jaussein, Laurent Castel)
THALES SIX for boards design, manufacturing & tests
(Julien Coutet)
ESA OSIP organization & follow up (Joaquin Jimenez)

THANK YOU!

Thales SIX GTS France SAS

OSIP