

Opportunities for COTS SiC JFETs in space power applications

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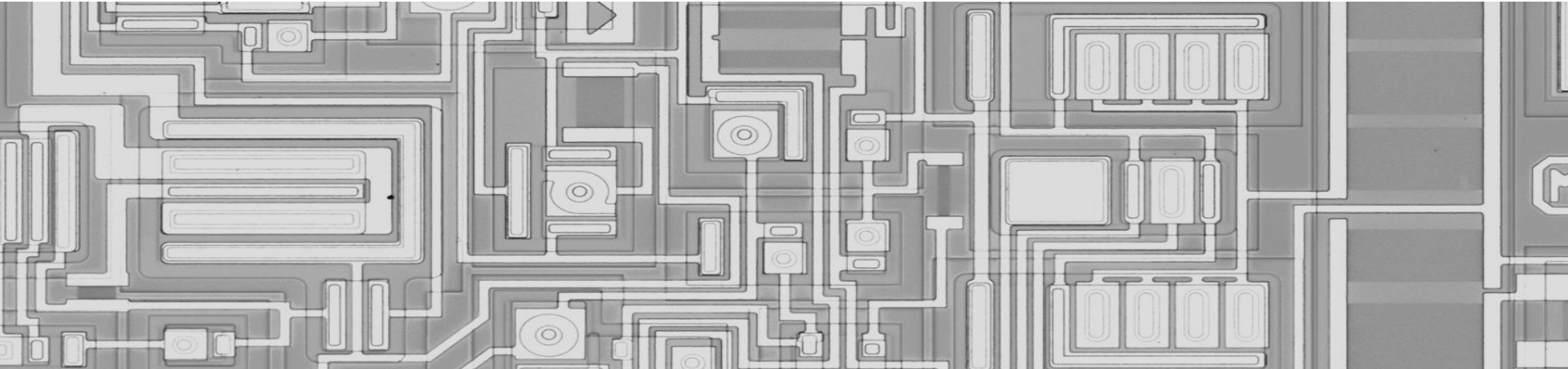
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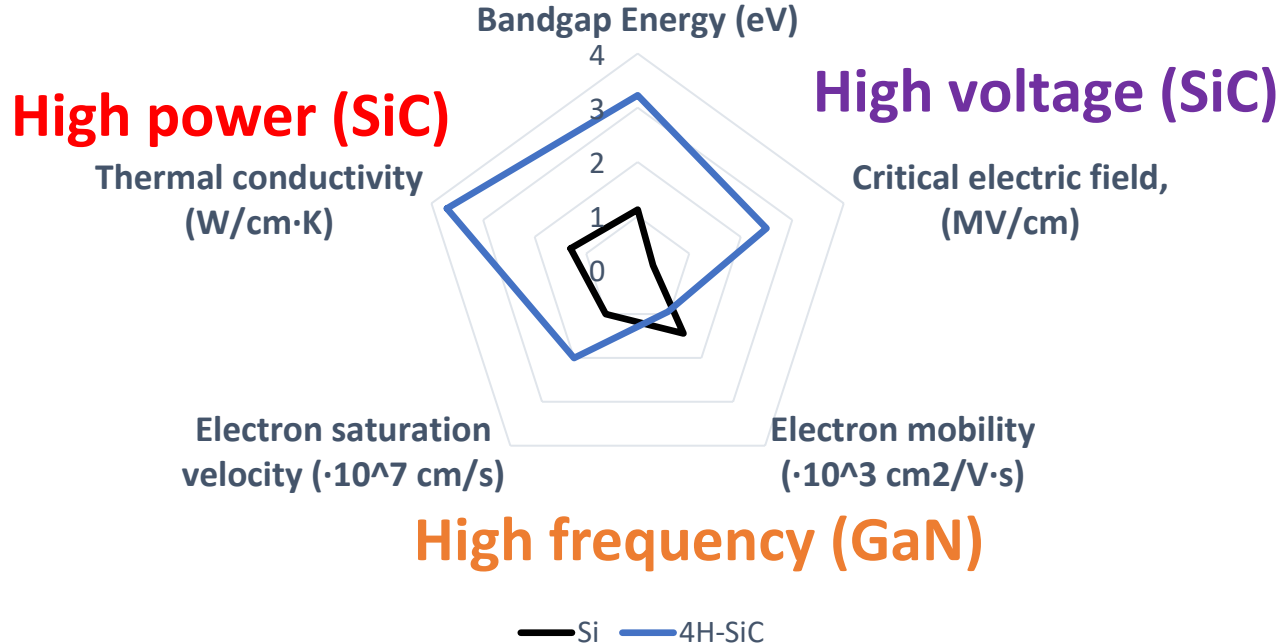


Space Power & Electronic Systems



Introduction

Silicon Carbide (SiC) offers much **better performance** than Si in power conversion: **Are there opportunities for SiC power devices in space applications?**



Power levels & applications & power semiconductor technology

Regulated bus	Unregulated bus		
Bus voltage	Bus voltage	Power	Standard
28V		< 1.5kW	ECSS-E-ST-20C AS5698 AIAA S-122
	22V – 38V 23V – 36V		ECSS-E-ST-20-20C AS5698
50V		< 5kW	ECSS-E-ST-20C AIAA S-122
	32V – 52V		ECSS-E-ST-20-20C
70V		< 10kW	AIAA S-122
100V		< 20 kW	ECSS-E-ST-20C AIAA S-122
120V			ECSS-E-ST-20C AS5698
	98V – 136V		AS5698

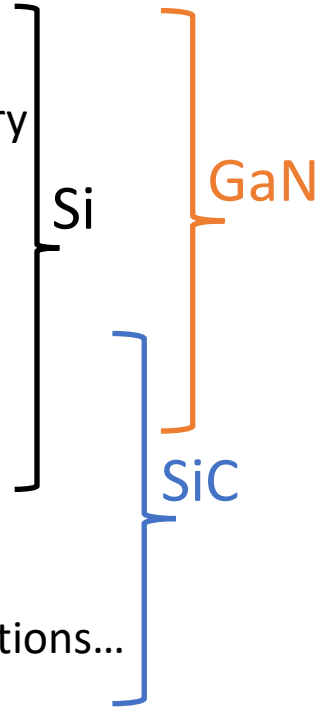
Applications

LEO satellites, interplanetary probes...

Telecom GEO satellites...

Large satellites, Electric Propulsion, ISS...

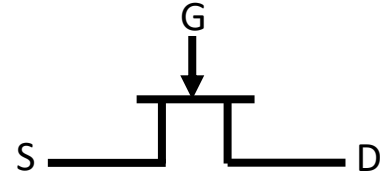
HP electric prop., space stations...
Microgrids (Lunar, Mars...)



Power semiconductor: basic requirements

- Maximum voltage **PASS**
- Conduction and switching losses **PASS**
- Normally-off device (transistors) **FAIL**

SiC JFET



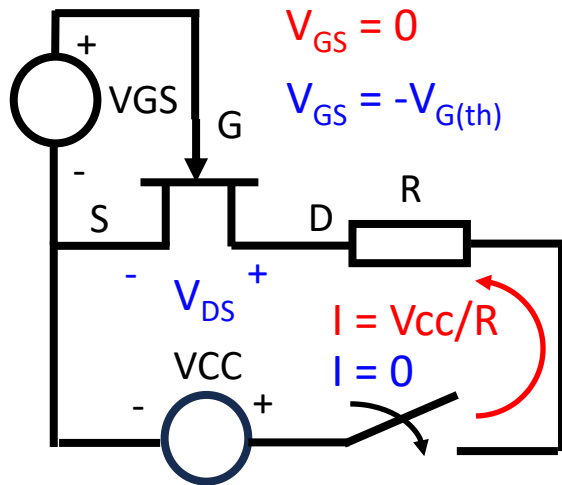
COTS for space applications: additional requirements

- Robustness and reliability
 - Temperature **TO STUDY**
 - Radiation (TID & SEE) **TO STUDY**
 - Electrical stress **TO STUDY**
- Availability & traceability **PARTLY**
- Versatility (technology building blocks) **TO STUDY**

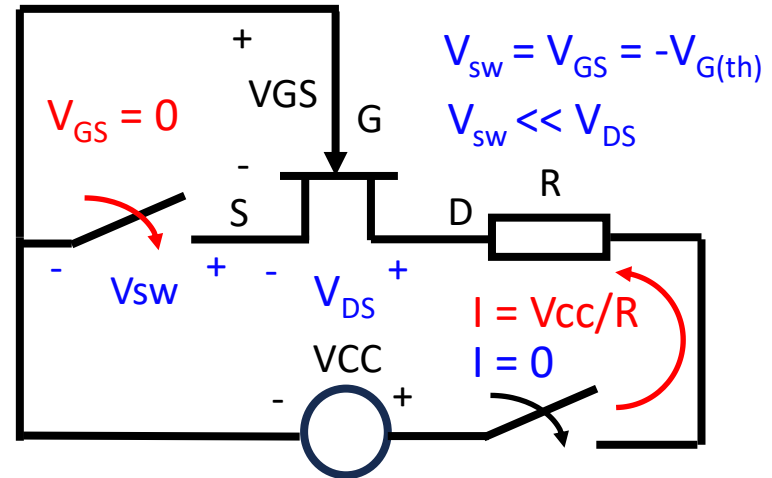
Normally-on to normally-off device: cascode configuration

- Serialization of a depletion mode normally-on device (i.e. $V_{GS} < 0V$ to turn-off) and a control device, transforming the arrangement into a normally-off device

SiC JFET: normally-on

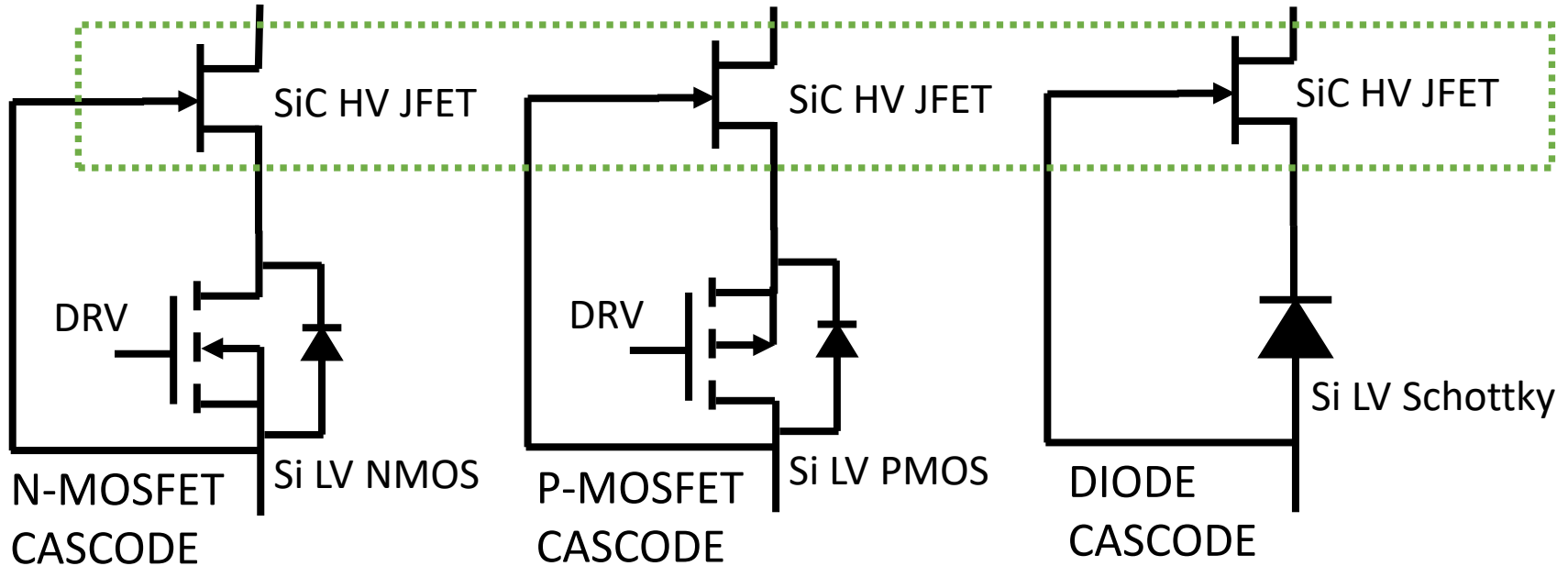


SiC JFET cascode: normally-off



Cascode configuration: some interesting features (II)

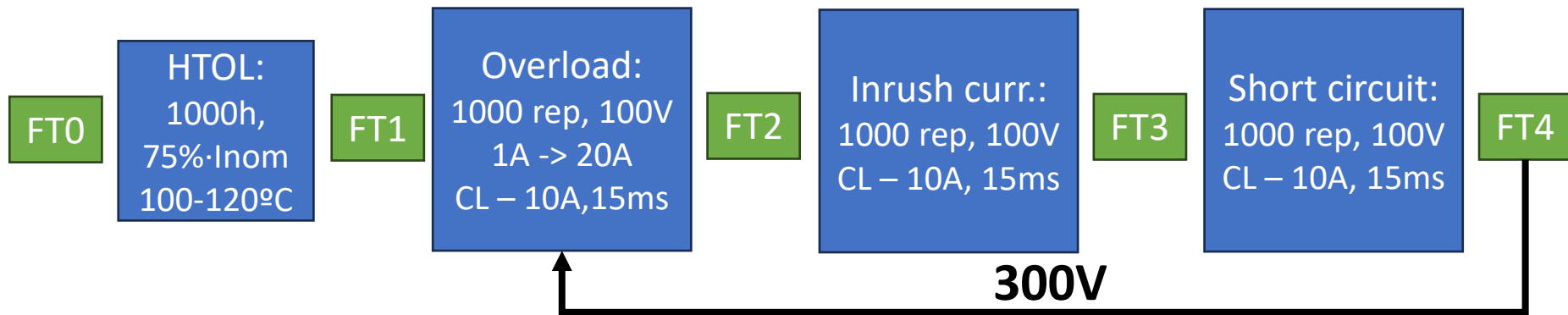
3) Basic power switches can be implemented using different control devices



ALL BASIC POWER PROCESSING FUNCTIONS COVERED WITH THE SAME HV DEVICE

SiC JFET test campaign: Electrical stress

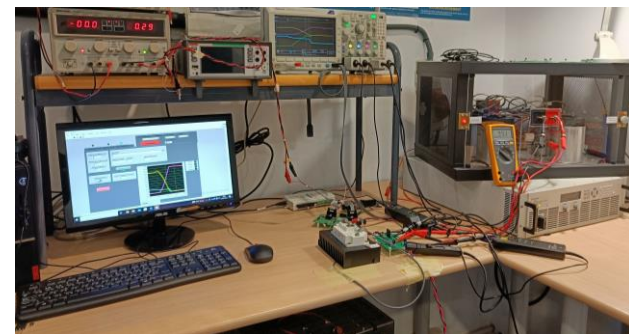
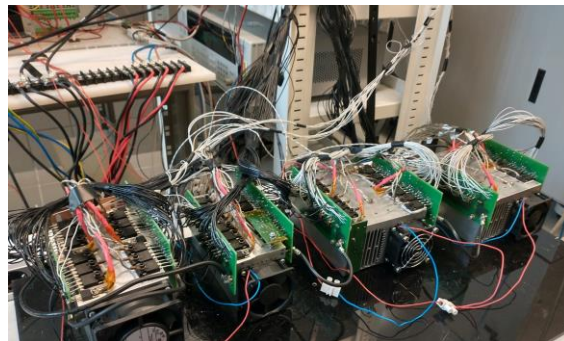
4 SiC JFET refs.
16 devices / ref



VNIVERSITAT
DE VALÈNCIA



UNIVERSITAS
Miguel Hernández



SiC JFET test campaign: TID & SEE



4 SiC JFET refs.
12 devices / ref

FT0

TID:
Co-60, 1.25 MeV, 200krad (Si)
Conduction state
On-line monitoring: V & I

FT1



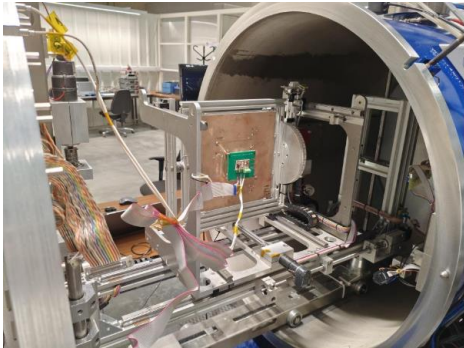
ALTER

1 SiC JFET refs.
6 devices

FT0

SEE:
UCL, Cyclone
Blocking state
 I_{DS} monitoring, V_{DS} stepping
Ions (Ar, Ni, Kr, Xe)

FT1



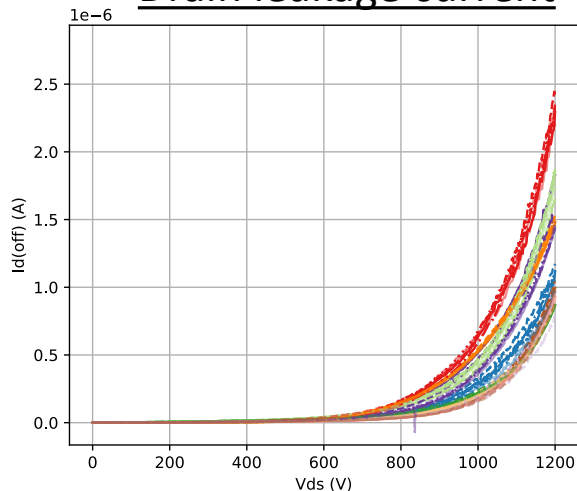
Electrical stress tests: results (I)

- Superimposed curves after each characterization of the devices (FT0 – FT5)

Output characteristics: $I_{d(off)}$ vs V_{DS}

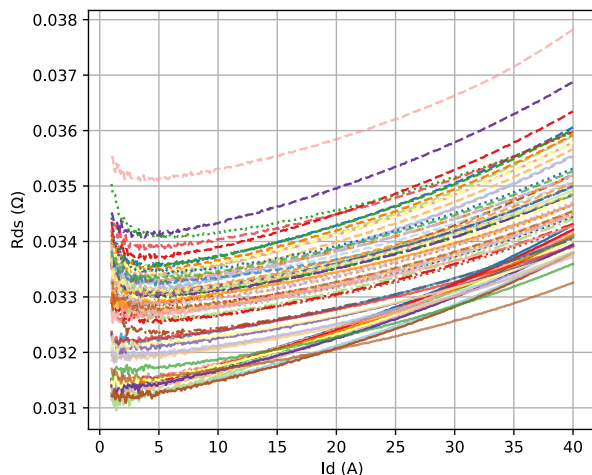
Input characteristics: $I_{d(off)}$ vs V_{GS}

Drain leakage current



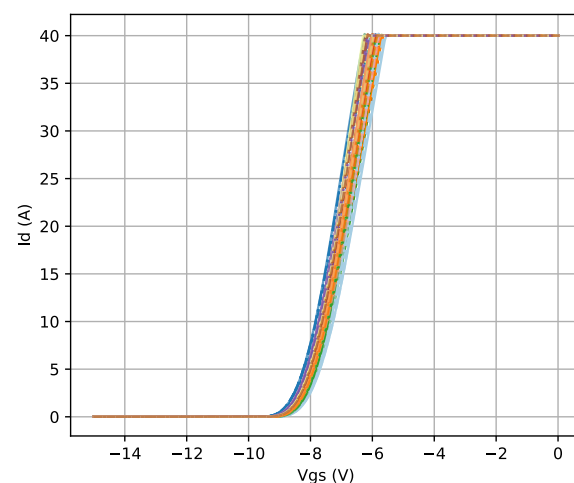
VGS= -20V, Tamb.
 Datasheet NOM: $I_{d(off)}$ = 10 μ A
 Datasheet MAX: $I_{d(off)}$ = 60 μ A

ON resistance



VGS= 0V, I_d max =0 to 40A, Tamb.
 Datasheet NOM: $R_{ds(on)}$ =35m Ω
 Datasheet MAX: $R_{ds(on)}$ =45m Ω

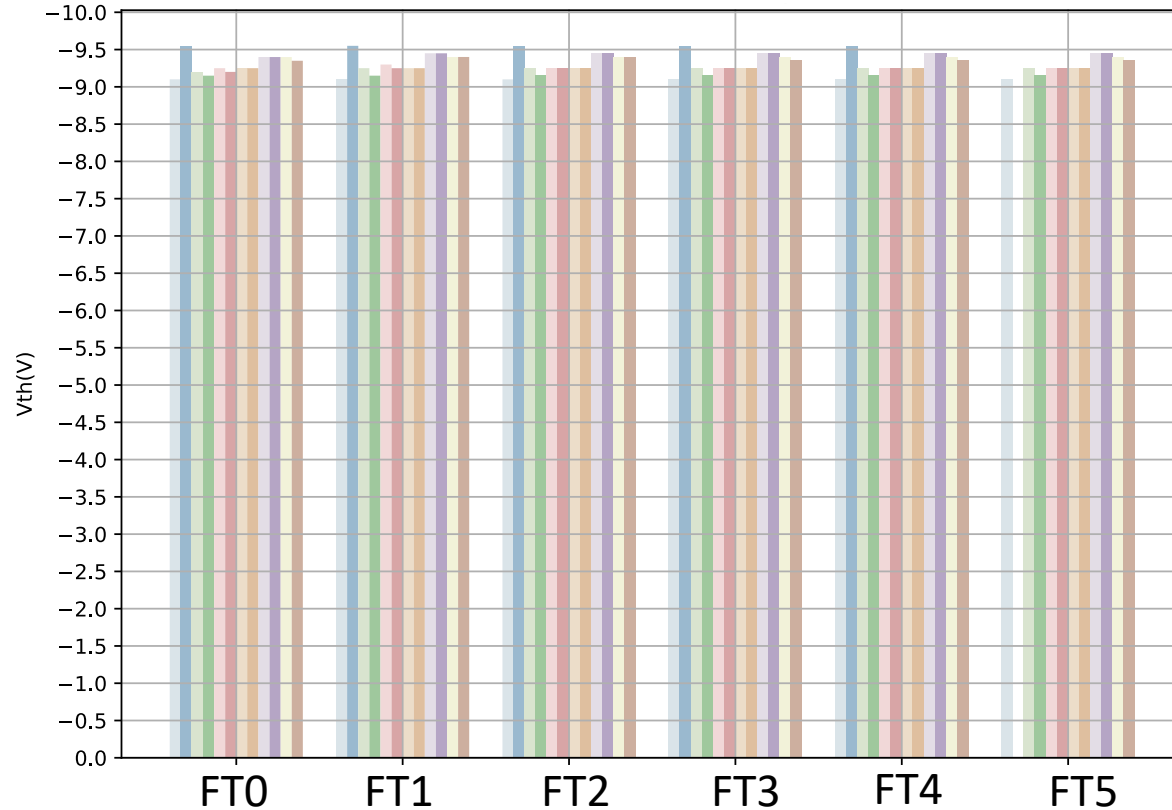
Transconductance and Vth



VGS= -20V to 0V,
 I_d max =40A, Tamb.

Electrical stress tests: results (II)

- Threshold voltage V_{TH} after each test (FT0 – FT5)



Method $I_d(V_{th}) = 10\text{mA}$

Total Ionizing Dose tests: results

- Superimposed curves pre and post irradiation (FT0 – FT1)

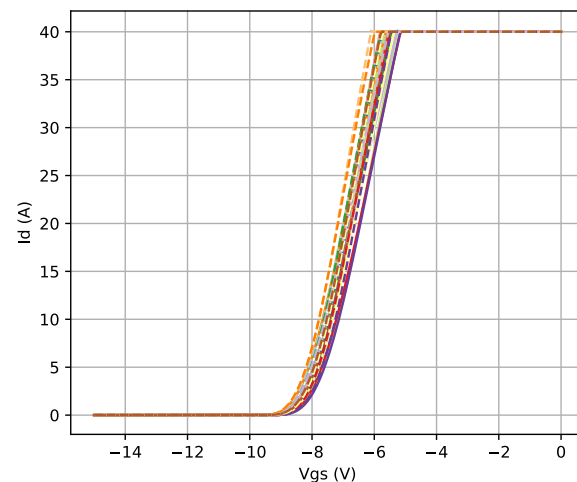
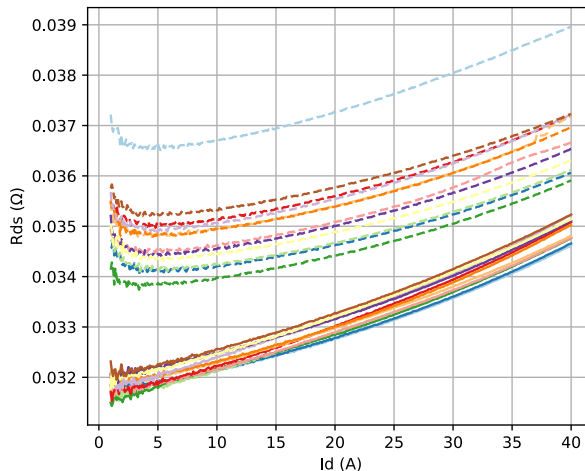
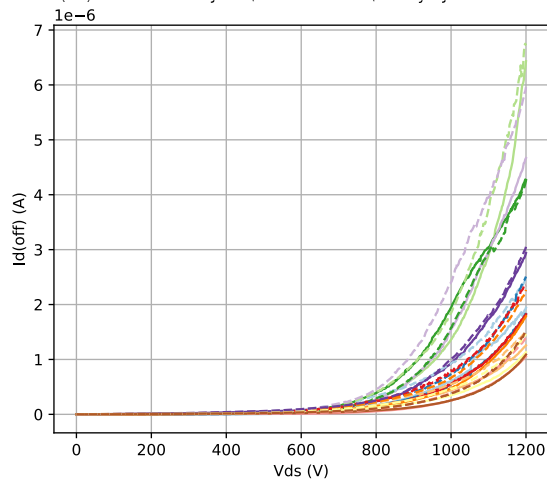
Output characteristics: $I_{d(off)}$ vs V_{DS}

Input characteristics: $I_{d(off)}$ vs V_{GS}

Drain leakage current

ON resistance

Transconductance and V_{th}



VGS= -20V, Tamb.

Datasheet NOM: $I_{d(off)}$ = 10 uA

Datasheet MAX: $I_{d(off)}$ = 60 uA

VGS= 0V, I_d max =0 to 40A, Tamb.

Datasheet NOM: $R_{ds(on)}$ =35mΩ

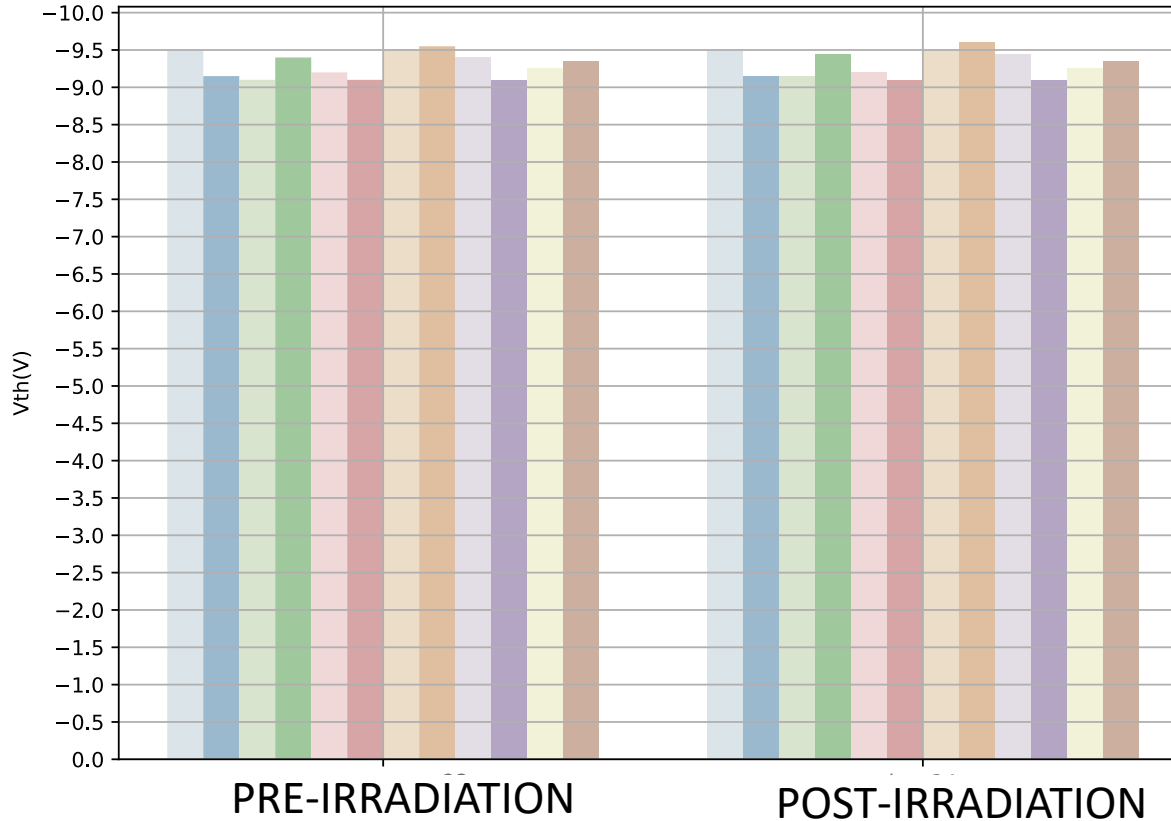
Datasheet MAX: $R_{ds(on)}$ =45mΩ

VGS= -20V to 0V,

I_d max =40A, Tamb.

Total Ionizing Dose test: results (II)

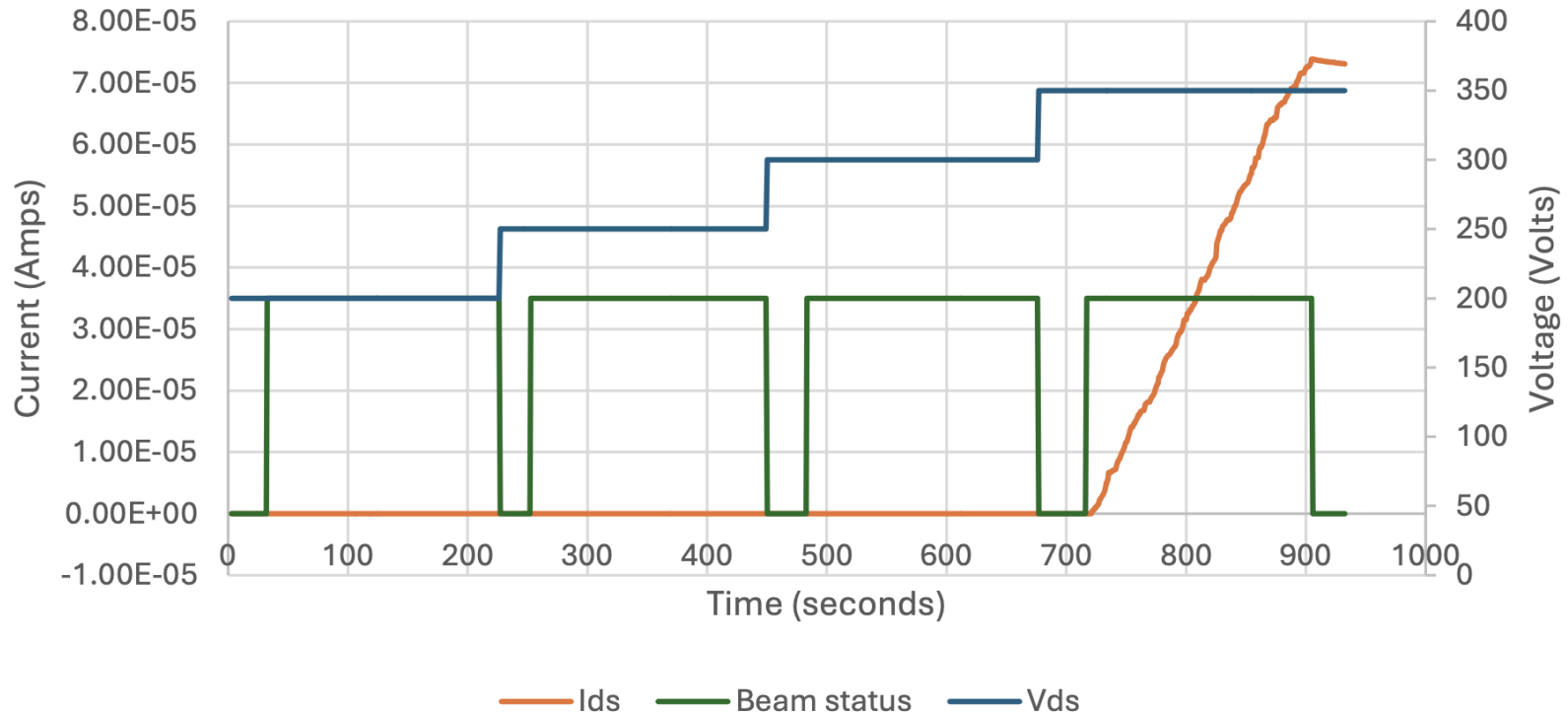
- Threshold voltage V_{TH} after each test (FT0 – FT1)



Method $I_d(V_{th}) = 10\text{mA}$

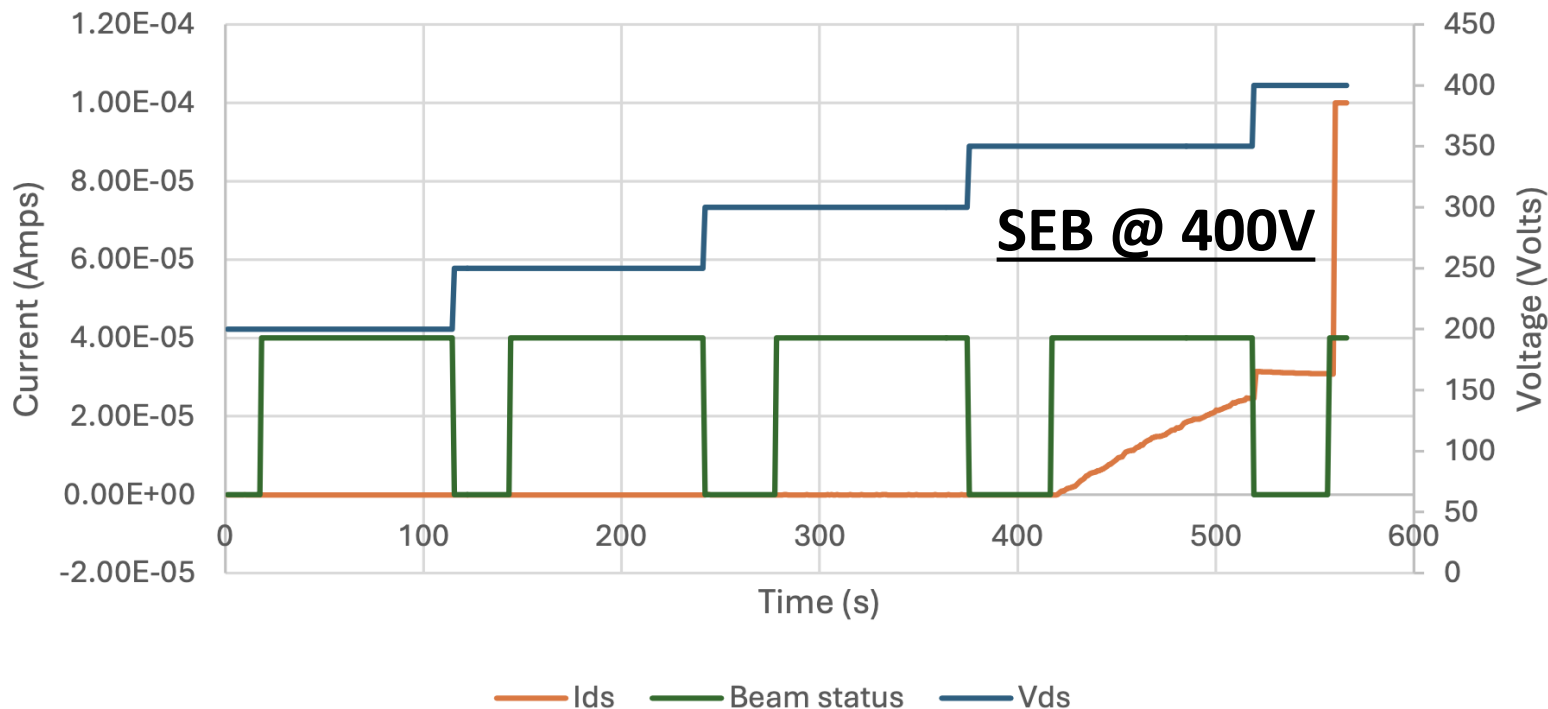
Single Event Effects test: results (I)

- Xe, 995 MeV, LET (Si) = 62.5 MeV cm²/mg, 1000 ions/s/cm²
- I_{DSS} stable up to 300V, 0.37uA/1000 ions @ 350 V, PIGS passed

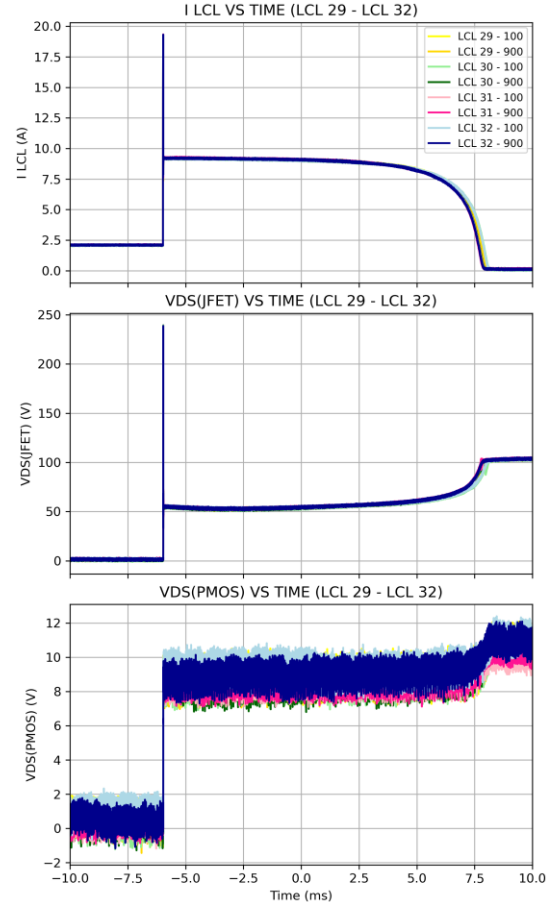
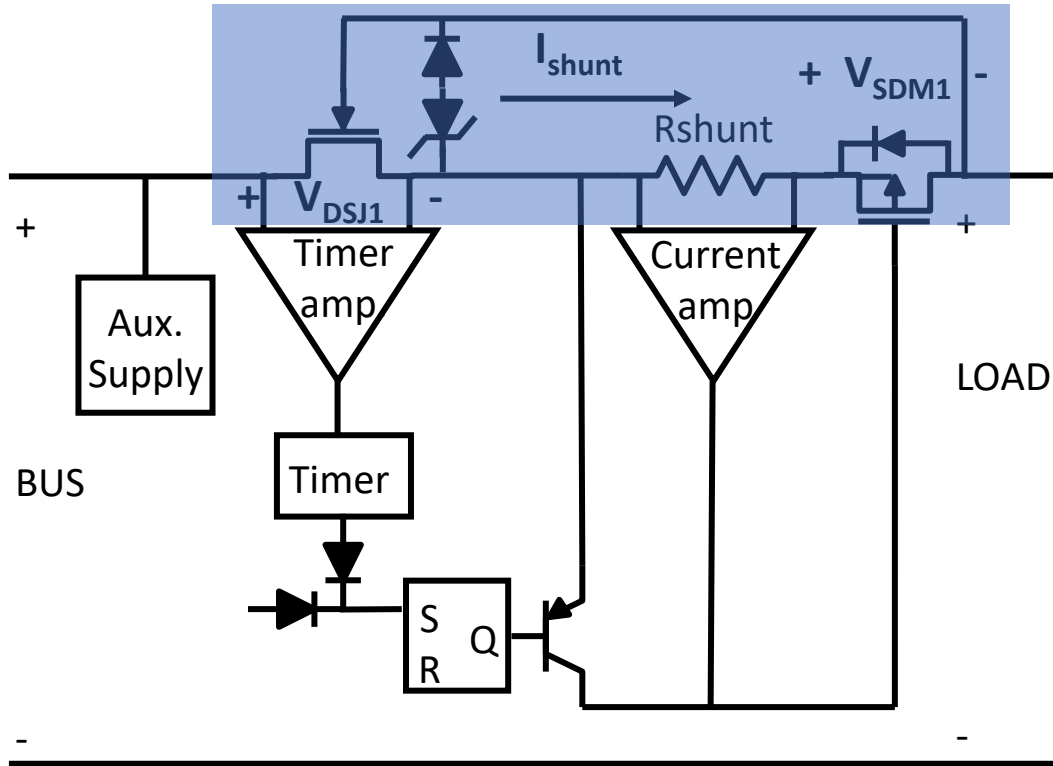


Single Event Effects test: results (II)

- Kr, 769 MeV, LET (Si) = 32.4 MeV cm²/mg, 2000 ions/s/cm²
- I_{DSS} stable up to 300V, 0.115uA/1000 ions @ 350 V, PIGS passed

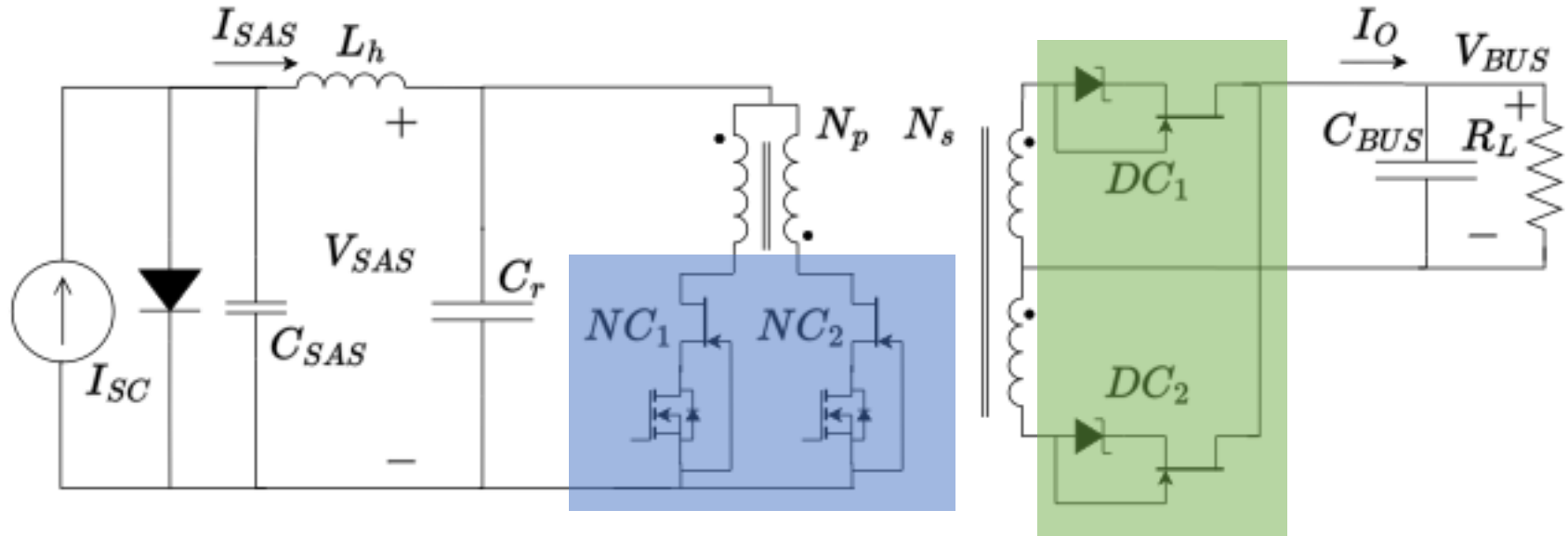


Application P-MOSFET cascode: Latching Current Limiter



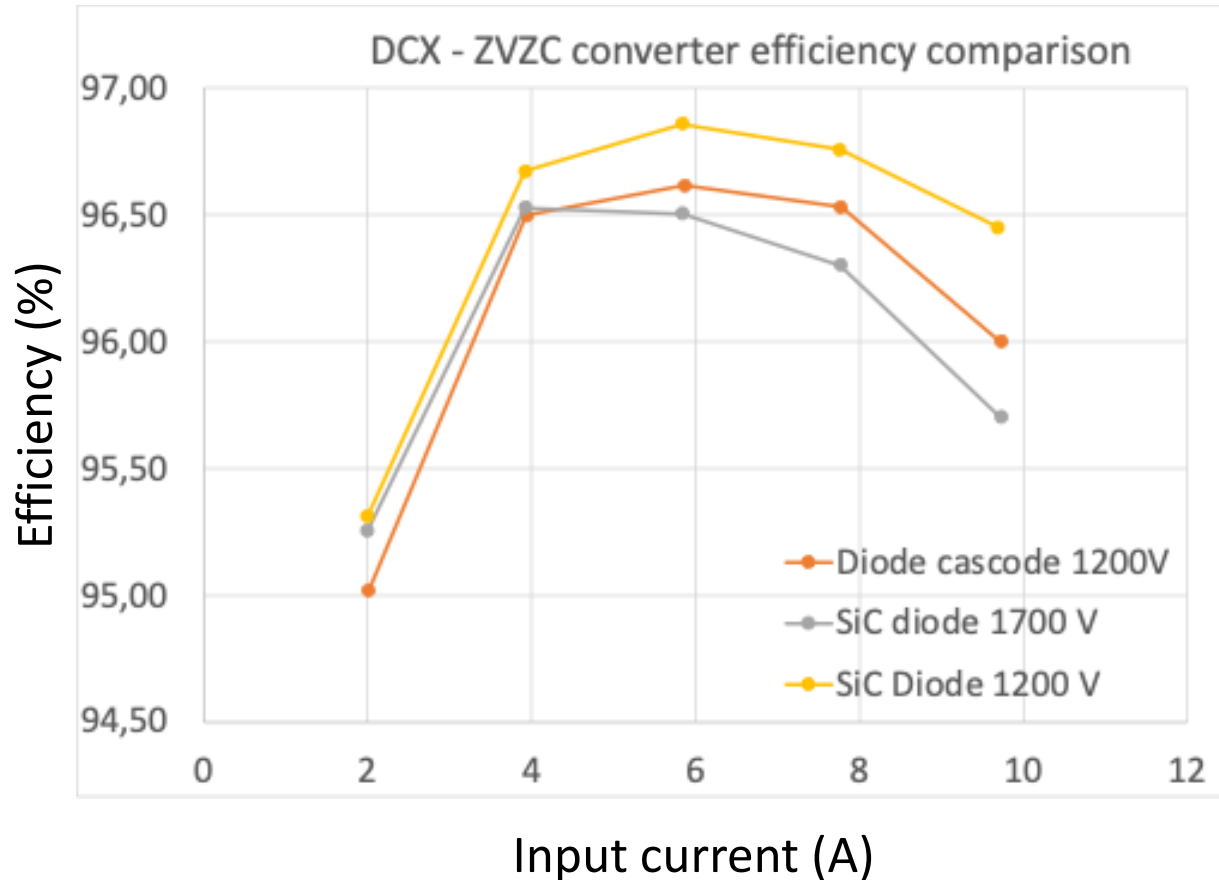
✓ The LCL has been stressed with **5.000 current limiting events** with no failure (at **100V** and **300V**)

Application N-MOSFET cascode and diode cascode: SAR-DCX



- ✓ Push-pull structure: primary & secondary
- ✓ 100V to 300V (1:3 transformer)
- ✓ ZVS and ZCS converter
- ✓ All SiC JFET cascode

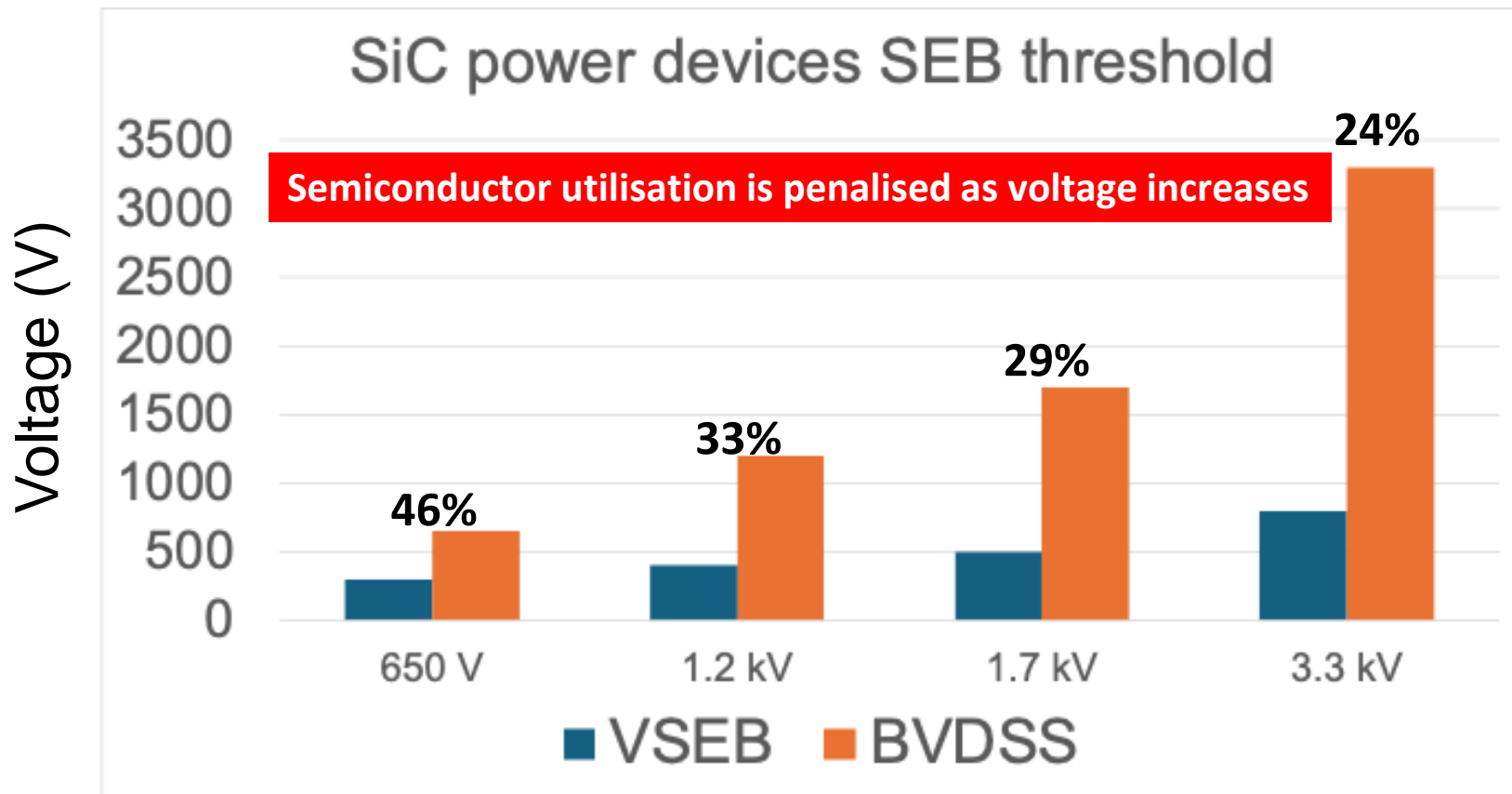
Application N-MOSFET cascode and diode cascode: SAR-DCX results



Measurement conditions:

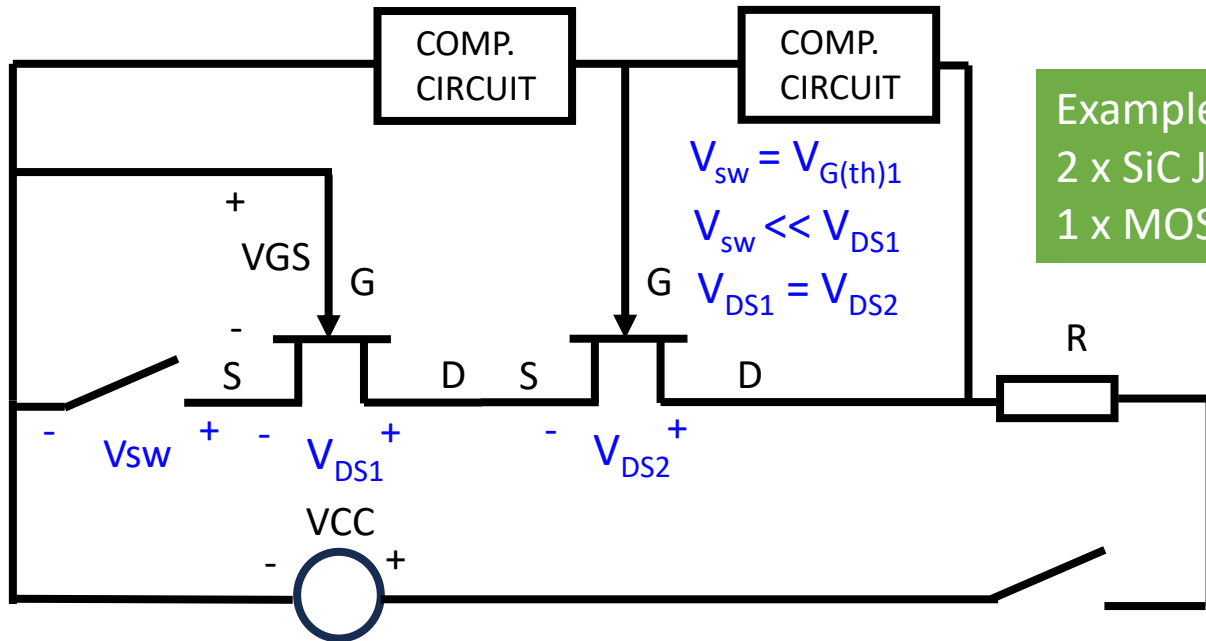
- $V_{in} = 100 \text{ V}$; $V_o = 300 \text{ V}$
- Similar t_{on}
- Different switching frequency

Next steps: very high voltage applications



Next steps: very high voltage applications

- Supercascode: serialization of more than one depletion mode normally-on device (i.e. $V_{GS} < 0V$ to turn-off) and a control device.



Example:

2 x SiC JFET 1.2 kV \rightarrow VSEB=800V
 1 x MOSFET 3.3 kV \rightarrow VSEB=800V

Conclusions

- High voltage, high current power devices are demanded for future space applications: **WBG power devices**.
- SiC JFET is a competitive alternative: **robust and basic building block**.
- SiC JFET cascodes: **versatile**.
- SiC JFET supercascodes: **SEB**.

Thank you for your attention!!!

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