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ACCEDE I ESCCON

2025 Seville, Spain 25 - 27 March

SESSION:
COTS Component manufacturer updates

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3D PLUS

Talk:

MNEMOSYNE Project RHBD Non Volatile Memory ASIC.

MNEMOSYNE

A RHBD Non Volatile Memory ASIC

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Seville, ACCEDE I ESCCON

March, 26th, 2025

Public Information

AGENDA

- INTRODUCTION
- TEST VEHICLE
- PROTOTYPE
- SUMMARY

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INTRODUCTION

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1 CONTEXT

EU Horizon 2020 program for research and innovation

European Commission

3D plus a HEICO company

imec

TRAD Tests & radiations a HEICO company

NanoXplore

beyond gravity

1 REQUIREMENTS

- **Non volatile memory with SPI interface**
- **High Density**
- **Radiation Immune**
- **Developped by 3D PLUS** in the frame of Horizon 2020 : an EU research and innovation program
- **Fully manufactured in Europe**
- **Cross validated by Space Electronics Experts:**

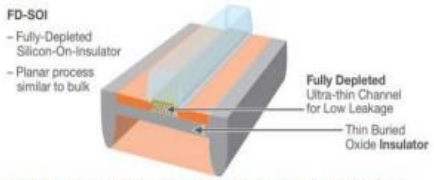
  3D PLUS, IMEC, Padova Uni, TRAD, Beyond Gravity, NanoXplore,
- **Applications:**
  - FPGA boot and bitstream storage
  - Code storage for microcontrollers & processors

1 TECHNICAL OBJECTIVES

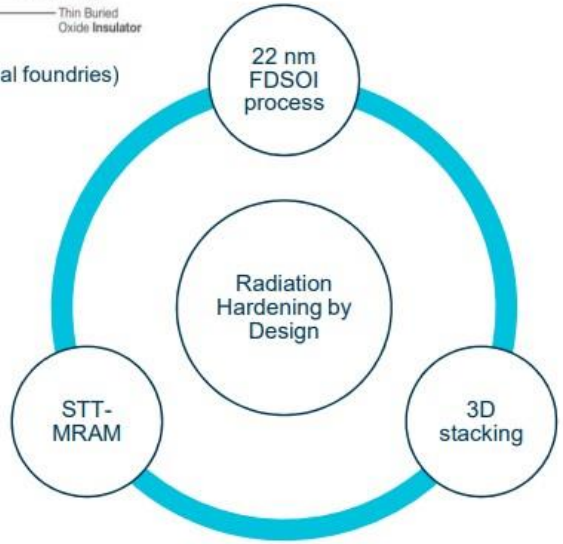
- Identify and analyse the process & circuit radiation sensitivity and verify the memory cells SEU/SEL immunity on the STT-MRAM FDSOI process.
- Mitigate the risks of TID which degrade the performance and lead to functional failure at component level.
- Mitigate the risk of SET/SEFI leading to component level data loss or functional error.
- Strengthen the reliability (temperature, data retention, life time) to reach space requirements.
- Design the control logic and interface around the MRAM to adapt to space design requirements.

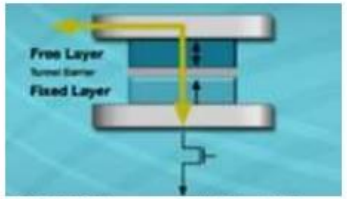
TECHNOLOGY EVALUATION

Design Trade-offs



FD-SOI Technology (Credit Global foundries)

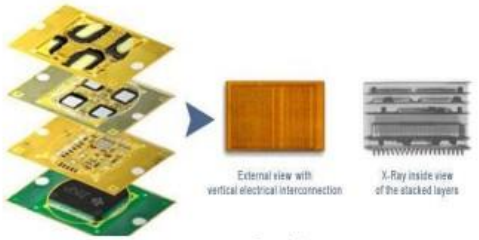




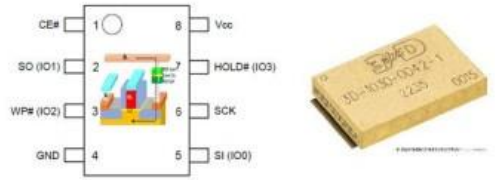
STT-MRAM Memory Cell (Credit Everspin)

- **SEU immune Memory cell**

- **SEL immune chip**
- **Rad Hard Digital library**
- **Mature, reliability** proven and commercially available in Europe
- **40% die scaling, and 70% power saving** vs 28 nm



3D stacking (Credit 3D PLUS)



- To achieve **higher densities**

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64 MBIT TEST VEHICLE

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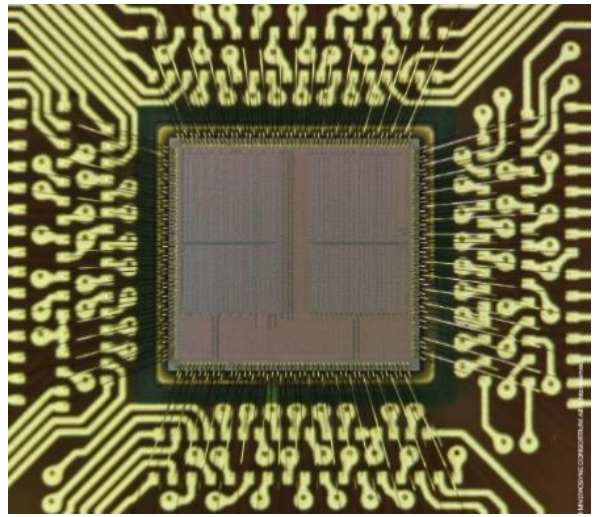
2 RADIATION TECHNIQUES ON DESIGN

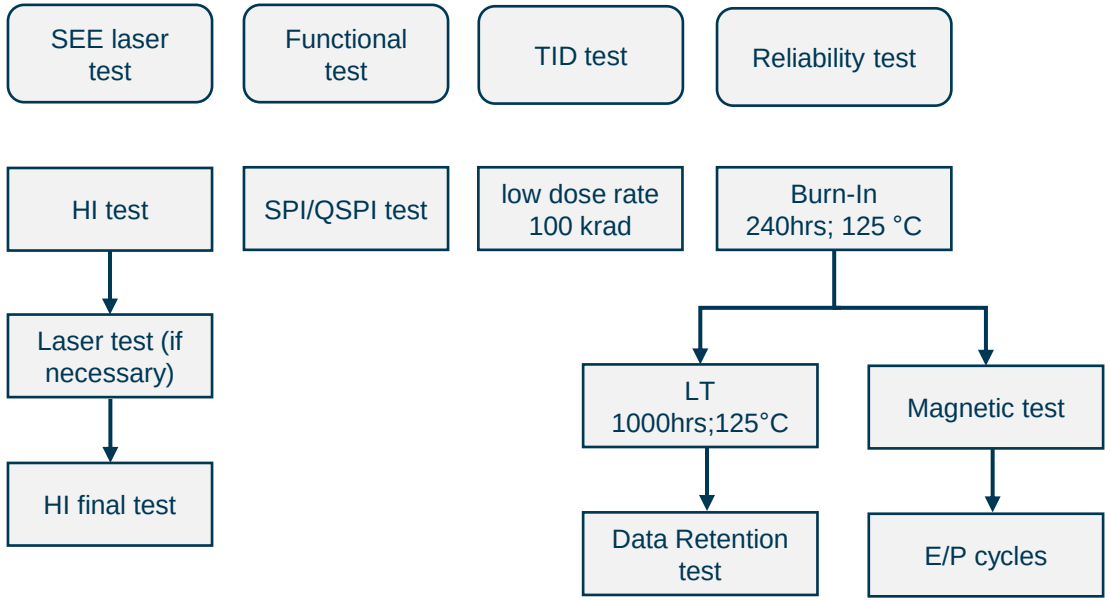
- Body-bias techniques to reduce leakage
- Rad hard design techniques on control logic and interfaces
- TMR
- SET immune cells on clock and reset trees
- Glitch filters on strategic nodes
- Derating accounting for device aging and TID.



64 Mbit Test Vehicle ASIC

2 TEST VEHICLE

Tests and results



Results	Conditions
TID > **60 krad(Si)**	60Co Source
SEL/SEU Leth > **60 MeV.cm²/mg**	
Laser test: **SEE sensitive pints located**	
1000 hours Life test: **pass**	@125 °C 3 teta measurements
1000 Gauss X-axis: **pass** 500 Gauss Y and Z-axis: **pass**	Static field
Magnetic field > **1000 A/m**	Power Frequency
Functional test: **pass**	SPI 1V8 interface

128 MBIT PROTOTYPE

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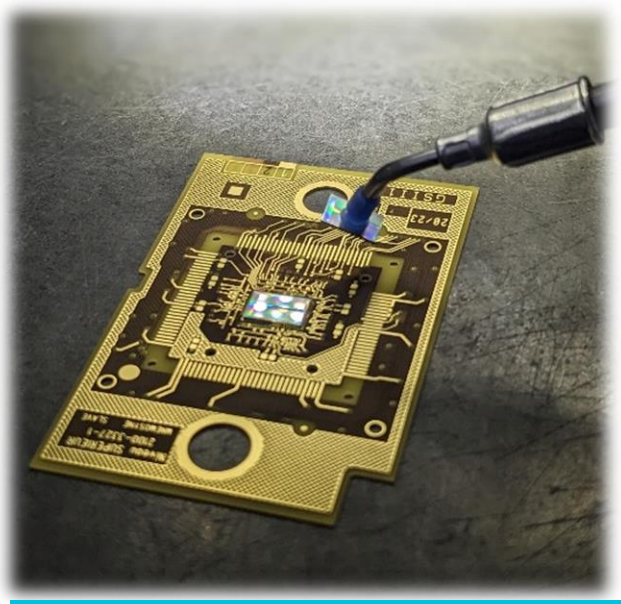
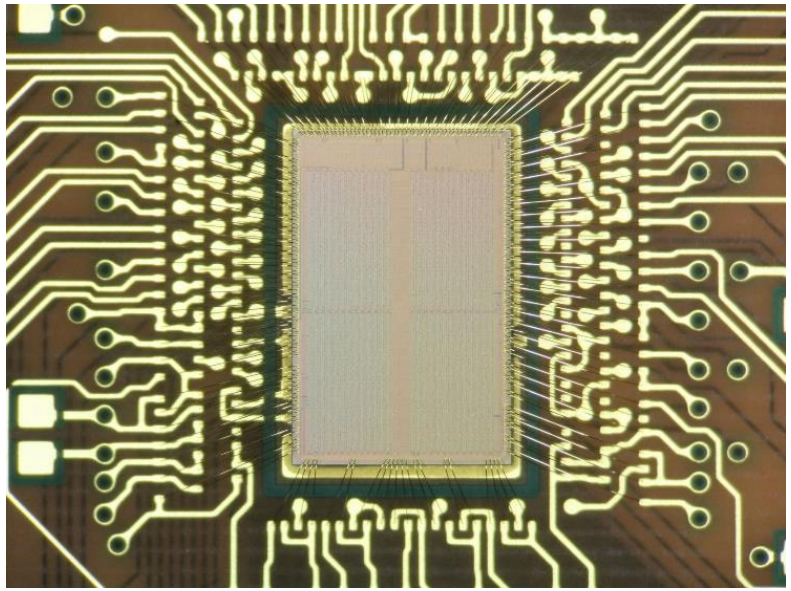
3 PROTOTYPE ASIC

- Correction of blocks showing SEE sensitivity
- Addition of parallel interface (3V3 EEPROM)
- Increase of the density:

  64 Mbit → 128 Mbit

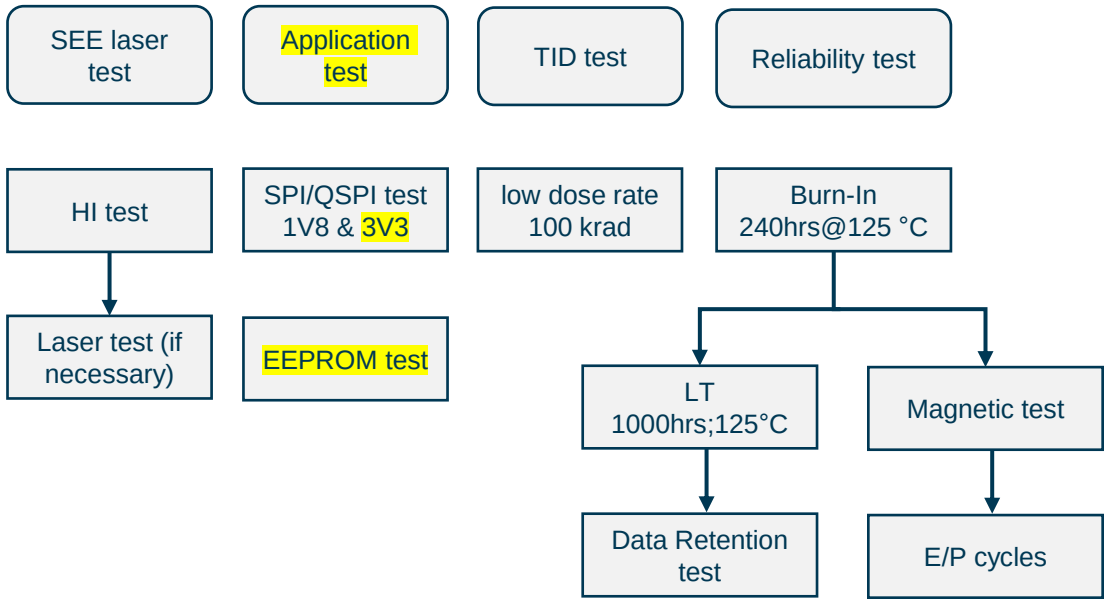




128 Mbit Prototype ASIC

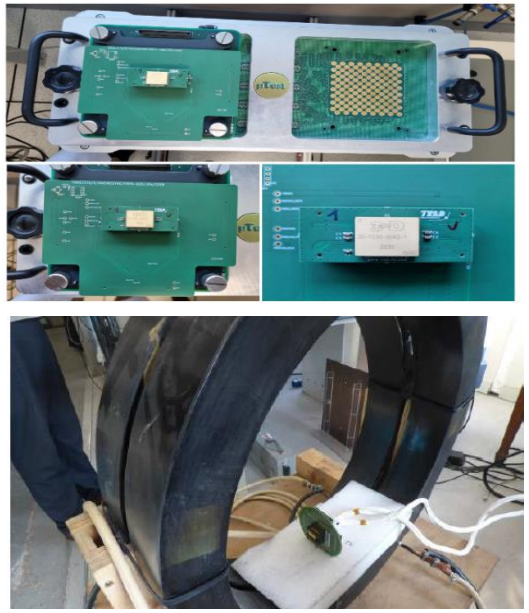
3 PROTOTYPE

Test flow

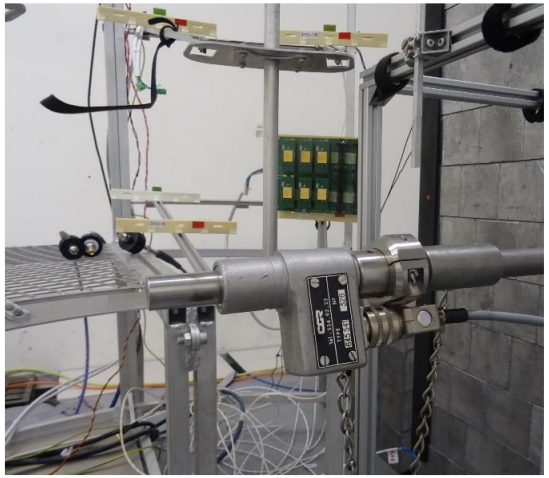


3 PROTOTYPE TID AND MAGNETIC TESTS

Results



Magnetic test setup



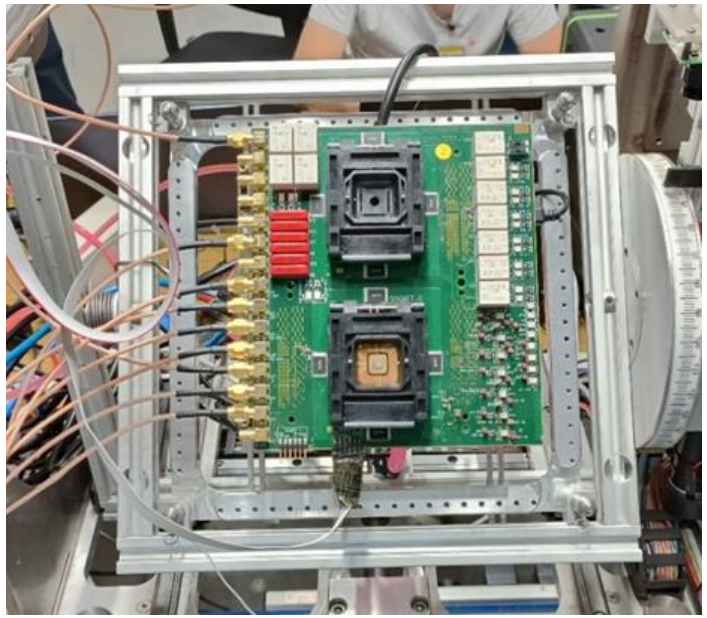
TID test setup

Results	Conditions
TID > **100 krad(Si)**	60Co source
Magn. Field **> 1000 Gauss**	Static
Magn. Field **> 1000A/m**	Power Frequency

TRAD Tests & radiations a HEICO company

PROTOTYPE SEE TESTS

SEE immune on 1V8 SPI and 3V3 EEPROM

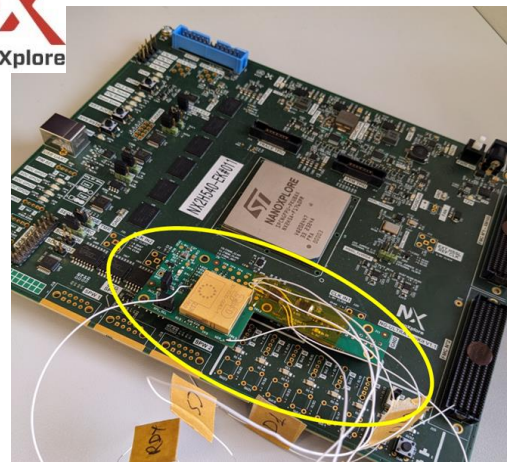


SEE test bench

Results	Interfaces
SEL LETth **> 85 MeV.cm²/mg**	All interfaces
SEFI LETth **> 85 MeV.cm²/mg**	All interfaces
SEU LETth **> 85 MeV.cm²/mg**	All interfaces
SET LETth **> 85 MeV.cm²/mg**	1V8 SPI and 3V3 EEPROM For 3V3 SPI transient observed in **read mode only**

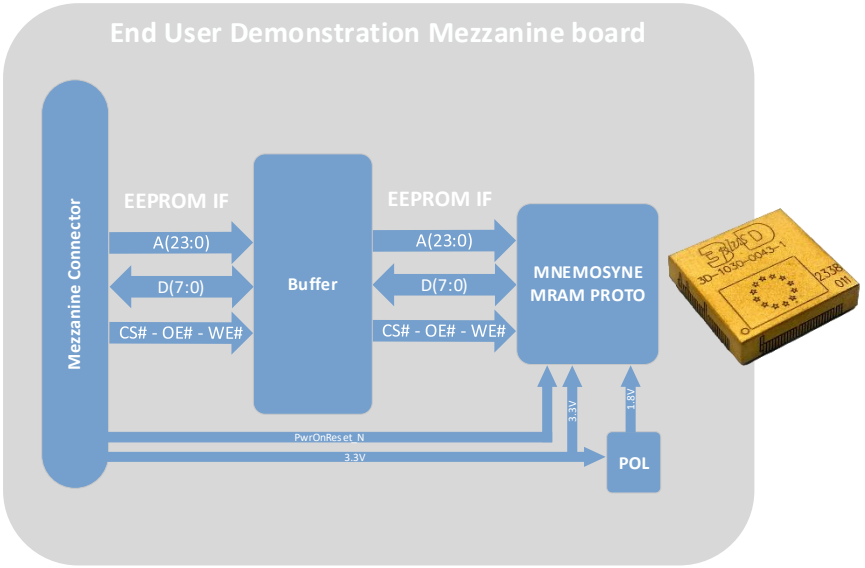
3 PROTOTYPE APPLICATION TESTS

3V3 SPI and 3V3 EEPROM interfaces



- NG MEDIUM : Successful operation
- NG ULTRA 300 : in progress, first analysis shown positive feasibility
- NG ULTRA : Flash boot time: miss match boot time performances.

- The PROTOTYPE worked as expected with a processor using the ASIC memory EEPROM interface

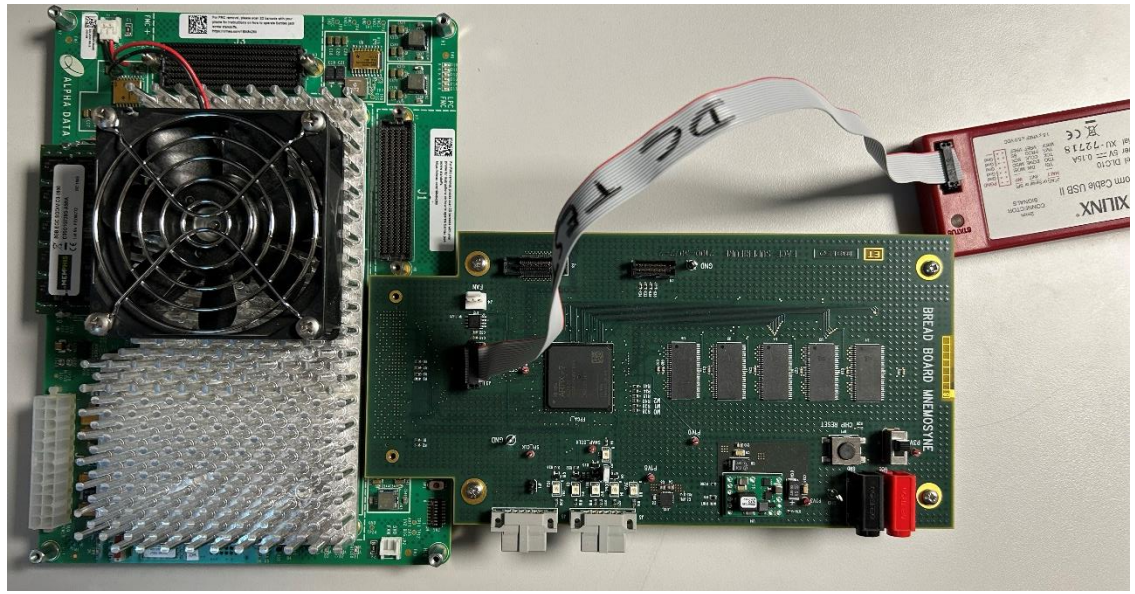


3 PROTOTYPE APPLICATION TESTS

1V8 SPI interface

- Test boot of XQRKU060 FPGA
- Use XQRKU060 FPGA as hardware validation platform

→ The ASIC model implemented in a FPGA was able to succesfully boot the XQRKU060



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SUMMARY

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CHECK ON TECHNICAL REQUIREMENTS

Identify and analyse the process & circuit radiation sensitivity and verify the memory cells SEU/SEL immunity on the STT-MRAM FDSOI process.	OK up to 85 MeV.cm²/mg
Mitigate the risks of TID which degrade the performance and lead to functional failure at component level	OK up to 100 krad(Si)
Mitigate the risk of SET/SEFI leading to component level data loss or functional error.	OK up to 85 MeV.cm²/mg except SET on 3V3 SPI (read mode only)
Strengthen the reliability to reach space requirements. • Life test • Magnetic test	 OK OK
• 128M-bit single die with capability to reach density up to 1G-bit • Serial interface • Optional with x8b parallel interface	OK OK OK
Technology Readiness: TRL3 to TRL5	OK

4 PROJECT OUTPUTS

Products released

	P/N	DENSITY	MODE SUPPORTED
1V8 SPI	3DMN512M08US4853	512 Mbit	SPI, QUAD, OCTAL
	3DMN1G08US8854	1 Gbit	
3V3 EEPROM	3DMN128M08VS1852	128 Mbit	ASYNC. PARALLEL
3V3 SPI	3DMN512M04VS4867	512 Mbit	SPI, QUAD
	3DMN1G04VS8868	1 Gbit	

- Qualification is on-going. By Q2/2025, it will be TRL8

The authors would like to thank the European Commission and all the consortium partners