FRONTGRADE Gaisler

# COTS AI in Space

**Lucas Antunes Tambara**

Lars Wallhede (presenter)

A world leader in embedded computer systems for harsh environments

Experts in fault-tolerant computing

We provide a full ecosystem to support hardware and software design for:

- Standard components
- Semi-custom FPGA
- Full custom ASIC

Based on SPARC and RISC-V architectures

FRONTGRADE Gaisler

Established 2001 as a spin-off from the European Space Agency and Chalmers

Located in Gothenburg, Sweden

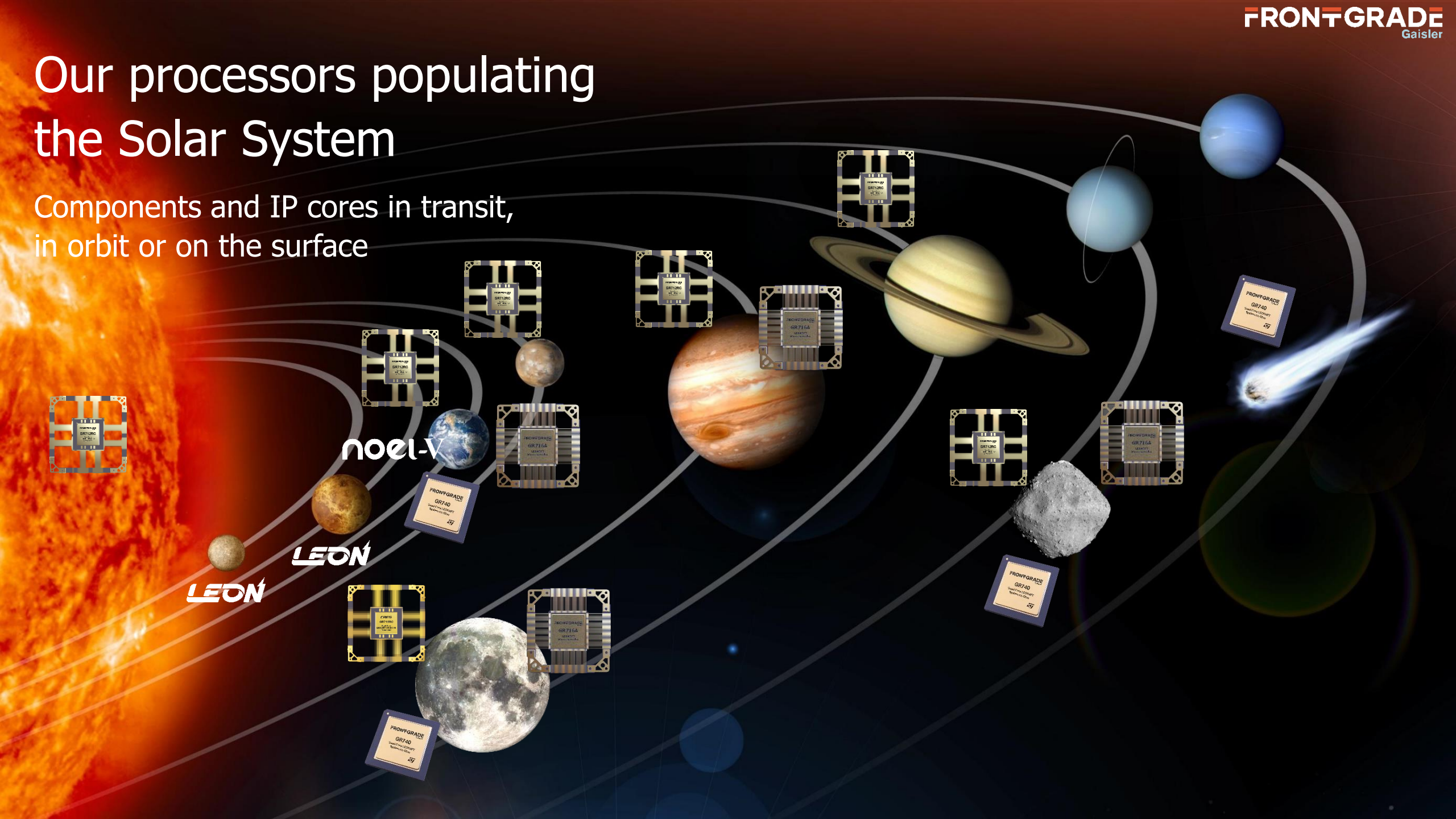
60+ employees in Sweden, Spain, Germany, France and the United Kingdom

Capabilities: software and ASIC/FPGA design

Facilities: component lab

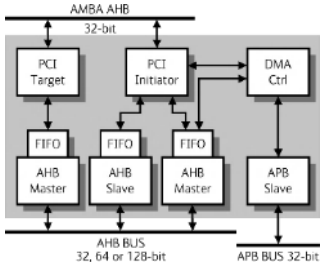
# Our processors populating the Solar System

Components and IP cores in transit, in orbit or on the surface

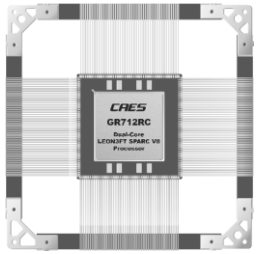


# Complete offering of embedded computer systems for harsh environments

## IP core building blocks




## Components




## Software

WIND

Linux

SYSGO
EMBEDDING INNOVATIONS

fentISS

Embedded With RTEMS

## Development & Test

## Services

# Agenda

**01** Introduction

**02** Devices under test

**03** Screening approach

**04** Screening results

**05** Conclusions and lessons learned

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01

# Introduction

# Introduction

## Background / Motivation

- Today, AI is one of the most important areas that world resources are currently poured into.
- It is a business environment where research ideas and results are converted to integrated silicon in short time, quickly adopting new technology nodes as soon as they become available.
- The rapid development in this area, as well as the vastness of its applicability to all aspects of life, makes it nearly impossible to match dedicated developments in the space domain.
- Lack of clear path-to-flight for complex AI-oriented devices.
  - Not part of ESA's COTS plan (~2021).

## Objectives

- In some cases, it is necessary to rely on COTS components to stay abreast with technological progress and take advantage of its benefits in the space domain.
- ESA's (Open Space Innovation Platform (OSIP) activity (COTS AI in Space, contract 4000136130):
  - Evaluate and progress the screening of AI devices.
  - Establish know-how that could be applied to future testing of COTS AI accelerators.
  - Output one flight-capable COTS component.

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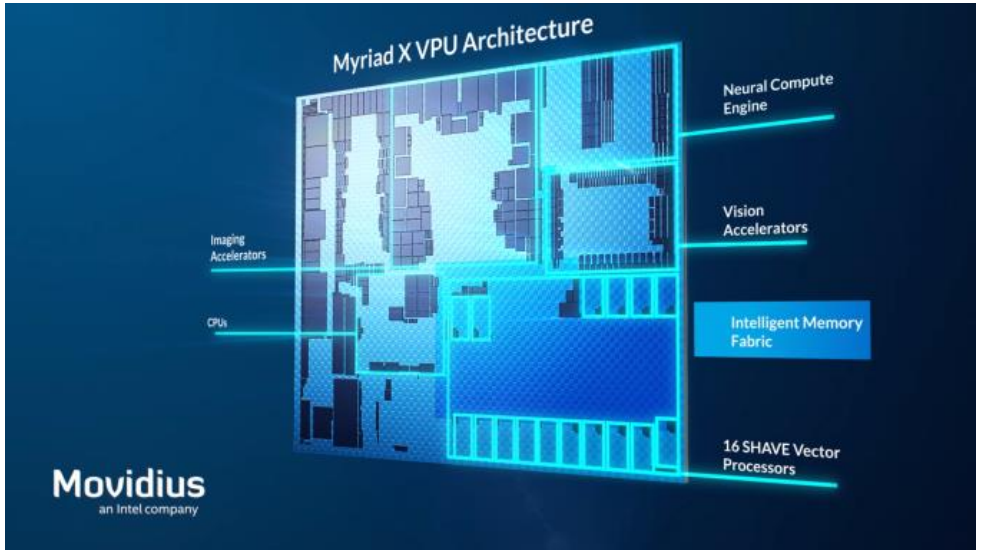
02

# Devices under test

# Devices under test

**Intel Movidius' Myriad Vision Processing Units (VPU)**

- Myriad 2 (2016) and Myriad X (2020)
  - AI computing capability for lower complexity algorithms while maintaining their Size, Weight, Power, and Cost (SWaP-C) requirements low.
  - Frontgrade Gaisler's LEON4 processor cores.
  - Have recently been integrated into low-cost spaceflight platforms.




Images from: https://www.anandtech.com/show/11771/intel-announces-movidius-myriad-x-vpu

| Movidius Myriad Family VPUs | | |
|---|---|---|
| | Myriad 2 | Myriad X |
| **Compute Capacity** | >1 TOPS | >4 TOPS |
| **Vector Processors** | 12x SHAVE Processors | 16x SHAVE Processors |
| **CPUs** | 2x LEON4 cores (RISC; SPARC V8) | 2x LEON4 cores (RISC; SPARC V8) |
| **On-chip Accelerators** | ~20 image/vision processing accelerators | 20+ image/vision processing accelerators<br>Neural Compute Engine (DNN accelerator) |
| **Neural Network Capability** | 1st Gen DNN Support (Up to 100 GFLOPS) | Neural Compute Engine (Up to 1 TOPS) |
| **On-chip Memory and Bandwidth** | 2 MB (400GB/sec) | 2.5 MB (450GB/sec) |
| **DRAM Support** | Max: 8Gb<br>LPDDR2 (533MHz, 32-bit)<br>LPDDR3 (933MHz, 32-bit) | Max: 16Gb<br>LPDDR4 (1600MHz, 32-bit) |
| **DRAM Configurations** | 1Gbit LPDDR2 (MA215X)<br>4Gbit LPDDR3 (MA245X) | No in-package memory (MA2085)<br>4Gbit LPDDR4 (MA2485) |
| **Encoder/Codec** | VGA, 720p, 1080p, H.264 (software encoder) | M/JPEG 4K at 60Hz encoder<br>H.264/H.265 4K at 30Hz encoder |
| **Key Interfaces** | 12x MIPI lanes (DPHY 1.1)<br>USB 3<br>SPI<br>I2S<br>SD<br>1GbE | 16x MIPI lanes (PHY 1.2)<br>USB 3.1<br>Quad SPI<br>I2S<br>2x SD<br>10GbE<br>PCIe 3.0 |
| **Process** | 28nm HPC+/HPC/HPM (TSMC) | 16nm FFC (TSMC) |
| **Package** | 6.5mm x 6.5 mm (MA215X)<br>8mm x 9.5 mm (MA245X) | 8.1mm x 8.8mm (MA2085, MA2485) |

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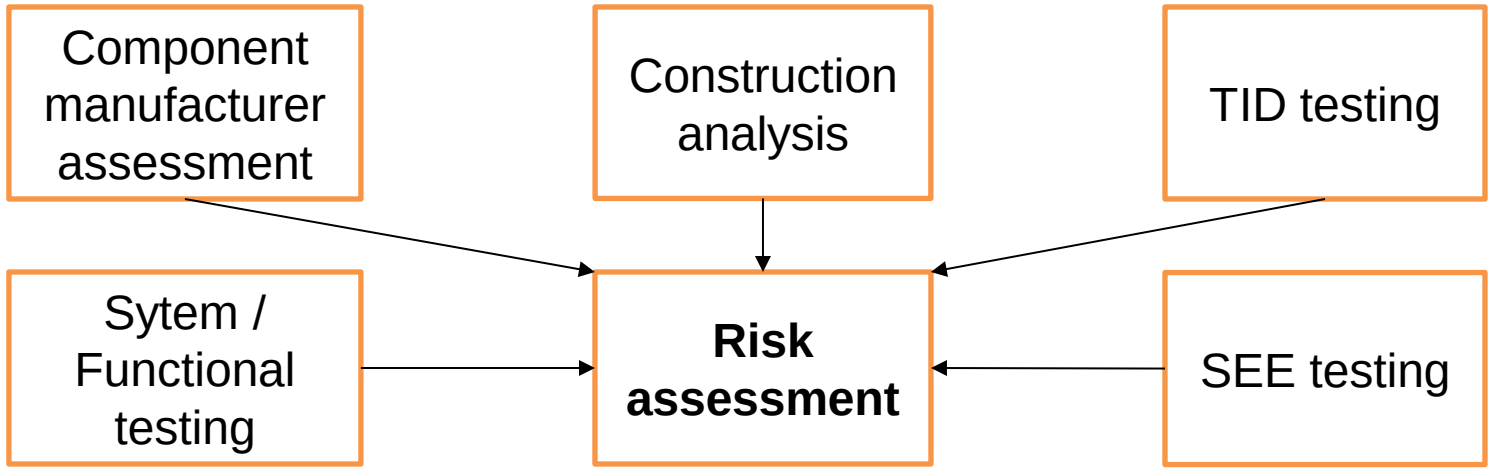
03

# Screening approach

# Screening approach

## Baseline

- Component manufacturer assessment:
  - Analysis of the available data on the manufacturer and the component (available only under NDA).
  - Evaluate potential access to the production test program (usually not possible or with low engagement from the manufacturer) or development of electrical test platform in-house (time-consuming and expensive).
    - Alternative: System-level / Functional testing.
- ECSS-Q-ST-60-13C (Space product assurance - Commercial electrical, electronic and electromechanical (EEE) components):
  - Class 3, Component evaluation:
    - Construction analysis.
    - Radiation tests.



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# Screening results

# Screening results

## Construction analysis

- Based on ECSS-Q-ST-60-13C, Annex H (“Flow chart for construction analysis and destructive physical analysis”).

| Sequence | Test | Procedure | Samples allocation |
|---|---|---|---|
| 1 | External visual inspection | MIL-STD-883, TM 2009 | SN #1-5 |
| 2 | Physical dimensions | MIL-STD-883, TM 2016 | SN #1-5 |
| 3 | X-ray inspection | MIL-STD-883, TM 2012 | SN #1-5 |
| 4 | Preconditioning | JEDEC 22-A113D, MSL 3 | SN #1-5 |
| 5 | C-SAM test | JEDEC J-STD-020 | SN #1-5 |
| 6 | Permanence of marking | ESCC 24800 | SN #1-5 |
| 7 | Solderability | JEDEC J-STD-002D | SN #1,2 |
| 8 | Decapsulation | ESCC 25300 | SN #1-4 |
| 9 | Internal visual inspection | ESCC 2059000 | SN #1-4 |
| 10 | SEM inspection | MIL-STD-883, TM 2018 | SN #1,2 |
| 11 | Bond strength/shear (if applicable) | MIL-STD-883, TM 2011 / JEDEC JASD22-B116 | SN #1-3 |
| 12 | Glassivation integrity | MIL-STD-883, TM 2021 | SN #2-4 |
| 13 | Flip-chip pull-off (if applicable) | MIL-STD-883, TM 2031 | SN #2,3 |
| 14 | Tg measurement | - | SN #5 |
| 15 | Package level cross-sectioning | - | SN #5 |
| 16 | SEM and material analysis | - | SN #5 |
| 17 | CA report | - | - |

<u>Myriad 2</u>

- Multi-die package
  - Flip-chip SoC (bottom)
  - Wire-bond LPDDR3 (top)

<u>Myriad X</u>

- Single-die package
  - Flip-chip SoC
- All parts passed

Additional tests were performed on Myriad 2, but the remaining of the presentation focus only on the Myriad X due to time constraints.

# Screening results

## Test platform development

- Hardware:
  - Frontgrade Gaisler GR-VPX-XCKU060 board:
    - Based on Xilinx/AMD XCKU060 FPGA.

https://www.gaisler.com/products/gr-vpx-xcku060

  - Frontgrade Gaisler GR-FMC-MX board:
    - Based on Intel's Myriad X VPU.

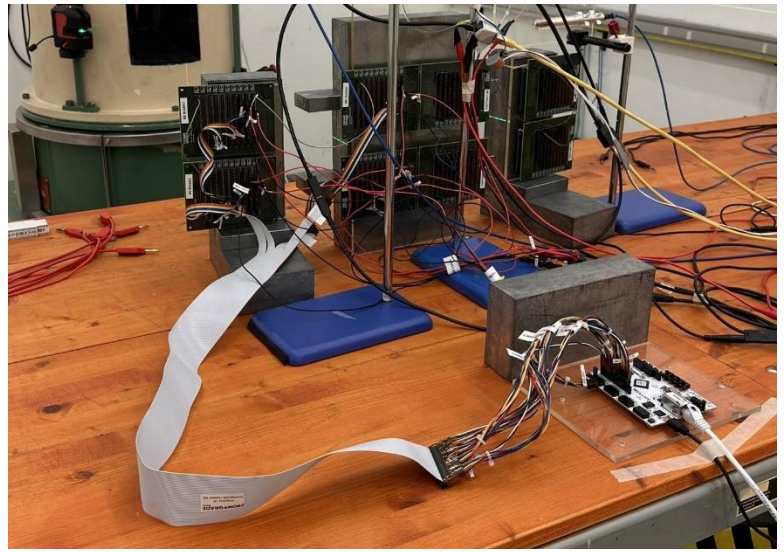
- Software:
  - Test software developed by Ubotica Technologies.
  - Static memory tests:
    - LEON OS Level 1 instruction and data caches (LOSL1C), LEON OS Level 2 cache (LOSL2C), SHAVE Level 1 instruction and data caches (SHVL1C), SHAVE Level 2 cache (SHVL2C), CMX (CMXStatic), and DRAM (DDRStatic).
  - Dynamic inference network tests:
    - mobileNet, diabetic retinopathy (DR), and ship segmentation (shipSeg).
    - Each inference network test could be executed with different hardware configurations (varying type and number of resources).

# Screening results

## TID testing

- Based on ESCC 22900 (“Total Dose Steady-State Irradiation Test Method - ESCC Basic Specification No. 22900”).
- Test facility: ESA’s ESTEC Co-60 facility, Noordwijk, The Netherlands.
- Test samples: 2x biased, 2x unbiased, 1x reference.
- Average dose rate: 0.777 krad(Si)/h.
- Test steps with remote functional testing (krad(Si), approximately): 0, 14, 29, 45, 58, 100.
  - Remote functional testing was also executed post-24h and -168h annealing steps (room temperature).
  - Remote functional testing = test platform software.
- A companion LPDDR4 memory was also tested.

- Results:
  - No functional failures were observed up to 100 krad(Si).
  - An increase in the supply current consumption of the core supply of about 18% was observed at 100 krad(Si) with no impact on the performance of the test samples. Such an increase remained after the room-temperature annealing steps.

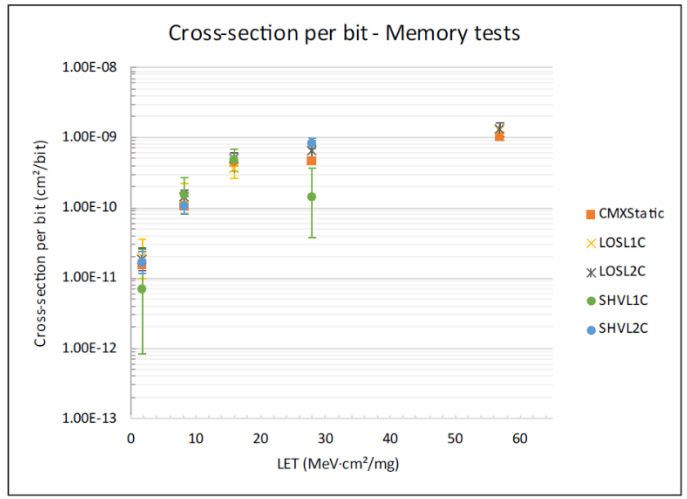


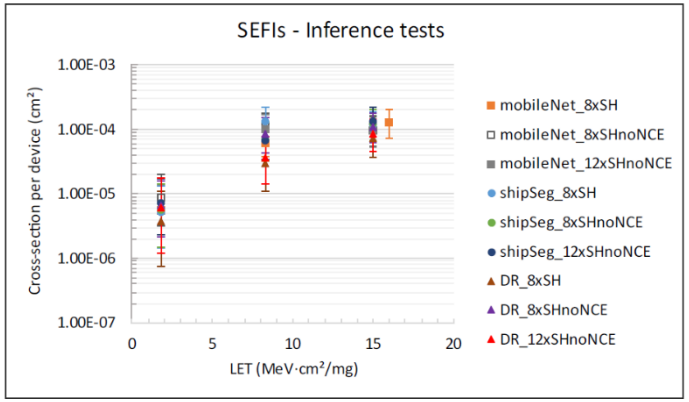
# Screening results

## SEE testing

- Based on ESCC 25100 (“Single Event Effects Test Method and Guidelines - ESCC Basic Specification No. 25100”).
- Test facilities: PIF/PSI, Villigen, Switzerland (protons); RADEF/JYU, Jyväskylä, Finland (heavy ions).
- Test samples: 2x for protons, 3x for heavy ions.
- Energies and LETs: from 34 to 200 MeV (protons) and from 1.8 to 58 MeV·cm²/mg (heavy ions).
- A companion LPDDR4 memory was also tested for proton-induced SEE.

- Results:
  - Cross-section per bit results aligned with other devices built on the same or similar technology (16nm FinFET, DDR4).
  - Functional cross-sections acceptable for a COTS device and with no clear dependency on the complexity of the tests.
  - Additional data is available and was presented at RADECS 2024 (paper to be available soon at IEEE Xplore).
    - Not all data is presented here due to time constrains.



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# Conclusions and lessons learned

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## Results achieved

- Development of a modular test platform for system-level / functional testing:
  - Hardware: device under test can be changed (FMC concept).
  - Software: static memory tests can be ported to other devices, and dynamic inference network tests are based on open models.
- Execution of construction analysis on different devices with very different results obtained.
- SEE and TID test results in good agreement with similar data existing in the literature, reinforcing the correctness of the work performed.
  - Evaluation of a companion LPDDR4 memory (AEC-Q100 qualified).

- Screening flow can be considered successful as the Myriad X and the companion LPDDR4 have been selected by a customer for use in an “accelerator system”.
  - A batch (single date code) of each device was acquired.
    - Construction analysis repeated with success (additional tests performed). TID not repeated as the radiation dose margin of the application is significantly lower than 100krad(Si).

# Conclusions and lessons learned

## Lessons learned

- Execute constructional analysis first and do a first risk assessment based on the results obtained.
  - Reject the part or perform additional tests.

- Never count on support from the manufacturer of a COTS devices for performing additional tests.
  - Space is a niche market with low volumes involved, so it is difficult to get attention from them.

- One should consider evaluating the documentation available about the COTS device of interest as a decision point for its selection.
  - Such devices are very complex, and developing a test system with good supporting documentation may not be easy. Some manufacturers require an NDA to get access to the datasheet.

- Developing a test platform for characterizing complex devices like the AI ones, even at the system/functional level, is still time-consuming and expensive.
  - Any project intended to do that should not underestimate the effort needed to execute such an activity.

- As in any other radiation testing activity, but mainly when testing complex devices like the AI ones, one should always be prepared to react quickly to unforeseen events to not jeopardize the project's schedule or even lose a test campaign.


# THANK YOU!

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