ECSS-Q-ST-70-60C Rev.1
30 April 2025

Space product assurance

Qualification and procurement of printed circuit boards

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Section
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Foreword

ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards. Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

This Standard has been prepared by the ECSS-Q-ST-70-60C Rev.1 Working Group, reviewed by the ECSS Executive Secretariat and approved by the ECSS Technical Authority.

Disclaimer

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Change log

ECSS-Q-ST-70-60C 1 June 2018	First issue Merge of ECSS-Q-ST-70-10C and ECSS-Q-ST-70-11C and published as new ECSS Standard
ECSS-Q-ST-70-60C Corrigendum 1 1 March 2019	First issue, Corrigendum 1
ECSS-Q-ST-70-60C Rev.1 30 April 2025	First issue, Revision 1 The main changes respect to ECSS-Q-ST-70-60C Corr.1 (1 March 2019) are related to the implementation of HDI PCB technology. All changes are marked with revision tracking.
History of superseded versions	
ECSS-Q-70-10A ECSS-Q-70-11A 23 November 2001	First issue
ECSS-Q-70-10B ECSS-Q-70-11B	Never issued
ECSS-Q-ST-70-10C ECSS-Q-ST-70-11C 15 November 2008	Second issue Redrafting according to ECSS drafting rules and template. Reorganization of the content to separate descriptive text and requirements and creation of DRD.

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Introduction

PCBs are used for the mounting of electronic components to produce PCB assemblies that perform electrical functions. The PCBs are subjected to thermo-mechanical stress during assembly such as soldering of components, rework and repair under normal terrestrial conditions. In addition, the assembled PCBs are exposed to the launch and space environment. The reliability of the circuit depends on the robustness of the manufacturing processes, for which this standard specifies requirements. PCB technology needs detailed inspections to verify its reliability, which is specified for the qualification and procurement phases of the PCB technology.

1 Scope

This standard specifies the requirements for the PCB manufacturer, the procurement authority and the qualification authority for qualification and procurement of PCB technology.

ECSS-Q-ST-70-60 is applicable for all types of PCBs, including sequential, rigid and flexible PCBs, sculptured flex, HDI and RF PCBs.

This standard can be made applicable for other products combining mechanical and electrical functionality using additive or reductive manufacturing processes, as used in PCB manufacturing. Examples of such products are slip- rings, bus bars and flexible flat cables.

This standard may be tailored for the specific characteristics and constraints of a space project in conformance with ECSS-S-ST-00.

2
Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revision of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the more recent editions of the normative documents indicated below. For undated references, the latest edition of the publication referred to applies.

ECSS-S-ST-00-01	ECSS system — Glossary of terms
ECSS-Q-ST-10-09	Space product assurance — Nonconformance control system
ECSS-Q-ST-20	Space product assurance — Quality assurance
ECSS-Q-ST-70	Space product assurance — Material, mechanical parts and processes
ECSS-Q-ST-70-02	Space product assurance — Thermal vacuum outgassing test for the screening of space materials
ECSS-Q-ST-70-12	Space product assurance — Design rules for printed circuit boards
ECSS-Q-ST-70-21	Space product assurance — Flammability testing for the screening of space materials
ECSS-Q-ST-70-22	Space product assurance — Control of limited shelf-life materials
ECSS-Q-ST-70-29	Space product assurance — Determination of offgassing products from materials and assembled articles to be used in a manned space vehicle crew compartment
ECSS-Q-ST-70-61	Space product assurance — High reliability assembly for surface mount and through hole connections
EN 9100:2016	Quality management systems – Requirements for aviation, space and defense organisations
IEC 60326-2-am 1 (1992-06)	Printed boards. Part 2: Test methods
IEC 60194 (1999-04)	Printed board design, manufacture and assembly — Terms and definitions
IEC 63185 (2020)	Measurement of the complex permittivity for low-loss dielectric substrates balanced-type circular disk resonator method
IPC-A-600K (2020)	Acceptability of Printed Boards
IPC-T-50N (2021)	Terms and definitions for interconnecting and packaging electronic circuits

IPC-TM-650	Test methods manual
IPC-1710A (2004)	OEM Standard for Printed Board Manufacturers' Qualification Profile
IPC-4101E (2017)	Specification for base materials for rigid and multilayer printed boards
IPC-4103B (2017)	Specification for Base Materials for High Speed/ High Frequency Applications
IPC-4203B (2018)	Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Circuitry and Flexible Adhesive Bonding Films
IPC-4204B (2018)	Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry
IPC-6012F (2023)	Qualification and performance specification for rigid printed boards
IPC-6012FS (2024)	Space and military avionics applications addendum to IPC-6012F
IPC-6013E (2021)	Qualification and Performance Specification for Flexible Printed Boards
IPC-6018D (2022)	Qualification and Performance Specification for High Frequency (Microwave) Printed Boards
IPC-6018DS (2022)	Space and Military Avionics Applications Addendum to IPC-6018D
ISO 9001:2015	Quality management systems – Requirements
ISO-14644-1 (2015)	Cleanrooms and associated controlled environments - Part 1: Classification of air cleanliness by particle concentration

3
Terms, definitions and abbreviated terms

3.1 Terms from other standards

a. For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply, and in particular the following terms:

1. customer
2. supplier

NOTE See clause 4.2 for a description of roles of customer and supplier.

b. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-70-12 apply, and in particular the following terms:

1. annular ring
2. area array device (AAD)
3. aspect ratio
4. basic copper
5. blind via
6. bond-ply
7. build-up
8. buried via
9. conductor
10. external capture pad
11. FR4
12. hole wall pull away
13. heat sink
14. high density interconnect (HDI)
15. interlayer
16. internal landing pad
17. intralayer
18. laminate
19. microvia
20. no-flow prepreg
21. non-functional pad
22. non-pated hole
23. normal pitch

24. panel
25. plated through-hole (PTH)
26. prepreg
27. printed circuit board (PCB)
28. reliable insulation (also known as double insulation)
29. resin starvation
30. serialization
31. spacing
32. stack
33. track
34. via
35. X,Y direction
36. Z direction

3.2 Terms specific to the present standard

3.2.1 automated optical inspection (AOI)

inspection method using an automated equipment to verify the pattern on an etched layer

3.2.2 back-drilled via

type of via with part of its metallisation removed on one side by depth controlled mechanical drilling with a larger diameter drill

3.2.3 batch

group of PCBs and coupons that are covered by the same CoC and the same traveller

NOTE 1 A batch is processed approximately at the same time. See 6.8a.

NOTE 2 The terms “lot” and “work order” are synonymous.

3.2.4 blind-via-in-pad

type of via directly underneath a SMT pad

3.2.5 blister

delamination in the form of a localized swelling and separation between any of the layers of a laminated base material, or between base material and conductive foil or protective coating

[IPC-T-50N]

3.2.6 cap lift

separation between resin in blind via and copper cap plating on surface

NOTE Cap lift can be shown as bulging and as thin line separation, as shown in Table 10-19.

3.2.7 contamination

<CONTEXT: Qualification and procurement of PCBs>

foreign material embedded in dielectric material

NOTE 1 Synonyms are: FOD, inclusion (see definition 3.2.20), foreign material, debris, pollution.

NOTE 2 Contamination can be organic, metallic, particulate or fibres.

3.2.8 coupon

small piece of test circuitry that is used for quality conformance evaluation by specific tests and inspection

NOTE 1 The coupon is manufactured as part of a panel and at the final manufacturing stage it is separated from it. The coupon is thus associated with the PCBs within the panel, with which it was simultaneously manufactured.

NOTE 2 The term ‘coupon’ refers to a generic pattern, whereas the term ‘IST coupon’ refers to the specific IST pattern.

[adapted from IPC-T-50N]

3.2.9 coverlay

thin dielectric material used to encapsulate circuitry, most commonly for flexible circuit applications

NOTE The terms ‘cover layer’ and ‘cover material’ are synonymous.

3.2.10 crazing

condition that occurs in reinforced laminate base material whereby glass fibre bundles are separated from the resin not limited to the weave intersections

NOTE 1 This condition manifests itself in the form of connected white spots or crosses that are below the surface of the base material. It is usually related to thermally or mechanically induced stress. Crazing is a more severe defect than measling. Delamination is a further worsening of crazing.

NOTE 2 See also “measling”.

3.2.11 delamination

separation between plies within a base material, between base material and a conductive foil, or any other planar separation with a PCB

NOTE See also 'blister', which is a local delamination.

[IPC-T-50N]

3.2.12 destructive physical analysis (DPA)

analysis method using sampling, potting, grinding, polishing and inspection which, thus, destroys the test vehicle

NOTE The term 'microsectioning' is approximately synonymous.

3.2.13 dewetting

condition that results when molten solder coats a surface and then recedes to leave irregularly-shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the base metal not exposed

[IPC-T-50N]

3.2.14 dross

oxide and other contaminants that form on the surface of molten solder

[IPC-T-50N]

3.2.15 etchback

distance from resin of hole wall to innerlayer foil

3.2.16 fine pitch

spacing of tracks or pads that is more dense than for normal pitch

NOTE Pitch is specified in clause 7.4 of ECSS-Q-ST-70-12.

3.2.17 flexible

PCB technology that uses only flexible layers in its build up

NOTE The term 'flex' is synonymous.

3.2.18 glass compression

deformed glass fibre bundles of prepreg causing absence of resin between glass and copper due to profiled copper pattern

NOTE See also 'resin starvation'.

3.2.19 haloing

mechanically-induced fracturing or delamination affecting the external layers of base material, that is usually exhibited by a light area around holes or other machined features

[IPC-T-50N]

3.2.20 inclusion

foreign particle, metallic or non-metallic, that can be entrapped in an insulating material, conductive layer, plating, base material or solder connection

[IPC-T-50N]

3.2.21 interconnect defect (ICD)

separation at the interface between internal layer and copper plating

NOTE 1 The term 'innerlayer separation' is synonymous.

NOTE 2 See 'smear' for additional explanation.

[IPC-6012F]

3.2.22 interconnect stress test (IST)

a test method of rapid thermal cycling of a daisy-chain coupon, representative of the specific PCB design, from ambient temperature to a defined upper temperature through the application of direct current as defined by IPC-TM-650 test method 2.6.26

3.2.23 IST coupon

specific coupon for IST

NOTE The term 'coupon' refers to a generic pattern, whereas the term 'IST coupon' refers to the specific IST pattern.

3.2.24 key personnel

personnel with specialist knowledge responsible for defined production or product assurance areas

3.2.25 lay-out

design of the conductive pattern on a layer

3.2.26 measling

condition that occurs in laminated base material whereby glass fibre bundles are separated from the resin limited to the weave intersection

NOTE 1 This condition manifests itself in the form of discrete white spots or "crosses" that are below the surface of the base material. It is usually related to thermally-induced stress or humidity.

NOTE 2 See also "crazing", which is a further worsening of measling.

[IPC-T-50N]

3.2.27 metal core

layer or local insert of thick metal embedded inside the PCB usually used as a heat sink, grounding layer or for the restriction of thermal expansion

3.2.28 milling

mechanical method that removes a portion of the material outlining a PCB using a cutting bit

NOTE See also 'routing'.

3.2.29 multilayer

PCB technology that uses lamination of several copper layers and plated holes for interconnection

NOTE PCBs that are not multilayer, are double-sided or single-sided PCBs. See also "sequential".

3.2.30 plated hole

hole that is used as an interlayer connection

NOTE Types of plated holes are PTH and vias.

3.2.31 PCB manufacturer

entity that manufactures the PCB

NOTE The PCB manufacturer is supplier to the procurement authority.

3.2.32 PCB technology

category of manufacturing processes, materials and design for PCBs

NOTE Examples of PCB technology are:

- Polyimide sequential rigid
- Polyimide sequential rigid/flex
- Epoxy sequential rigid
- Epoxy non-sequential rigid/flex
- HDI with microvias
- RF
- Flexible and sculptured flex

3.2.33 plugged via

via type that is cap plated and filled with resin in a specific via filling process

NOTE Blind vias can be resin-filled using resin from the prepreg during sequential lamination. Plugged vias use a resin that does not originate from the prepreg and the filling process does not occur during lamination.

3.2.34 procurement authority

entity that procures the PCB

NOTE 1 The procurement authority is customer of the PCB manufacturer.

NOTE 2 The procurement authority can be supplier to the prime contractor.

3.2.35 qualification authority

entity that qualifies the PCB technology and PCB manufacturer

3.2.36 radio frequency (RF)

electronic functionality that requires specific design precautions on dielectric materials and copper pattern to maintain time dependant signal integrity

NOTE 1 The term 'high speed' is synonymous.

NOTE 2 The term 'RF PCB' identifies the PCB technology.

3.2.37 rigid

PCB technology that uses only rigid layers in its build-up

3.2.38 rigid/flex

PCB technology that uses a combination of rigid and flexible layers in its build-up

3.2.39 routing

the lay-out and connection of conductors between plated-holes and pads

NOTE The term 'routing' is also used for 'milling'. This second meaning is not used in ECSS-Q-ST-70-60 to avoid confusion.

3.2.40 scratch

narrow furrow or grove in a surface

NOTE It is usually shallow and caused by the marking or rasping of the surface with a pointed or sharp object.

[IEC 60194 (1999-04)]

3.2.41 sculptured flex

flexible PCB technology that uses profiled copper tracks

NOTE Aviflex is an example of a commercial identification of sculptured flex.

3.2.42 sequential

PCB technology that uses more than one lamination or drilling step

NOTE The term 'sequential' also implies that the PCB is of type 'multilayer'. The opposite is 'non-sequential'.

3.2.43 sequential via

via type that interconnects layers within the same plating sequence

NOTE Examples of sequential vias are blind vias and buried vias.

3.2.44 skip plating

local missing deposition of plating

NOTE Skip plating can occur on electroless copper plating on glass in the hole wall. Skip plating can also occur on surface finish.

3.2.45 smear

base material resin that covers the interface between the exposed edge of an innerlayer pad and through-hole plating

NOTE 1 The resin transfer is usually caused by the drilling operation and removed during the desmear process. The term 'resin smear' or 'smearing' are synonymous.

NOTE 2 The aspect of smear can be mistaken for interconnect defect, or vice versa. Smear is the presence of resin, whereas interconnect defect is an adhesive separation of copper plating.

[adapted from IPC-T-50N]

3.2.46 test pattern

part of the PCB or coupon that refers to the copper pattern for a specific test

[adapted from IPC-T-50N]

3.2.47 through-going via

type of via that is drilled through the entire thickness of the PCB

3.2.48 traveller

documentation kept with the batch during the manufacturing processes in which the order of specific processes are recorded

3.2.49 treatment side of foil

the side of copper foil that is submitted to a surface treatment process by the materials supplier or by the PCB manufacturer

NOTE The material supplier treatment side of copper foil on laminate is typically rougher. See Figure 3-1.

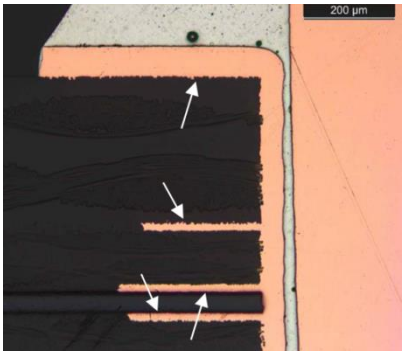


Figure 3-1: Example of material supplier treatment side of foil (white arrows) and PCB manufacturer treatment side of foil (opposite side)

3.2.50 waiver request

written agreement between PCB manufacturer and procurement authority to deliver PCBs with a nonconformance to a requirement from a specification

NOTE 1 The following terms are synonymous: “request for concession”, “demande de derogation”, “request for waiver”, “request for deviation”.

NOTE 2 In space projects the terms RFW and RFD have specific meaning as specified in ECSS-Q-ST-70. This specific meaning does not strictly apply in the context of PCB procurement.

3.2.51 weave exposure

a base material surface condition in which unbroken fibres of woven glass are not completely covered by resin

NOTE See also ‘weave texture’.

[IPC-T-50N]

3.2.52 weave texture

a surface condition of base material in which a weave pattern of cloth is apparent although the unbroken fibres of woven cloth are completely covered by resin.

NOTE See also ‘weave exposure’.

[IPC-T-50N]

3.2.53 wicking

infiltration of copper plating into the dielectric of the hole wall

NOTE The terms “copper infiltration” and “copper ingress” are synonymous.

3.2.54 work instruction

quality document that describes the technical details about processes, material usage, inspection and acceptance criteria

NOTE 1 The terms ‘manufacturing procedure’ or ‘control procedure’ or ‘process instruction’ are synonymous.

NOTE 2 Work instructions can include process flow charts, production documents (e.g. manufacturing plans, travelers, routers, work orders, process cards) and inspection documents.

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AAD	area array device
AC	alternating current
AOI	automated optical inspection
AR	as received
CDR	critical design review
CIC	copper-invar-copper
CITC	current induced thermal cycling test method
CoC	certificate of conformance
CTE	coefficient of thermal expansion
Cu	copper (element)
CVCM	collected volatile condensable material
DC	direct current
DML	declared materials list
DPA	destructive physical analysis
DR	design review
DRB	delivery review board
DRD	document requirements definition
DSC	differential scanning calorimetry
DWV	dielectric withstanding voltage
EBB	elegant breadboard
ECM	electrochemical migration
EM	engineering model
EOL	end of life
EQM	engineering qualification model
FAI	first article inspection
FCSI	final customer source inspection
FM	flight model
FOD	foreign object debris
FR4	type of epoxy resin for PCBs
FS	flight spare
HATS2	highly accelerated thermal shock test method
HDI	high density interconnect
HVLP	hyper very low profile
ICD	interconnect defect
IMC	intermetallic compound

Abbreviation	Meaning
IPA	isopropanol
IPC	association connecting electronic industries
IST	interconnect stress test method
KPI	key performance indicator
max	maximum
min	minimum
MIP	mandatory inspection point
MPCB	material and processes control board
MRR	manufacturing readiness review
MTO	metal turnover
n. a.	not applicable
NCR	nonconformance report
NRB	nonconformance review board
NSMD	non solder mask defined
OTD	on time delivery
OM	thermal stress test equipment
PCB	printed circuit board
PCN	process change notice
PDR	preliminary design review
PFM	proto flight model
PID	process identification document
PPE	polyphenylene ether
PTH	plated-through hole
PTFE	polytetrafluoroethylene
QA	quality assurance
QM	qualification model
QML	qualified manufacturers list
QPL	qualified product list
r.m.s.	root-mean-square
R&D	research and development
Ref	reference (for tables in clause 10)
RF	radio frequency
RFA	request for approval
RML	residual mass loss
RW	rework simulation
SB	solder bath float
SMT	surface mount technology
SPC	statistical process control

Abbreviation	Meaning
sq	square (in unit Ω/sq)
TBD	to be defined
TDR	time domain reflectometry
T288	time to delamination at 288°C
Td	temperature of decomposition
Tg	temperature of glass transition
TGA	thermogravimetric analysis
TMA	thermomechanical analysis
VLP	very low profile
wk	week

3.4 Nomenclature

The following nomenclature applies throughout this document:

a. The word "shall" is used in this Standard to express requirements. All the requirements are expressed with the word "shall".

b. The word "should" is used in this Standard to express recommendations. All the recommendations are expressed with the word "should".

NOTE It is expected that, during tailoring, recommendations in this document are either converted into requirements or tailored out.

c. The words "may" and "need not" are used in this Standard to express positive and negative permissions, respectively. All the positive permissions are expressed with the word "may". All the negative permissions are expressed with the words "need not".

d. The word "can" is used in this Standard to express capabilities or possibilities, and therefore, if not accompanied by one of the previous words, it implies descriptive text.

NOTE In ECSS "may" and "can" have completely different meanings: "may" is normative (permission), and "can" is descriptive.

e. The present and past tenses are used in this Standard to express statements of fact, and therefore they imply descriptive text.

4 Principles

4.1 General

This standard specifies requirements for the manufacture, qualification, procurement, test and inspection of PCBs.

4.2 Roles

In the context of ECSS-Q-ST-70-60 the roles “PCB manufacturer”, “procurement authority” and “qualification authority” were explicitly introduced and defined in clause 3.2 to allow proper allocation of requirements.

4.3 References to acceptance criteria

Clause 10 includes tables to specify acceptance criteria for certain technological features. The technological features can be further subdivided in each table. This is indicated with a reference letter in the first column and abbreviated as “Ref x”. This allows cross-referencing to specific line items in the table, rather than to an entire table. An example of this is “internal annular ring on an inner layer at the end of a blind via” which is cross-referenced as Ref. b in Table 10-1.

5
QA for qualification

5.1 Qualified PCBs

ECSS-Q-ST-70-60_1390001

a. Qualified PCBs for space applications shall meet all the following conditions:

   1. the PCB is procured in conformance with clauses 6 and 8,
   2. the PCB is procured from a PCB manufacturer that is qualified in conformance with clauses 5 and 7 and as specified in the PID,
   3. the PCB design is in conformance with the requirements of ECSS-Q-ST-70-12.

      NOTE Some specific PCB technologies can be used that are not covered by a valid PID or by a company qualification. Procurement can be done under RFA, including tests for (delta) qualification and tests for procurement but it can exclude the qualification of the company. Examples of specific PCB technology are complex HDI, complex RF and flex technology that are under development. This is described in clauses 5.2 and 7.7.

ECSS-Q-ST-70-60_1390002

b. The qualification of PCBs in conformance with this standard shall cover for a maximum operational temperature of 85 °C.

   NOTE 1 This is also described in 13.2.1a of ECSS-Q-ST-70-61.

   NOTE 2 This is in conformance with current rating requirements from clause 13.6.2 of ECSS-Q-ST-70-12.

   NOTE 3 PCBs are not qualified for a specific voltage as this is depending on PCB design in conformance with ECSS-Q-ST-70-12.

5.2 Ceramic PCB technology

ECSS-Q-ST-70-60_1390003

a. PCBs manufactured using ceramic filled laminate shall be in conformance with ECSS-Q-ST-70-60.

NOTE This is opposed to ceramic substrates using thick film or thin film processes that are in conformance with ESCC-2566000.

5.3 Flexible PCB

5.3.1 General

Flexible PCBs can be used as harness or cable for interconnection of PCB assemblies, components or detectors, in which case they are short, typically less than 0,5 m. Flexible PCBs can also be used to interconnect larger elements such as equipment, solar cells or solar panels. And they can be used as radiating RF element for antennae. In such applications the flexible PCBs can be long, typically more than 1 m. Moreover, they can be used in dynamic applications such as solar array drive mechanisms, thruster orientation mechanisms or antenna pointing mechanisms.

Products can include various terminology, such as “flat cable”, “flexprint”, “ribbon flex” and similar. These products are referred to in this standard as “flexible PCB”. A specific type of flexible PCB also referred to in this standard is the “sculptured flex PCB”, which is typically used for interconnection of components to PCBs or in between PCBs.

Encapsulation of separate copper strings or wires to form a flexible cable is not a conventional PCB manufacturing process, and can therefore be considered a cable. Etching of copper clad flexible laminate and lamination of coverlay, among others, are conventional PCB manufacturing processes and are covered by ECSS-Q-ST-70-60.

Heaters are in conformance with ESCC-4009. Cables are in conformance with ESCC-3901.

5.3.2 Qualification of flexible PCB

ECSS-Q-ST-70-60_1390724

a. For flexible PCBs, a company specific qualification with auditing and review of QA should be performed.

NOTE This is good practice to verify batch-to-batch reproducibility.

ECSS-Q-ST-70-60_1390004

b. In case the flexible PCB is not qualified in conformance with ECSS-Q-ST-70-60, the project qualification of flexible PCB shall be reviewed under RFA in conformance with clause 7.7.2.

ECSS-Q-ST-70-60_1390005

c. Flexible PCB for harness shall be qualified and procured as per ECSS-Q-ST-70-60 and designed as per ECSS-Q-ST-70-12, except for the cases from requirements 5.3.2d and 5.3.2e.

ECSS-Q-ST-70-60_1390006

d. In case the self-heating of maximum 10 °C in conformance with requirement 13.6.2a from ECSS-Q-ST-70-12 or in case the operational temperature of maximum 95 °C in conformance with requirement 13.6.2c from ECSS-Q-ST-70-12 is exceeded, it shall be specifically covered by the project qualification of flexible PCB for harness.

NOTE Current rating of ECSS-Q-ST-70-12 can be too conservative for harness applications for power lines.

ECSS-Q-ST-70-60_1390007

e. In case reliable insulation in Z-direction is not in conformance with Table 13-6 from ECSS-Q-ST-70-12, it shall be specifically covered by the project qualification of flexible PCB for harness.

NOTE The test plan can be based on the test selection for a change in dielectric material from clause 7.2d.

ECSS-Q-ST-70-60_1390008

f. Electrical testing of the integrated subsystem of connector and flexible PCB shall be specifically covered by the project qualification of flexible PCB for harness.

NOTE An example of a relevant electrical test is DWV in conformance with clause 9.6.4, using 1000 VDC for 30 s. Another example of a relevant electrical test is the whole length voltage test and whole length insulation resistance test in conformance with clauses 9.7b and 9.8b from ESCC-3901. Tests for qualification and for procurement in conformance with ECSS-Q-ST-70-60 includes high resistance electrical test with a 1 GΩ insulation resistance threshold in conformance with clause 9.3.7.2 and continuity test in conformance with 9.3.8.

ECSS-Q-ST-70-60_1390009

g. Dynamic application shall be specifically covered by the project qualification of flexible PCB for harness, including at least the following:

1. evaluation of the mechanical integrity of the insulation due to routing limitations, and
2. mechanical testing from ESCC-3901 tailored to meet the application, and
3. electrical evaluation before and after mechanical test and qualitative evaluation by microsectioning after mechanical test.

NOTE 1 Mechanical integrity of the insulation can be impacted by abrasion, point loads and the dynamic movement.

NOTE 2 In addition, dynamic application can be covered at unit level as specified in clause 4.8.3 of ECSS-E-ST-33-01. Unit level qualification testing is performed at a later stage in the project than qualification of subassemblies including the flexible PCB.

ECSS-Q-ST-70-60_1390010

h. RF application shall be specifically covered by the project qualification of flexible PCB.

ECSS-Q-ST-70-60_1390011

i. Assembly to flexible PCB using PTH or SMT shall be verified in conformance with ECSS-Q-ST-70-61.

5.4 Qualification process

ECSS-Q-ST-70-60_1390012

a. The process for PCB qualification shall contain the following stages:
   1. request for qualification and associated documentation in conformance with clause 5.5,
   2. evaluation of a technology sample in conformance with clause 5.8,
   3. audit of the manufacturing facility in conformance with clause 5.9,
   4. qualification programme in conformance with clause 5.10.

ECSS-Q-ST-70-60_1390013

b. The approval from the qualification authority of the completed qualification shall be in conformance with clause 5.12.

5.5 Request for qualification

ECSS-Q-ST-70-60_1390014

a. The PCB manufacturer shall send a formal request for qualification to the qualification authority.

ECSS-Q-ST-70-60_1390015

b. The PCB manufacturer shall provide the company profile including the following information:
   1. description of the manufacturer capabilities,
   2. business plan with basic financial figures for sales and R&D.

      NOTE The business plan demonstrates a healthy economical business and a strong commitment to quality assurance for space products.

ECSS-Q-ST-70-60_1390016

c. The PCB manufacturer shall demonstrate the heritage on the PCB technologies for which qualification is requested, by providing the types of technology and quantity of PCBs produced for non-space customers, industrial space customers and space agencies.

NOTE This is in particular important for the approved surface finishes, such as hot oil reflowed tin-lead.

ECSS-Q-ST-70-60_1390017

d. The PCB manufacturer shall provide a letter of support from the main industrial space customers.

ECSS-Q-ST-70-60_1390018

e. The PCB manufacturer shall provide a preliminary strategic planning, indicating the following:

1. the space projects for which qualified PCBs are foreseen to be provided,
2. identification of the current customers that can benefit from possible qualification,
3. identification of new customers or orders that can be gained in case qualification is achieved,
4. identification of technologies that are foreseen to be qualified initially and in the medium and longer term,
5. the internal resource estimate for achieving qualification,
6. a target schedule for all activities related to achieving qualification.

ECSS-Q-ST-70-60_1390019

f. The PCB manufacturer shall provide the completed survey for assessment of the PCB manufacturer's capabilities in conformance with IPC-1710.

ECSS-Q-ST-70-60_1390020

g. The PCB manufacturer shall demonstrate that it meets the requirements for quality assurance in conformance with clause 5.6.

5.6 Quality standards

ECSS-Q-ST-70-60_1390021

a. The quality assurance requirements specified in ECSS-Q-ST-20 shall apply.

ECSS-Q-ST-70-60_1390022

b. The PCB manufacturer shall manage nonconformances in accordance with ECSS-Q-ST-10-09.

ECSS-Q-ST-70-60_1390023

c. The PCB manufacturer shall hold certification for its quality management system in conformance with ISO 9001:2015 and EN 9100:2016 or demonstrate that he has a quality management system in line with the above standards.

5.7 Description of qualification vehicle

ECSS-Q-ST-70-60_1390024

a. The PCB manufacturer shall provide the PCB definition dossier, in conformance with the DRD in Annex A of ECSS-Q-ST-70-12, to the qualification authority for approval of the qualification vehicle.

ECSS-Q-ST-70-60_1390025

b. The qualification vehicle shall be representative of the highest technological complexity for which qualification is requested.

ECSS-Q-ST-70-60_1390026

c. The design of the qualification test vehicle shall accommodate the tests specified in clause 7.

NOTE Examples of test patterns are shown in IPC-2221C.

ECSS-Q-ST-70-60_1390027

d. The design of the qualification vehicle shall be in conformance with requirements from ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390028

e. The coupons that are included in the qualification vehicle shall be in conformance with the clauses 8.2.2 and 8.2.3.

ECSS-Q-ST-70-60_1390029

f. Initial qualification of a PCB manufacturer or PCB technology in conformance with requirement 7.2b shall be performed on at least 3 PCBs and the coupons in conformance with Figure 7-1.

ECSS-Q-ST-70-60_1390725

g. Initial qualification of a PCB manufacturer or PCB technology in conformance with requirement 7.2b should include a spare PCBs and spare coupons in conformance with Figure 7-1.

ECSS-Q-ST-70-60_1390030

h. Delta qualification and qualification renewal in conformance with requirement 7.2 shall be performed on at least 1 PCB and associated coupons.

5.8 Evaluation

ECSS-Q-ST-70-60_1390031

a. The requirements of clause 5.7 shall apply to the evaluation samples.

ECSS-Q-ST-70-60_1390032

b. The submission of evaluation samples shall include PCB, coupons, microsections and documentation in conformance with requirement 5.15a.

ECSS-Q-ST-70-60_1390726

c. A first set of evaluation samples should be evaluated by a third-party.

NOTE It is beneficial to request a third-party evaluation by a company with knowledge on evaluation in conformance with ECSS-Q-ST-70-60.

ECSS-Q-ST-70-60_1390033

d. The test flow for evaluation shall be in conformance with requirements from clause 7.5.

NOTE 1 This test flow includes DPA of PCB and coupons and IST.

NOTE 2 Any duplication of IST tests on panels for evaluation, qualification and procurement allows assessment of batch-to-batch reproducibility.

NOTE 3 The evaluation phase is only performed in case of qualification of new PCB manufacturers. It is intended as a relatively fast assessment of the quality to gain confidence in the product before initiating the full qualification programme. Therefore the evaluation typically does not include mission representative thermal cycling, which is included in qualification.

ECSS-Q-ST-70-60_1390034

e. The qualification authority shall perform the evaluation and issue the test report.

ECSS-Q-ST-70-60_1390035

f. The qualification authority shall provide to the PCB manufacturer the authorization to proceed with the qualification in case all the following conditions are met:

1. Evaluation is acceptable.
2. Assessment of the request for qualification, in conformance with the clause 5.5, is acceptable.

NOTE It is the intention to perform a PCB evaluation only once. In case the first attempt fails, a second final opportunity for passing the evaluation successfully can be offered. The qualification process can be discontinued in case the evaluation fails or in case the schedule as agreed in the strategic planning is exceeded.

5.9 Audit

ECSS-Q-ST-70-60_1390036

a. The qualification authority shall audit the manufacturing line.

ECSS-Q-ST-70-60_1390037

b. The audit shall occur when PCB production is in progress.

ECSS-Q-ST-70-60_1390038

c. Before the audit, the PCB manufacturer shall make the following documents available to the qualification authority for review and approval:

1. PID in conformance with the DRD in Annex D;
2. Qualification test plan in conformance with clause 7.1 including test description, test vehicle and schedule.

ECSS-Q-ST-70-60_1390039

d. The qualification authority shall submit to the PCB manufacturer an audit checklist that verifies the requirements from ECSS-Q-ST-70-60 and its normative references one month prior to the date of the audit.

ECSS-Q-ST-70-60_1390040

e. The PCB manufacturer shall provide the response to the audit checklist to the qualification authority at least one week prior to the date of the audit.

ECSS-Q-ST-70-60_1390041

f. The response from the PCB manufacturer in the audit checklist shall include the following:

1. compliance level as follows:
   (a) “compliant” or
   (b) “non-compliant” or
   (c) "partial compliant” or
   (d) “not applicable”,
2. a comment explaining any non-compliance, partial compliance or non-applicability,
3. references to work instructions that specify the verified requirement.

ECSS-Q-ST-70-60_1390042

g. During the audit, the PCB manufacturer shall make the following documents available to the qualification authority:

1. Documented information in conformance with EN 9100:2016 clause 4.2.2.
2. Business process procedures, in conformance with EN 9100.
3. Work instructions, in conformance with EN 9100.

NOTE 1 Quality manual is one possible type of Documented information from 5.9g.1.

NOTE 2 See definition of work instructions in clause 3.2.54.

ECSS-Q-ST-70-60_1390043

h. In case of an audit for qualification renewal, the PCB manufacturer shall provide the following:

1. A summary of the QA reports in conformance with clause 5.14.
2. Lists of PCBs per PID supplied in conformance with ECSS-Q-ST-70-60 since the previous audit.

ECSS-Q-ST-70-60_1390044

i. The qualification authority shall issue the audit report and any findings, in conformance with clause 5.9j.

NOTE The minutes of meeting can be the audit report.

ECSS-Q-ST-70-60_1390045

j. Findings from the audit shall be categorised by the qualification authority as follows:

1. “Major nonconformance” is a nonconformance against ECSS-Q-ST-70-60 that is evaluated by the qualification authority as mandatory to disposition by a corrective action for successful audit closure.
2. “Minor nonconformance” is a nonconformance against ECSS-Q-ST-70-60 that is a longer term action for continuous improvement and therefore not preventing successful audit closure according to the qualification authority.
3. “Observation” is a recommendation or observation that does not prevent successful audit closure and that is not a nonconformance against ECSS-Q-ST-70-60.

ECSS-Q-ST-70-60_1390046

k. The audit report and any findings shall be approved and signed by the PCB manufacturer and qualification authority.

ECSS-Q-ST-70-60_1390047

l. Corrective actions from findings shall be added to the updated audit report or minutes of meeting of a delta audit.

ECSS-Q-ST-70-60_1390048

m. The final conclusion of the audit process shall be provided in the final audit report or minutes of meeting.

5.10 Qualification test programme

ECSS-Q-ST-70-60_1390049

a. The requirements of clause 5.7 shall apply to the qualification vehicle.

ECSS-Q-ST-70-60_1390050

b. The PCB manufacturer shall perform the qualification tests as specified in the qualification test plan in conformance with requirement 7.2b and approved by the qualification authority in conformance with requirements 5.9c and 5.9k.

NOTE The PCB manufacturer can use labs from a third-party or from the customer to perform tests.

ECSS-Q-ST-70-60_1390051

c. The PCB manufacturer shall issue the qualification test report in conformance with the DRD in Annex C.

ECSS-Q-ST-70-60_1390052

d. The PCB manufacturer shall provide the qualification test report to the qualification authority for review and approval.

ECSS-Q-ST-70-60_1390727

e. The qualification authority may request to the PCB manufacturer an additional test vehicle or microsections for evaluation.

5.11 PID

ECSS-Q-ST-70-60_1390053

a. The PCB manufacturer shall issue the PID in conformance with the DRD of Annex D.

ECSS-Q-ST-70-60_1390054

b. The specific parts of the PID shall be issued, in conformance with D.2.1.2, for the following PCB technologies in separate documents:

1. Polyimide rigid
2. Polyimide rigid/flex
3. Epoxy rigid
4. Epoxy rigid/flex
5. HDI, including Polyimide HDI and High Speed HDI
6. RF
7. Flexible
8. Sculptured flex
9. Low thermal expansion materials

5.12 Qualification approval

ECSS-Q-ST-70-60_1390055

a. Upon successful qualification, the qualification authority shall issue a qualification letter in conformance with the DRD in Annex A.

ECSS-Q-ST-70-60_1390056

b. The qualification authority shall publish the qualification status.

ECSS-Q-ST-70-60_1390057

c. The reason for a change or updated qualification status shall be published as a comment to the qualification status.

NOTE The term "qualified" can be used to indicate a valid qualification status. The term "not qualified" can be used to indicate an invalid qualification status, for instance as a result of nonconformances during qualification renewal or as a result of an expired qualification period. The status is not definite and can be updated when new results are available. A comment is included to clarify the reason for the qualification status. A definite disqualification or discontinuation of PCB technology or PCB manufacturer can be indicated by deletion from the published list or by the terms "disqualified" or "discontinued".

ECSS-Q-ST-70-60_1390058

d. The qualification authority shall grant qualification approval to the PCB manufacturer based on the acceptance of the evaluation in conformance with clause 5.8, the audit in conformance with clause 5.9 and the qualification programme in conformance with clause 5.10.

ECSS-Q-ST-70-60_1390059

e. The qualification approval shall be valid for a period of maximum two years.

ECSS-Q-ST-70-60_1390728

f. In case nonconformances have been encountered, the qualification authority may grant a period of validity for the qualification that is shorter than two years.

NOTE One year is a commonly used qualification period to ensure a more frequent verification of the process control for a critical technology.

5.13 Process change

ECSS-Q-ST-70-60_1390060

a. Process changes shall include process parameters, chemistry, material, equipment, process flow and inspections.

ECSS-Q-ST-70-60_1390061

b. Process changes shall be categorised by the PCB manufacturer as “major” or “minor” in the PCN.

ECSS-Q-ST-70-60_1390062

c. Requests for major process changes shall be submitted to the qualification authority for approval.

NOTE Review of process changes by the qualification authority in a timely manner is important for the continuation of manufacturing.

ECSS-Q-ST-70-60_1390063

d. The implementation of a major change shall be submitted to the qualification authority for approval.

ECSS-Q-ST-70-60_1390729

e. Minor process changes may be implemented by the PCB manufacturer without prior approval of the qualification authority.

NOTE The PCN for a minor change includes the acceptable evaluation of the affected acceptance criteria in conformance with E.2.1b6.

ECSS-Q-ST-70-60_1390064

f. For major and minor process changes, the PCB manufacturer shall issue a process change notice in conformance with the DRD in Annex E to the qualification authority.

ECSS-Q-ST-70-60_1390730

g. All process change notices should be submitted to the procurement authority for information.

ECSS-Q-ST-70-60_1390731

h. Major process change notices should be submitted to the procurement authority for approval.

5.14 QA report

ECSS-Q-ST-70-60_1390065

a. The PCB manufacturer shall issue a QA report to the qualification authority in conformance with the DRD in Annex F.

ECSS-Q-ST-70-60_1390066

b. The QA report shall be issued quarterly.

5.15 Qualification renewal

ECSS-Q-ST-70-60_1390067

a. The PCB manufacturer shall submit to the qualification authority the following items for qualification renewal at least two months prior to expiration of the qualification:

1. A PCB from a normal production batch, not older than one year, that is representative of the highest technological complexity that is qualified,
2. CoC in conformance with requirement 6.4b.1,
3. Coupons and microsections in conformance with clause 8.2,
4. The description, drawing and review items from the PCB definition dossier in conformance with clauses A.2.1<2> , A.2.1<4> A.2.1<6> of ECSS-Q-ST-70-12,
5. The justification from the PCB manufacturer for the highest technological complexity being submitted,
6. The PCB manufacturer's test report on a second identical PCB.

NOTE 1 The coupons from 5.15a.3 include an IST coupon if this is specified for the technology in accordance with requirement 8.2.3a. The coupons from 5.15a.3 also include several coupons that are untested by the PCB manufacturer, in conformance with Table 8-2. It is important that these coupons are included, as it is good practice to perform, for instance, peel strength testing for qualification renewal.

NOTE 2 The highest technological complexity is difficult to obtain on a single PCB for all design features. Therefore the PCB manufacturer justifies the selection of technology submitted for qualification renewal.

NOTE 3 It is good practice to manufacture two PCBs in a panel, one of which is evaluated by the PCB manufacturer, and the other one submitted for qualification renewal together with the required coupons.

ECSS-Q-ST-70-60_1390068

b. In case requirement 5.15a is not achieved because the sample is sent late, the qualification status shall be "not qualified" after the expiration date until completion of qualification renewal, including a comment to the qualification status in conformance with the requirement 5.12c.

NOTE It is good practice that the PCB manufacturer sends the sample earlier than 2 months before expiration. If the PCB manufacturer sends multiple samples at the same time, it is good practice to allow for more than 2 months for evaluation.

ECSS-Q-ST-70-60_1390069

c. The qualification authority shall issue a qualification renewal test report.

ECSS-Q-ST-70-60_1390070

d. An audit of the PCB manufacturer shall be performed by the qualification authority at least every second year.

ECSS-Q-ST-70-60_1390071

e. Upon successful qualification renewal, the qualification authority shall approve the qualification in conformance with the clause 5.12 and issue a new qualification letter in conformance with requirement 5.12a.

ECSS-Q-ST-70-60_1390732

f. The qualification authority may decide to initiate a new qualification in the following cases:

1. the manufacturing was interrupted or qualification was expired for more than 2 years,
2. major changes in production line and its location.

5.16 Nonconformances during qualification renewal

ECSS-Q-ST-70-60_1390072

a. In case nonconformances are observed during qualification renewal, the PCB manufacturer shall perform the following:

1. Investigate root cause, implement corrective actions on associated processes and materials, demonstrate repeatability.
2. Investigate why nonconformance was not detected by outgoing inspection and perform training.
3. Verify how the nonconformance affects the running orders and inform customers.
4. Evaluate a new PCB and provide test report in conformance with 5.15a.6.
5. Have a new PCB sample evaluated by a third-party lab and provide test report.
6. Upon approval from the qualification authority, submit a new sample for qualification renewal.

NOTE Third-party evaluation from requirement 5.16a.5 is also specified in requirement 5.8c.

ECSS-Q-ST-70-60_1390733

b. In case nonconformances are observed during qualification renewal, the qualification authority should indicate the qualification status as “not qualified” until acceptable completion of the qualification renewal, including a comment to the qualification status in conformance with the requirement 5.12c, except in case of 5.16c.

ECSS-Q-ST-70-60_1390734

c. In case the PCB manufacturer demonstrates that nonconformances observed during qualification renewal are of a one-time occurrence, the qualification authority should indicate for a maximum period of 6 months the qualification status as "qualified" with a comment to identify the failed and ongoing qualification renewal.

NOTE 1 A one-time occurrence of a nonconformance does not invalidate the qualification of other orders in case the efficiency of outgoing inspection is verified. A one-off nonconformance is relatively straightforward to correct for and the qualification renewal of a second sample is, therefore, done within the maximum period of 6 months.

NOTE 2 Since the PCB manufacturer re-submits the sample for qualification renewal 2 months prior to the expiration of the qualification status in conformance with requirement 5.15a, this provides him with 4 months to complete remanufacture of the sample, third-party evaluation and all other actions specified in 5.16a.

ECSS-Q-ST-70-60_1390735

d. The qualification authority may withdraw the qualification in case:

1. Repeated nonconformances are observed during evaluation of a PCB during qualification renewal,
2. Repeated nonconformances are observed during audits,
3. Repeated nonconformances are observed with respect to the quality requirements from ECSS-Q-ST-70-60.

6
QA for manufacture and procurement

6.1 Overview

This clause describes requirements on quality assurance during the procurement and the manufacturing stages of the PCB.

6.2 Procurement process

6.2.1 Overview

This clause describes various steps in the procurement process of PCBs. This is followed by the manufacturing and inspection. Table 6-1 provides an estimation of typical lead time for the various phases for a typical batch size.

Table 6-1: Example of lead time in weeks (wk) for various phases of PCB procurement, manufacture, test and inspection.

Phase	Rigid non sequential	Rigid sequential	Flex rigid	HDI
Tooling including design review and MRR	2-3 wk	2-3 wk	2-3 wk	2-3 wk
IST coupon design data	2 wk	2 wk	2 wk	2 wk
MRR approval	0,5-1 wk	0,5-1 wk	0,5-1 wk	0,5-1 wk
Manufacturing & inspection	4 wk	5-6 wk	5-6 wk	6-7 wk
IST	2,5-4 wk	2,5-4 wk	2,5-4 wk	2,5-4 wk
Total	11-14 wk	12-16 wk	12-16 wk	13-17 wk

6.2.2 Procurement specification

ECSS-Q-ST-70-60_1390073

a. ECSS-Q-ST-70-60 shall be used as the PCB procurement specification.

NOTE It is not good practice that the procurement authority issues his own procurement specification in which he refers to ECSS-Q-ST-70-60 as an applicable or a reference document. A reason for this is because traceability of compliance to ECSS-Q-ST-70-60 can be lost. Another reason for this is because the PCB manufacturer issues its CoC against the procurement standard and he categorises his KPIs according to the used procurement standard. In case the procurement authority desires specific additional requirements that are not covered by ECSS-Q-ST-70-60, it is good practice to include these in the PCB definition dossier or in the purchase order.

6.2.3 Quotation

ECSS-Q-ST-70-60_1390074

a. The procurement authority shall start the procurement process by requesting the quotation and lead time from the PCB manufacturer for tooling, production and test of a specified quantity based on the provided PCB definition dossier.

NOTE The provided PCB definition dossier can be in a draft form, as specified in requirement 5.2e of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390075

b. The procurement authority shall maintain the PCB definition dossier under configuration control.

ECSS-Q-ST-70-60_1390736

c. The procurement authority should specify in the PCB definition dossier the reporting of work in progress, content and frequency.

ECSS-Q-ST-70-60_1390076

d. The procurement authority shall record reliable insulation in the PCB definition dossier.

NOTE Reliable insulation is specified for critical nets in conformance with requirement 13.9.2a from ECSS-Q-ST-70-12. Reliable insulation is synonymous of double insulation, as described in clause 3.2.57 of ECSS-Q-ST-70-12 and ECSS-E-ST-20C Rev.2.

ECSS-Q-ST-70-60_1390737

e. The presence of blind-via-in-pad for soldering should be recorded in the PCB definition dossier.

NOTE This can be done by a tick box.

ECSS-Q-ST-70-60_1390077

f. In case the procurement authority does not define the tolerances in the PCB definition dossier, the following tolerances shall be used:

1. external dimension: ± 0,2 mm,
2. thickness over dielectric: ± 10 %,
3. diameter of all hole types: ± 0,1 mm,
4. external dimension for flex PCB: ± 0,4 mm;
5. thickness for flex PCB: ± 20 %;
6. clearance in coverlay for flex PCB: ±0,50 mm;
7. scaling of external conductors: ± 0,15 mm for PCB size up to 35 cm or ± 0,2 mm for PCB size up to 55 cm.

NOTE 1 For point 3: Tolerance of ±0,1mm on hole diameter is equal to Δ maximum of 0,2mm.

NOTE 2 For point 7: The tolerance of scaling is determined with respect to the design file. Scaling is the compensation in the design of layers to accommodate the shrinking or elongation of that layer after all manufacturing processes.

ECSS-Q-ST-70-60_1390850

g. Scaling of external conductors shall be a review item in case it is less than specified in 6.2.3f.7 or for larger PCB dimensions.

6.2.4 Purchase order

ECSS-Q-ST-70-60_1390078

a. The procurement authority shall issue the purchase order including the reference to the quotation, the ordered quantity of PCBs, the contact persons and the completed MRR checklist in conformance with Annex G of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390079

b. The PCB manufacturer shall acknowledge the purchase order, confirm the delivery date and start the tooling activities.

6.2.5 Design review (DR)

ECSS-Q-ST-70-60_1390080

a. The PCB manufacturer shall initiate the DR, as specified in requirement 5.2a to 5.2g from ECSS-Q-ST-70-12 and provide compliance of the provided PCB definition dossier to the PID.

NOTE 1 This is also done at MRR which is at a later stage in the procurement. It is important that this information is available at the quotation phase.

NOTE 2 Design review includes design rule check (DRC).

NOTE 3 Design review is included within the tooling process.

6.2.6 MRR

ECSS-Q-ST-70-60_1390081

a. The PCB manufacturer shall complete the MRR checklist.

NOTE See example of MRR checklist in Annex G of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390082

b. The PCB manufacturer shall perform the MRR in conformance with the requirements 5.2h to 5.2k from ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390083

c. The PCB manufacturer and procurement authority shall review during the MRR as a minimum the following aspects:

1. Design review of PCB definition dossier including review items
2. Traceability of any design modifications
3. Build-up
4. Panelisation, placement of coupons and PCBs in the panel
5. Risk assessment
6. Compliance to ECSS-Q-ST-70-12
7. Compliance to ECSS-Q-ST-70-60
8. Compliance to PID recorded in PCB approval sheet part 2 from Annex G.2.1b.

NOTE For the risk assessment, it is good practice to use a risk rating from 1 to 5. At a risk rating until 3 it is typical that the PCB manufacturer endorse the responsibility of the risk. At a risk rating of 4 or 5 it is typical that the procurement authority endorses the responsibility of the risk. At a risk rating from 3 to 5 it is good practice to involve the project for acceptance of the risk, because there can be a potential schedule impact.

ECSS-Q-ST-70-60_1390084

d. In case more than three prepreg sheets are used between layers, it shall be a review item in the MRR.

NOTE More than three prepreg sheets can be used in case a large volume to be filled with resin while maintaining a specific dielectric thickness, such as for thick copper layers or blind vias.

6.3 Final and in-process inspection

ECSS-Q-ST-70-60_1390085

a. The PCB manufacturer shall demonstrate that the available manpower and equipment are able to perform the final and in-process inspection.

NOTE The verification of this requirement is performed during the audit.

ECSS-Q-ST-70-60_1390086

b. The PCB manufacturer shall include coupons on the panel for in-house quality control.

NOTE The panel also includes coupons for batch release and spare coupons. These are described in clause 8.

ECSS-Q-ST-70-60_1390087

c. Visual standards that specify the quality characteristics shall be available to each inspector.

NOTE Visual standards for final inspection can consist of photos or drawings of microsections, which are given in clause 10.

ECSS-Q-ST-70-60_1390088

d. Work instructions shall specify the processes for which an in-process inspection is performed.

ECSS-Q-ST-70-60_1390089

e. Work instructions shall specify the methodology for final inspection in conformance with clause 8.

ECSS-Q-ST-70-60_1390090

f. In-process inspection shall be specified in the PID, at least for the following processes:

1. Microvia laser drilling, to verify the diameter to the internal landing pad;
2. Microvia cleaning, to verify its efficiency;
3. Etching, to verify the tolerances on track width and spacing;
4. The AOI process, to verify its efficiency by calibration;

5. Coverlay bonding, to verify the aspect of flex laminate and coverlay in conformance with Table 10-55 and the absence of overlap of coverlay and pads in conformance with Table 10-16 Ref. c;
6. Thickness measurements after lamination.

NOTE 1 For microvia laser drilling and microvia cleaning in process 6.3f.1 and 6.3f.2, a homogeneous dielectric thickness in microvia layers is necessary to avoid nonconformances such as interconnect defect. The local thickness of dielectric can be affected by the designed footprint and the tolerances of prepreg thickness.

NOTE 2 This requirement specifies which processes are verified by in-process inspection. The work instructions referenced in the PID specify the verification method, in conformance with D.2.1.1a.8.

ECSS-Q-ST-70-60_1390091

g. Comparison of lay-out to the drawing from the PCB definition dossier shall be performed to verify presence of plated and non-plated holes and milling.

ECSS-Q-ST-70-60_1390092

h. The PCB manufacturer shall specify in its PID an approach for TMA measurements to determine Tg and CTE in Z-direction, including frequency of test and material and technology of test vehicle.

NOTE This test is specific for a build-up and for the used process equipment.

ECSS-Q-ST-70-60_1390093

i. The PCB manufacturer shall specify in its PID the range of etchback.

ECSS-Q-ST-70-60_1390094

j. In-process control by IST testing shall be in conformance with clause 9.5.5.2.1.

ECSS-Q-ST-70-60_1390851

k. The quality of drilling of mechanical holes of ≥2 mm in polyimide shall be verified by a drill hit count study.

NOTE Drill hit count studies are good practice for all materials. Polyimide resin is more brittle and more prone to resin cracks.

ECSS-Q-ST-70-60_1390852

l. The PCB manufacturer shall have a work instruction for microvia manufacture that specifies the quality aspects and the means of verification for in-process, periodic, qualification and final inspections.

NOTE Examples of microvia quality aspects are cleanliness of internal landing pad, copper

roughness of internal landing pad, penetration depth into internal landing pad, undercut, drill diameter, contact diameter, aspect ratio, barrel shape, hole wall roughness, etc.

6.4 Quality records for manufacture and procurement

ECSS-Q-ST-70-60_1390095

a. The PCB manufacturer shall retain the quality records for at least ten years and in accordance with business agreement requirements.

ECSS-Q-ST-70-60_1390096

b. The quality records shall be composed of the following:

1. Documentation of the final inspection of manufactured PCBs, including CoC and lab reports in conformance with Annex B;
2. Nonconformance reports and corrective actions in conformance with ECSS-Q-ST-10-09;
3. Qualification test reports, in conformance with requirement 5.10c;
4. Traveller;
5. Batch summary statistics;
6. Process records.

NOTE Process records typically include SPC of chemical processes, maintenance and calibration records.

ECSS-Q-ST-70-60_1390097

c. Non-nominal performance of equipment, materials or processes shall be documented including the following topics:

1. Root cause investigation;
2. Corrective action;
3. Effect on previous, ongoing and future manufacturing batches;
4. Assessment by QA personnel.

NOTE These topics are the same as for an NCR in conformance with ECSS-Q-ST-10-09.

ECSS-Q-ST-70-60_1390098

d. The PCB manufacturer shall maintain a database for calibration of electrical and mechanical manufacturing and test equipment.

ECSS-Q-ST-70-60_1390738

e. The PCB manufacturer should provide to the procurement authority the list of nonconformances specific to them, as reported quarterly in the QA report in conformance with F.2.1a.3.

ECSS-Q-ST-70-60_1390853

f. The PCB manufacturer shall define a control plan of key processes for periodic quality control.

ECSS-Q-ST-70-60_1390854

g. Key processes should include drilling, plating, lamination, surface finish, via prefilling, planarization.

ECSS-Q-ST-70-60_1390855

h. For key processes the following periodic quality controls should be implemented:

1. Identification of key process parameters, means and frequency of verification and recording of documentation;
2. Records of audits of line surveys from chemistry and equipment suppliers to verify and approve that processes are operated within recommended conditions.

ECSS-Q-ST-70-60_1390856

i. The PCB manufacturer shall have a maintenance plan.

NOTE The maintenance plan can cover the following:

- chemical processes; pre dip, post dip and rinse: air exhaust system, external regeneration system, chemical storage, dosing and control system, criteria for make up, regeneration during production and maximum shelf life
- plating lines: cleanliness of electrical contacts, anodes/bags, rectifiers for output current, signal shape for pulse plating, vibration, agitation by mechanical/air/venturi/ultra sonic system
- other manufacturing equipment: filtering system , heating/cooling external systems, lamination press
- tooling used for PCB handling during manufacturing: lamination caul plate, plating racks, baskets
- measurement systems: XRF, Hall effect probe, Xray.

6.5 Control of materials and chemistry

ECSS-Q-ST-70-60_1390099

a. The base materials shall be in conformance with clause 5 from ECSS-Q-ST-70.

ECSS-Q-ST-70-60_1390100

b. The base materials shall be in conformance with IPC-4101E for rigid laminates, IPC-4103B for RF laminates, IPC-4204B for flexible laminates and IPC-4203B for coverlay.

ECSS-Q-ST-70-60_1390101

c. In case of reliable insulation in conformance with requirement 6.2.3d, the base materials for rigid laminates and prepreg shall be in conformance with IPC-4101E Appendix A.

NOTE Reliable insulation is specified in clause 13.9 of ECSS-Q-ST-70-12. Annex I describes the more stringent cleanliness requirements for prepreg and laminate from IPC-4101E Appendix A.

ECSS-Q-ST-70-60_1390102

d. Base materials in conformance with IPC-4101E Appendix A shall be manufactured by a laminate supplier that is listed in the IPC QPL or that passed a specific audit from the PCB manufacturer.

ECSS-Q-ST-70-60_1390739

e. For requirement 6.5b, newer revisions of the referenced IPC standards may be used in case raw materials can only be procured in conformance to those newer revisions.

ECSS-Q-ST-70-60_1390740

f. For requirement 6.5c and 6.5d, newer revisions of the referenced IPC-4101E standard may be used in case

1. raw materials can only be procured in conformance to those newer revisions, and
2. it is in conformance with Appendix A from IPC-4101E.

NOTE The text from Appendix A of IPC-4101E is included in Annex I.

ECSS-Q-ST-70-60_1390103

g. Prepreg, laminate, flex laminate, coverlay, bond-ply, copper foil, heat sinks and metal core shall be selected, inspected and tested in conformance with the work instruction as specified in the PID.

NOTE Tests can include chemical and physical testing.

ECSS-Q-ST-70-60_1390104

h. The PCB manufacturer shall separate, and prevent the use of raw materials and semi-finished products that are awaiting completion of test results.

ECSS-Q-ST-70-60_1390105

i. The PCB manufacturer shall segregate, mark and record noncompliant materials and PCBs.

ECSS-Q-ST-70-60_1390106

j. The PCB manufacturer shall control the storage conditions and duration of materials and chemistry with limited shelf-life and verify the validity of the relevant material for use.

ECSS-Q-ST-70-60_1390107

k. The verification and relife procedure of limited shelf-life materials shall be in accordance with ECSS-Q-ST-70-22, except for prepreg in conformance with requirement 6.5l.

ECSS-Q-ST-70-60_1390108

l. The verification and relife procedure of prepreg shall be performed by the raw material supplier and documented in a new CoC for the prepreg.

NOTE 1 The new prepreg CoC include a new shelf-life. Shelf-life and storage conditions are important for the flow factor of prepreg, particularly for no-flow prepreg.

NOTE 2 It is good practice to allow for the lead time for relife tests when anticipating supply of material for PCB manufacture.

ECSS-Q-ST-70-60_1390857

m. To improve outgassing performance, curing of solder mask should be done with an additional UV bump.

6.6 Control of plating chemistry

ECSS-Q-ST-70-60_1390109

a. Pure tin finish with > 97 % purity shall not be used, in conformance with the requirement 5.2.2a of ECSS-Q-ST-70.

ECSS-Q-ST-70-60_1390110

b. Electrolytic copper plating shall have a purity of ≥ 99,5 % copper.

ECSS-Q-ST-70-60_1390111

c. Electrolytic soft gold plating shall have a purity of ≥ 99,8 % gold, except for the case of electrolytic hard gold plating.

ECSS-Q-ST-70-60_1390741

d. Electrolytic hard gold plating may contain 0,3 % cobalt.

ECSS-Q-ST-70-60_1390112

e. For solderless interconnection hard gold shall be used.

NOTE 1 The thickness of the hard gold layer is important.

NOTE 2 Alternative surface finishes can be used for solderless connection under RFA in conformance with ECSS-Q-ST-70-61. It is not good practice to use tin-lead finish for these applications.

ECSS-Q-ST-70-60_1390113

f. For electrical interconnection by wire bonding, adhesive bonding or bolted interconnection, soft gold may be used.

NOTE 1 For wire bonding bright aspect is preferred but matt aspect can be used.

NOTE 2 Tin-lead finish is not used for these applications, as specified in 11.2.g of ECSS-Q-ST-70-61.

ECSS-Q-ST-70-60_1390114

g. Electrolytic pure nickel plating shall have a purity of ≥ 99,95 % nickel, except in the case of electrolytic nickel alloy plating.

ECSS-Q-ST-70-60_1390115

h. Electrolytic gold plating shall have ≤ 0,2 % silver.

ECSS-Q-ST-70-60_1390116

i. ENIG, ENEPIG and ENIPIG finish plating thickness shall be verified once per panel in conformance with Table 10-13.

ECSS-Q-ST-70-60_1390117

j. ENIG, ENEPIG and ENIPIG finish plating thickness shall be in conformance with IPC-4552A, IPC-4556, chemistry supplier specifications and plating company work instructions.

ECSS-Q-ST-70-60_1390118

k. ENIG, ENEPIG and ENIPIG thickness measurements using XRF shall be calibrated in conformance with IPC-4552A and IPC-4556.

ECSS-Q-ST-70-60_1390119

l. ENIG, ENEPIG and ENIPIG adhesion shall be verified once per batch by tape test on a coupon with finest pitch pattern as representative of the specific PCB design, as specified by the PCB manufacturer.

ECSS-Q-ST-70-60_1390120

m. The responsible operator for ENIG, ENEPIG and ENIPIG process shall be informed about the type of dielectric materials of the PCB.

ECSS-Q-ST-70-60_1390121

n. Conformance with IPC-4552A and IPC-4556 for ENIG, ENEPIG and ENIPIG processes shall be evaluated by audit, including MTO, physical and chemical bath parameters, bath contamination, SPC and verification procedures.

ECSS-Q-ST-70-60_1390858

o. Hypercorrosion of ENIG shall be in conformance with the Table 10-39.

ECSS-Q-ST-70-60_1390859

p. Hypercorrosion of ENEPIG and ENIPIG shall be in conformance with the Table 10-40.

6.7 Cleanliness of PCB processes

6.7.1 Overview

PCBs can fail due to latent short circuits, which can be caused by random contamination inside the dielectric PCB material. Contamination can comprise of fibres in laminate or on prepreg layers and can originate from the PCB manufacturing processes or from the base material supply chain.

Cleanliness of base materials is addressed to the base material supply chain as described in requirements 6.5c and 6.5d.

High resistance electrical test is specified on final PCBs with the aim to identify leakage current that can be caused by contamination, as specified in 9.3.7.

THB test on coupons is specified in 9.7.2 with the aim to determine the effects of contamination on ECM.

Clause 6.7.2 specifies requirements for the PCB manufacturing processes. The processes after innerlayer etching until lay-up are considered critical with respect to cleanliness. The PCB manufacturing processes are mostly taking place in rooms with controlled environment. This environment can, however, include the risk of collecting dust particles on materials processed or stored in these rooms. The lay-up process is the final process during which innerlayers can be inspected. This process is also the most critical one for introducing unwanted contamination. The requirements specified in this clause address this risk. This can be referred to by the term “FOD prevention”.

Another risk can be created by contaminants, such as agglomerations of solvent residue, that can be embedded and remain invisible on raw materials. High temperature during lamination can cause these contaminants to carbonise. This risk is not specifically addressed or mitigated by this clause.

An example of room configuration implementing cleanliness practices in the lay-up room from the innerlayer bond preparation process to lamination is shown in Figure 6-1.

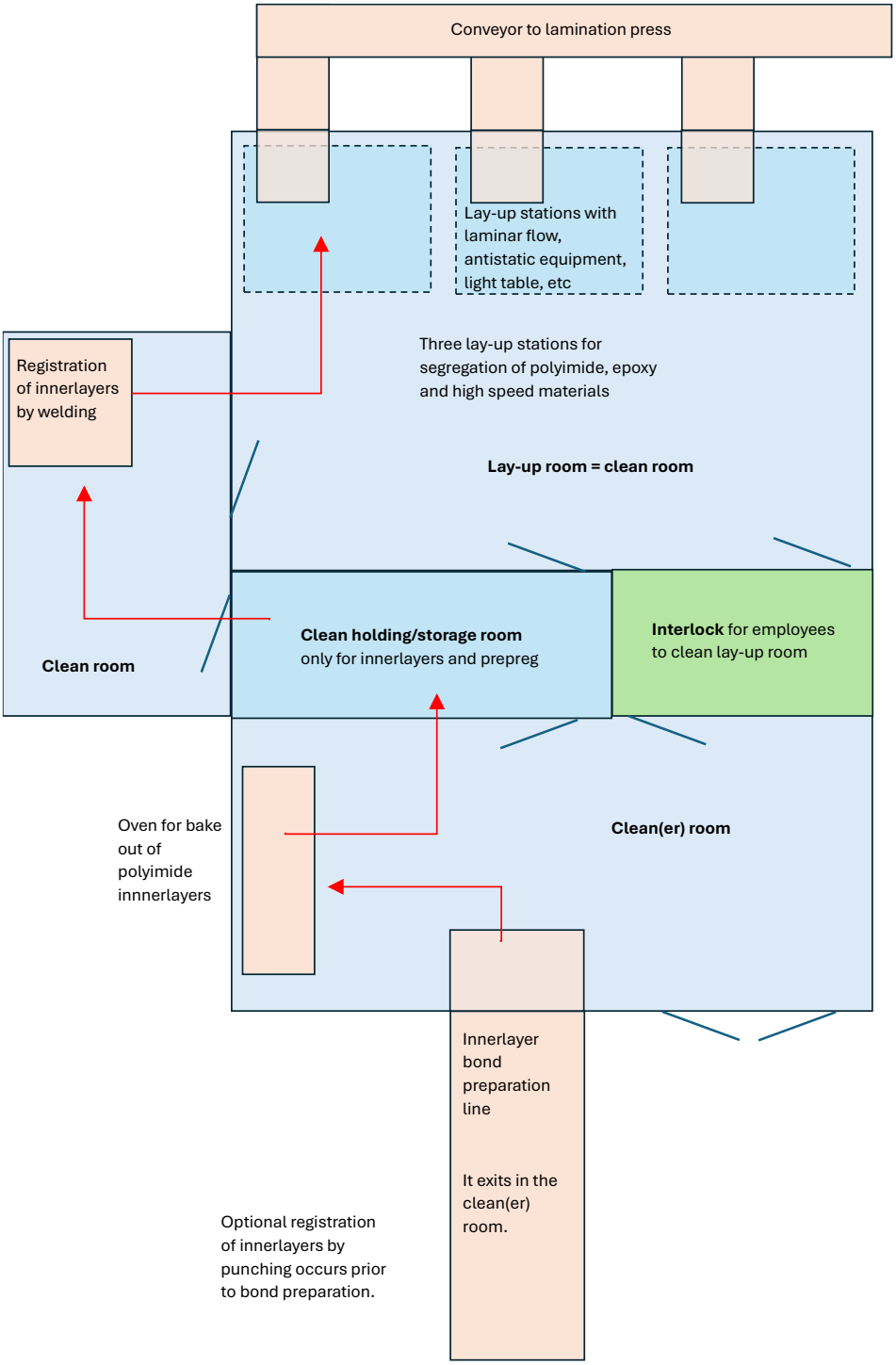


Figure 6-1: Example of cleanliness practices in the lay-up room

6.7.2 Cleanliness control

ECSS-Q-ST-70-60_1390122

a. The PCB manufacturer shall treat all processes from innerlayer etching until lay-up as critical processes with respect to cleanliness.

ECSS-Q-ST-70-60_1390123

b. The PCB manufacturer shall have a cleanliness control procedure that includes at least the following:

1. cleanliness of prepreg sheets until the lay-up process and any cleaning methods in conformance with requirement 6.7.2f;
2. cleanliness of etched innerlayers until the lay-up process and any cleaning methods in conformance with requirement 6.7.2f;
3. verification of the efficiency of cleaning on innerlayers and prepreg and its acceptance criteria;
4. restrictions of the use of materials that charge statically and attract fibres;
5. clean room practices in lay-up area in conformance with requirements 6.7.2c, 6.7.2d, 6.7.2e, 6.7.2g and 6.7.2h;
6. reference to work instructions for the general cleaning of the room;
7. reference to work instructions to segregate epoxy resin dust from polyimide in conformance with requirement 6.7.2i.

NOTE 1 Materials used with innerlayers that show static charging are, for instance, separator sheets or transport trays.

NOTE 2 Verification of cleanliness of innerlayers or prepreg can be done by inspection under UV light and bright light. Dust particles are UV fluorescent. Epoxy resin dust is UV fluorescent. Polyimide resin dust is typically not UV fluorescent.

ECSS-Q-ST-70-60_1390124

c. The room for the lay-up process shall include the following:

1. overpressure;
2. filtered air supply;
3. protective clothing that do not release fibres for operators;
4. prevention of sticky surfaces or cavities in furniture where fibres collect.

NOTE Protective clothing can include shoes, hat, coat, and gloves.

ECSS-Q-ST-70-60_1390742

d. The room for the lay-up process should include the following:

1. monitoring of airborne contamination;
2. general clean room class 8 or better, in accordance with ISO-14644-1:2015.

NOTE A formal cleanroom class as per ISO specification is difficult to obtain because of handling prepreg inside the room that creates dust. The objective is to reduce the risk of foreign contaminants in the room.

ECSS-Q-ST-70-60_1390743

e. Local measures for cleanliness at the lay-up area should include the following:

1. laminar flow bench;
2. de-ionisation equipment;
3. local monitoring of particulate contamination;
4. local cleanliness class 6 or better, in accordance with ISO-14644-1:2015.

ECSS-Q-ST-70-60_1390744

f. Prior to lay-up, cleaning of prepreg sheets and etched inner layers should be performed by using vacuum hovering or by use of tacky rollers or wipes.

ECSS-Q-ST-70-60_1390745

g. Motor parts for any vacuum hovering should be located outside of the room for lay-up.

NOTE A vacuum hose can be brought into the room through the wall.

ECSS-Q-ST-70-60_1390746

h. The use of particle counters at the lay-up area should allow for the presence of prepreg dust.

NOTE Measurements can be taken on Monday morning prior to the first operation in the room. As soon as prepreg sheets are handled, measurements are compromised by the prepreg dust that is not a breach of cleanliness as long as it is similar material used for the lay-up.

ECSS-Q-ST-70-60_1390125

i. Segregation of polyimide and epoxy materials in the lay-up area shall prevent inclusion of epoxy prepreg dust in the lay-up of polyimide.

NOTE This is done because epoxy can decompose and carbonise during the processing of polyimide. This can also be important for other materials combinations.

ECSS-Q-ST-70-60_1390126

j. The PCB manufacturer shall provide instructions to operators on the measures specified in its cleanliness control procure.

NOTE Examples of instructors to operators can include labels on the work floor, photographic instructions on best practices, identification of critical areas, and training.

6.8 Traceability

ECSS-Q-ST-70-60_1390127

a. The PCB manufacturer's records shall identify for all batches of PCBs the traceability of all raw materials and semi-finished products listed in the traveller and the individual process steps mentioned herein.

NOTE 1 In most cases a batch of PCBs is manufactured using raw materials from the same production batch. But it is also common practice to mix raw material from various production batches within the same PCB batch. This requirement provides this traceability.

NOTE 2 Traceability to raw materials does not need to be included in the CoC, since the procurement authority is not able to evaluate this information. Instead, the QA documentation of the PCB manufacturer is subject to audit or to specific enquiry from its customers.

ECSS-Q-ST-70-60_1390128

b. All panels within a batch shall be laminated on the same day and plated on the same day, except the case in requirement 6.8c.

ECSS-Q-ST-70-60_1390129

c. In case panels within a batch are not laminated on the same day or not plated on the same day, it shall be reported on the CoC.

ECSS-Q-ST-70-60_1390747

d. In case panels within a batch are not laminated on the same day or not plated on the same day, the reason for it should be reported on the CoC.

ECSS-Q-ST-70-60_1390130

e. Each PCB and coupon shall have a unique marking for traceability to batch and panel number.

ECSS-Q-ST-70-60_1390131

f. The marking on PCB and coupon shall be resistant to tests and processes.

ECSS-Q-ST-70-60_1390132

g. Marking on coverlay for flexible PCB and sculptured flex PCB shall not lift after tape test in conformance with clause 9.4.5.

ECSS-Q-ST-70-60_1390133

h. The marking shall be in conformance with the PCB definition dossier.

ECSS-Q-ST-70-60_1390134

i. The outgassing of marking shall be in conformance with ECSS-Q-ST-70-02.

ECSS-Q-ST-70-60_1390135

j. Conductive marking shall be treated as a conductive element on the PCB.

ECSS-Q-ST-70-60_1390136

k. The traceability from the PCB manufacturer shall enable localisation of PCBs and coupons on the panel.

ECSS-Q-ST-70-60_1390137

l. The PCB manufacturer shall issue a CoC in conformance with the DRD from Annex B for delivered PCBs within the batch.

ECSS-Q-ST-70-60_1390138

m. In case some PCBs within the batch are delivered later, the PCB manufacturer shall at least issue a new declaration of conformance from the CoC in conformance with B.2.1.2.

NOTE Spare PCBs can be stored by the PCB manufacturer and delivered to the customer at a later time if re-ordered. In case the lab reports from the original delivered CoC covers the spare ones, a new lab report does not need to be issued. The new declaration of conformance is sufficient to ensure traceability.

6.9 Operator and inspector training

ECSS-Q-ST-70-60_1390139

a. All operators and inspectors shall be trained for their task and for the understanding of the applicable quality assurance requirements.

ECSS-Q-ST-70-60_1390860

b. For operator dependant processes, the following shall be specified in the work instructions:

1. operator training;
2. verification;
3. the method to obtain repeatability;
4. the number of capable operators, including back-up.

NOTE Example of operator dependant processes are SnPb hot oil reflow and manual planarization.

6.10 Repair of bare PCBs

6.10.1 Overview

Repair are operations done on a PCB at the end of the manufacture. They are usually the consequence of the visual inspection.

6.10.2 General

ECSS-Q-ST-70-60_1390140

a. Repair operations shall be documented and justified in a work instruction by the PCB manufacturer and referenced in the PCB manufacturer's PID.

ECSS-Q-ST-70-60_1390141

b. Prior approval from the procurement authority shall be obtained for repair operations.

NOTE Approval can be recorded for instance in MRR, statement of compliance to this standard or the PCB definition dossier.

ECSS-Q-ST-70-60_1390142

c. The capability of operators performing repair operations shall be validated by the PCB manufacturer.

NOTE This is the case for all operations, but is specifically mentioned here because of the criticality of the repair operation.

ECSS-Q-ST-70-60_1390143

d. The repaired area shall be re-submitted to visual inspection in conformance with clause 9.3.1 and 9.3.2 by the PCB manufacturer by a different operator than the one who performed the repair.

ECSS-Q-ST-70-60_1390144

e. The CoC shall provide traceability of all repair operations.

NOTE This traceability includes the location on the PCB.

ECSS-Q-ST-70-60_1390145

f. The repaired area shall be submitted to visual inspection in conformance with clause 9.3.1 and 9.3.2 by the procurement authority during incoming inspection.

ECSS-Q-ST-70-60_1390748

g. In case SnPb is missing on the surface, it may be added with a solder iron and flux on bare surface copper in case all the following conditions are met:

1. the documented repair operation includes limits for temperature, duration and flux in conformance with clause 10 of ECSS-Q-ST-70-61;
2. the PCB manufacturer has inspected plated holes to verify the absence of missing SnPb inside them;
3. the PCB manufacturer has verified that the copper is non-etched in the area of missing SnPb.

NOTE Non-etched copper has a flat surface, whereas etched copper has a concave surface. In case copper is affected by etching, the missing SnPb is a process indicator of a problem that can affect plated holes, which cannot be repaired.

ECSS-Q-ST-70-60_1390749

h. In case dual surface finish of SnPb and electrolytic gold is used, oxidation of SnPb may be removed with a solder iron and flux.

ECSS-Q-ST-70-60_1390750

i. Excess surface copper may be removed in case it is submitted to visual inspection for the absence of weave exposure in conformance with Table 10-47, Table 10-48 and other nonconformances.

NOTE Copper removal can be done with a scalpel or laser.

ECSS-Q-ST-70-60_1390146

j. The total number of repairs in conformance with the requirements 6.10.2g, 6.10.2h, 6.10.2i and 6.10.2q shall not exceed 6 per 50 cm^2 and 6 per PCB.

NOTE This is based on ECSS-Q-ST-70-28 considering a maximum per PCB and per surface area, whichever is more restrictive.

ECSS-Q-ST-70-60_1390751

k. Haloing exceeding the requirements of Table 10-54 and Table 10-49 may be repaired using adhesive in case all the following conditions are met:

1. the haloing is not in contact with conductors on surface layer and the underlying layer;
2. the length of PCB edge for a single repair does not exceed 1 cm;
3. the total number of repairs on the PCB edges do not exceed 4.

NOTE Depaneling can cause haloing if an inadequate cutting method is used.

ECSS-Q-ST-70-60_1390752

l. In case a PCB exceeds warp or twist requirements from clauses 9.3.3.2 or 9.3.3.3, it may be flattened using pressure and elevated temperature in case the initial warp and twist does not exceed 1,6 %.

NOTE Approval for this process is specified in requirement 6.10.2b because the PCB can increase its non-flatness after storage, bake-out or assembly processes. These processes are not under control of the PCB manufacturer. The main cause for non-flatness is asymmetric build-up or shape, which is driven by the design from the procurement authority.

ECSS-Q-ST-70-60_1390753

m. Nodules that reduce the diameter of PTH to below the requirement may be removed in case all the following conditions are met:

1. The nodules are caused by fibres connecting to only 1 side of the hole wall;
2. The nodules are removed by applying slight mechanical force by probing with a gauge;
3. The integrity of the hole wall after repair is not compromised;
4. The integrity of the hole wall after repair is verified by inspection by the PCB manufacturer using a prismatic ocular;
5. SnPb is not reflowed after removal of nodule;
6. The number of repairs of nodules does not exceed 2 per PCB.

ECSS-Q-ST-70-60_1390147

n. Other repairs that are not specified in this clause shall not be performed.

NOTE Examples of such repairs are:

- repair of burrs;
- brushing of overhang of Ni/Au or Au;
- repair of PTH with too small diameter due to excessive SnPb thickness.

ECSS-Q-ST-70-60_1390861

o. Touch up of missing solder mask may be performed.

ECSS-Q-ST-70-60_1390862

p. Removal of inclusion in solder mask, followed by touch up may be performed.

ECSS-Q-ST-70-60_1390863

q. Scratches in dielectric and removal of inclusions, which exceed the limitations from ref B in Table 10-47, may be repaired by applying adhesive in case the following conditions are met:

1. scratches do not reach the copper of the internal layer;
2. scratches are not connecting two separate conductors in X,Y direction.

6.11 Packaging

ECSS-Q-ST-70-60_1390148

a. The PCBs shall be clean and baked out before packaging.

NOTE Bake out by PCB manufacturer is specified in requirements 9.2.2a and 9.2.2c.

ECSS-Q-ST-70-60_1390149

b. The PCBs and the coupons shall be packed to prevent corrosion or physical damage.

ECSS-Q-ST-70-60_1390150

c. The PCBs shall be individually packed.

ECSS-Q-ST-70-60_1390151

d. The packaging material shall be non-corrosive and not leave residue on the PCB.

ECSS-Q-ST-70-60_1390152

e. The packaging shall consist of sealed antistatic plastic bags.

ECSS-Q-ST-70-60_1390153

f. PVC packaging shall not be used.

ECSS-Q-ST-70-60_1390154

g. Packaging materials shall be in conformance with clause 5.4.5 of ECSS-Q-ST-70-61.

NOTE Requirement f of the referred clause states that pink-polyethylene (pink-poly) bags, film, bubble wrap or foam near any ESD-sensitive item or within an ESD protected area are not used.

ECSS-Q-ST-70-60_1390155

h. One of the following packaging methods shall be used:

1. Desiccant using plastic bags;
2. Dry nitrogen filling using moisture barrier bags;
3. Vacuum packing using moisture barrier bags.

ECSS-Q-ST-70-60_1390156

i. If desiccant is used, precautions shall be taken to prevent damage due to contact between desiccant and PCB.

NOTE Damage can include mechanical damage due to pressure or friction. Damage can include chemical damage to the surface finish.

ECSS-Q-ST-70-60_1390157

j. If desiccant is used, means for indication of moisture content shall be provided.

ECSS-Q-ST-70-60_1390754

k. If moisture indicator is present, it should not exceed 10% R.H.

NOTE This is specified in IPC-1602A.

ECSS-Q-ST-70-60_1390158

l. The PCBs and coupons shall be packed avoiding pressure on, or friction between the PCBs.

ECSS-Q-ST-70-60_1390755

m. Tissue or paper may be used to wrap PCBs.

ECSS-Q-ST-70-60_1390159

n. Each shipping container shall be marked according to requirements from the procurement authority.

6.12 Storage and baking of PCB and coupons

ECSS-Q-ST-70-60_1390160

a. The procurement authority shall retain the quality records, coupons and microsection for at least ten years and in accordance with business agreement requirements.

NOTE A similar requirement, see 6.4a, applies to the PCB manufacturer.

ECSS-Q-ST-70-60_1390161

b. PCBs shall be stored in a dry environment until they are soldered.

NOTE It is preferred to store in a nitrogen-purged cabinet. Alternatively dry storage can be implemented using desiccant. It is good practice to include humidity indicators, and to ensure the correct activation of the desiccant. Humidity present in standard cleanroom conditions is absorbed by the laminate and can be difficult to desorb by baking. In addition, it can be detrimental to solderability.

ECSS-Q-ST-70-60_1390162

c. PCBs shall be stored free from mechanical stress.

ECSS-Q-ST-70-60_1390756

d. Spare coupons may be stored in an uncontrolled environment.

NOTE This is acceptable because it is considered worst-case. However, it is good practice to store coupons together with PCBs as this ensures representativity in case any test, such as relife testing, is undertaken.

ECSS-Q-ST-70-60_1390163

e. Baking of PCBs prior to soldering, after short or long storage, shall be performed in conformance with requirements 9.2.2a and 9.2.2b.

6.13 Shelf-life and relife testing

ECSS-Q-ST-70-60_1390164

a. Shelf-life of PCBs shall be 5 years for SnPb finish and 1 year for ENIG/ENEPIG/ENIPIG finish.

NOTE 1 The term shelf-life refers to the period of storage of the bare PCB to the start of the soldering process.

NOTE 2 It is reasonable to expect no impact on solderability when PCBs with ENIG/ENEPIG/ENIPIG finish are stored in a dry nitrogen-purged cabinet for a period that exceeds the 1 year shelf life.

ECSS-Q-ST-70-60_1390165

b. Shelf-life shall include storage at the procurement authority and storage at the PCB manufacturer.

ECSS-Q-ST-70-60_1390757

c. Shelf-life should be calculated from the date code on the CoC.

NOTE The date code on CoC corresponds approximately to the date of manufacture.

ECSS-Q-ST-70-60_1390166

d. In case shelf-life is exceeded, the following shall be performed to relife the PCB:

1. evaluate solderability in conformance with clause 9.4.11 on one coupon of the batch in conformance with requirement 8.2.3d;
2. visual inspection of the surface finish on one PCB from the batch;

NOTE 1 Requirement 6.12b specifies that PCB are stored in dry conditions. This prevents uptake of moisture. In case PCBs are not stored in dry conditions, temporarily or prolonged, it is good practice, besides bake out, to verify the integrity of the build-up by performing a solder bath float test.

NOTE 2 No specific inspection of IMC is necessary as it is not expected to change significantly in the specified storage conditions. SnPb coverage in compliance with Table 10-12 is essential to pass the solderability test and the SnPb coverage has been verified at outgoing (and incoming) inspection.

ECSS-Q-ST-70-60_1390167

e. The relife period of a PCB shall be 6 months after successful relife testing.

NOTE This is different from relife testing as described in ECSS-Q-ST-70-22, which allows a relife period from the date of expiration.

6.14 QA for PCB procurement in space projects

ECSS-Q-ST-70-60_1390168

a. ECSS-Q-ST-70-60 shall be applicable for procurement of PCBs for flight models and for qualification models.

NOTE 1 Flight models include FM, FS, PFM. Qualification models include QM, EQM.

NOTE 2 There is no requirement to apply ECSS-Q-ST-70-60 to EM and EBB. However, nothing prevents to do it if so decided.

NOTE 3 This requirement is specified to ensure that the PCB manufacturer has feedback on meeting the requirements of ECSS-Q-ST-70-60 prior to manufacturing the flight batch and to avoid nonconformances due to lower quality levels for the referenced models.

NOTE 4 This standard can be tailored for the specific characteristics and constraints of a space project in conformance with ECSS-S-ST-00 as described in clause 1.

ECSS-Q-ST-70-60_1390758

b. The same PCB manufacturer should be used for PCB manufacture for flight models and qualification models.

ECSS-Q-ST-70-60_1390169

c. In case a different PCB manufacturer or different PCB material is used for flight models compared to qualification models, the procurement authority shall analyse in a technical note the impact on the following items:

1. Electrical performance of the equipment;
2. Mechanical performance of the equipment;
3. Thermal performance of the equipment;
4. Assembly approval status;
5. Any modifications of the PCB definition dossier done by the previous PCB manufacturer.

NOTE In case the PCB definition dossier is identical, it is not typical that change of PCB manufacturer has significant impact on electrical, mechanical or thermal performance for non-critical applications. Examples of critical technology can be impedance control, RF or specific mechanical stress applied during assembly.

ECSS-Q-ST-70-60_1390170

d. The procurement authority shall ensure that all procured PCBs meet the project requirements.

NOTE Examples of applications for projects with specific requirements are human spaceflight, long-term storage, detector technology, planetary exploration.

ECSS-Q-ST-70-60_1390171

e. The procurement authority shall list each PCB technology, in conformance with the requirement 5.11b, in the DML as a separate item.

ECSS-Q-ST-70-60_1390759

f. Individual raw materials and PCB manufacturing processes need not to be listed in the DML and DPL.

NOTE This is specified, because raw materials and manufacturing processes are covered by the PCB technology listed in conformance with 6.14e.

ECSS-Q-ST-70-60_1390172

g. The procurement authority shall specify in the DML for each PCB technology the following:

1. PCB manufacturer;
2. PCB procurement specification;
3. PCB technology description in conformance with the requirement 5.11b;
4. traceability to individual PCBs and their PCB approval sheet.

NOTE The acronym or name of the PCB in the DML can provide the traceability to the PCB approval sheet.

ECSS-Q-ST-70-60_1390173

h. The procurement authority shall complete a PCB approval sheet part 1 for each individual PCB type in conformance with requirement G.2.1a of the DRD in Annex G.

ECSS-Q-ST-70-60_1390174

i. PCB approval sheet part 1 shall be submitted prior to the PDR and subject to approval during MPCB.

ECSS-Q-ST-70-60_1390175

j. The procurement authority shall complete a PCB approval sheet part 2 for each individual PCB type in conformance with requirement G.2.1b of the DRD in Annex G.

ECSS-Q-ST-70-60_1390176

k. PCB approval sheet part 2 shall be submitted prior to the CDR and subject to approval during MPCB.

NOTE 1 The reviewed PCB approval sheets 1 and 2 are available during equipment MRR.

NOTE 2 The PCB MRR provides input for PCB approval sheet part 2.

ECSS-Q-ST-70-60_1390760

l. The procurement authority may reuse PCB approval sheets part 1 and part 2 from previous procurement in case the PCB design is recurrent.

NOTE A description of 'recurrent' designs is given in clause 4.1 of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390177

m. The procurement authority shall provide the PCB approval sheet part 1 and part 2 to its customer for review and approval during MPCBs.

ECSS-Q-ST-70-60_1390761

n. During the MPCB, the customer may request to the procurement authority the review of the PCB definition dossier.

ECSS-Q-ST-70-60_1390178

o. Customer approval shall be based on the compliance of technology parameters to the PID, as declared on the PCB approval sheet part 2.

ECSS-Q-ST-70-60_1390179

p. In case of non-compliance of a technology parameter to the PID, a delta qualification plan shall be submitted to the customer in conformance with requirement 6.14q.

NOTE Clause 7.6 specifies the requirements of tests, inspections and specimen for delta qualification.

ECSS-Q-ST-70-60_1390180

q. The delta qualification shall be covered by an RFA in conformance with clause 7.7 and reviewed during MPCB.

ECSS-Q-ST-70-60_1390181

r. The documentation of FAI on PCB in conformance with clause 8.5 shall be available for review during MPCB.

ECSS-Q-ST-70-60_1390182

s. The approval of the item in the DML shall be based on the review of PCB approval sheets of all PCBs covered by the item of the DML.

NOTE Approval by RFA in the DML is indicated by 'X' with the RFA reference number as described in table A-4 of ECSS-Q-ST-70.

ECSS-Q-ST-70-60_1390183

t. The CoC of the PCB, its records of incoming inspection and any associated RFA shall be made available by the procurement authority at the equipment MRR.

NOTE 1 In the context of space projects, the term "equipment MRR" is not the same as MRR for PCB manufacture, as specified in requirement 6.2.6b. The latter is referred to in this clause 6.14 as "PCB MRR" to distinguish from "equipment MRR".

NOTE 2 The CoC includes traceability to any repair as per requirement 6.10.2e.

ECSS-Q-ST-70-60_1390864

u. The checklist of Annex K should be used for the review of PCB technology as part of the MPCB.

ECSS-Q-ST-70-60_1390865

v. Prior to higher level integration, all FM electronic equipment may be submitted to screening thermal cycles as per the following conditions:

1. ≥4x thermal cycles are performed not exceeding acceptance levels at non-operational, or operational conditions, whichever are worst-case;
2. Thermal cycling is followed by functional and performance testing at min and max (operational) acceptance temperature levels, as per 5.5.4.1k of ECSS-E-ST-10-03.
3. This is followed by burn-in testing as per requirement 6.14w.

NOTE This can be done in vacuum or under atmospheric pressure. The reason for this acceptance level thermal cycling is specified in 4.5.3b of ECSS-E-ST-10-03 and table 5-3. This is considered a risk mitigation against infant mortality caused by open circuit failure due to a lack of thermal reliability. This thermal cycling can be followed by burn-in testing. Screening thermal cycling, even when done at benign acceptance levels for a low amount (of 4) cycles, can introduce some fatigue and consequently it can 'eat some life away' from the module.

ECSS-Q-ST-70-60_1390866

w. Prior to higher level integration, all FM electronic equipment may be submitted to burn-in testing as per the following conditions:

1. Prior to burn-in, there is the option for screening thermal cycling, as per requirement 6.14v;
2. Immediately before burn-in, the board is conditioned in normal clean room environment for 7 days (thus, not baked and not exposed to vacuum);
3. The burn-in is for ≥168 hours in ambient clean room conditions with all nets powered, as much as possible in nominal operation. The burn-in is dedicated and continuous for its duration;
4. The burn-in is followed by functional and performance testing, as per 5.5.1.1 of ECSS-E-ST-10-03.

NOTE Accumulation of nominal testing in the appropriate environmental conditions can cover for the burn-in, subject to customer approval. However, this is considered a less robust approach compared to running the burn-in "dedicated and continuous for its duration".

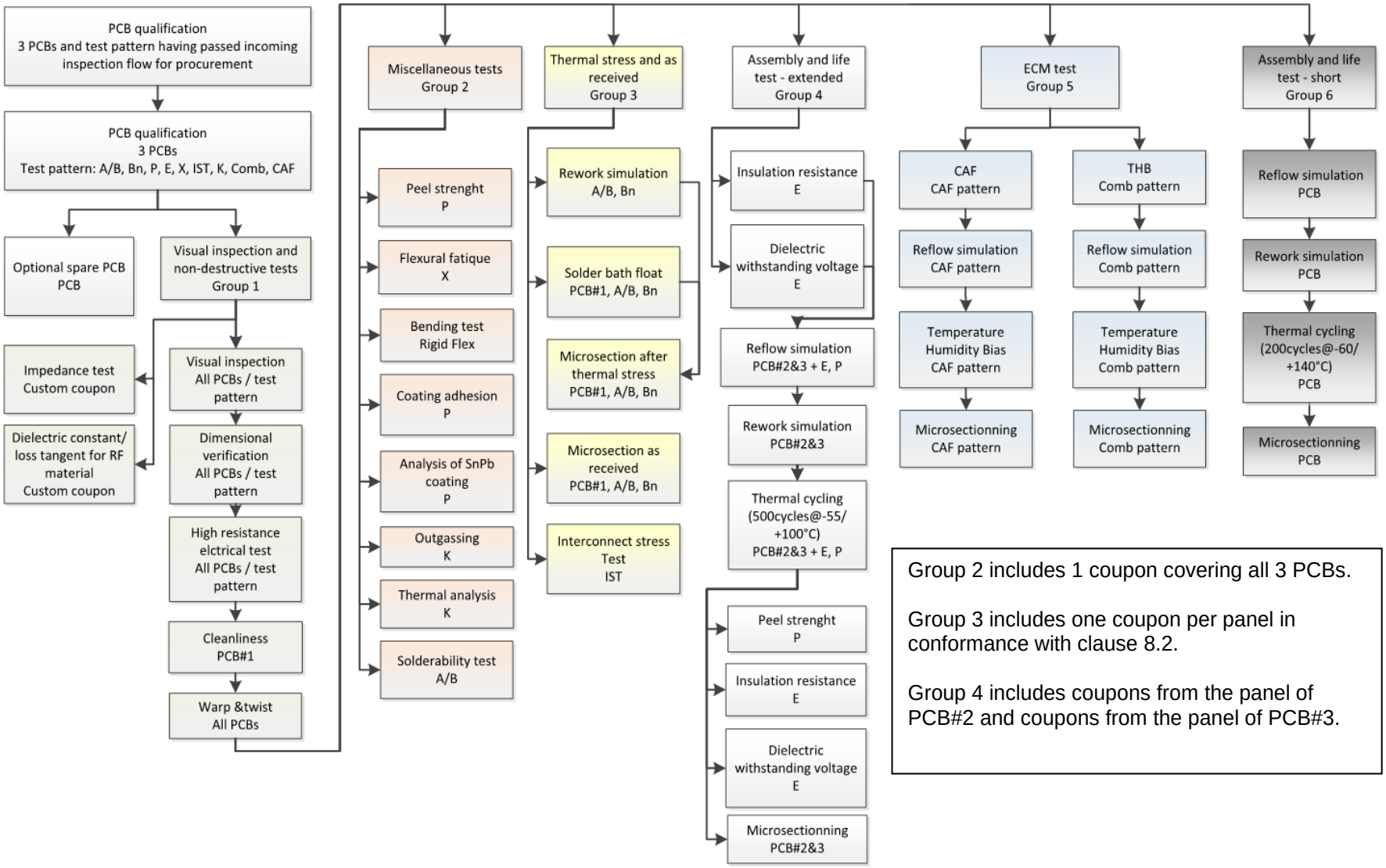
Running the burn-in at module level provides early de-risking, as opposed to at equipment level, which is later in the assembly/integration cycle. The reason for this burn-in is specified in 4.5.3b of ECSS-E-ST-10-03 and table 5-3. This is considered a risk mitigation against electromigration and latent short circuit failures (or leakage currents).

7 Test and inspection for qualification

7.1 Overview

The matrix of selected tests for various qualification activities is shown in Table 7-2.

The tests included in each test group (group 1 to group 6) and the test vehicle is shown in Figure 7-1. A list of coupons with pattern ID is shown in Table 7-1.



ECSS-Q-ST-70-60_1390184

Figure 7-1: Test flow for qualification

Table 7-1: List of coupons with pattern ID, description and references to definition requirements

Pattern ID	Description	Requirement definition
A/B	combined coupon of plated-through holes (A) and through-going vias (B)	8.2.2c.1
Bn (=B1, B2, B3, etc.)	combined coupon of sequential vias (excluding through-going vias)	8.2.2c.2
IST	coupon for interconnect stress test	9.5.5.3
custom	custom coupon for impedance test	9.3.4
custom	custom coupon for dielectric constant and loss tangent	9.3.5
P	coupon for peel strength, coating adhesion and analysis of SnPb	9.4.2, 9.4.5, 9.4.6
X	coupon for flexural fatigue	9.4.3
rigid-flex	coupon or PCB for bending test	9.4.4
K	coupon for outgassing; thermal analysis, flammability, offgassing	9.4.7, 9.4.8, 9.4.9, 9.4.10
E	coupon for insulation resistance and dielectric withstanding voltage	9.6.3, 9.6.4
Comb	coupon containing comb pattern for THB test	9.7.2.2
CAF	coupon for CAF test	9.7.3.2
PCB#1, PCB#2, PCB#3	PCBs for visual inspection, dimensional verification, cleanliness, microsectioning as-received and after thermal stress, assembly and life testing short and extended	9.3.2, 9.3.3, 9.3.6, 9.5, 9.6, 9.8
G	coupon for solder mask adhesion by tape test	8.2.4o
AAD	custom coupon by copying the AAD footprint from the specific PCB	8.2.3l, 8.2.4m

7.2 Test selection for qualification activities

ECSS-Q-ST-70-60_1390185

a. For all qualification activities, the PCBs and coupons shall be submitted to outgoing inspection and documentation in conformance with clauses 8.1, 8.2 and 8.3.

NOTE See Annex J for an overview of a qualification programme.

ECSS-Q-ST-70-60_1390186

b. For initial qualification of a PCB manufacturer or a PCB technology, all tests of groups 1, 2, 3, 4, and 5 shall be performed on PCB and coupon.

ECSS-Q-ST-70-60_1390187

c. For qualification renewal of a technology the following test shall be performed on PCB and coupon:

1. Group 2: peel strength and solderability;
2. Group 3: all.

ECSS-Q-ST-70-60_1390188

d. For delta qualification of a process or equipment change that affects the properties of the dielectric material, the following tests shall be performed on PCB and coupons:

1. Group 1, 3, 5: all;
2. Group 4 or 6: all;
3. Group 2: peel strength, flexural fatigue, bending test, outgassing, thermal analysis.

ECSS-Q-ST-70-60_1390189

e. For delta qualification of a process or equipment change that affects the properties of the copper plating or surface finish, the following tests shall be performed on PCB and coupons:

1. Group 1: visual inspection;
2. Group 3: all;
3. Group 4 or 6: all;
4. Group 2: peel strength, solderability on PTH and SMT pad, analysis and coating adhesion of surface finish.

ECSS-Q-ST-70-60_1390190

f. For delta qualification of PCB design features, the following tests shall be performed on PCB and coupons, except for track width and spacing as specified in requirement 7.2g:

1. Group 1, 3: all;
2. Group 4 or 6: all.

NOTE PCB design features include hole size, aspect ratio, number of layers, lamination or drilling sequences, thickness of Cu or PCB, presence or absence of nonfunctional pads, microvia stacking and superpositioning, back-drilling, hole plugging material.

ECSS-Q-ST-70-60_1390191

g. For delta qualification of track width and spacing, the following tests shall be performed on PCB and coupons:

1. Group 1: visual inspection;
2. Group 3: microsectioning as received including at least the following aspects:
   (a) track width on foot and tolerances;
   (b) insulation distance and tolerances;
   (c) undercut;
   (d) etching efficiency and absence of spurious copper;
   (e) encapsulation of track by resin.

ECSS-Q-ST-70-60_1390192

h. For qualification of HDI technology, the following tests shall be performed on PCB and coupons:

1. Group 1, 3, 4, 5: all;
2. Group 2: peel strength.

ECSS-Q-ST-70-60_1390867

i. Qualification of solder mask shall meet the following conditions:

1. It is in conformance with IPC-SM-840 class H;
2. Outgassing is in conformance with ECSS-Q-ST-70-02 and clause 9.4.7;
3. Tape test as-received and after group 6 or group 4 is in conformance with clause 9.4.5.

NOTE It is good practice to include in the PID an evaluation of typical undercut on areas with minimum solder mask width and high solder mask thickness. See an example of solder mask undercut in Figure 7-2.

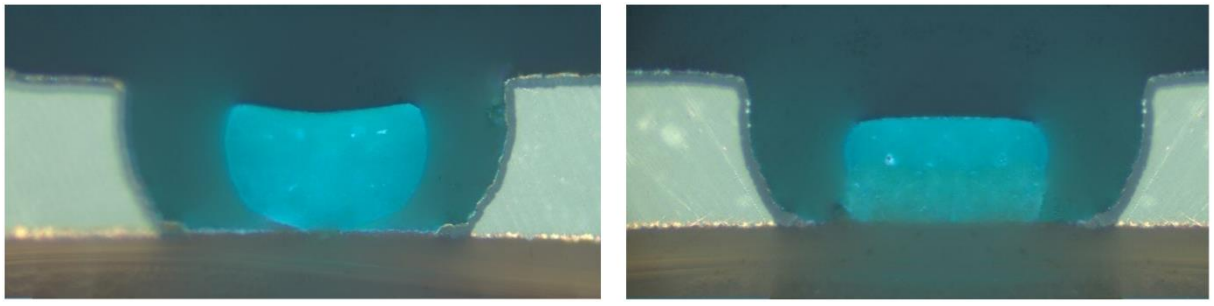


Figure 7-2: Example of solder mask undercut (left) and absence of undercut (right)

ECSS-Q-ST-70-60_1390868

j. THB testing in group 5 shall be performed to evaluate cleanliness of lay-up processes and raw materials.

ECSS-Q-ST-70-60_1390869

k. CAF testing of group 5 shall be performed to evaluate insulating properties of the dielectric for HDI technology.

Table 7-2: Test matrix for qualification and procurement

Scope of testing	Group 1 Visual inspection and non-destructive tests	Group 2 Miscellaneous tests	Group 3 Thermal stress and as-received	Group 4 Assembly and life test -extended	Group 5 ECM test	Group 6 Assembly and life test - short
Y - indicates test group to be included P - indicates part of test group to be included, followed by listed the tests that are included N – indicates test group not to be included						
Initial qualification **requirement 7.2b**	Y	Y	Y	Y	Y	N
Qualification renewal **requirement 7.2c**	Y	P peel strength, solderability	Y	N	N	N
Delta qualification **requirement 7.2d** **Process or equipment change affecting dielectric material**	Y	P peel strength, flexural fatigue, bending test, outgassing, thermal analysis	Y	Y	Y	Y
Delta qualification **requirement 7.2e** **Process or equipment change affecting plating**	P visual inspection	P peel strength, solderability, analysis of SnPb coating, coating adhesion of non-fused SnPb	Y	N	N	Y
Delta qualification **requirement 7.2f** **PCB design features** **(hole size, aspect ratio, number of layers, lamination or drilling sequences, thickness of Cu or PCB)**	Y	N	Y	N	N	Y

Scope of testing	Group 1 Visual inspection and non-destructive tests	Group 2 Miscellaneous tests	Group 3 Thermal stress and as-received	Group 4 Assembly and life test -extended	Group 5 ECM test	Group 6 Assembly and life test - short
Y - indicates test group to be included P - indicates part of test group to be included, followed by listed the tests that are included N – indicates test group not to be included						
Delta qualification requirement 7.2g PCB design features (track width and spacing)	P visual inspection	N	N	Y	N	N
Qualification of HDI Technology requirement 7.2h	Y	P peel strength	Y	Y	Y	Y, in case of project qualification
Project qualification clause 7.7	Y	N	Y	N	N	Y
FAI clause 8.5	Y	N	Y	N	N	N
Procurement clause 8	Y	N	Y	N	N	N

7.3 Initial qualification of PCB manufacturer

ECSS-Q-ST-70-60_1390193

a. Initial qualification of a PCB manufacturer shall be in conformance with clause 5.

ECSS-Q-ST-70-60_1390194

b. The test selection for initial qualification of PCB manufacturer shall be in conformance with requirement 7.2b.

7.4 Initial qualification of PCB technology

ECSS-Q-ST-70-60_1390195

a. The test selection for initial qualification of PCB technology shall be in conformance with requirement 7.2b.

ECSS-Q-ST-70-60_1390196

b. The PCB manufacturer of the new technology shall already hold a qualification in conformance with clause 5.

ECSS-Q-ST-70-60_1390197

c. The PCB manufacturer shall issue a new PID for the new technology to be qualified, in conformance with the requirement 5.11b.

ECSS-Q-ST-70-60_1390198

d. The preparation of the microsection for the qualification of the rigid-to-flex interface shall be performed using UV fluorescent resin and vacuum potting and inspected using polarised light.

NOTE See example in Figure 8-5.

ECSS-Q-ST-70-60_1390870

e. For qualification of PCB technology at least 3 PCBs shall be used in conformance with Figure 7-1.

ECSS-Q-ST-70-60_1390871

f. The PCBs from the clause 7.4e shall be from at least 2 different manufacturing panels.

NOTE The panels used for qualification include IST coupons among other coupons as specified in 7.2b.

7.5 Qualification renewal

ECSS-Q-ST-70-60_1390199

a. The test selection for qualification renewal shall be performed by the qualification authority in conformance with requirement 7.2c.

7.6 Delta qualification

ECSS-Q-ST-70-60_1390200

a. The test selection for delta qualification of materials, processes, design or equipment shall be performed by the PCB manufacturer in conformance with requirements 7.2d, 7.2e, 7.2f and 7.2g.

ECSS-Q-ST-70-60_1390762

b. The baseline test flow may be tailored and supplemented by additional tests to cover the delta qualification.

ECSS-Q-ST-70-60_1390201

c. The delta qualification shall be in conformance with clause 5.13 and documented in the process change notice.

ECSS-Q-ST-70-60_1390202

d. Upon approval of the delta qualification test report in conformance with requirements 5.10c and 5.10d, the PCB manufacturer shall document the qualified changes in the PID.

ECSS-Q-ST-70-60_1390203

e. Delta qualification of track width and spacing shall include records of AOI and visual inspection on etched inner layer to check for top and bottom of track, etch definition and spurious copper in clearance.

NOTE This is performed to evaluate the efficiency of the AOI processes for its ability to detect all dimensions under delta qualification.

ECSS-Q-ST-70-60_1390204

f. In case delta qualification is initiated in the context of a space project, the procurement authority shall handle it through an RFA, in conformance with clause 7.7.

7.7 Project qualification and RFA

7.7.1 Overview

It is preferred to use PCB technology and PCB manufacturers that are qualified in conformance with ECSS-Q-ST-70-60. Project qualification can be necessary for the use of technology that is not available from qualified sources, for instance in case innovative technology is needed. Such project qualification includes a risk to the project because the PCB technology is not widely used and because the project qualification can fail.

In case project qualification is needed, it is preferred to perform it at a PCB manufacturer that is already qualified for other technology in conformance with ECSS-Q-ST-70-60 because QA and capability has been reviewed during periodic auditing.

In case delta qualification is initiated for a space project and it is handled through an RFA, in conformance with the requirement 7.6f, it is good practice if the delta qualification for a project results in an update of the PID of the qualified PCB manufacturer. In this case, upon future procurement of the same technology, a new project qualification is not needed.

Project qualification provides approval of a PCB technology for the batch used on that project only. In case of recurrent PCB procurement, a new project qualification of the new batch is needed if the PID does not include the technology.

Project qualification typically uses a group 6 test flow which is designed to be a fast test flow on a limited number of test vehicles. This can be insufficient justification for an update of the PID depending on the technology under evaluation. Delta qualification can ensure a more thorough assignment of test flows and test vehicles with the objective to provide justification for the update of the PID.

Similarity of PCB designs covered by the project qualification can be reviewed during the DR and can result in tailoring of the project qualification test plan.

7.7.2 Requirements for project qualification and RFA

ECSS-Q-ST-70-60_1390205

a. PCB technology that is not qualified in conformance with requirement 5.1a shall be subject to project qualification for each batch using an RFA in conformance with clause 5.4.2 from ECSS-Q-ST-70.

ECSS-Q-ST-70-60_1390206

b. Project qualification shall provide approval of a PCB technology for the batch used on that project only.

ECSS-Q-ST-70-60_1390207

c. In case of recurrent PCB procurement, a new project qualification of the new batch shall be performed if the technology is not included in the PID in conformance with ECSS-Q-ST-70-60.

NOTE It is, therefore, good practice to perform delta qualification of a qualified PCB manufacturer and update its PID, in conformance with requirement 7.7.2o.

ECSS-Q-ST-70-60_1390208

d. Before the PCB procurement, the procurement authority shall submit to its customers for approval the RFA part 1 including the following:

1. PCB approval sheet in conformance with Annex G;
2. Compliance matrix to ECSS-Q-ST-70-60 for PCB qualification and description of the non-qualified aspects;
3. Compliance matrix to ECSS-Q-ST-70-12 for PCB design;
4. Compliance matrix to the PID from the PCB manufacturer;

5. Compliance to inspection on PCB and coupon for procurement in conformance with clause 8.
6. Description of the thermal, electrical and mechanical environment of the application;
7. Project qualification test plan;
8. Technical justification in case a single PCB design is intended to cover several PCBs to be used for the project;
9. Verification and inspection to be performed in case several batches are manufactured to cover for the qualification vehicle and the FMs.

NOTE 1 See Annex J for an overview of a qualification programme.

NOTE 2 The verification for batch-to-batch reproducibility from 7.7.2d.9 can include a project audit, dedicated evaluation on coupons or group 6 on spare PCBs. This is important for PCB manufacturers that are not qualified in conformance with ECSS-Q-ST-70-60 as described in the note of requirement 7.7.2e.

ECSS-Q-ST-70-60_1390763

e. The procurement authority should ensure that the group 6 from the qualification test plan is performed on one spare PCB from the FM batch.

NOTE The advantage of testing the FM batch is to ensure representativity. This is important when using non-qualified PCB manufacturers for whom batch-to-batch QA has not been verified by an audit in conformance with ECSS-Q-ST-70-60. The disadvantage of testing the FM batch is that any nonconformances are discovered at a late stage of the procurement.

ECSS-Q-ST-70-60_1390764

f. Non-qualified PCB technology should be procured from a PCB manufacturer that is qualified in conformance with ECSS-Q-ST-70-60 for other technology.

NOTE In this case only a delta qualification can be performed for the specific technology feature that is not qualified. This reduces the risk, since other technologies are already qualified and periodic auditing has been performed.

ECSS-Q-ST-70-60_1390209

g. The project qualification test plan shall include tests and inspections to evaluate all PCB technology features under qualification.

ECSS-Q-ST-70-60_1390210

h. The project qualification test plan shall include group 6 in conformance with clause 9.8 and be tailored for the following:

1. qualification status of the PCB manufacturer in conformance with ECSS-Q-ST-70-60;
2. specific project requirements;
3. PCB technology features under qualification.

NOTE The test selection specified in clause 7.2 can be used as a guideline for the project qualification test plan.

ECSS-Q-ST-70-60_1390765

i. The project qualification test plan may include specific evaluations on coupons and non-destructive inspection on PCBs.

ECSS-Q-ST-70-60_1390211

j. The project qualification test plan shall include IST testing in conformance with the requirement 9.5.5.2.3a.

ECSS-Q-ST-70-60_1390212

k. DR shall be performed in conformance with 6.2.5a with support of the PCB manufacturer to review the manufacturability and reliability of the design and to review previous heritage and test campaigns performed.

ECSS-Q-ST-70-60_1390766

l. The DR should be performed together with the final customer.

ECSS-Q-ST-70-60_1390213

m. In case risk factors are identified during DR, specific tests and inspections shall be specified in the project qualification test plan to mitigate the risk.

ECSS-Q-ST-70-60_1390214

n. After PCB procurement, the procurement authority shall submit to its customers for approval the RFA part 2 including the following:

1. project qualification test report;
2. test report for specific evaluation on coupons and PCBs in conformance with 7.7.2i and 7.7.2j;
3. outgoing inspection on PCB and coupons in conformance with 8.1 and 8.2;
4. CoC and its lab reports in conformance with 8.3a;
5. incoming inspection in conformance with 8.4.

ECSS-Q-ST-70-60_1390767

o. In case delta qualification is initiated for a space project under RFA in conformance with the requirement 7.6f, the project qualification should result in an update of the PID of the qualified PCB manufacturer.

p. In case suppliers use IPC standards as PCB procurement specification, all the following conditions shall be met:

1. The project qualification is performed using group 6 in conformance with clause 7.7.2.
2. The PCB design is in conformance with chapter 6.3 from IPC-2221C for electrical clearance.
3. IPC-6012F and IPC-6012FS for space applications are used for rigid PCBs.
4. IPC-6018D and IPC-6018DS for space applications are used for RF PCBs.
5. IPC-6013E is used for flexible and rigid-flex PCB.
6. PCB manufacturers are on the IPC QML or have passed a specific audit from the procurement authority to assess compliance to the IPC standards from conditions 3, 4 and 5.
7. Coupons and PCBs of all panels are evaluated in conformance with clause 8.
8. Coupon inspection is performed by a third-party lab for evaluation in conformance with IPC-A-600K and the applicable IPC standards from conditions 3, 4 and 5.

NOTE 1 For requirement 7.7.2p.1 during the project qualification, any HDI technology or embedded film components are evaluated.

NOTE 2 Requirement 7.7.2p.1 is in conformance with IPC-6011A clause 3.6 which specifies that the qualification assessment is as agreed between user and supplier (AABUS).

NOTE 3 Requirement 7.7.2p.2 is particularly important in case reliable insulation is applicable. However, IPC-2221C is not necessarily meeting the requirements from ECSS-Q-ST-70-12 for reliable insulation. It is good practice to implement the additional risk mitigations for reliable insulation in conformance with the present standard and ECSS-Q-ST-70-12. In case the PCB design is not performed as per ECSS-Q-ST-70-12 as described in requirement 7.7.2p.2, it is good practice to provide a compliance matrix to insulation distance for reliable insulation from clause 13.9 of ECSS-Q-ST-70-12 and requirements 6.5c and 8.5c of ECSS-Q-ST-70-60.

NOTE 4 For requirement 7.7.2p.3 it is not good practice to use only IPC-6012F class 3, which represents a lower quality class.

NOTE 5 For requirement 7.7.2p.5 it is good practice to use IPC-6013ES for space applications when this is issued.

NOTE 6 The evaluation from requirement 7.7.2p.7 includes the following:

- coupon evaluation includes IST testing in conformance with clause 9.5.5 when this is applicable to the technology,
- coupon evaluation includes three times solder bath float test and rework simulation, among others,
- PCB visual inspection is performed using 10-40x magnification,
- PCB evaluation includes high resistance electrical test with 1 GΩ insulation resistance threshold.

ECSS-Q-ST-70-60_1390872

q. For project qualification of HDI, a CAF risk assessment shall be performed.

NOTE The CAF risk assessment includes a comparison of insulation distances to the CAF test patterns of Table 9-2, Table 9-3 and Table 9-4 of clause 9.7.3. The risk of CAF is considered to be low in case the insulation is above the one specified for the ECSS pattern from these tables. CAF testing is done for generic qualification but usually not for project qualification. Nevertheless, for project qualification the risk of CAF is assessed.

8
Test and inspection for procurement

8.1 Outgoing inspection on PCB

ECSS-Q-ST-70-60_1390216

a. The PCB manufacturer shall submit PCBs to outgoing inspection as follows:

   1. visual inspection in conformance with clause 9.3.2;
   2. dimensional verification in conformance with clause 9.3.3.1;
   3. warp and twist in conformance with clauses 9.3.3.2 and 9.3.3.3;
   4. high resistance electrical test and continuity test in conformance with clauses 9.3.7 and 9.3.8.

      NOTE Solder mask is hampering visual inspection of the dielectric material on outer layers.

ECSS-Q-ST-70-60_1390217

b. The sample plan for the outgoing inspection from requirement 8.1a shall be in conformance with Table 8-1.

   NOTE Table 8-1 specifies sampling on external layers of PCBs during outgoing visual inspection. Internal layers are inspected during microsectioning for outgoing inspection as specified in clause 8.2. In addition some in-process inspections are specified in clause 6.3.

ECSS-Q-ST-70-60_1390768

c. The PCB manufacturer and procurement authority may specify a more frequent sampling plan or additional measurement locations in the PCB definition dossier.

   NOTE This can be the case if a review item has been identified during MRR, for instance for the compliance of dimensional aspects. This can be the case for small connectors using small diameter PTH that can be blocked with SnPb. This can also be the case when board geometry is critical for placement in an electronic box. Some designs can specify the thickness over metallisation. Some designs can have complex geometry due to rigid-flex or cut-outs.

ECSS-Q-ST-70-60_1390218

d. The PCB manufacturer shall perform referee testing on a spare PCB in case this is specified in Table 10-27 and 10.6.3c.

   NOTE Referee testing is specified in Ref. b and c from Table 10-27.

ECSS-Q-ST-70-60_1390219

e. The presence of coupons, the evaluation of coupons, the delivery of coupons to the customer and the delivery of microsection to the customer shall be in conformance with Table 8-2.

ECSS-Q-ST-70-60_1390220

Table 8-1: Sampling plan for outgoing visual inspection on PCB

Test method and inspected feature	Sampling
Visual inspection	all PCBs and coupons
Dimensional verification: Thickness	1 PCB per panel
Dimensional verification: Length and width	1 PCB from the batch
Dimensional verification: Diameter of all PTH size	1 PCB from the batch for PTH < 0,6 mm upon customer request: all PCBs
Dimensional verification: Smallest conductor width and spacing	1 PCB from the batch for fine pitch: all PCBs
Dimensional verification: Warp and twist	1 PCB from the batch that is worst-case
High resistance electrical test and continuity test	all PCBs and coupons

8.2 Outgoing inspection on coupons

8.2.1 Overview

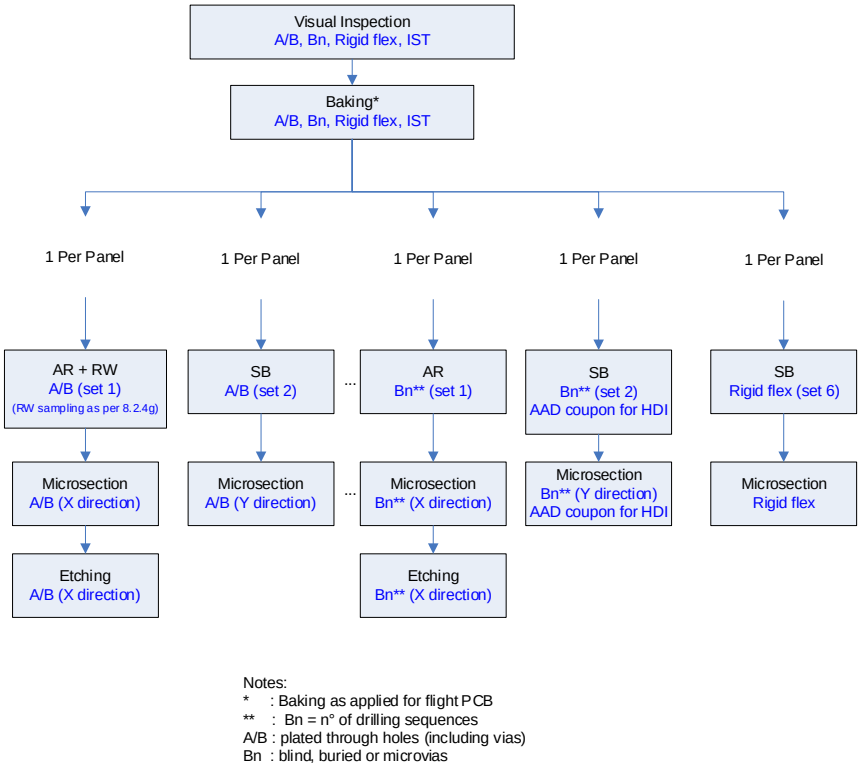
This clause describes the test flow, coupon configuration and inspection methods on coupons and PCBs for procurement. Table 8-2 and Figure 8-1 shows an overview of coupons and tests specified in this clause. This table shows when evaluations are performed.

ECSS-Q-ST-70-60_1390221

Table 8-2: Overview of coupons

Set ID	Location	Feature and name of coupon as per IPC-2221C	Test	Condition for presence of coupon	Condition for evaluation of coupon	Coupon delivered to customer	Microsection delivered to customer
set 1	one corner X-direction	PTH and via on A/B	AR + RW	yes	yes, per panel sampling for RW as per 8.2.4q	no	yes
		sequential via on Bn	AR	yes	yes, per panel	no	yes
		PTH and via on A/B	customer coupon	yes	yes, per panel	yes	no
		sequential via on Bn	customer coupon	yes	yes, per panel	yes	no
		tracks on A/B	min track width and spacing	yes	optional	yes	optional
set 2	opposite corner Y-direction	PTH and via on A/B	SB	yes	yes, per panel	no	yes
		sequential via on Bn	SB	yes	yes, per panel	no	yes
		PTH and via on A/B	customer coupon	yes	yes, per panel	yes	no
		sequential via on Bn	customer coupon	yes	yes, per panel	yes	no
		tracks on A/B	min track width and spacing	yes	optional	yes	optional
set 3	anywhere	PTH on A/B	solderability	yes	yes for SnPb < 1 µm, per panel	yes	n.a.
set 4	4 corners	electrical registration on R	electrical registration	yes for annular ring < 50 µm	yes, per panel	yes	n.a.
set 5	as per 9.5.5.3d, e and f	IST coupon	IST test	yes for applicable technology	yes, per panel	yes	optional

Set ID	Location	Feature and name of coupon as per IPC-2221C	Test	Condition for presence of coupon	Condition for evaluation of coupon	Coupon delivered to customer	Microsection delivered to customer
set 6 (mechanical)	anywhere	peel strength on P	peel strength	yes	optional	yes	n.a.
		coating adhesion on P	tape test	yes	optional	yes	n.a.
		solder mask adhesion on G	tape test	yes for applicable technology	yes, per batch	optional	n.a.
		flex bend cycles on X	bend test	yes for applicable technology	optional	optional	optional
		rigid-flex interface on X	SB	yes for applicable technology	yes, per panel	no	yes
set 7 (electrical)	anywhere	insulation resistance on E	insulation resistance	yes	optional	yes	n.a.
		DWV on E	DWV	yes	optional	yes	n.a.
		controlled impedance on Z	controlled impedance	yes for applicable technology	optional	optional	n.a.
		embedded film resistance	resistance	yes for applicable technology	optional	optional	optional
set 8	anywhere	pure laminate	thermal analysis	yes	optional	yes	n.a.
set 9	anywhere	"AAD-coupon"	SB	yes for HDI	yes for HDI, per panel can replace Bn coupon set 2	no	yes



ECSS-Q-ST-70-60_1390222

Figure 8-1: Flow for preparation, test and microscopic inspection of standard coupons for microsectioning

8.2.2 Configuration of coupons for plated holes

ECSS-Q-ST-70-60_1390223

a. The preparation, test and microscopic inspection of coupons for microsectioning shall be in conformance with Figure 8-1.

ECSS-Q-ST-70-60_1390224

b. Coupons shall be designed in conformance with clause 15 of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390225

c. Each panel shall include the following coupons for plated holes:

1. Coupon A/B;
2. Coupon B1, B2… Bn.

NOTE These coupons can be designed in accordance with IPC-2221C. However, other custom designs are used that cover the same features.

ECSS-Q-ST-70-60_1390226

d. Coupon A/B shall include the following features:

1. PTH with maximum or most frequently used diameter;
2. through-going via with minimum diameter.

NOTE 1 For 8.2.2d.1 coupon A of IPC-2221C can be used, and for 8.2.2d.2 coupon B of IPC-2221C.

NOTE 2 Plated holes for mechanical purpose are not represented in coupons. Risks associated with mechanical drilling are mitigated by visual inspection, high resistance electrical testing and process audit. In case of specific criticality of mechanical holes, the PCB procurement authority can add a coupon for it in the PCB definition dossier.

ECSS-Q-ST-70-60_1390227

e. Coupon A/B shall include at least 4 holes per drilling sequence.

ECSS-Q-ST-70-60_1390228

f. Coupon Bn shall include at least 3 holes per drilling sequence.

NOTE See an example of 3 holes per drilling sequence for coupon Bn in Figure 8-2. The top layer is a different drill sequence than the bottom layer and therefore 3 holes are present in the coupon for both layers.

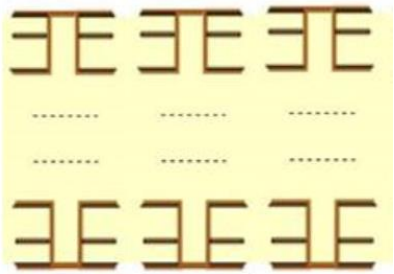


Figure 8-2: Example of Bn coupon with 3 holes per drilling sequence

ECSS-Q-ST-70-60_1390229

g. Coupon Bn shall include the following features:

1. blind via for each plating sequence with minimum diameter;
2. buried via for each plating sequence with minimum diameter;
3. microvia for each plating sequence with minimum diameter.

NOTE This is coupon B1, B2, etc. of IPC-2221C.

ECSS-Q-ST-70-60_1390230

h. The suffix of coupon B1, B2… Bn shall indicate the plating sequence of the vias that are included.

NOTE An example of vias manufactured at different plating sequences is shown in Figure 8-4.

ECSS-Q-ST-70-60_1390231

i. The term "coupon Bn" shall indicate all coupons B1, B2 … Bn for all plating sequences.

ECSS-Q-ST-70-60_1390232

j. Coupons for plated holes shall include rows and columns of holes to enable microsectioning of a coupon in both X-direction and Y-direction.

NOTE The IPC coupons are designed in a square.

ECSS-Q-ST-70-60_1390233

k. In case superpositioned blind vias are present in the PCB it shall be included in the design of the coupon Bn.

ECSS-Q-ST-70-60_1390234

l. At least two coupons for plated holes shall be placed on opposite corners of the panel to enable assessment of annular ring in both corners.

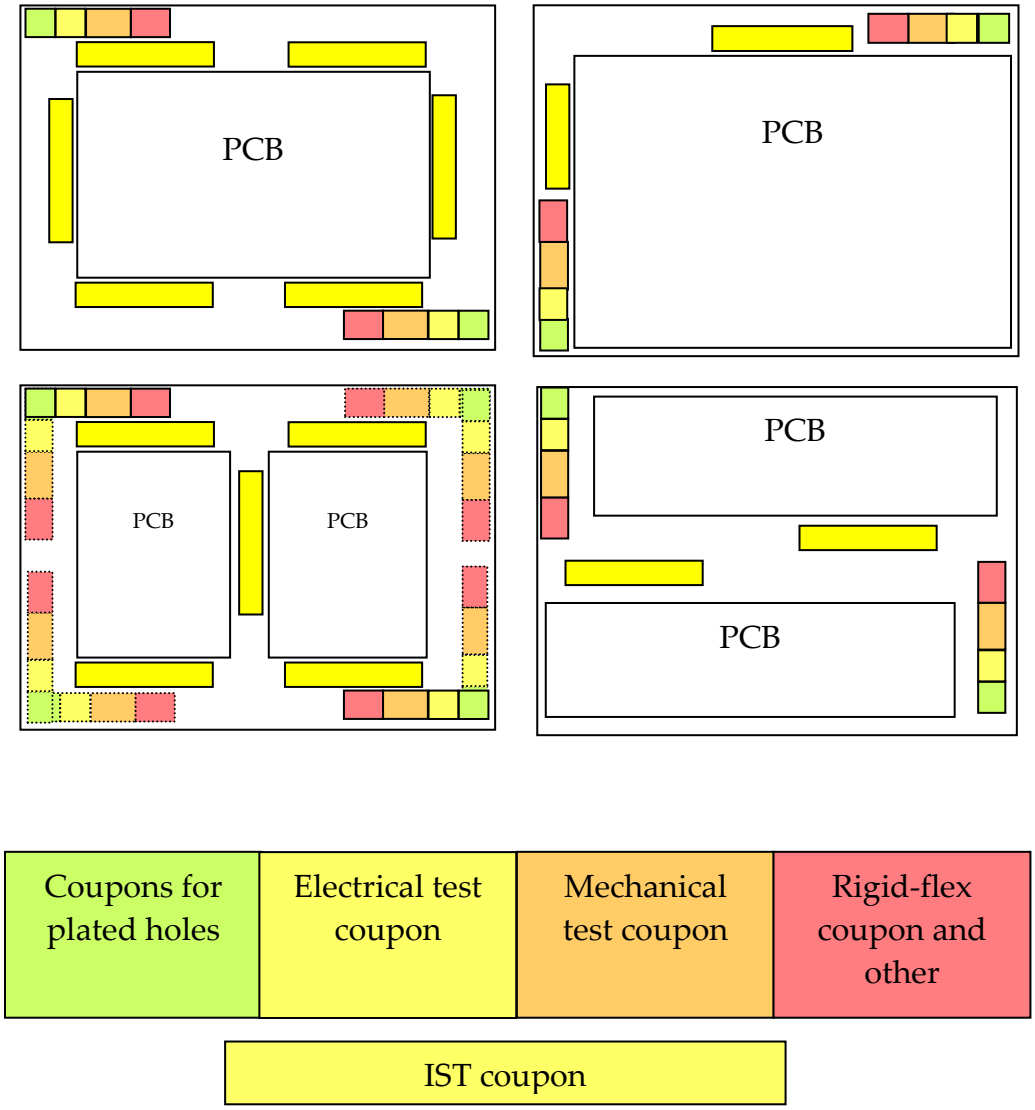


Figure 8-3: Example of placement of coupons and PCB in usable area of manufacturing panel

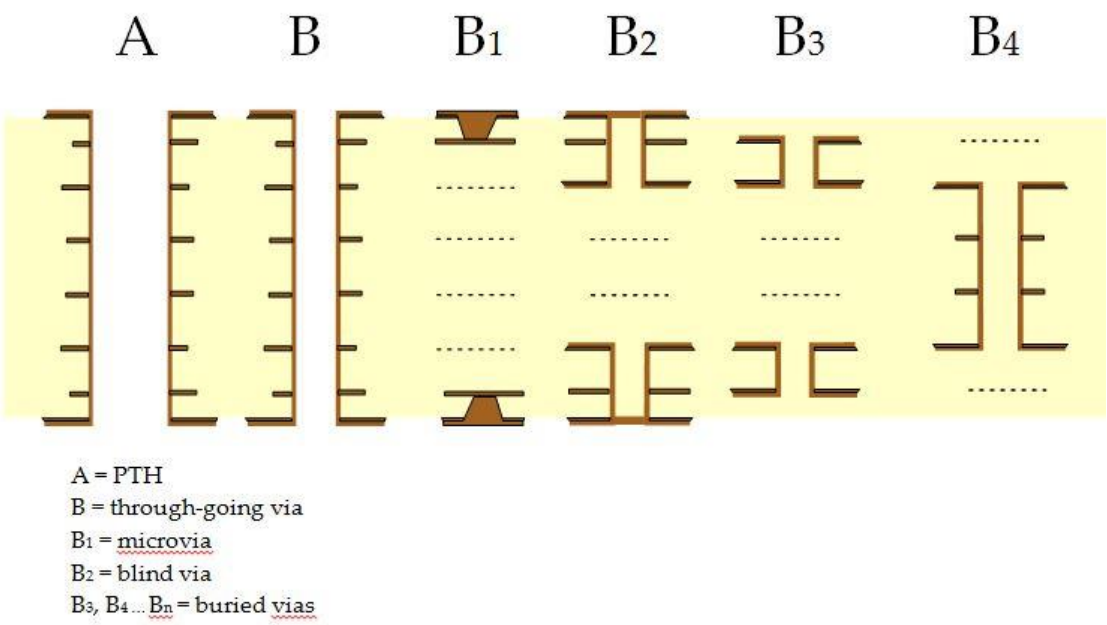


Figure 8-4: Example of vias manufactured at different plating and drilling sequences

8.2.3 Configuration of dedicated coupons

ECSS-Q-ST-70-60_1390235

a. In case the technology is within the technology perimeter for IST as specified in the clause 9.5.5.2, the IST coupon shall be designed and tested in accordance with clause 9.5.5.

ECSS-Q-ST-70-60_1390236

b. In case of a rigid-flex PCB, a coupon with rigid-to-flex interface shall be included on each panel.

NOTE It is good practice to include in this coupon the via nearest to the rigid-to-flex interface.

ECSS-Q-ST-70-60_1390237

c. For designs with reduced annular ring of 25 µm in conformance with requirement 7.5.3l of ECSS-Q-ST-70-12, electrical registration coupons shall be included on all four corners to verify the annular ring in the full circumference.

NOTE This is coupon R of IPC-2221C. Alternatively, a dedicated pattern can be available on IST coupons.

ECSS-Q-ST-70-60_1390238

d. A coupon shall be present for solderability testing.

NOTE 1 This can be achieved by repeating the A/B coupon of IPC-2221C.

NOTE 2 Performing solderability testing is specified in case SnPb < 1 µm in conformance with Table 10-12.

ECSS-Q-ST-70-60_1390769

e. In case more than one PCB is placed in the panel, a coupon for evaluation of plating should be placed in the middle of the panel.

NOTE A coupon for plating can be an IST coupon, A/B coupon or a spare PCB. An example of coupon placement in the centre of the panel is shown in Figure 8-3.

ECSS-Q-ST-70-60_1390239

f. If embedded film resistors are used, they shall be included in the coupons, in conformance with requirement 15.2d.13 of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390240

g. If controlled impedance is used, it shall be included in the coupons, in conformance with requirement 15.2g of ECSS-Q-ST-70-12.

NOTE Commonly used test probes need a coupon to verify controlled impedance. Some advanced test probes are available, however, that allow testing on the PCB.

ECSS-Q-ST-70-60_1390241

h. A coupon shall be present that include minimum track width and spacing on each layer, in conformance with requirement 15.2d.9 of ECSS-Q-ST-70-12.

NOTE It is good practice to include minimum track width and spacing in the A/B coupon for plated holes.

ECSS-Q-ST-70-60_1390242

i. A coupon shall be present that include patterns for mechanical tests in conformance with requirement 15.2f.2 of ECSS-Q-ST-70-12.

NOTE Mechanical tests include peel strength and coating adhesion. Flex bend cycles can be performed on the coupon with rigid-to-flex interface of requirement 8.2.3b.

ECSS-Q-ST-70-60_1390243

j. A coupon shall be present that includes patterns for electrical tests in conformance with requirement 15.2f.3 of ECSS-Q-ST-70-12.

NOTE Electrical tests include insulation resistance, dielectric withstanding voltage. Specific electrical test conditions can be specified by the procurement authority in conformance with requirement 9.6.3d.

ECSS-Q-ST-70-60_1390244

k. A coupon shall be present to perform thermal analysis.

NOTE 1 The coupon can be an area of approximately 1x1 cm without copper and without vias.

NOTE 2 Thermal analyses are used to investigate stability of materials, processes and design. Strict acceptance criteria can be unavailable in which case the test is evaluated against the heritage and datasheets or used for failure investigation.

ECSS-Q-ST-70-60_1390873

l. For HDI technology, an AAD-coupon shall be present.

NOTE The AAD-coupon copies the footprint of the AAD from the PCB. Its dimensions can be limited to implement it side by side with other coupons to ensure no extra space on the panel is lost. This is indicated as set 9 in Table 8-2.

ECSS-Q-ST-70-60_1390874

m. For procurement of PCBs with solder mask, a coupon shall be present to enable evaluation of solder mask adhesion on fine pitch footprint.

NOTE It is good practice to use IPC coupon type 'G', or a spare PCB.

8.2.4 Evaluation of coupons

ECSS-Q-ST-70-60_1390245

a. All coupons shall be evaluated by visual inspection, in accordance with requirements from clause 9.3.1 and 9.3.2.

ECSS-Q-ST-70-60_1390246

b. Evaluation of acceptance criteria for visual inspection and microsectioning shall be performed in accordance with requirements from clause 10.

ECSS-Q-ST-70-60_1390770

c. The coupons specified in requirements 8.2.3d, 8.2.3h, 8.2.3i, 8.2.3j and 8.2.3k may remain untested for procurement.

ECSS-Q-ST-70-60_1390247

d. Coupons for plated holes shall be submitted to microscopic inspection in the following conditions:

1. each hole type: as received;
2. each hole type: solder bath float in accordance with clause 9.5.2;
3. at least one PTH: rework simulation in accordance with clause 9.5.4, with the possible sampling specified in requirement 8.2.4q.

NOTE The holes adjacent to the one submitted to RW are considered to be in as-received condition. This allows assessment of both conditions in a single microsection.

ECSS-Q-ST-70-60_1390248

e. Microsectioning on coupon A/B shall be performed on at least 4 holes per drilling sequence and on coupon Bn on at least 3 holes per drilling sequence.

NOTE See Figure 8-2 for an example of drilling sequence of holes.

ECSS-Q-ST-70-60_1390249

f. The microsectioning of coupons for plated holes of each hole type shall be performed in both X-direction and Y-direction for assessment of annular ring in both directions.

NOTE To reduce the number of coupons and microsections, it is common practice to microsection the thermally stressed coupon in perpendicular direction to the as received coupon.

ECSS-Q-ST-70-60_1390250

g. The microsections of the as-received coupons for plated holes shall be submitted to microscopic inspection in as-polished and micro-etched conditions.

ECSS-Q-ST-70-60_1390251

h. The microsection of the thermally stressed coupons for plated holes shall be submitted to microscopic inspection in as-polished condition.

NOTE This is specified because micro-etch reveals the interface between plated copper layers. Therefore this is less efficient to evaluate any plating separation.

ECSS-Q-ST-70-60_1390252

i. Solderability test on PTH shall be performed for procurement, except in case of requirement 8.2.4j.

ECSS-Q-ST-70-60_1390771

j. Solderability test need not to be performed for procurement in case all the following conditions are met:

1. The surface finish is hot oil reflowed SnPb;
2. The thickness of the SnPb as specified on the CoC of the panel is in conformance with the requirements of Table 10-12;
3. The PID does not specify that solderability testing is mandatory for procurement.

NOTE In case the thickness of SnPb is not in conformance with the requirements of Table 10-12 as determined during qualification (renewal), the PID can specify that solderability test is performed for all procurement. This is usually the case upon request by the qualification authority.

ECSS-Q-ST-70-60_1390253

k. The microsection of the coupon with the rigid-to-flex interface shall be submitted to microscopic inspection after solder bath float, in as-polished condition.

ECSS-Q-ST-70-60_1390772

l. The preparation of the microsection of the coupon with the rigid-to-flex interface should be done using UV-fluorescent resin and vacuum potting and inspected using polarised light.

NOTE This is mandatory for qualification as specified in requirement 7.4d.

ECSS-Q-ST-70-60_1390875

m. The evaluation of the AAD-coupon shall be performed after SB and include all via types present in the coupon and all sequences on both sides.

NOTE All via types in the AAD-coupon include core vias and all microvias. All sequences on both sides in the AAD-coupon include all levels of microvias. This can be evaluated by the PCB manufacturer in outgoing inspection by progressive polishing through a coupon, or by combining the coupons from different panels. The microsection of the AAD-coupon is delivered to the procurement authority. In case the procurement authority wishes to reinspect all via types in this coupon as incoming inspection, this is possible by progressive polishing through the remainder of the coupon.

ECSS-Q-ST-70-60_1390876

n. The evaluation and presence of the AAD-coupon may replace the evaluation and presence of Bn-coupons as specified in the requirement 8.2.4e in case the conditions of the requirement 8.2.2g are fulfilled.

NOTE It is common practice that 4 microsections on 4 Bn-coupons are available for evaluation of 4 sequential via types. In case of using the AAD-coupon this can be combined in this one coupon.

ECSS-Q-ST-70-60_1390877

o. For procurement of PCBs with solder mask, a tape test shall be performed in as-received conditions once per batch on an area that is representative of the fine pitch of the solder mask design in conformance with 8.2.3m.

ECSS-Q-ST-70-60_1390878

p. In case the PCB definition dossier specifies a maximum thickness of solder mask on conductor, it shall meet the following conditions:

1. it is a review item for the MRR,
2. maximum solder mask thickness is evaluated on microsectioned coupons.

ECSS-Q-ST-70-60_1390879

q. Sampling for rework simulation may be performed to cover ≥25% of the panels in a batch.

NOTE 1 For instance, a batch of 9 would need to be screened by 3 panels to meet the ≥25% criterion.

NOTE 2 This sampling is justified by the experience that rework on PTH does not usually introduce nonconformances that are not screened by other methods, such as solder bath float test or as-received condition. Moreover, the effort involved with rework simulation is deemed relatively high.

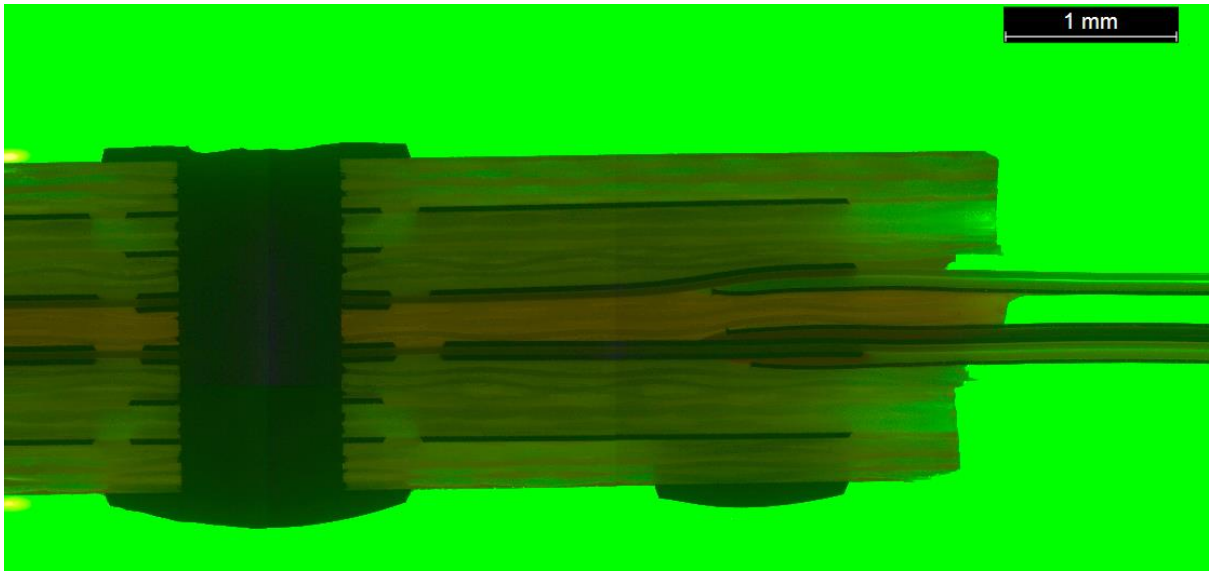


Figure 8-5: Example of target quality of microsection of rigid-flex interface with UV fluorescent resin and polarised light

8.2.5 Delivery of coupons, microsections and spare coupons

ECSS-Q-ST-70-60_1390254

a. Coupons shall be delivered to the procurement authority in conformance with the Table 8-2.

ECSS-Q-ST-70-60_1390773

b. The IST coupon may be send later than the other coupons, due to its logistics of test and shipment.

ECSS-Q-ST-70-60_1390255

c. The following microsections shall be delivered to the procurement authority:

1. Microsections of coupons for plated holes;
2. Microsections of coupon for rigid-to-flex interface.

NOTE This is summarised in Table 8-2.

8.3 Reporting of outgoing inspection and delivery

ECSS-Q-ST-70-60_1390256

a. The PCB manufacturer shall report the results of the outgoing inspection on PCB and coupons in the lab reports of the CoC, in conformance with the DRD of Annex B.

NOTE 100 % visual inspection of PCBs is specified in requirement 8.1a.1, whereas the lab report specifies the requirements for the documentation of the visual inspection.

ECSS-Q-ST-70-60_1390257

b. The CoC and its lab reports shall be delivered to the procurement authority.

ECSS-Q-ST-70-60_1390258

c. The PCB manufacturer shall not deliver a PCB with nonconformances to ECSS-Q-ST-70-60.

ECSS-Q-ST-70-60_1390259

d. The PCB manufacturer shall not deliver without approval from the procurement authority a PCB with nonconformances to the PCB definition dossier.

NOTE This includes definition of holes, milling, non-plated holes, dimensional and mechanical requirements, among other things as described in the DRD of Annex A of ECSS-Q-ST-70-12.

8.4 Incoming inspection by procurement authority

ECSS-Q-ST-70-60_1390260

a. The procurement authority shall perform incoming inspection as follows:

1. Visual inspection on all PCBs, in conformance with the clause 9.3,
2. Microscopic inspection on microsections, in conformance with the clause 10, by one of the following institutes:
   (a) procurement authority;
   (b) external third-party lab;
   (c) assembly house;
   (d) PCB manufacturer using another inspector than the one for outgoing inspection.
3. Verification of the CoC and its lab reports, in conformance with the Annex B,
4. Verification of quantity,
5. Verification of integrity of packaging.

NOTE 1 The PCB manufacturer provides microsections used for the CoC and customer coupons. Both

can be used for the incoming inspection. To avoid deterioration of the surface quality of microsections, it is preferred to perform incoming inspection as soon as possible after delivery.

NOTE 2 Microsection inspection for qualitative aspects is important and detection can be operator dependent. Therefore this requirement specifies to perform an additional verification.

ECSS-Q-ST-70-60_1390774

b. The procurement authority need not to perform microscopic inspection of the microsection of the reworked hole in as-polished condition.

NOTE This is specified because the microsection with the reworked hole includes other holes as-received. These as-received holes are inspected as-polished and after micro-etching. The procurement authority can only inspect in as-polished condition by repolishing the etched section.

ECSS-Q-ST-70-60_1390261

c. The procurement authority shall maintain records of the accepted incoming inspection.

NOTE Records of incoming inspection are made available during equipment MRR as specified in 6.14t.

ECSS-Q-ST-70-60_1390262

d. In case of nonconformances during incoming inspection an NCR shall be issued by the procurement authority to the PCB manufacturer.

ECSS-Q-ST-70-60_1390775

e. The procurement authority may perform incoming inspection at their own premises or at the premises of the PCB manufacturer.

NOTE If performed at the premises of the PCB manufacturer, the inspection is typically named: FCSI or MIP or DRB or buy-off.

ECSS-Q-ST-70-60_1390263

f. The procurement authority shall complete the incoming inspection within 3 months after availability of the PCBs.

8.5 FAI on PCB by microsectioning

ECSS-Q-ST-70-60_1390264

a. When specified, FAI on PCB shall include the microsectioning of a representative PCB from the batch for the first procurement.

NOTE 1 FAI is performed in supplement of the standard outgoing and incoming inspection on PCBs and coupons.

NOTE 2 The requirement 8.5a specifies that FAI is performed on the first procured batch only. Subsequent batches are not subject of FAI in case they meet the definition of "recurrent" as specified in 4.1 of ECSS-Q-ST-70-12. The requirement 8.5e specifies that FAI is performed in case of a new PCB manufacturer, even if the design is recurrent.

ECSS-Q-ST-70-60_1390265

b. FAI on PCB shall be performed in case this is specified by the procurement authority.

ECSS-Q-ST-70-60_1390266

c. FAI on PCB shall be performed in case reliable insulation applies, in conformance with the requirement 13.9.2d of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390776

d. FAI on PCB should be performed in case the PCB design is complex and the coupon cannot be designed with full representativity, in conformance with the requirement 15.2b of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390777

e. FAI on PCB should be performed on a representative PCB from the batch for the first procurement, if a technology is procured from a PCB manufacturer for the first time.

ECSS-Q-ST-70-60_1390267

f. During FAI on PCB, the microsectioning shall verify the technology features that are procured for the first time.

ECSS-Q-ST-70-60_1390268

g. In case of FAI on PCB, it shall be performed and documented by the procurement authority within 4 months after availability of the PCBs, by using one of the institutes specified in requirement 8.4a.2.

ECSS-Q-ST-70-60_1390269

h. The documentation of FAI on PCB shall be provided by the procurement authority to the PCB manufacturer.

NOTE 1 It is important for the PCB manufacturer to have the feedback from the FAI.

NOTE 2 FAI is reviewed during MPCB as specified in requirement 6.14r.

i. For HDI technology, “DPA on PCB” shall be performed and meet the following conditions:

1. One PCB per manufacturing batch is subject to evaluation;
2. Microsectioning is performed on a minimum of 3 locations;
3. Evaluation includes all dimensional and qualitative aspects for PTH, core via and microvias at both sides of the board as well as all the dielectric and copper thicknesses in the build-up;
4. The evaluation includes all via types in high-density areas (e.g. the AAD fan-out) as well as isolated features relevant to the inspection;
5. The samples are in as-received condition.

NOTE 1 It is good practice to use a PCB that is rejected at outgoing inspection, as it went through the same processes as the rest of the manufacturing batch.

NOTE 2 DPA on PCB is done on each manufacturing batch. This is different to FAI that is performed only for first procurement.

9
Test descriptions

9.1 Overview

This clause describes the test methods for the groups 1 to 6. An overview of this is shown in Figure 7-1.

Some test methods can include acceptance criteria. Test methods that include visual inspection of PCBs and coupons, and microscopic inspection of microsections have acceptance criteria specified in clause 10.

Examples of test patterns and coupons are included in each test method. Reference is made to test patterns from IPC-2221C. In future it is expected that other IPC standards also include test patterns.

9.2 Additional tests

9.2.1 Cleanliness

ECSS-Q-ST-70-60_1390270

a. The cleanliness of the samples prior to test and inspection shall be in conformance with 6.11a.

NOTE In case samples need to be cleaned, cleaning methods are specified in clauses 6.4, 7.5.3 and 11.1 of ECSS-Q-ST-70-61.

9.2.2 Bake-out

ECSS-Q-ST-70-60_1390271

a. Standard bake-out shall be minimum 8 hours at 120 ˚C in ambient pressure.

NOTE 1 Baking is performed to remove humidity from the dielectric materials prior to thermal excursions. PCB laminates are known to be hygroscopic.

NOTE 2 For sensitive PCB technology such as rigid-flex, this bake-out can cause damage when the heating rate is high. In this case a tailoring of the bake-out profile is good practice as per requirement 9.2.2b.

NOTE 3 Bake-out can be tailored based on results obtained from assembly verification and heritage, provided that storage conditions are dry, and depending on the sensitivity of the PCB technology (surface finish, dielectric material, thickness, copper planes).

ECSS-Q-ST-70-60_1390778

b. In case the PCB technology or the test criteria are affected by humidity, the bake-out may be tailored to improve its efficiency.

NOTE Improving efficiency of the bake-out can be established by a longer duration, vacuum or dry environment or a stepped baking profile. This can be necessary for thick PCBs, a high number of copper plane layers, flex laminate layers or samples stored in non-controlled environment. Tests that can be significantly affected by humidity include thermal excursions and high resistance electrical test. Baking in vacuum or dry nitrogen purge is good practice as this reduces oxidation of surface finish, as well as it improves dehumidification.

ECSS-Q-ST-70-60_1390779

c. The PCB manufacturer may tailor the bake-out in case samples are processed immediately after reflow as a final process step.

ECSS-Q-ST-70-60_1390272

d. After bake-out, re-absorption of humidity shall be prevented until thermal stress testing.

NOTE Precautions can include short duration (for example less than 8 hours) of storage between bake-out and thermal stress test or storage in dry conditions.

9.2.3 Plated copper tensile strength and elongation

ECSS-Q-ST-70-60_1390273

a. Plated copper tensile strength and elongation shall be performed in conformance with test method 2.4.18.1a from IPC-TM-650 or an equivalent test method.

ECSS-Q-ST-70-60_1390274

b. Plated copper tensile strength shall be ≥ 276 MPa.

ECSS-Q-ST-70-60_1390275

c. Plated copper elongation shall be ≥ 18 %.

9.2.4 Steam ageing

ECSS-Q-ST-70-60_1390276

a. When performed, the steam aeging test shall be carried out in conformance with test 20a of IEC 60326-2-am 1 (1992-06).

NOTE This test method was specified in ECSS-Q-ST-70-10 and is included here for completeness. However, it is not included in any of the test groups. The test is intended to give an indication of the effects of storage on the solderability of the PCBs. Steam ageing is also described in paragraphs 3.4.3 and 3.4.4. of IPC-J-STD-003C.

ECSS-Q-ST-70-60_1390277

b. The specimen shall be exposed in the steam generator machine for approximately 80 minutes.

ECSS-Q-ST-70-60_1390278

c. After closing the generator, it shall be purged with nitrogen at a flow rate between 250 ml/minute and 750 ml/minute.

ECSS-Q-ST-70-60_1390279

d. The temperature inside machine shall be (100 ± 2) °C and stabilized for (5 ± 1) minutes.

ECSS-Q-ST-70-60_1390280

e. The nitrogen flow shall be switched off.

ECSS-Q-ST-70-60_1390281

f. The 90 °C condensed steam rate in the chamber shall be controlled to (5 ± 0,5) l/minute.

ECSS-Q-ST-70-60_1390282

g. A mixture of pure oxygen 20 % and nitrogen 80 % with a flow rate of (100 ± 10) ml/minute shall be switched on for (60 ± 5) minutes.

ECSS-Q-ST-70-60_1390283

h. After removing the specimens from the steam generator machine, they shall be dried.

9.3 Group 1 – Visual inspection and non-destructive tests

9.3.1 Visual inspection - general

ECSS-Q-ST-70-60_1390284

a. Visual inspection shall be performed using 10x to 40x magnification.

NOTE Examples of equipment used for visual inspection are: binoculars, loups, single scope.

ECSS-Q-ST-70-60_1390285

b. Visual inspection shall cover the entire surface of both sides of the sample.

ECSS-Q-ST-70-60_1390286

c. Visual inspection shall be performed using high illuminating light sources.

NOTE ECSS-Q-ST-70-61 clause 5.3a requires 1080 lux. However, higher intensities are typically used for bare board inspection.

ECSS-Q-ST-70-60_1390287

d. In case of any suspected nonconformance, the area shall be re-examined at higher magnification of 20x to 40x.

9.3.2 Visual inspection for qualitative aspects

ECSS-Q-ST-70-60_1390288

a. Visual inspection for qualitative aspects shall be performed on PCB and coupons for conformance with acceptance criteria from clauses 10.4 and 10.5.

9.3.3 Visual inspection for dimensional verification

9.3.3.1 General

ECSS-Q-ST-70-60_1390289

a. Physical dimensions shall be measured for verification of the PCB definition dossier.

NOTE 1 In addition to the specified measurement, the physical dimensions are also submitted to visual inspection in conformance with clause 9.3.2.

NOTE 2 The mechanical drawing is typically used to specify physical dimensions and tolerances of the PCB.

ECSS-Q-ST-70-60_1390290

b. PCB thickness shall be measured over base laminate on corners and on the middle of the PCB, unless another methodology is specified in the PCB definition dossier.

ECSS-Q-ST-70-60_1390291

c. Length and width of the PCB shall be measured over all edges of the inspected PCB.

ECSS-Q-ST-70-60_1390292

d. The diameter of plated and non-plated holes shall be verified for all hole diameters.

ECSS-Q-ST-70-60_1390293

e. The number of hole diameters for verification on the inspected PCB shall be specified by the PCB manufacturer.

NOTE Hole diameters can be measured with measuring gauges, a measuring microscope or dedicated automatic systems.

ECSS-Q-ST-70-60_1390780

f. Vias of < 0,6 mm may be omitted during dimensional verification of its diameter, unless dimensional verification of these holes is specified in the PCB definition dossier.

NOTE This is because these holes can be blocked with SnPb in conformance with requirement 10.6.3g.

ECSS-Q-ST-70-60_1390294

g. Minimum conductor width and spacing shall be measured on external layers.

NOTE 1 Conductors include tracks and SMT pads.

NOTE 2 Conductor width and spacing on internal layers are present on the coupon in conformance with 8.2.3h for optional evaluation by microsectioning. Minimum track width and spacing on internal layers are evaluated by in-process inspection in conformance with 6.3f.3.

ECSS-Q-ST-70-60_1390295

h. Minimum conductor width and spacing shall be measured at the foot of the conductor, except for the case specified in requirements 9.3.3.1i and 9.3.3.1j.

NOTE An example of conductor width measured at the foot is shows as seen in a cross-section in Figure 9-1.

ECSS-Q-ST-70-60_1390296

i. In case overhang or undercut causes the top of the conductor to protrude from the foot, conductor width and spacing shall be measured at the widest point of the conductor.

ECSS-Q-ST-70-60_1390781

j. In case of RF PCBs the conductor width may be measured in conformance with the PCB definition dossier.

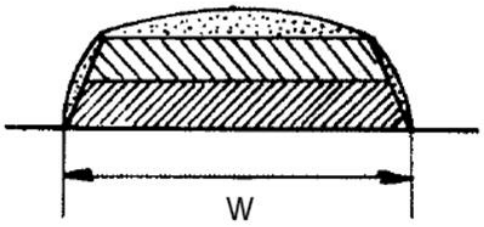


Figure 9-1: Conductor width (w) measured at the foot as seen in a cross-section.

9.3.3.2 Warp

ECSS-Q-ST-70-60_1390297

a. Warp shall be measured in conformance with the test method 2.4.22c from IPC-TM-650.

NOTE "Bow" is a term that is synonymous to "warp".

ECSS-Q-ST-70-60_1390298

b. The PCBs shall be placed unrestrained on a horizontal surface with the convex side upward.

ECSS-Q-ST-70-60_1390299

c. The two corners of the measured edge shall be in contact with the horizontal surface.

ECSS-Q-ST-70-60_1390300

d. The maximum distance between the horizontal surface and the PCB shall be measured as specified in Figure 9-2.

ECSS-Q-ST-70-60_1390301

e. The length of the PCB shall be measured.

ECSS-Q-ST-70-60_1390302

f. The warp shall be expressed in percentage terms.

ECSS-Q-ST-70-60_1390303

g. Warp shall be calculated as follows:

1. Warp [%] = max distance [mm] / length of PCB [mm] x 100

ECSS-Q-ST-70-60_1390304

h. The maximum warp shall be ≤ 1,5 %.

ECSS-Q-ST-70-60_1390782

i. The procurement authority may specify a more stringent requirement for warp in the PCB definition dossier.

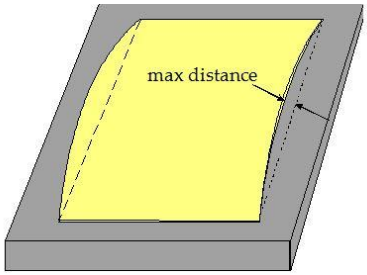
NOTE 1 A typical stringent warp and twist requirement is ≤ 0,75 %, which is in conformance with IPC-6012FS reference 3.4.3.

NOTE 2 This can be done for complex assembly, such as large components without stress relief, where

less warp and twist can avoid stress on component assembly.

NOTE 3 Warp and twist are strongly affected by the symmetry of the build-up. In case the PCB is designed with asymmetric build-up in conformance with requirements 7.1.1a, 7.1.1b, 7.1.2a and 7.1.2d from ECSS-Q-ST-70-12, the procurement authority and PCB manufacturer mutually define the value of max warp in the MRR and in the PCB definition dossier. This agreed value cannot exceed 1,5 % in conformance with requirement 9.3.3.2h.

NOTE 4 On PTFE-based laminates it is not applicable to measure warp and twist because of the material softness.



ECSS-Q-ST-70-60_1390305

Figure 9-2: Warp

9.3.3.3 Twist

ECSS-Q-ST-70-60_1390306

a. Twist shall be measured in conformance with the test method 2.4.22c from IPC-TM-650.

ECSS-Q-ST-70-60_1390307

b. The PCB shall be placed on a horizontal surface so that it rests on three corners.

ECSS-Q-ST-70-60_1390308

c. In case three corners cannot rest on the horizontal surface by restraining only one corner, the referee test shall be performed in conformance with chapter 5.3 of the test method 2.4.22c from IPC-TM-650.

ECSS-Q-ST-70-60_1390309

d. The distance between the horizontal surface and the fourth corner of the PCB shall be measured as specified in Figure 9-3.

ECSS-Q-ST-70-60_1390310

e. The length of the diagonal of the PCB shall be measured.

ECSS-Q-ST-70-60_1390311

f. The twist shall be expressed in percentage terms.

ECSS-Q-ST-70-60_1390312

g. Twist shall be calculated as follows:

1. Twist [%] = max distance [mm] / (2 x length of PCB diagonal [mm]) x 100

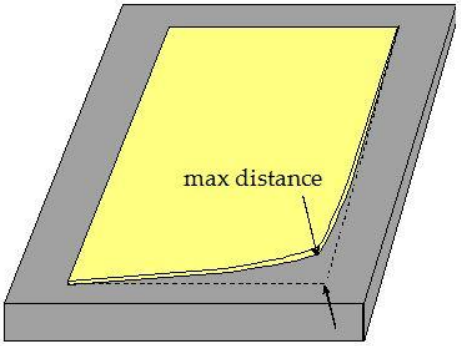
ECSS-Q-ST-70-60_1390313

h. The maximum twist shall be ≤ 1,5 %.

ECSS-Q-ST-70-60_1390783

i. The procurement authority may specify a more stringent requirement for twist in the PCB definition dossier.

NOTE See the notes 1, 2, 3 and 4 from clause 9.3.3.2.



ECSS-Q-ST-70-60_1390314

Figure 9-3: Twist

9.3.4 Impedance test

ECSS-Q-ST-70-60_1390315

a. Impedance test for controlled impedance lines shall be performed using TDR in conformance with test method 2.5.5.7a of IPC-TM-650.

ECSS-Q-ST-70-60_1390316

b. The measurement method for impedance test shall be specified by the procurement authority in the PCB definition dossier.

NOTE This includes nominal impedance and tolerances, transmission line types and reporting. Typical acceptable tolerance can be 10%. DC resistance compensation can be used.

ECSS-Q-ST-70-60_1390784

c. Impedance test may be performed on specific coupons or on PCB.

NOTE Specific equipment and training is needed for impedance testing on PCB. It can be difficult to design an impedance coupon that is representative of the PCB. Therefore, this measurement is typically performed on the PCB.

9.3.5 Dielectric constant and loss tangent

ECSS-Q-ST-70-60_1390317

a. Dielectric constant and loss tangent at 1 MHz should be measured on specific coupons in conformance with test method 2.5.5.2a of IPC-TM-650.

ECSS-Q-ST-70-60_1390318

b. The measurement method for dielectric constant and loss tangent shall be specified by the procurement authority in the PCB definition dossier.

NOTE This includes tolerances and reporting.

ECSS-Q-ST-70-60_1390881

c. Dielectric constant and loss tangent at higher frequencies than specified in 9.3.5a, should be measured in conformance with the parallel plate test method 2.5.5.9 of IPC-TM-650 or the balanced-type circular disk resonance method of IEC 63185 (2020).

NOTE The parallel plate method is suitable for ≤ 1,5GHz. Above this frequency, the balanced-type circular disk resonance method is used.

9.3.6 Cleanliness

ECSS-Q-ST-70-60_1390319

a. Cleanliness testing of PCB shall be performed in conformance with clause 11.1.2 of ECSS-Q-ST-70-61 and test method 2.3.25.1 from IPC-TM-650.

ECSS-Q-ST-70-60_1390320

b. The cleanliness value shall be ≤ 1,56 µg NaCl eq /cm².

NOTE 1 This value is historically driven by the limit for an assembled PCB. However, the cleanliness of a bare PCB is typically orders of magnitude better. Nevertheless, a more stringent value is not specified. It is good practice to have a cleanliness value of ≤ 0,1 µg NaCl eq /cm².

NOTE 2 Guidelines for cleanliness of bare PCB and assembled PCB are given in IPC-5703 and IPC-5704.

9.3.7 High resistance electrical test

9.3.7.1 Overview

PCBs can fail due to latent short circuits. It is acknowledged that random contamination inside the dielectric PCB material is of concern, as discussed in clause 6.7. Contamination can comprise of fibres in laminate or on prepreg layers and can originate from the PCB manufacturing processes or from the base material supply chain. The presence of contamination can provide a pathway for leakage current and possible ECM.

Typical electrical testing applied on PCBs by a flying probe equipment, is specified in IPC-9252B and is based on an insulation threshold of 10 MΩ, corresponding to level C for IPC-6012F class 3. The objective of this test method is to verify electrical design, i.e. the absence of unintended connections in the circuit. For IPC-6012FS this test method is amended to 100 MΩ under 250 V bias.

The purpose of the high resistance electrical test method is to determine the quality of the insulation and possible imperfections in the dielectric material. The rationale is that contamination between nets can provide a high-Ohmic path that can be detected under high voltage bias and therefore fails this test. On PCBs that fail the high insulation requirement, it has been demonstrated by DPA that the high-Ohmic path was caused by contamination in the dielectric material.

Clause 9.6.3 requires insulation resistance of ≥1 GΩ (and orders of magnitude higher) for interlayer and intralayer on dedicated test patterns. The requirement for high insulation is further substantiated by the typical volume resistivity of dielectric materials in the order of 10^8 MΩ-cm, determined at humid conditions of 90% RH in accordance with test method 2.5.17.1 of IPC-TM-650.

It is not the purpose of the high resistance test method to stress the dielectric material by screening for the operational voltage with a specified margin. For operational voltages higher than the test voltage (of 250V), a specific test can be specified by the procurement authority in the PCB definition dossier, such as a dielectric withstanding voltage test. The high test voltage of 250 V is applied because it is necessary to generate a leakage current that can be detected by the test equipment and that corresponds to a high insulation threshold of 1 GΩ.

Application of the test voltage of 250V on the smallest as-manufactured insulation distance of 96 µm for standard technology and of 63 µm for Polyimide HDI technology, as per Table 13.7 of ECSS-Q-ST-70-12, results in a worst-case electrical field of 2,6 kV/mm and 4 kV/mm respectively. This is acceptable for the purpose of this high resistance test, because of the heritage with this test voltage on PCBs, the electrical strength specified in datasheets in the order of ≥30 kV/mm and the short duration of the sustain time.

Precautions, such as dehumidification of air, are needed to prevent discharge due to ionisation of air, which has a breakdown strength of 1,5 kV/mm – 3 kV/mm depending on humidity. This is important for surface conductors spaced approximately 170 µm or closer.

9.3.7.2 High resistance electrical test method

ECSS-Q-ST-70-60_1390321

a. High resistance electrical test shall be performed on final PCBs using flying probe equipment.

ECSS-Q-ST-70-60_1390322

b. The test voltage shall be ≥ 250 V.

ECSS-Q-ST-70-60_1390323

c. The insulation threshold shall be ≥ 1 GΩ.

ECSS-Q-ST-70-60_1390324

d. The sustain time shall be ≥ 5 ms.

NOTE It is common that the sustain time is more than 5 ms to allow the voltage ramp up, especially in case large ground layers are present.

ECSS-Q-ST-70-60_1390325

e. During the ramp-up from 0 V to 250 V, the test voltage shall be monitored.

ECSS-Q-ST-70-60_1390326

f. Lack of voltage stability during the sustain time and during the ramp-up shall be recorded as test failure.

ECSS-Q-ST-70-60_1390327

g. The horizontal adjacency distance shall be ≥ 1,27 mm in-plane.

ECSS-Q-ST-70-60_1390328

h. The vertical adjacency distance shall be ≥ 1,27 mm in-plane on the layers above and below the specified net.

NOTE Horizontal and vertical adjacency is specified as a distance in-plane of the PCB to the tested net. This is illustrated in Figure 9-4.

ECSS-Q-ST-70-60_1390329

i. Direct resistive isolation testing shall be performed.

ECSS-Q-ST-70-60_1390330

j. Indirect isolation testing by signature comparison shall not be performed.

ECSS-Q-ST-70-60_1390785

k. The PCB should be dehumidified by baking prior to testing.

ECSS-Q-ST-70-60_1390786

l. In case the first test fails between 0,1-1,0 GΩ, one further bake and re-test may be performed.

ECSS-Q-ST-70-60_1390331

m. In case the test fails below 0,1 GΩ, re-test shall not be performed.

NOTE Failure above 0,1 GΩ can occur due to insufficient surface cleaning or insufficient dehumidification. High temperature during baking can affect the quality of the surface finish which is verified by the PCB manufacturer.

ECSS-Q-ST-70-60_1390787

n. In case the test fails because the set voltage is not achieved due to high capacitance caused by presence of plane layers, one further re-test may be performed with adjusted parameters.

NOTE Such adjustment can include longer sustain time or longer ramp-up time.

o. The PCB procurement authority shall specify in the PCB definition dossier in case the high resistance electrical test includes text and logo.

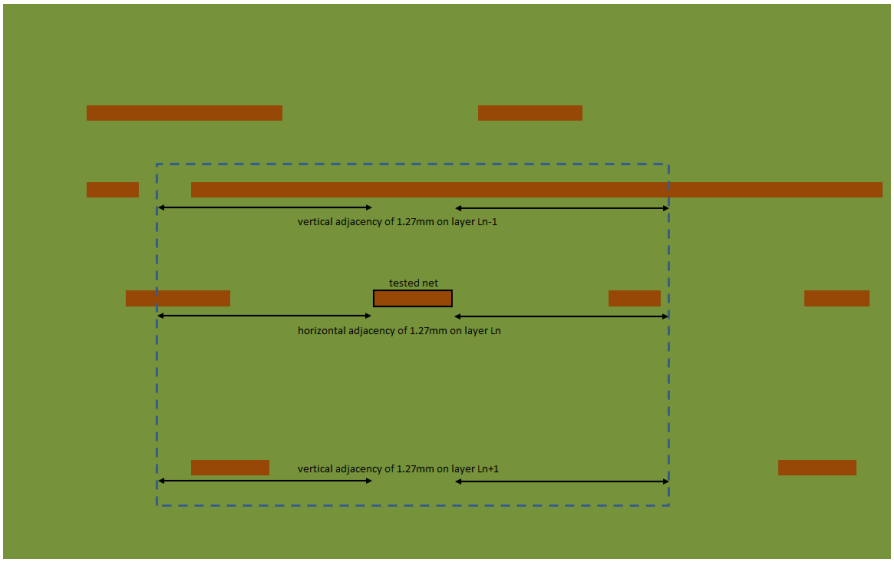


Figure 9-4: Horizontal adjacency on layer Ln and vertical adjacency on the layers above and below.

9.3.8 Continuity test

9.3.8.1 Overview

Continuity test aims at screening all nets of the PCB for unintentional open circuit. The test is based on IPC-9252A level C and it provides specific detail for test point assignment. The specified test point assignment does not include all pads on top and bottom layer of all plated holes. This is done to limit the test duration.

A midpoint is a node (e.g. SMT pads, component holes, or vias) that is positioned within the network in such a way that its removal has the effect of creating two or more separate networks from the original network. If a node is not a midpoint, it is classified as an endpoint. See Figure 9-5.

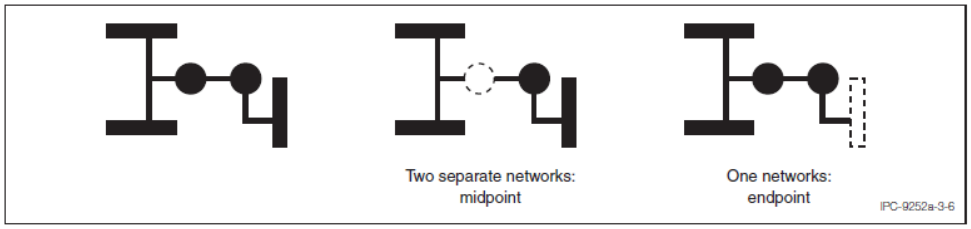


Figure 3-6 Test for Midpoint Classification

Figure 9-5: Midpoint classification

9.3.8.2 Continuity test method

ECSS-Q-ST-70-60_1390333

a. Resistive continuity testing shall be performed on final PCBs using flying probe equipment.

ECSS-Q-ST-70-60_1390334

b. The test voltage shall be maximum 10 VDC.

ECSS-Q-ST-70-60_1390335

c. The current shall be maximum 30 mA.

ECSS-Q-ST-70-60_1390336

d. The resistance threshold shall be maximum 10 Ω in conformance with IPC-9252A class C, except for nets that are designed with high resistance in PCB definition dossier.

NOTE Examples of nest designed with high resistance are planar transformers and coils.

ECSS-Q-ST-70-60_1390337

e. All end points of all nets shall be tested.

ECSS-Q-ST-70-60_1390338

f. The diameter of plated holes and the size of pads shall not be used as a criterion to exclude them from testing.

NOTE A pad can be an SMT pad, a circular or oblong pad of a plated hole.

ECSS-Q-ST-70-60_1390339

g. Test point assignment shall be set as follows:

1. On the top and bottom layer of a drilled pad that is not connected with any track.
2. On the top layer of a drilled pad that is not connected with any track on the top layer and connected with only one track on the bottom layer.
3. On the bottom layer of a drilled pad that is not connected with any track on the bottom layer and connected with only one track on the opposite layer.
4. On the top and bottom layer of a drilled pad that is not connected with any track on the top layer or the opposite layer, but is connected to one inner layer.
5. On the bottom layer of a drilled pad that is not connected with any track on the bottom layer and connected with more than one track on the opposite layer.
6. On the top layer of a drilled pad that is not connected with any track on the top layer and connected with more than one track on the opposite layer.

7. On the top and bottom layer of a drilled pad that is not connected with any track on the top layer or the opposite layer, but is connected to two or more inner layers.

NOTE These 7 conditions for test point assignment are illustrated in Figure 9-6.

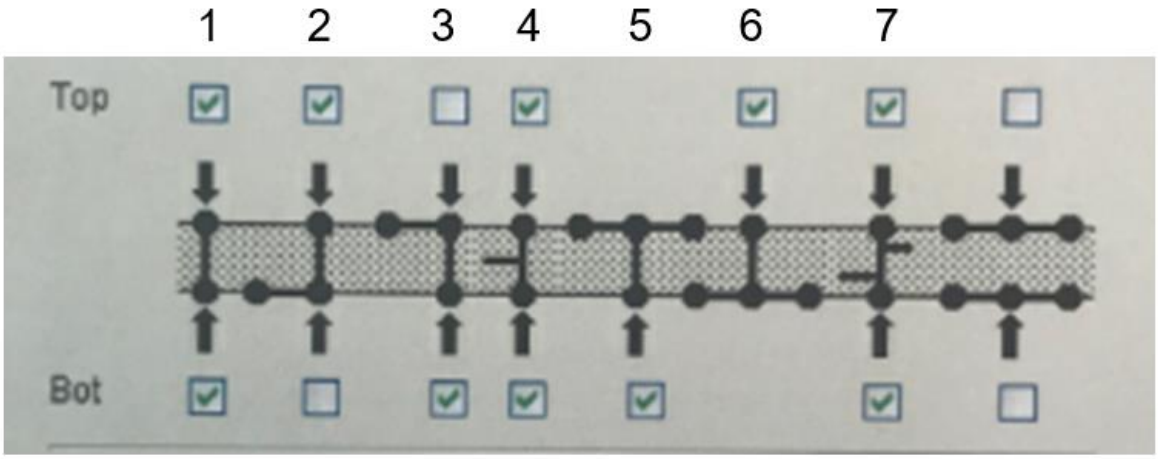


Figure 9-6: Setting of test point assignments. The numbers 1 to 7 correspond to the conditions of requirement 9.3.8.2g.

ECSS-Q-ST-70-60_1390340

h. During the data preparation, the PCB manufacturer shall verify that end points are included in the test in conformance with requirement 9.3.8.2g.

NOTE To fulfil this requirement 9.3.8.2h, it is good practice that the PCB manufacturer defines the PCB data as a “flash”, not as a “contour”, or as a “complex aperture”.

ECSS-Q-ST-70-60_1390788

i. The PCB procurement authority should include in its PCB definition dossier the data preparation for continuity test in conformance with requirements 9.3.8.2g and 9.3.8.2h.

ECSS-Q-ST-70-60_1390341

j. The PCB procurement authority shall specify in the PCB definition dossier in case the continuity test includes text and logo.

9.4 Group 2 - Miscellaneous tests

9.4.1 Overview

Long-time overload and short-time overload testing had been specified in ECSS-Q-ST-70-10 clauses 7.3.5.1.2 and 7.3.5.1.3. These tests assess the ability of copper tracks and vias to carry a specified current. This test is considered obsolete and covered by the following:

- copper foil and copper plating quality is monitored by specifying purity , elongation, layer thickness and its procurement specification,
- dielectric quality and thermal robustness is monitored by thermal stress tests and by specifying layer thickness and its procurement specification,
- current carrying capacity and self-heating of conductors is specified in PCB design in clause 13.6 of ECSS-Q-ST-70-12.

Internal short circuit testing has been specified in ECSS-Q-ST-70-10 clauses 7.3.5.2. This test assesses leakage current in dielectric insulation between different nets on specific test patterns on coupons. This test is considered obsolete and covered by the following:

- High resistance electrical testing on PCBs in conformance with clause 9.3.7.

Water absorption testing had been specified as an optional test in ECSS-Q-ST-70-10 clauses 7.3.6.1. This test assesses the weight percentage of water that can be absorbed by the dielectric materials. This test is considered obsolete and covered by the following:

- Water absorption is described in the specifications of raw materials, such as IPC-4101E for rigid laminates, IPC-4103B for RF laminates, IPC-4204B for flexible laminates, IPC-4203A for coverlay.
- A standard bake-out and prevention of re-absorption are specified for thermal stress tests and assembly.
- The effect of water absorption on ECM is assesses by THB and CAF testing in conformance with clause 9.7.

9.4.2 Peel strength

ECSS-Q-ST-70-60_1390342

a. The test shall be carried out in conformance with condition A of test method 2.4.8c from IPC-TM-650.

ECSS-Q-ST-70-60_1390343

b. The conductor selected shall be peeled back at one end for a length of approximately 10 mm.

ECSS-Q-ST-70-60_1390344

c. The detached end of the conductor shall be gripped over its whole width.

ECSS-Q-ST-70-60_1390345

d. Traction shall be applied in a direction perpendicular to the plane of the sample until the copper starts to peel away.

ECSS-Q-ST-70-60_1390346

e. The rate of traction shall be kept constant at 50 mm/minute.

ECSS-Q-ST-70-60_1390347

f. The traction direction shall be kept perpendicular to the plane of the sample.

NOTE This can be achieved by positioning the sample on a sliding platform.

ECSS-Q-ST-70-60_1390348

g. Machine inertia shall have no effect on the measurement.

ECSS-Q-ST-70-60_1390349

h. The conductor width shall be the measured width over which the conductor is adhered to the substrate.

NOTE Test coupon P from IPC-2221C is an example of a suitable test pattern.

ECSS-Q-ST-70-60_1390350

i. Peel strength of copper foil on laminate or prepreg shall be in conformance with the specification from the datasheet from the raw material manufacturer and from IPC-4101E.

ECSS-Q-ST-70-60_1390351

j. Peel strength shall be determined on representative build-up with either copper foil and prepreg or laminate as external layer.

ECSS-Q-ST-70-60_1390789

k. Peel strength of copper foil ≥ 17 µm should be as follows:

1. Epoxy: ≥ 12 N/cm;
2. Polyimide: ≥ 12 N/cm;
3. PTFE reinforced/ceramic filled or non-filled: ≥ 8 N/cm;
4. Cross-linked hydrocarbon: ≥ 8 N/cm;
5. Aramide/polyimide: ≥ 6 N/cm;
6. Flex laminate: ≥ 10 N/cm;
7. PPE for (H)VLP copper foil: ≥ 5,1 N/cm.

NOTE Peel strength below this requirement 9.4.2k is evaluated by thermal cycling in qualification.

ECSS-Q-ST-70-60_1390790

l. <<deleted>>

9.4.3 Flexural fatigue

ECSS-Q-ST-70-60_1390352

a. Flexural fatigue shall be determined only for flexible laminate.

NOTE The objective of the flexural fatigue test is to determine the ductility and adhesion of copper cladding, kapton laminate and coverlay.

ECSS-Q-ST-70-60_1390353

b. The flexible sample shall include etching of the pattern and coverlay bonding representative of the PCB.

ECSS-Q-ST-70-60_1390354

c. Flexural fatigue test shall be performed for a flexible PCB.

NOTE A flexible PCB can be manufactured using a double sided flex laminate or sculptured copper layer.

ECSS-Q-ST-70-60_1390355

d. Flexural fatigue test shall be performed for a rigid-flex PCB on the individual flexible laminate.

NOTE Flexural fatigue test assesses the bare laminate properties. The individual flexible laminate can be non-representative of a rigid-flex PCB in case multiple flexible layers are used or laminated together. In this case, the bending test assesses the representative construction.

ECSS-Q-ST-70-60_1390356

e. Flexural fatigue test shall cover only static applications.

NOTE Dynamic applications are project qualified in conformance with requirement 8.6.2b of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390357

f. The test shall be carried out in conformance with test method 2.4.3.1c of IPC-TM-650.

NOTE The equipment can be similar to the automated equipment described in IPC-TM-650 test method 2.4.3.1c. Alternatively the test can be performed using a manual equipment.

ECSS-Q-ST-70-60_1390358

g. The test shall be performed using the following parameters:

1. Number of cycles is 250;
2. One cycle includes bending the flex laminate upwards 90° and downwards 90°;

3. The diameter of the mandrel over which the flex laminate is bend is between 3 mm and 10 mm;
4. The rate does not exceed 20 cycles per minute.

NOTE For requirement 9.4.3g.3, IPC-TM-650 test method 2.4.3.1c recommends 6,35 mm for single sided flex laminate. ECSS-Q-ST-70-10 clause 7.3.3.3 specifies 9,6 mm. A typical test is performed using 3,2 mm.

ECSS-Q-ST-70-60_1390359

h. Before and after the test, the resistance shall be measured using 4-wire resistance measurement with the sample in flat condition, bend 90° upwards and bend 90° downwards.

ECSS-Q-ST-70-60_1390360

i. The flexural fatigue test shall be performed on two samples manufactured in zero and 90°, covering both orthogonal directions.

NOTE This is done to allow T-shaped and L-shaped flex sections. In addition, the raw material CoC can lack the traceability of the processing direction of the copper cladding. A typical flex laminate can use rolled and annealed copper in conformance with requirement 8.3.3d and 8.3.3.e of ECSS-Q-ST-70-12. In this case, the performance of flexural fatigue can be better in the rolled direction than in the other direction. This is caused by the long grain direction of the rolled copper.

ECSS-Q-ST-70-60_1390361

j. The test vehicle shall be microsectioned at the zone that was bend during the test.

ECSS-Q-ST-70-60_1390362

k. The acceptance criteria shall be as follows:
1. Resistance change is ≤ 10 %;
2. Visual and microscopic inspection is in conformance with clause 10.

NOTE 1 This is done to verify absence of adhesion defects between coverlay and copper, between coverlay and flex laminate and between copper and flex laminate in the bend flexible zone.

NOTE 2 Test coupon X from IPC-2221C is an example of a suitable test pattern.

9.4.4 Bending test

ECSS-Q-ST-70-60_1390363

a. Bending test shall be performed only for rigid-flex PCBs.

NOTE The objective of the bending test is to determine the adhesion of flex layers and the rigid-to-flex interface.

ECSS-Q-ST-70-60_1390364

b. Bending test shall cover only static applications.

NOTE Dynamic applications are project qualified in conformance with requirement 8.6.2b of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390365

c. The test shall be carried out in conformance with requirements 9.4.3f and 9.4.3g, 9.4.3h, except for the following:

1. Number of cycles is 25;
2. The radius of the mandrel over which the flexible section is bend equals 12x the total thickness of the flexible section.

NOTE The build-up of flex laminate with lowest thickness includes 25 µm flex laminate, with 35 µm copper cladding on both sides, with 25 µm coverlay on both sides, with approximately 10 µm to 20 µm adhesive between coverlay and flex laminate. This results in approximately 165 µm thickness. The minimum bend radius of 12x is in conformance with clause 8.6.2a of ECSS-Q-ST-70-12. The minimum mandrel radius therefore equals 1,98 mm, corresponding to a diameter of 3,96 mm.

ECSS-Q-ST-70-60_1390366

d. The test vehicle shall be the final rigid-flex PCB or a representative coupon.

NOTE This is representative of the number of flex laminates, the thickness of flex laminate, thickness of copper cladding, thickness of coverlay, thickness of bond-ply and penetration of coverlay and bond-ply into the rigid section.

ECSS-Q-ST-70-60_1390367

e. The test vehicle shall be microsectioned at the rigid-flex interface and at the zone that was bend during the test.

ECSS-Q-ST-70-60_1390368

f. The acceptance criteria shall be as follows:

1. Resistance change is ≤ 10 %.
2. Visual and microscopic inspection is in conformance with clause 10.

NOTE This is done to verify absence of adhesion defects between coverlay and copper, between coverlay and flex laminate, between copper and flex laminate and between prepreg and coverlay in the rigid-to-flex interface and in the bend flexible zone.

9.4.5 Coating adhesion – tape test

ECSS-Q-ST-70-60_1390369

a. The coating adhesion test shall be performed in conformance with test method 2.4.1e from IPC-TM-650.

NOTE Coating adhesion test is performed to determine adhesion of surface finish. Examples of surface finish that can be submitted to this test are SnPb, galvanic Au or Ni-Pd-Au.

ECSS-Q-ST-70-60_1390370

b. After cleaning, an adhesive tape, at least 50 mm long, shall be applied to the test surface and pressed down to eliminate all air bubbles.

ECSS-Q-ST-70-60_1390371

c. After 1 minute, the tape shall be quickly pulled off perpendicular to the coating surface.

ECSS-Q-ST-70-60_1390372

d. The surface area to be tested shall be at least 1 cm^2 of conductor.

ECSS-Q-ST-70-60_1390373

e. The tape shall have an adhesion of at least 4,4 N/cm.

NOTE Example of tape that can be used is 3M Brand 600 with a width of 13 mm.

ECSS-Q-ST-70-60_1390374

f. The surface finish shall not peel from the test surface or stick to the tape.

NOTE Coating adhesion test can be performed on coupon P from IPC-2221C.

ECSS-Q-ST-70-60_1390882

g. In case a tape test is performed on a PCB to be delivered, it shall be a review item during MRR.

NOTE Tape testing can leave some residue. This can be important for sensitive pads, such as for wire bonding.

9.4.6 Analysis of tin-lead coating

ECSS-Q-ST-70-60_1390791

a. The tin-lead alloy should be chemically dissolved.

ECSS-Q-ST-70-60_1390792

b. The relative quantities of tin and lead should be determined by atomic absorption spectrometry.

NOTE This is the preferred method for SnPb.

ECSS-Q-ST-70-60_1390793

c. Another method resulting in the same degree of precision may be used.

ECSS-Q-ST-70-60_1390375

d. The composition of tin-lead shall be: Sn = 63 % ± 8 %

NOTE 1 Lead-rich underplating of tin-lead finish can cause the content of tin in the final reflowed finish to be below the required 55 %.

NOTE 2 Analysis of SnPb coating can be measured coupon P from IPC-2221C.

9.4.7 Outgassing

ECSS-Q-ST-70-60_1390376

a. The outgassing test shall be performed in conformance with ECSS-Q-ST-70-02.

ECSS-Q-ST-70-60_1390377

b. The outgassing test shall be performed on a specimen without copper.

ECSS-Q-ST-70-60_1390378

c. The outgassing shall be determined by measurement of the difference in weight of the specimen before and after the test.

ECSS-Q-ST-70-60_1390379

d. The outgassing shall be:

1. RML ≤ 1 %;
2. CVCM < 0,1 %.

NOTE Clauses 5.1.a and 5.5.1.b from ECSS-Q-ST-70-02 specify that a standard outgassing test can be valid for continuous operation of general materials up to 50 °C. However, PCBs are qualified for a maximum operational temperature of 85 °C in conformance with requirement 5.1b of ECSS-Q-ST-70-60. Projects with critical applications can specify more stringent assessment on outgassing in conformance with ECSS-Q-ST-70-02, but this is not covered by generic qualification of PCBs in conformance with ECSS-Q-ST-70-60.

9.4.8 Thermal analysis

ECSS-Q-ST-70-60_1390794

a. Thermal analysis should be performed on a sample without copper.

ECSS-Q-ST-70-60_1390380

b. Temperature of decomposition, Td, shall be measured in conformance with test method 2.4.24.6 of IPC-TM-650 using TGA.

ECSS-Q-ST-70-60_1390381

c. Time to delamination at 288°C, T288, shall be measured in conformance with test method 2.4.24.1 of IPC-TM-650 using TMA.

ECSS-Q-ST-70-60_1390795

d. Tg should be measured in conformance with test method 2.4.25c of IPC-TM-650 using DSC.

ECSS-Q-ST-70-60_1390796

e. Tg may be measured in conformance with test method 2.4.24c of IPC-TM-650 using TMA.

NOTE Tg, T288 and Td are important properties that affect the thermal reliability, especially for assembly operations.

ECSS-Q-ST-70-60_1390382

f. CTE in Z-direction or Z-axis expansion shall be measured in conformance with test method 2.4.24c of IPC-TM-650 using TMA.

NOTE CTE in Z-direction is an important property that affects the thermal reliability of a via. “Z-axis expansion” is measured over a wide temperature range of (50-260) °C, which typically generates more reliable test data than “CTE in Z-direction”.

ECSS-Q-ST-70-60_1390797

g. The results of thermal analysis should be verified against the slash sheet of IPC-4101E and the supplier specification of the raw materials.

NOTE It is not expected that this verification shows measurements identical to the datasheets. This is performed to obtain reference measurements.

ECSS-Q-ST-70-60_1390883

h. CTE in X,Y-direction should be measured using TMA.

NOTE CTE in X,Y-direction is an important property for assembly verification.

9.4.9 Flammability

ECSS-Q-ST-70-60_1390383

a. Flammability shall be in conformance with ESA-HRE-IPL-RQ-0002 chapter 9.2.3.

ECSS-Q-ST-70-60_1390798

b. Flammability testing should be performed in conformance with ECSS-Q-ST-70-21.

NOTE This is important for human spaceflight. Product Assurance and Safety Requirements for ISS Pressurized Payloads ESA-HRE-IPL-RQ-0002 chapter 9.2.3 specifies "All payloads materials shall be assessed for flammability by analysis or test according to the flammability requirements in paragraphs 3.10.2 to 3.10.2.2 of SSP 51700 and JSC 29353."

9.4.10 Offgassing

ECSS-Q-ST-70-60_1390384

a. Offgassing shall be in conformance with ESA-HRE-IPL-RQ-0002 chapter 9.2.4.

ECSS-Q-ST-70-60_1390799

b. Offgassing testing should be performed in conformance with ECSS-Q-ST-70-29.

NOTE This is important for human spaceflight. Product Assurance and Safety Requirements for ISS Pressurized Payloads ESA-HRE-IPL-RQ-0002 chapter 9.2.4 specifies "Determination of offgassing products from materials and assembled articles shall meet the offgassing acceptance criteria in paragraph 7.7.3 of NASA-STD-6001B."

9.4.11 Solderability on PTH

9.4.11.1 Overview

The objective of the test is to verify the wettability on PTH. This is performed by floating a sample on molten solder and by assessing the rise of the solder in the PTH. Coverage of solder on the corner of a PTH is more difficult to achieve uniformly compared to an SMT pad. When the solderability test passes on PTH, it is, therefore, also expected to pass on SMT pads.

9.4.11.2 Test vehicle

ECSS-Q-ST-70-60_1390385

a. The test pattern for solderability test shall be one of the following:
   1. Coupon A/B with PTH as specified in requirement 8.2.2d, or
   2. PCB sample with PTH.

ECSS-Q-ST-70-60_1390386

b. The coupon shall include representative PTH in accordance with ECSS-Q-ST-70-12 requirements 15.2d.2, 15.2d.4, 15.2d.5(a) and 15.2d.8.

NOTE 1 Requirements 15.2d.2 and 15.2d.4 specify to include a representative configuration of copper planes and internal heat sink. Requirements 15.2d.5(a) and 15.2d.8 specify to include PTH with hole sizes of maximum or most frequently used dimensions.

NOTE 2 Solderability coupon type “S” from IPC-2221C specifies dimensional parameters and need to be tailored to meet requirement b.

ECSS-Q-ST-70-60_1390387

c. The coupon shall include minimum three PTH.

9.4.11.3 Solderability test parameters

ECSS-Q-ST-70-60_1390388

a. The solder shall be type “63 tin solder” in conformance with table 6-1 of ECSS-Q-ST-70-61.

ECSS-Q-ST-70-60_1390389

b. The flux shall be type “ROL0” in conformance with table 6-2 of ECSS-Q-ST-70-61.

ECSS-Q-ST-70-60_1390390

c. The solder bath shall be temperature controlled in conformance with pretinning in Table 7-2 of ECSS-Q-ST-70-61.

ECSS-Q-ST-70-60_1390391

d. The tolerance of the temperature control of the solder bath shall be ±5°C.

ECSS-Q-ST-70-60_1390392

e. The solder bath temperature shall be set at 235°C.

9.4.11.4 Test flow

ECSS-Q-ST-70-60_1390393

a. After sampling the coupon, it shall be cleaned using a cleaning agent in accordance with clause 6.4 of ECSS-Q-ST-70-61.

NOTE Bake-out is not mandatory. Bake-out can slightly increase the intermetallic layer. This effect is minor compared to the pre-conditioning.

ECSS-Q-ST-70-60_1390800

b. Pre-conditioning of the sample should be performed by applying a heating profile to the coupon in conformance with IPC-TM-650 test method 2.6.27 that is representative of vapour phase reflow.

NOTE 1 This pre-conditioning method can be simulated by 2 X 5 minutes at 230°C in an oven, which is in accordance with Table 4-2 of IPC-J-STD-003C. The oven is set at and pre-heated to 230°C. The timing of 5 minutes is in between door openings. A forced air convection oven provides the best transfer of heat to the sample.

NOTE 2 The purpose of pre-conditioning is to simulate the vapour phase reflow that can occur on both sides of a PCB with SMT components prior to soldering of PTH. However, this preconditioning is not a mandatory part of the test flow because it is difficult to perform in a representative manner and because historically customers have not reported poor solderability on SnPb surface finish.

ECSS-Q-ST-70-60_1390394

c. Flux shall be applied to the test area and drained on absorbent, clean material prior to solderability test.

ECSS-Q-ST-70-60_1390395

d. The solderability test shall be performed in not less than one minute, and not more than five minutes after application of flux.

ECSS-Q-ST-70-60_1390396

e. Dross and burned, residual flux shall be removed from the surface of the molten solder immediately prior to solderability test.

ECSS-Q-ST-70-60_1390397

f. Solderability test shall be performed by floating the coupon on molten solder for a maximum duration of 30 s.

ECSS-Q-ST-70-60_1390801

g. During solderability test, the coupon may be depressed into the solder bath to a maximum of 50 % of the coupon thickness.

NOTE This solderability test is in conformance with paragraph 4.4.1 of IPC-J-STD-003C.

ECSS-Q-ST-70-60_1390398

h. After the elapsed time, the coupon shall be removed from the molten solder and maintained still and horizontal until the solder on the coupon solidifies.

ECSS-Q-ST-70-60_1390399

i. Prior to examination, all specimens shall have the flux removed using a cleaning agent in accordance with clause 6.4 of ECSS-Q-ST-70-61.

ECSS-Q-ST-70-60_1390400

j. Test specimens shall be examined at 10X magnification by visual inspection on the side that was not in contact with the solder.

NOTE Microsectioning is not needed.

9.4.11.5 Acceptance criteria

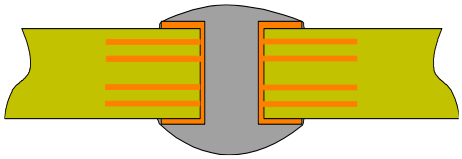
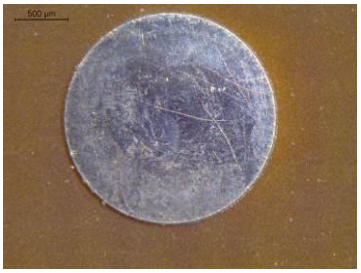
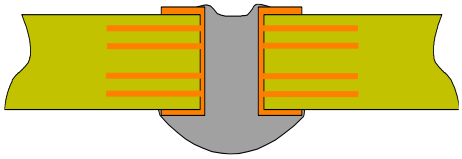
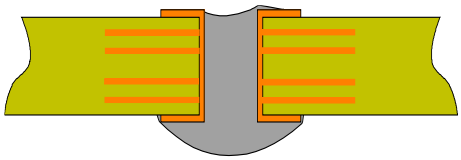
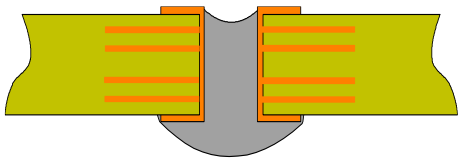
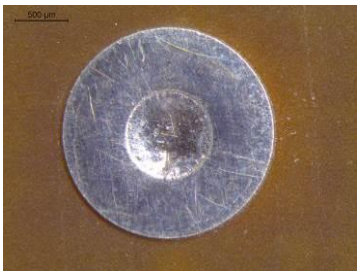
ECSS-Q-ST-70-60_1390401

a. Acceptance criteria for solderability of PTH shall be as specified in Table 9-1.

NOTE 1 The nonconformance criteria are based on visual inspection. The schematic drawings of cross-sections are only shown for illustration and information. The wetting angle is not evaluated in this test.

NOTE 2 In case of unacceptable solderability in conformance with this test method, it is good practice to further investigate by soldering a wire in conformance with ECSS-Q-ST-70-61.

Table 9-1: Nonconformance criteria for solderability of PTH

Schematic cross-section (for information)	Nonconformance criteria based on visual inspection	Evaluation
		Acceptable if: Solder rises to the top of the PTH on the full circumference and the corner has been wetted on the full circumference.
		
		Acceptable if: Solder rises to the top of the PTH on the full circumference and the corner has been wetted on ≥ 25 % of the circumference.
		Not acceptable if: Solder does not rise to the top of the PTH, or corner has been wetted on <25 % of the circumference.

9.4.12 Solderability on SMT pads

ECSS-Q-ST-70-60_1390884

a. Solderability on SMT pads shall be performed using a wetting balance tester in conformance with J-STD-003D.

NOTE 1 Further details of possible test methods and patterns are provided in clause 1.5.2 and 4.2.3 of J-STD-003D. To avoid a high thermal dissipation of the coupon, it is good practice to remove all internal layers in this pattern, as well as to pre-heat the coupon. In addition, the IPC-4552A and IPC-4556 provide further instructions and criteria, but are only relevant to ENIG and ENEPIG.

NOTE 2 It is good practice to perform solderability testing on SMT pads for qualification. It is not specified for procurement.

9.5 Group 3 – Thermal stress and as-received

9.5.1 Overview

The solder bath test is a quick and easy test method to assess robustness of the sample under thermal stress.

Rework simulation is performed to simulate the thermal stress caused by hand solder assembly, rework and repair. The quality of the solder joint is not assessed. This test method can be tailored to be performed on SMT pads.

The rework simulation test method specifies 10 heat cycles. However, worst-case assembly, rework and repair can include more than 10 heat cycles. The stress specified by the test method covers a typical assembly process, but it does not cover worst-case. In case it is foreseen to exceed these test conditions, it is good practice to perform a specific evaluation.

A sample for rework simulation typically includes other holes for evaluation as-received.

9.5.2 Microsectioning

9.5.2.1 Method

ECSS-Q-ST-70-60_1390802

a. The methods for microsectioning from test method 2.1.1f from IPC-TM-650 should be used.

9.5.2.2 Sampling

ECSS-Q-ST-70-60_1390403

a. The sampling method shall not damage the area of interest to be inspected in the microsection.

NOTE For instance, milling or sawing can cause vibrations that can cause delamination. This is especially important for the rigid-to-flex interface. It is good practice to saw far away from the plane of interest and to grind to the plane of interest once the sample is potted.

9.5.2.3 Potting

ECSS-Q-ST-70-60_1390404

a. Samples and cups for potting shall be clean.

NOTE Cleaning can be done ultrasonically with isopropanol.

ECSS-Q-ST-70-60_1390405

b. Potting of the sample with resin shall provide edge retention.

NOTE Edge retention is achieved by using a hard resin, such as epoxy. However, also some acrylic resins can achieve good results. Acrylic resins can be

preferred in an industrial environment above epoxy ones because of the faster curing time.

ECSS-Q-ST-70-60_1390803

c. The potting should be free from air bubbles.

NOTE Absence of air bubbles can be achieved by submitting the uncured potted microsection to a vacuum or overpressure.

ECSS-Q-ST-70-60_1390406

d. The curing of the potting resin shall not generate heat that cause damage to the sample.

ECSS-Q-ST-70-60_1390407

e. The mixing time and ratio of the resin as specified by the supplier shall be followed.

ECSS-Q-ST-70-60_1390804

f. Fluorescent dye should be used for potting of the rigid-to-flex interface.

ECSS-Q-ST-70-60_1390408

g. In case fluorescent dye is not used for potting of rigid-to-flex interface, the following shall be demonstrated:

1. the efficiency to detect possible delamination without the contrast from the fluorescent dye;
2. any possible delamination is not caused by the microsectioning.

9.5.2.4 Surface preparation

ECSS-Q-ST-70-60_1390409

a. The quality of as-polished microsections shall be free of scratches.

NOTE Examples of microsectioning and microscopy showing target quality are shown in Figure 9-7.

ECSS-Q-ST-70-60_1390410

b. The quality of grinding and polishing of microsection shall prevent smearing of soft materials, such as copper.

NOTE 1 Smearing of copper can cover interface lines that can be indicative of adhesion defects, such as interconnect defect.

NOTE 2 It is good practice to perform grinding with incremental grit, for instance 180, 320, 800, 1200, 2500.

NOTE 3 It is good practice to perform polishing with decremental polishing paste size, for example:

- 6 µm polish pad and diamant paste, 20N, 150 rpm, 120 sec;
- 3 µm polish pad and diamant paste, 20N, 150 rpm, 90 sec;

- 1 µm polish pad and diamant paste, 20N, 150 rpm, 60 sec;
- 0,25 µm polish pad and diamant paste, 20N, 150 rpm, 45 sec.

ECSS-Q-ST-70-60_1390411

c. Micro-etching of microsections shall be sufficient to reveal interfaces between plating steps.

NOTE 1 Adhesion defects are investigated on as-polished microsections, without the use of micro-etching. This is because micro-etching always causes an interface line to become visible between different copper plating steps. After a defect has been identified, it is useful to micro-etch the microsection to investigate at which plating interface the defect is observed. If potential nonconformances are observed, a polish-etch-polish process can provide a more detailed investigation method.

NOTE 2 An adequate etching can be achieved, for example, by submerging the sample for 5 to 10 seconds in a solution of 25 ml demineralised water, 25 ml ammonia solution 25 % and 1 ml hydrogen peroxide solution 30 %.

ECSS-Q-ST-70-60_1390805

d. The plane of the microsection should be in the centre of the hole.

NOTE 1 This is especially important for dimensional measurements.

NOTE 2 This is described in test method 2.1.1f from IPC-TM-650.

9.5.2.5 Microscopy

ECSS-Q-ST-70-60_1390412

a. Quality of metallisation shall be inspected in bright field.

NOTE Bright field achieves the best contrast in the metallised areas.

ECSS-Q-ST-70-60_1390413

b. Quality of laminate shall be inspected in dark field or an equivalent lighting method.

NOTE 1 Dark field uses a high illumination intensity showing features underneath the surface of the microsection by transparency of the resin. A similar high illumination intensity can be obtained using polarisation filters.

NOTE 2 Subsurface cracks in laminate can be visible as an area showing “iridescence” in dark field. To

conclude on the nature of the iridescence it is good practice to perform progressive polishing to have the surface of the microsection at the same level of the feature. In this case a crack shows up in bright field since it is in the surface of the microsection.

ECSS-Q-ST-70-60_1390806

c. The magnification for microscopic inspection may be 50x to 1000x.

ECSS-Q-ST-70-60_1390414

d. The specific magnification for microscopic inspection for each acceptance criteria shall be as specified in clause 10.

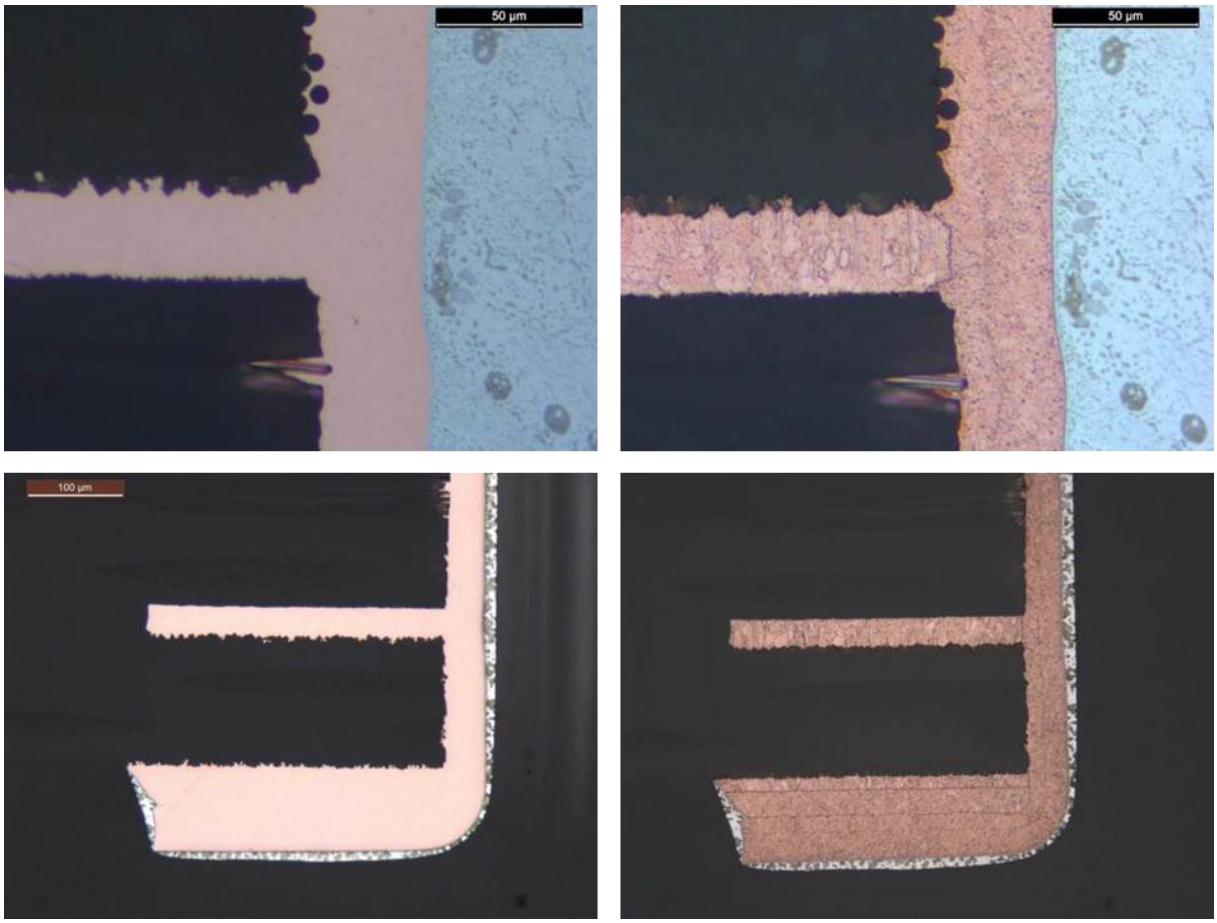


Figure 9-7: Example of target quality of microsection of innerlayer (top) and knee of the hole (bottom), as-polished (left) and after micro-etch (right).

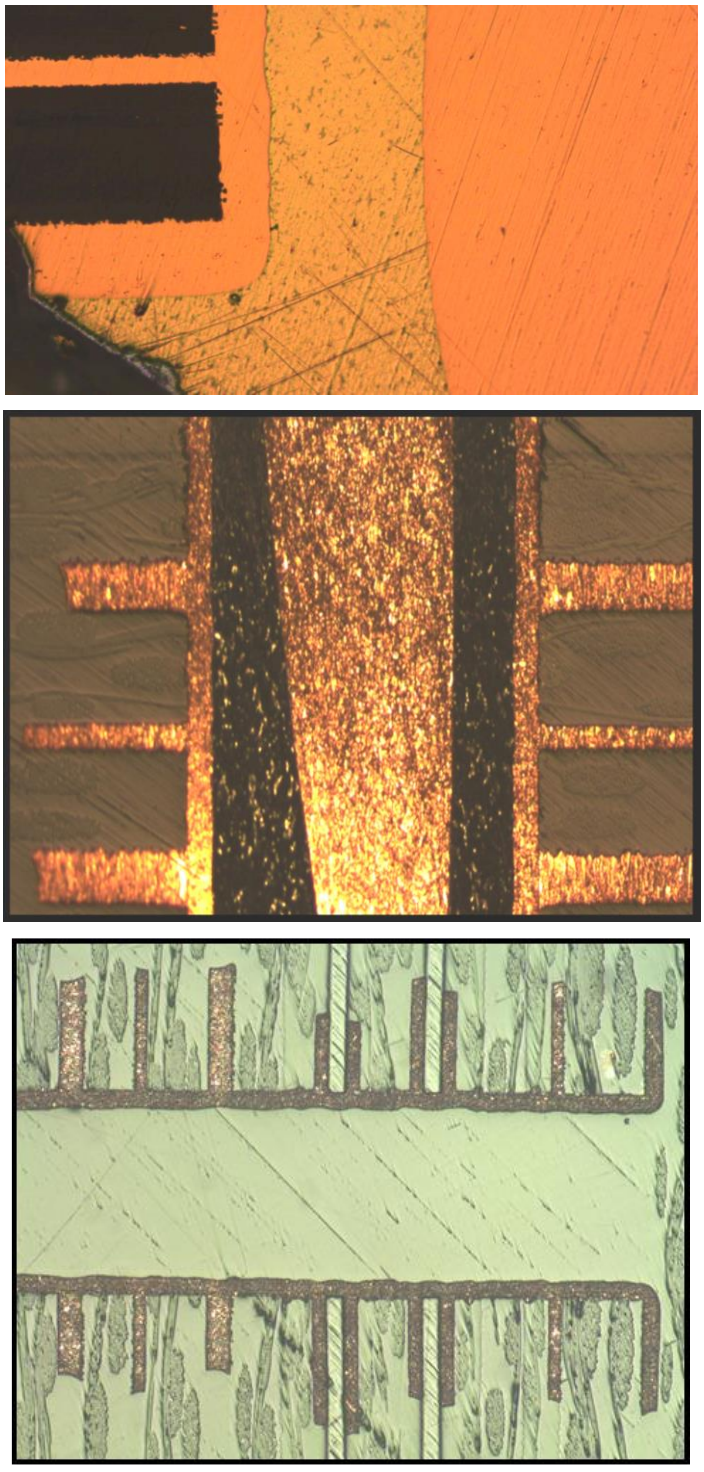


Figure 9-8: Examples of inadequate quality of microsection showing in the top image inadequate polishing, leaving scratches on surface, in the middle image over-etched sample and in the bottom image inadequate lighting, revealing no detail on metallisation, nor on laminate by transparency.

9.5.3 Solder bath float

ECSS-Q-ST-70-60_1390415

a. The test shall be carried out in conformance with condition A of test method 2.6.8e of IPC-TM-650.

ECSS-Q-ST-70-60_1390416

b. Samples shall be baked in conformance with clause 9.2.2.

ECSS-Q-ST-70-60_1390417

c. The solder bath float shall be performed to one side of the sample by floating it for 10 s in a solder bath maintained at 288 °C.

ECSS-Q-ST-70-60_1390418

d. The sample shall be removed from the bath and cooled down to ambient conditions for a duration of at least 2 minutes.

ECSS-Q-ST-70-60_1390419

e. The solder bath float and cool down from requirements 9.5.3c and 9.5.3d shall be performed 3 times in total.

NOTE The acronym for the solder bath float test is "SB". This acronym refers to this test method which specifies 3 cycles. Thus, "SB" does not imply only 1 heat cycle.

ECSS-Q-ST-70-60_1390420

f. The samples shall be inspected to ensure that holes are wetted.

ECSS-Q-ST-70-60_1390421

g. The samples shall be inspected to evaluate the visual aspects of the substrate in conformance with clause 10.4.

ECSS-Q-ST-70-60_1390422

h. The samples shall be microsectioned for evaluation of qualitative aspects in conformance with clause 10.3.

9.5.4 Rework simulation

9.5.4.1 Test vehicle

ECSS-Q-ST-70-60_1390423

a. The test pattern for rework simulation test shall be one of the following:

1. Coupon A/B with PTH as specified in requirement 8.2.2d, or
2. PCB sample with PTH and via-in-pad.

ECSS-Q-ST-70-60_1390424

b. The coupon shall include representative PTH in accordance with ECSS-Q-ST-70-12 requirements 15.2d.5(a) and 15.2d.8.

NOTE These clauses specify to include PTH with hole sizes of maximum or most frequently used dimensions.

9.5.4.2 Rework simulation test parameters

ECSS-Q-ST-70-60_1390425

a. The solder shall be type “63 tin solder” in conformance with table 6-1 of ECSS-Q-ST-70-61.

ECSS-Q-ST-70-60_1390807

b. The flux should be type “ROL0” in conformance with table 6-2 of ECSS-Q-ST-70-61.

ECSS-Q-ST-70-60_1390426

c. The solder iron and solder tip shall in conformance with clause 10.2.5 of ECSS-Q-ST-70-61.

NOTE To meet requirement 10.2.5j of ECSS-Q-ST-70-61 it is good practice to use a solder iron with a power of ≥ 80 W.

ECSS-Q-ST-70-60_1390427

d. The solder tip temperature shall be set at 350 °C.

NOTE ECSS-Q-ST-70-61 10.2.5c and d specify a maximum soldering temperature of 330°C for epoxy and 340°C for polyimide. PTH in polyimide with thermal drain can be soldered with 380°C. The test temperature of 350°C for rework simulation is defined based on test heritage.

ECSS-Q-ST-70-60_1390885

e. In frame of group 4 or group 6 testing for qualification, additional high temperature rework simulation on PTH should be performed at 380 °C.

NOTE This is specified to have information about the ability of the PCB technology to withstand incidental assembly operations at 380 °C, as permitted in 10.2.5d of ECSS-Q-ST-70-61. This information can be provided in the PID of the PCB manufacturer. However, acceptance criteria after high temperature rework are not specified for PCB qualification. In case PCB technology shows weakness to pass this high temperature rework, it is good practice that the assembler mitigates this risk prior to executing the process. This can be done, for instance, by testing a representative coupon.

ECSS-Q-ST-70-60_1390886

f. Test parameters, test vehicle and test flow should be tailored for rework simulation on via-in-pad technology, as specified in the requirements 9.6.2c.6 and 9.8.2c.4.

NOTE 1 Via-in-pad technology can include blind vias or microvias. The maximum solder temperature for

SMT devices is 340 °C, as specified in clause 10.2.5 of ECSS-Q-ST-70-61.

NOTE 2 In frame of group 4 and group 6 testing, the wire for rework is left soldered on the test vehicle, which subsequently goes through thermal cycling. A copper wire soldered on a footprint for a component with two non-leaded terminations is considered to be representative. However, this approach is not fully representative for an AAD footprint, as an AAD device includes some stress relief in the solder columns and is typically assembled with a hot air station and preheating. Moreover, it is good practice to tailor the number of temperature elevations to be representative of the used assembly processes.

9.5.4.3 Test flow

ECSS-Q-ST-70-60_1390428

a. Bake-out of the sample shall be performed in conformance with the clause 9.2.2.

ECSS-Q-ST-70-60_1390808

b. Copper wires should have a diameter of 0,2 mm to 0,7 mm smaller than the diameter of the PTH.

ECSS-Q-ST-70-60_1390809

c. Copper wires may be solid wire or stranded wire.

ECSS-Q-ST-70-60_1390429

d. The wire and PTH shall be fluxed.

ECSS-Q-ST-70-60_1390430

e. The wire shall be pretinned.

ECSS-Q-ST-70-60_1390431

f. The wire shall be inserted in the PTH and soldered.

NOTE Rework can be performed on SMT pads for specific technology as specified in requirement 9.8.2h. For an AAD footprint with small pads that will be submitted to subsequent thermal cycling as part of a group 6 test, it is good practice to remove the wire as the CTE mismatch without stress relief can be not representative.

ECSS-Q-ST-70-60_1390432

g. During soldering the tip of the solder iron shall be in contact with the pad of the PTH and the wire for a maximum duration of 5 seconds.

ECSS-Q-ST-70-60_1390810

h. Sample with high thermal mass should be submitted to pre-heating during the rework simulation test.

NOTE This is done to limit the soldering time to maximum 5 seconds.

ECSS-Q-ST-70-60_1390433

i. After soldering, the sample shall be allowed to cool down for at least 30 s.

ECSS-Q-ST-70-60_1390434

j. Additional flux shall be applied after the cool down, just prior to the next solder cycle.

ECSS-Q-ST-70-60_1390435

k. While the solder is molten in conformance with requirement 9.5.4.3g, the wire shall be moved by at least 5 mm.

NOTE It is good practice not to remove the wire from the PTH and not to re-insert during subsequent solder cycle. This is done to avoid mechanical stress, which is considered to be less reproducible and dependant on operator and dimensions of wire and PTH. The test method is intended to impose thermal stress only. However, removal of wire can be optionally performed but this only provides a conclusive outcome if results are positive.

ECSS-Q-ST-70-60_1390436

l. Clauses 9.5.4.3i, 9.5.4.3j and 9.5.4.3k shall be repeated 10 times in total.

NOTE 1 The wire is left inside the PTH.

NOTE 2 The acronym for the rework simulation is “RW”. This acronym refers to this test method which specifies 10 cycles. Thus, “RW” does not imply only 1 heat cycle.

NOTE 3 The worst-case combination of initial assembly, maximum number of repairs and maximum number of rework per component assembly can include a number of heat cycles that is higher than the 10 specified in this test method.

ECSS-Q-ST-70-60_1390437

m. A microsection shall be performed on the soldered hole including the wire to evaluate the qualitative aspects in conformance with clause 10.3.

9.5.5 Interconnect stress test (IST)

9.5.5.1 Overview

IST testing is a test method that performs rapid thermal cycling on IST coupons. The IST coupons are daisy-chained vias with power circuits through which a current is applied to heat the IST coupon and sense circuits that are used to monitor the resistance change as function of thermal cycling.

PCB technology of highest complexity or with aspects that are expected to affect thermal endurance are IST tested within the technology perimeter for procurement as specified in 9.5.5.2.2. In addition, in-process IST testing as well IST testing for qualification is performed. The thermal endurance of PCB technology that does not fall within the technology perimeter as specified in 9.5.5.2.2 is, therefore, covered by the in-process IST verification.

IST is a specific type of accelerated coupon test. The following provides a non-exhaustive list of available methods:

- assembly reflow simulation as per IPC-TM-650 test method 2.6.27
- air-to-air thermal shock as per IPC-TM-650 test method 2.6.7.2
- current induced thermal cycling as per IPC-TM-650 test method 2.6.26A method A for IST and method B for CITC

Furthermore, these test methods can be performed on several test equipment and corresponding coupon designs, as listed below:

- IST equipment and IST coupon
- CITC equipment and CITC coupon
- OM test equipment and IPC D-coupon
- HATS2 equipment and HATS2 coupon or IPC D-coupon

This clause only specifies the IST test method. The potential use of other test methods is subject to review with the customer chain.

9.5.5.2 Technology perimeter

9.5.5.2.1 In-process control

ECSS-Q-ST-70-60_1390438

a. The PCB manufacturer shall have a work instruction for in-process IST control.

ECSS-Q-ST-70-60_1390439

b. In-process IST control shall enable quantification of the reliability and monitoring of the stability.

ECSS-Q-ST-70-60_1390440

c. The PCB manufacturer shall specify the IST coupon design and IST test method to be used.

NOTE This can deviate from the IST test parameters from clause 9.5.5.4.

ECSS-Q-ST-70-60_1390441

d. The work instruction for in-process IST control shall specify the following:

1. The technology, build-up and design reference of the IST coupon;
2. The rationale for the IST coupon design based on the PID;
3. IST test parameters;
4. Test moment and frequency;
5. Statistical Process Control (SPC) limits.

NOTE A typical frequency of testing is once per week or two weeks.

9.5.5.2.2 Procurement

ECSS-Q-ST-70-60_1390442

a. IST shall be performed for procurement in case the PCB definition dossier includes one or more of the following:

1. Any PCB with ≥ 0,3 mm in Z-direction as-designed insulation distance of no-flow prepreg or 85NT;
2. Epoxy PCB with ≥ 12 copper layers;
3. Rigid-flex PCB with one or more of the following aspects:
   (a) ≥ 12 copper layers, or
   (b) ≥ 2 flex laminates, or
   (c) asymmetric build-up or asymmetric lamination;
4. HDI PCB with microvias or with aspect ratio > 7.

NOTE 1 For no-flow prepreg and 85NT, and other materials, with high thermal expansion in Z-direction: the thermal expansion is the driver for barrel crack and therefore necessitates IST testing.

NOTE 2 See Table B-6 for an example of a build-up report with as-designed insulation distance.

ECSS-Q-ST-70-60_1390443

b. At least one coupon shall be included per panel and submitted to IST testing.

ECSS-Q-ST-70-60_1390887

c. All panels that have passed outgoing inspection shall be submitted to IST testing.

NOTE 1 This includes potential overmake or yield compensation initiated by the PCB manufacturer.

NOTE 2 To improve statistic by testing multiple coupons for small order quantities, it is good practice that the procurement authority orders IST testing of all panels in the batch including potential overmake.

9.5.5.2.3 Qualification

ECSS-Q-ST-70-60_1390444

a. IST shall be performed for qualification activities in conformance with clause 7.2.

ECSS-Q-ST-70-60_1390445

b. IST shall be performed until 5 % resistance increase is reached or until a maximum of 1500 cycles.

NOTE 1 Acceptance criteria are as per clause 9.5.5.4.3. Testing to EOL is performed to provide information about the limits of the robustness.

NOTE 2 At least 3 IST coupons are used for initial qualification and at least 1 IST coupon is used for delta qualification and qualification renewal, in conformance with clause 5.7.

NOTE 3 For qualification it is not practical to test microvias after having tested other via types on that coupon to EOL.

9.5.5.3 IST coupon design and location on panel

ECSS-Q-ST-70-60_1390446

a. The IST coupon design shall be type “X”.

NOTE 1 For instance “TVX” or “SLX”. This indicates the presence of an internal (‘P’) and external (‘H’) heating circuit.

NOTE 2 An IST coupon typically includes two power circuits (H and P) and two sense circuits (S1 and S2). One sense circuit can include more than one plating sequence. In some cases more than one IST coupon is needed to represent all vias and plating sequences.

NOTE 3 The sense circuit is typically designed to be sensitive to barrel crack. The power circuit applies heat to the coupon and in addition it is typically designed to be sensitive to interconnect defect. The standard power circuit is applied through interconnects on 4 internal layers. Therefore these are assessed by IST, whilst other layers remain unassessed. In case the need arises for more comprehensive assessment of interconnections of all layers, PWB Corp can be requested to design specific coupons.

ECSS-Q-ST-70-60_1390447

b. IST coupon design shall be representative of the PCB for the following features:

1. minimum drill diameter;
2. minimum drill pitch for the via type;
3. all plating sequences, except for the case 9.5.5.3c;
4. pad diameter;
5. copper foil thickness;
6. presence of non-functional pads;
7. layer function for signal or plane;
8. diameter of clearance holes in planes.

NOTE 1 For generating IST coupon design, it is good practice to provide the PCB Gerber design files to PWB Corp to ensure that the relevant technology features are represented in the coupons. Alternatively, an IST coupon design work sheet is available on the test equipment supplier's website www.pwbcorp.com that includes these items.

NOTE 2 Space PCBs typically use SnPb surface finish. During IST testing it has been observed that SnPb enters into barrel cracks and crack initiations. This can accelerate crack growth due to wedging. This can also mask or delay resistance increase. Therefore SnPb finish can be stripped and bare copper coupons can be tested. Studies have shown correlation between both configurations.

NOTE 3 Multiple coupons can be necessary to accommodate IST on all plating sequences.

NOTE 4 The procurement authority is accountable for the design of the IST coupon in conformance with requirement 15.1a. from ECSS-Q-ST-70-12.

NOTE 5 For 9.5.5.3b.2 the minimum drill pitch is included because of statistical significance and because it represent worst-case copper plating conditions. However, maximum drill pitch, or an isolated via, can provide more stress to a single via from the thermal expansion of the surrounding dielectric. This can be a motivation to include maximum pitch, or single via, in the coupon design for an in-depth investigation.

ECSS-Q-ST-70-60_1390811

c. The plating sequence to manufacture a buried via across top and bottom layer of a single laminate need not to be included in the IST coupon.

ECSS-Q-ST-70-60_1390812

d. The coupon should be located as close as possible to the PCB.

ECSS-Q-ST-70-60_1390813

e. In case of more PCBs per panel, one IST coupon should be located as close as possible near the centre of the panel, and another one on the edge.

ECSS-Q-ST-70-60_1390814

f. The coupon should not be located in the corner of the panel.

NOTE This is done to be representative of worst-case Cu coverage. Location of IST coupon on the panel is shown in Figure 8-3. However, the sides and corner of the panel can be worst-case for registration and dielectric thickness. This can be a motivation to include both the centre and the edge of the panel in an in-depth investigation. However, the PCB manufacturer usually prefers to place PCBs in the centre of the panel for best processing conditions.

9.5.5.4 IST test method

9.5.5.4.1 Preparation

ECSS-Q-ST-70-60_1390815

a. Electrical pre-screening and possible down selection should be performed in conformance with instruction PWB-150316 in case multiple IST coupons are available.

NOTE The referenced work instruction is available on the website of the test equipment supplier.

ECSS-Q-ST-70-60_1390448

b. Bake-out of IST coupons shall be performed in conformance with requirement 9.2.2a.

ECSS-Q-ST-70-60_1390449

c. After bake-out, connectors shall be soldered to the IST coupon.

ECSS-Q-ST-70-60_1390816

d. Reabsorption of humidity in IST coupons should be prevented in conformance with requirement 9.2.2d.

ECSS-Q-ST-70-60_1390817

e. Correct soldering of connectors should be verified by measuring again the resistance of IST coupons.

ECSS-Q-ST-70-60_1390450

f. In uncontrolled conditions, IST coupons shall be submitted to IST testing within 12 hours after baking.

ECSS-Q-ST-70-60_1390818

g. In case re-absorption of humidity is mitigated in conformance with point 9.5.5.4.1d, IST coupons need not to be submitted to IST testing within 12 hours after baking.

9.5.5.4.2 IST test parameters

ECSS-Q-ST-70-60_1390451

a. IST shall be performed in conformance with test method 2.6.26A from IPC-TM-650, except for the parameters specified in this clause 9.5.5.4.2.

ECSS-Q-ST-70-60_1390452

b. The IST preconditioning cycles shall meet the following conditions:

1. It is representative of assembly conditions;
2. It includes 6 heating cycles to 230 °C, except for the case specified in 9.5.5.4.2c.

ECSS-Q-ST-70-60_1390819

c. The IST preconditioning cycles may be tailored in case all the following conditions are met:

1. The IST preconditioning cycles are representative of the assembly environment and potential repair and rework;
2. The IST preconditioning cycles are minimum 3 times to 230 °C.

NOTE Preconditioning parameters specified in this clause are representative of the assembly environment, which typically uses tin-lead solder. In case of lead-free assembly, it is expected that the preconditioning is increased to 245-260 °C and this can have significant impact on IST endurance.

ECSS-Q-ST-70-60_1390453

d. The power circuit for preconditioning shall be the “superheat” circuit

NOTE Superheat circuit is identified by “H”.

ECSS-Q-ST-70-60_1390454

e. IST cycling shall be performed to the following temperature limits:

1. polyimide or PPE: 170 °C;
2. epoxy: 150 °C;
3. microvias on polyimide or PPE: 210 °C;
4. microvias on epoxy: 190 °C.

NOTE An example of material type PPE is MEGTRON 7N.

ECSS-Q-ST-70-60_1390455

f. Failure threshold of resistance change shall be 5 % for standard holes.

NOTE In case a resistance below 250 mΩ is measured during electrical pre-screening, in conformance with 9.5.5.4.1a, the noise can be high. In this case it is good practice to confirm the failure threshold with the test equipment supplier. This can result in re-design of the coupon for future use.

ECSS-Q-ST-70-60_1390456

g. Failure threshold of resistance change shall be 4 % for microvias.

ECSS-Q-ST-70-60_1390457

h. The failure threshold for resistance change shall apply to all circuits on the IST coupon.

NOTE 1 A failure on the internal power circuit indicates a weak interconnection. This is not the typical failure mode in an IST test. This can cause local over-temperature due to high resistance.

NOTE 2 A failure on the sense circuit indicates barrel crack. This is the typical failure mode in an IST test. This does not cause local over-temperature because this circuit is passive.

ECSS-Q-ST-70-60_1390458

i. "Compensation" shall be "Calculated" for standard tests.

ECSS-Q-ST-70-60_1390459

j. "Compensation" shall be "None" for microvia testing and for testing standard vias with a pitch of ≥ 2,5 mm.

ECSS-Q-ST-70-60_1390460

k. "Sense Fail Type" shall be "A or B".

ECSS-Q-ST-70-60_1390461

l. The power circuit for IST cycling shall be the internal power circuit for standard vias.

NOTE 1 The internal power circuit is identified by "P".

NOTE 2 IST cycling includes the first few IST cycles before preconditioning and all IST cycles after preconditioning.

ECSS-Q-ST-70-60_1390462

m. For testing microvias, the power cable shall be connected to the superheat "H" circuit and the microvias monitored as the sense circuit.

NOTE By using the superheat circuit, the coupon is heated from the external layer. This is considered to be more representative compared to heating the microvias by direct current. In addition, using the superheat circuit is considered to be a slightly more benign heating method.

ECSS-Q-ST-70-60_1390888

n. Other materials than the ones specified in 9.5.5.4.2e shall be tested at a comparable strain level.

NOTE MEGTRON 7N/V has been evaluated and found to be compatible with the temperature profiles for polyimide.

ECSS-Q-ST-70-60_1390889

o. The T_0 reference resistance should be taken prior to preconditioning.

NOTE 1 The T_0 reference resistance is the initial resistance of the daisy-chain. The relative resistance change as a function of thermal cycles is determined versus this initial resistance.

NOTE 2 For 9.5.5.4.2f and 9.5.5.4.2g it is good practice to set the test for a higher resistance threshold than 4% or 5% (such as 10%). This prevents that early failure is triggered in case of high noise or environmental drift. The 4% or 5% acceptance criterion is applied on the data in retrospect to determine the cycles to failure.

ECSS-Q-ST-70-60_1390890

p. A drift of resistance of the superheat circuit should be compensated by a software algorithm to prevent a drift in temperature cycling.

NOTE The resistance of the superheat circuit can change by interaction of the copper conductor with the surface finish as a result of the temperature excursions.

9.5.5.4.3 IST acceptance criteria

ECSS-Q-ST-70-60_1390463

a. Any coupon shall have an IST endurance of ≥ 400 cycles for standard holes.

ECSS-Q-ST-70-60_1390464

b. Any coupon shall have an IST endurance of ≥ 400 cycles for microvias.

NOTE 1 IST testing of microvias can be performed after IST testing of standard holes in case both hole types are present on the same coupon. The IST cycles for standard holes occur to a lower temperature, which does not impact the IST performance of the microvia circuit tested subsequently.

NOTE 2 For 9.5.5.4.3a and 9.5.5.4.3b it is good practice to set the test for a higher IST endurance than 400 (such as 500). This prevents that early failure is triggered in case of high noise or environmental drift.

ECSS-Q-ST-70-60_1390820

c. <<deleted>>

9.5.5.4.4 Analysis and reporting

ECSS-Q-ST-70-60_1390821

a. After IST testing, the coupon should be submitted to microsectioning.

ECSS-Q-ST-70-60_1390465

b. In case the required number of IST cycles are not achieved, the coupon shall be submitted to microsectioning to investigate the cause of failure and possible corrective actions.

ECSS-Q-ST-70-60_1390822

c. The location for microsectioning should be determined by observing the hotspot during infrared thermography while a small current is passed through the failed circuit.

NOTE 1 The purpose is to get a visual confirmation of the failure mechanism in the metallisation. Barrel crack, wear-out of the copper barrel and innerlayer separation should be the main focus of this inspection.

NOTE 2 In case tin-lead is included on the IST coupon, it is good practice to verify the absence of tin-lead in barrel cracks by microsectioning, as this can impact the measured IST endurance. An example of this is shown in Figure 9-9.

ECSS-Q-ST-70-60_1390466

d. The IST test report shall include the following:

1. Summary of test parameters;
2. Reference to the coupon design drawing;
3. Graph of resistance change as function of IST cycles.

ECSS-Q-ST-70-60_1390891

e. IST test report shall include results from all tested coupons.

ECSS-Q-ST-70-60_1390892

f. In case of IST failures, prior to batch release it shall be ensured by root cause analysis as specified in 9.5.5.4.4b that other panels in the batch - for which IST has passed - are not affected.

NOTE It is not good practice to use IST testing as a screening method to select good panels from bad ones.

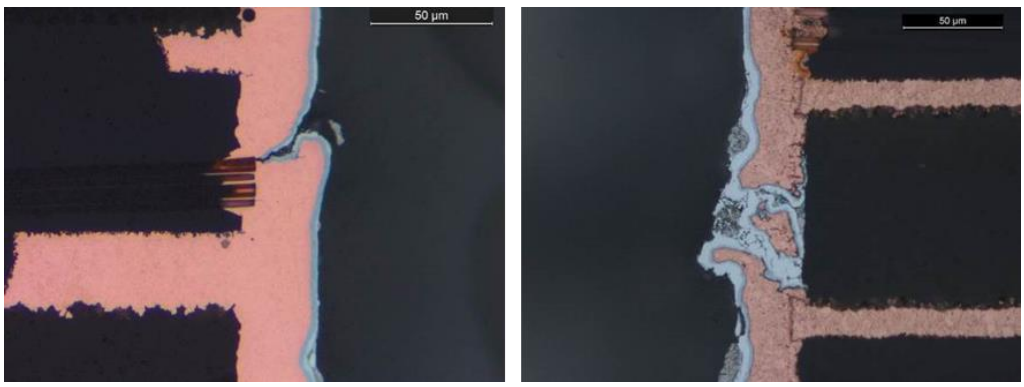


Figure 9-9: Examples of barrel cracks after IST testing showing a nominal crack size (left) and a large crack filled with SnPb (right)

9.5.5.5 Special IST test for RF PCB technology

9.5.5.5.1 Overview

Standard IST coupon design includes interconnects on L2+3 (and Ln-1 and Ln-2) in the power circuit. The sense circuit is designed to be sensitive for barrel crack, as it includes no innerlayer connections. For special technology, this design can be modified to have better sensitivity for interconnects on critical layers. This is of value in case laminate materials are used that are prone to smear, such as PTFE based materials for RF PCBs. Smear can be impacted by drill size and drill bit quality.

9.5.5.5.2 IST coupon design for interconnect verification in RF PCBs

ECSS-Q-ST-70-60_1390467

a. Standard IST coupons shall be included for RF PCB in case this is within the technology perimeter in conformance with 9.5.5.2.2a.

NOTE Standard IST coupons evaluate mainly barrel strength.

ECSS-Q-ST-70-60_1390823

b. Specific IST coupons for interconnect verification may be included for RF PCB technology to assess smear.

ECSS-Q-ST-70-60_1390824

c. Specific IST coupons for interconnect verification should include all drill sizes for holes that interconnect on RF laminate.

NOTE This does not include non-functional pads.

ECSS-Q-ST-70-60_1390825

d. The daisy-chain should include the largest drill diameter for holes that interconnect on RF laminates.

NOTE Interconnection in large holes are most stressed during IST cycling.

ECSS-Q-ST-70-60_1390826

e. The daisy-chain should include interconnection on all RF innerlayers.

ECSS-Q-ST-70-60_1390827

f. The daisy-chain should include interconnection on outermost RF innerlayers.

NOTE 1 This is for example L2, L3, Ln-1 and Ln-2.

NOTE 2 The interconnects on outermost innerlayers are most stressed during IST cycling.

ECSS-Q-ST-70-60_1390828

g. The power cable should be connected to the superheat circuit.

NOTE This circuit is not affected by the quality of interconnects and provides a stable heat source.

h. The IST cycling may be performed to a temperature of 210 °C.

NOTE The high temperature is used to provide sufficient stress to the interconnections on thermally robust PTFE layers. The possible presence of low Tg laminate needs to be evaluated, but is not deemed critical to this test temperature as sensitivity to barrel strength is designed to be low.

9.6 Group 4 – Assembly and life test - extended

9.6.1 Overview

ECSS-Q-ST-70-10 group 4 included thermal cycling. This is superseded by the accumulative test flows of group 4 and group 6 described in this clause and in clause 9.8.

Group 4 includes a higher number of 500 thermal cycles with a lower temperature range of 155 °C. In addition, group 4 includes electrical testing and peel strength. The group 4 is performed for initial qualification of a material or technology and provides evidence that the PCB technology withstands the thermal excursions from assembly verification, in conformance with requirement 14.11d of ECSS-Q-ST-70-61. See clause 9.8.1 for an overview of group 6. Group 4 includes a smaller range of thermal cycling compared to group 6, compensated by a higher number of cycles. Group 4 testing is considered more representative, but it involves a longer test duration.

9.6.2 Test flow for group 4

ECSS-Q-ST-70-60_1390468

a. The test vehicle for group 4 shall include the PCB.

ECSS-Q-ST-70-60_1390469

b. The test vehicle for group 4 shall include coupons that are specified for each test method.

ECSS-Q-ST-70-60_1390470

c. The following test steps shall be performed for group 4 in this order:

1. bake-out in conformance with clause 9.2.2;
2. intralayer and interlayer insulation resistance with DC voltage in conformance with clause 9.6.3;
3. intralayer and interlayer dielectric withstanding voltage with DC voltage in conformance with clause 9.6.4;
4. reflow simulation in conformance with clause 9.8.3;
5. rework simulation on at least 2 PTH of the PCB in conformance with clause 9.5.4 and requirement 9.5.4.2e;
6. rework simulation on at least 2 via-in-pad on top side and 2 via-in-pad on bottom side of the PCB in conformance with requirement 9.5.4.2f;
7. thermal cycling in conformance with clause 9.8.4 with the following modifications:
   (a) for requirement 9.8.4g the minimum temperature is -55 °C;
   (b) for requirement 9.8.4h the maximum temperature is +100 °C;
   (c) for requirement 9.8.4i the temperature range is 155 °C;
   (d) for requirement 9.8.4j the number of thermal cycles is 500;

8. intralayer and interlayer insulation resistance with DC voltage in conformance with clause 9.6.3;
9. intralayer and interlayer dielectric withstanding voltage with DC voltage in conformance with clause 9.6.4;
10. peel test in conformance with clause 9.4.1;
11. microsectioning in conformance with clause 9.5.2;
12. evaluation of acceptance criteria in conformance with clause 10.

NOTE Via-in-pad can include blind vias or microvias.

ECSS-Q-ST-70-60_1390471

d. Microsectioning and evaluation in conformance with 9.6.2c.11 and 9.6.2c.12 shall be performed on the following:
   1. The PTH and via-in-pad from the PCB that have been subjected to rework simulation;
   2. All technology features under qualification.

      NOTE Technology features under qualification can include all via types, the build-up and materials.

ECSS-Q-ST-70-60_1390830

e. Interconnection resistance on a daisy-chain coupon may be monitored during thermal cycling.

ECSS-Q-ST-70-60_1390472

f. In case a daisy-chain coupon is used in conformance with requirement 9.6.2e, change of interconnection resistance shall be ≤ 10 %.

ECSS-Q-ST-70-60_1390831

g. The daisy-chain coupon may be an IST coupon.

   NOTE 1 Continuous in-situ measurement using four-wire resistance is commonly performed on coupons in a thermal cycling chamber. The daisy-chain is designed with sufficient length to allow a sensitive measurement.

   NOTE 2 This evaluation can provide correlation of traditional chamber thermal cycling with IST cycling by continuous measurement of interconnection resistance on the same pattern. It can also quantify the electrical performance of a thermally stressed daisy-chain by measuring before and after the group 4 test flow.

   NOTE 3 Rework simulation is only performed on the PCB. It is not performed on coupons for insulation resistance, dielectric withstanding voltage, IST or peel strength.

9.6.3 Insulation resistance

ECSS-Q-ST-70-60_1390473

a. The insulation resistance test shall be performed in conformance with tests 6a for external intralayer insulation resistance, test 6b for internal intralayer insulation resistance and test 6c for interlayer insulation resistance of IEC 60326-2-am 1 (1992-06).

NOTE This test is superseded by the high resistance electrical test on PCB. However, insulation resistance is still measured on coupons before and after environmental testing.

ECSS-Q-ST-70-60_1390474

b. A direct voltage of 250 V shall be applied between the two closest conductors that are not electrically connected.

NOTE Table 13-3 and Table 13-4 of ECSS-Q-ST-70-12 allow, for instance, a minimum conductor spacing of 200 µm on external layers without conformal coating, 63 µm on internal layers for HDI and 25 µm between layers on flex laminate.

ECSS-Q-ST-70-60_1390475

c. Test voltage shall be DC for qualification activities.

ECSS-Q-ST-70-60_1390832

d. The procurement authority may define in the PCB definition dossier specific AC insulation resistance testing on coupons or PCB.

NOTE 1 The majority of applications for space are in DC. It is important to note that DC/DC converters can have some AC sections.

NOTE 2 Peak transient voltages in AC or DC is covered by requirement 13.8.2b. from ECSS-Q-ST-70-12.

NOTE 3 The failure mechanisms of primary concern in PCB materials are of slow time constant, such as ECM. In this case, DC is deemed worse-case than AC.

ECSS-Q-ST-70-60_1390476

e. When the voltage is applied, the insulation resistance (R) shall be measured after 1 minute, except the case specified in 9.6.3f.

ECSS-Q-ST-70-60_1390833

f. In case a stable reading is obtained earlier, the insulation resistance (R) may be measured before 1 minute.

ECSS-Q-ST-70-60_1390477

g. The test pattern for intralayer insulation resistance shall have at least 25 mm parallel conductors.

NOTE Insulation distance between tracks or between layers is representative of the PCB, as specified in clause 15.2a of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390478

h. The test pattern for interlayer insulation resistance shall have at least 1 cm^2 superimposed conductors.

NOTE Test coupon E of IPC-2221C can be used for intralayer insulation resistance. For interlayer insulation resistance, test coupon E is modified as per requirement 9.6.3h.

ECSS-Q-ST-70-60_1390479

i. The intralayer insulation resistance as received shall be ≥ 10 GΩ.

ECSS-Q-ST-70-60_1390480

j. The interlayer insulation resistance as received shall be ≥ 100 GΩ.

ECSS-Q-ST-70-60_1390481

k. The intralayer insulation resistance after thermal stress shall be ≥ 1 GΩ.

ECSS-Q-ST-70-60_1390482

l. The interlayer insulation resistance after thermal stress shall be ≥ 10 GΩ.

NOTE To measure such high resistance it is good practice to use an equipment with a measurement range up to 1000 GΩ.

9.6.4 Dielectric withstanding voltage (DWV)

ECSS-Q-ST-70-60_1390483

a. The test shall be carried out in conformance with IPC-6012F chapter 3.8.1 and condition B of test method 2.5.7d of IPC-TM-650.

NOTE 1 This method specifies 1000 V DC for 30 s. The procurement authority can define specific AC testing on coupons or PCB as specified in requirement 9.6.3d.

NOTE 2 PCB qualification does not cover for continuous operation of the assembled PCB at any voltage, which is typically performed at unit level. Bare PCBs are not subject to tests and requirements for rating and derating.

ECSS-Q-ST-70-60_1390484

b. For interlayer measurements the test voltage shall be applied between two superimposed conductors with a surface area of ≥ 1 cm^2.

ECSS-Q-ST-70-60_1390485

c. For intralayer measurements the test voltage shall be applied between two adjoining, but not electrically connected conductors within the same layer with a total length of ≥ 25 mm.

NOTE Insulation distance between tracks or between layers is representative of the PCB, as specified in clause 15.2 of ECSS-Q-ST-70-12.

d. Visual inspection shall show no evidence of breakdown, flashover or sparking.

NOTE 1 Test coupon E of IPC-2221C can be used for intralayer DWV. For interlayer DWV, test coupon E is modified as per requirement 9.6.4b.

NOTE 2 Advanced test equipment are capable to monitor voltage or leakage current continuously during the applied test voltage. A sudden drop in voltage is indicative of a discharge. This is relevant because visual inspection is not fully efficient on internal layers covered by plane layers.

9.7 Group 5 – ECM tests

9.7.1 Overview

Group 5 in ECSS-Q-ST-70-10 included a damp heat test. This is superseded by the THB and CAF tests specified in this clause.

The THB test has the objective to assess the cleanliness of the sample, which includes cleanliness of raw laminate and cleanliness of PCB manufacturing processes. The adhesion of resin to, for instance, fibre contamination can be degraded during thermal stress of assembly, such as vapour phase reflow. Fibre contamination can provide a pathway for ECM. Because of the relatively large particle size of typical contamination, this type of ECM is possible for PCB designs using standard insulation distance.

The CAF test has the objective to assess the material properties for its CAF resistance. The adhesion of resin to glass fibre reinforcement can be degraded during thermal stress. The glass-to-resin interface, or a hollow glass fibre, can provide a pathway for ECM. The CAF mechanism is only probable at small insulation distance, as for HDI designs. The CAF test can also detect contamination as for the THB test, but this is not its objective.

THB is performed for process control on standard PCB technology. CAF is performed for HDI technology.

The environment of THB and CAF tests include a temperature of 85 °C because this is the maximum operational temperature for which PCBs are qualified in conformance with requirement 5.1b. The tests include a relative humidity of 75% RH because this provides some margin and acceleration of test compared to the maximum relative humidity of 65 % in clean rooms. However, it is possible that PCB assemblies are tested or operated at higher humidity outside of cleanrooms.

Ground-based testing at unit level is deemed the worst-case environment for a potential ECM because of the presence of humidity in the atmosphere. However, studies have shown that the time constant of desorption of humidity from the somewhat hygroscopic laminate can be underestimated significantly in the presence of ground-planes and other complex PCB geometry.

9.7.2 Temperature, Humidity, Bias (THB)

9.7.2.1 General

ECSS-Q-ST-70-60_1390487

a. A justification shall be provided in case any part of this test method is tailored.

NOTE The specified method can be superseded by future test campaigns to implement lessons learned or to represent applications.

9.7.2.2 Test vehicle

ECSS-Q-ST-70-60_1390488

a. The lay-out of the test vehicle for THB test shall meet all the following conditions:

1. It includes two comb patterns in X and Y-direction on each internal layer;
2. It includes 150 µm as-designed insulation distance D between tracks;
3. Each comb pattern covers an area of ≥ 30x30 mm;
4. The sensitivity of the pattern is ≥ 20000 number of squares.

NOTE 1 An example of a test vehicle for THB testing is shown in Figure 9-10.

NOTE 2 150 µm as-designed can result in minimum 120 µm as-manufactured.

ECSS-Q-ST-70-60_1390489

b. The sensitivity S of the pattern shall be calculated using the following formula:

$$S = LxN/D$$

Where:

L: length of track

N: number of gaps between tracks

D: insulation distance

NOTE 1 The unit of the sensitivity is "number of squares". This is a dimensionless value representing the interface area, that is proportional to the sum of the length of parallel tracks and inverse proportional to the insulation distance.

NOTE 2 The pattern in Figure 9-10 uses 150 µm track width and 150 µm insulation distance over an area of 30 mm length and width. This results in 30/(0,15+0,15)=100 gaps N. Therefore the sensitivity S= 30 x 100 / 0,15 = 20000 number of squares.

ECSS-Q-ST-70-60_1390490

c. The THB test shall assess internal layers.

ECSS-Q-ST-70-60_1390491

d. The build-up of the test sample shall include ≥ 8 copper layers, uni-flow prepreg, no-flow prepreg, flex laminate and rigid laminate materials in conformance with the PID.

NOTE An example of the build-up is shown in Figure 9-11.

ECSS-Q-ST-70-60_1390492

e. The thickness shall be 1,6 mm ± 10 % over connector metallisation.

ECSS-Q-ST-70-60_1390493

f. The manufacture of samples shall follow the process flow as specified in the PID including the manufacture of windows in no-flow prepreg as for rigid-flex PCBs.

NOTE Manufacture of windows and use of various materials are sources of contamination which are aimed to be included in the test vehicle.

ECSS-Q-ST-70-60_1390494

g. Copper foil thickness shall be 35 µm.

ECSS-Q-ST-70-60_1390495

h. Surface finish on connector shall not be SnPb

NOTE This is specified because SnPb can contaminate the connector pins on the test rack. Alternative finishes, such as galvanic Au and/or Ni or ENEPIG do not show this problem. External layers and surface finish is not within the scope of the test method.

ECSS-Q-ST-70-60_1390496

i. In total four samples shall be tested from at least two different panels.

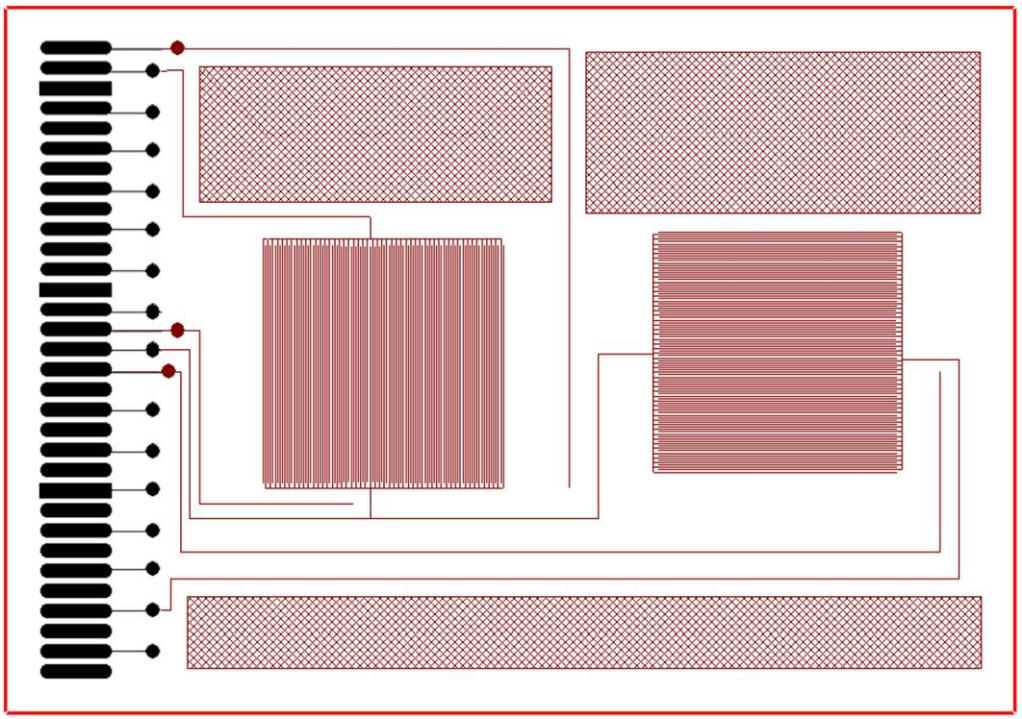


Figure 9-10: THB test pattern

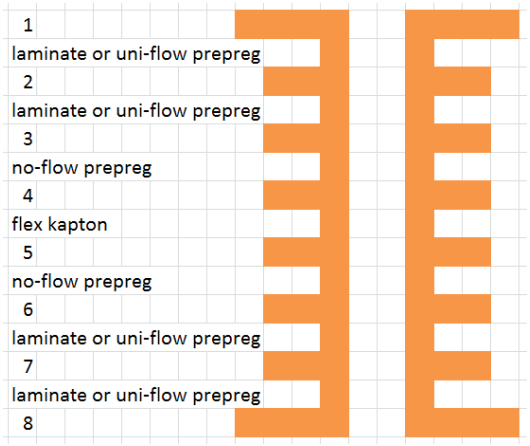


Figure 9-11: Build-up for THB test vehicle

9.7.2.3 Test method

ECSS-Q-ST-70-60_1390497

a. The sample preparation method shall be as follows:

1. bake-out in conformance with clause 9.2.2;
2. two times reflow simulation in conformance with clause 9.8.3;
3. ultrasonic cleaning followed by bake-out in conformance with clause 9.2.2.

NOTE 1 Reflow simulation is performed to represent assembly environment and because the high temperature can carbonise contaminants or can weaken the adhesion between resin and contaminant.

NOTE 2 Ultrasonic cleaning can be performed in IPA. This is done to ensure clean surfaces in the connector pattern.

ECSS-Q-ST-70-60_1390498

b. The THB method shall be as follows:

1. THB Ambient using the parameters: 24h, 25°C, 50% RH, 50V;
2. THB ECM using the parameters: 150h, 85°C, 75% RH, 50V;
3. THB Ambient using the parameters: 24h, 25°C, 50% RH, 50V.

NOTE 1 The THB Ambient part is done to determine ambient insulation resistance prior to and after the THB ECM part. This verifies that any failures during the THB ECM part persist after returning to ambient conditions.

NOTE 2 It is good practice to verify that changes in the environmental chamber do not cause high humidity or condensation on samples. From Ambient to ECM, this is achieved by increasing temperature prior to increasing RH. From ECM to Ambient this is achieved by decreasing RH prior to decreasing temperature and by using a slow rate of temperature change.

ECSS-Q-ST-70-60_1390499

c. During THB Ambient and THB ECM insulation resistance of all patterns shall be measured periodically using an electrometer capable of measuring high resistances combined with a switchbox, while maintaining the bias voltage.

NOTE The AutoSIR equipment can perform this task.

ECSS-Q-ST-70-60_1390500

d. Acquisition rate shall be at least once in 10 minutes.

NOTE A faster acquisition rate is good practice to be able to detect transient changes.

ECSS-Q-ST-70-60_1390501

e. After THB test, samples shall be microsectioned to determine the cause of a breach of insulation resistance.

NOTE 1 It is good practice to perform horizontal microsectioning just adjacent to the layer that has failed. After that, cross-sectioning can be performed in addition to provide better visibility of the failure site.

NOTE 2 Infrared thermography can be performed, possibly using "lock-in" technique, to determine the failure location in X,Y-direction. The location in Z-direction is known because each layer is acquired individually. It is good practice to ensure that the voltage used during thermography is not higher than the test voltage during THB and that the current does not heat up and damage the failure site. Instead of failure location using thermography, the whole 3x3 cm pattern can be included in horizontal microsectioning. This minimizes the risk of damage due to heat and it is relatively simple to perform microscopy on such sample area.

ECSS-Q-ST-70-60_1390502

f. It shall be determined if a breach of insulation occurred in prepreg or in laminate layers.

NOTE The cleanliness of prepreg layer is under control by the PCB manufacturer. The cleanliness of laminate layers is under control by the laminate supplier.

9.7.2.4 Acceptance criteria

ECSS-Q-ST-70-60_1390503

a. A sudden drop in resistance by an order of magnitude shall be breach of insulation.

NOTE Breach of insulation can occur intermittent or continuous. Examples of stable insulation and breach of insulation are shown in Figure 9-12.

ECSS-Q-ST-70-60_1390504

b. Breach of insulation that is demonstrated by microsectioning to be caused by lack of cleanliness shall be evaluated during the audit in conformance with clause 6.7.

NOTE The test can only be treated as nonconform in case contamination is demonstrated to be the cause of breach of insulation. The electrical response only, is not sufficient. Hence, it is not necessary that the environmental parameters are fully representative of operational use. The test only serves to find contamination, if any. Test results of contamination causing breach of insulation are evaluated together with the cleanliness of processes during the audit.

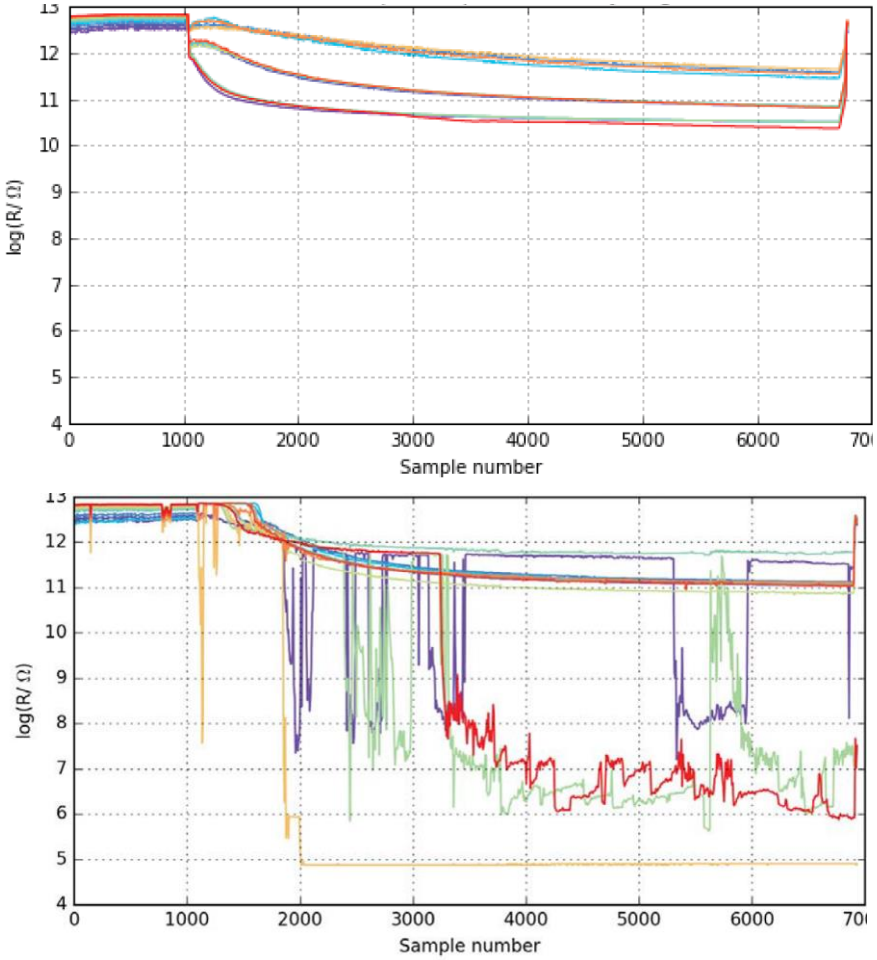


Figure 9-12: Insulation resistance during THB Ambient (until sample nr 1000) and THB ECM showing continuous breach of insulation on 4 patterns in the lower graph. The top graph shows stable insulation.

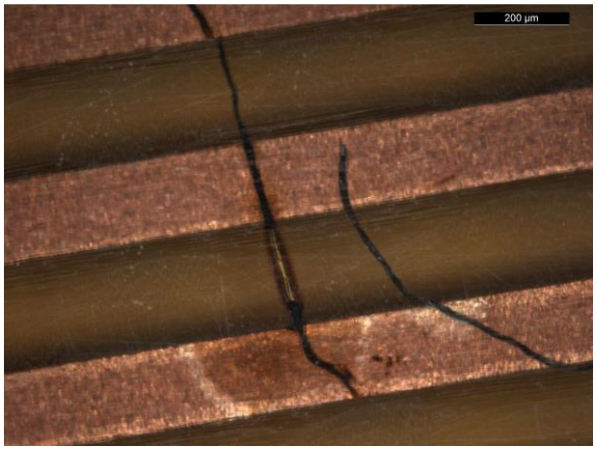


Figure 9-13: Horizontal microsection showing fibre contamination on tracks in prepreg resin causing breach of insulation.

9.7.3 Conductive Anodic Filament (CAF)

9.7.3.1 General

ECSS-Q-ST-70-60_1390505

a. A justification shall be provided in case any part of this test method is tailored.

NOTE The specified method can be superseded by future test campaigns to implement lessons learned or to represent applications.

9.7.3.2 Test vehicle

ECSS-Q-ST-70-60_1390506

a. The lay-out of the test vehicle for CAF test shall meet all the following conditions:

1. It includes the pattern configuration A as specified in Table 9-2 for aligned vias using ≥20x20 vias configured in X and Y-direction;
2. It includes the pattern configuration B as specified in Table 9-3 for staggered vias using ≥10x20 vias;
3. It includes the pattern configuration C as specified in Table 9-4 for vias in plane using ≥20x20 vias with all non-functional pads removed;
4. Electrical registration coupons in X and Y-direction for verification of registration.

NOTE 1 For requirement 9.7.3.2a.1 such comb pattern of aligned vias result in 20 vias x 19 spacing = 380 CAF opportunities within a layer.

NOTE 2 For requirement 9.7.3.2a.2 such comb pattern of staggered vias result in 10 vias x 19 spacings x 2 manhattan paths = 380 CAF opportunities within a layer.

NOTE 3 For requirement 9.7.3.2a.3 the C pattern of vias-in-plane is used to represent via-to-track. The non-functional pad is removed on all layers, otherwise the failure mechanism can be as for the configuration conductor-to-conductor.

NOTE 4 For requirement 9.7.3.2a.3 C pattern is designed with bias voltage connected to the vias. Therefore the vias are positive, i.e. the anode. CAF grows from the anode, hence CAF can grow from the via, which is the purpose of this test pattern design.

NOTE 5 For requirement 9.7.3.2a.1 test pattern A is deemed to be most susceptible to CAF.

NOTE 6 It is good practice to implement an incremental spacing to rows of vias to avoid that the via

pattern always aligns with the glass weave of the laminate.

NOTE 7 Laser drilled microvias give less propensity for CAF compared to mechanical vias, because:

- smaller diameter and smaller contact area to glass
- less desmear
- less vibrations during hole wall formation

Based on this, testing a mechanical via is considered representative or slightly worse-case of a microvia. For microvia, the critical spacing is to a conductor, not to an adjacent microvia. This is therefore covered by test pattern C. By design, microvias can be spaced further apart than mechanical vias because of small feature size and possibility to stagger.

ECSS-Q-ST-70-60_1390507

b. The build-up of the test vehicle for CAF test shall meet all the following conditions:

1. Representative of the PID for material and PCB technology;
2. ≥ 10 copper layers;
3. 1,6 mm ± 10 % thickness over connector metallisation;
4. Single sequence for drilling and plating;
5. Sequential lamination.

NOTE 1 The stack-up is laminated once, after which it passes through the lamination process for a second time to simulate sequential construction.

NOTE 2 It is important to note in Table 9-2, Table 9-3 and Table 9-4 that hole diameters are specified as drill bit diameter, not finished hole diameter.

NOTE 3 The 1,6 mm connector thickness is important for fitting the test sample footprint into the connector slot. However, different equipment are available, in which case it is good practice to adjust the test sample accordingly.

ECSS-Q-ST-70-60_1390508

c. The manufacture of samples shall follow the process flow as specified in the PID.

ECSS-Q-ST-70-60_1390509

d. Surface finish on connector shall not be SnPb

NOTE This is specified because SnPb can contaminate the connector pins on the test rack. Alternative finishes, such as galvanic Au and/or Ni or ENEPIG do not show this problem.

ECSS-Q-ST-70-60_1390510

e. In total 10 test vehicles shall be tested from at least two different panels.

ECSS-Q-ST-70-60_1390834

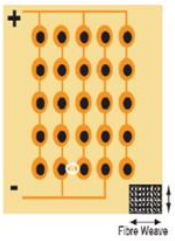
f. Registration should be ≤ 80 µm.

ECSS-Q-ST-70-60_1390511

g. The actual registration achieved on each coupon shall be included for the calculation of minimum insulation distances.

ECSS-Q-ST-70-60_1390512

Table 9-2: CAF pattern dimensions – via-to-via straight

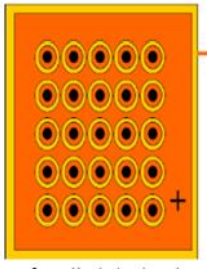
Description	Pattern	Drill diam. (µm)	Pad diam. (µm)	Via edge to via edge (µm)
X and Y-direction 1020 pitch 	IPC A1	750	860	270
	IPC A2	650	810	370
	IPC A3	500	750	520
	IPC A4	350	690	670
	ECSS A4	300	600	720

ECSS-Q-ST-70-60_1390513

Table 9-3: CAF pattern dimensions – via-to-via staggered

Description	Pattern	Drill diam. (µm)	Pad diam. (µm)	Via edge to via edge (µm)	Via edge to via edge Manhattan distance (µm)
1080 pitch 	IPC B1	800	940	280	396
	IPC B2	700	890	380	537
	IPC B3	550	840	530	750
	IPC B4	450	750	630	891
	ECSS B4	300	600	780	1103

Table 9-4: CAF pattern dimensions – via-to-plane

Description	Pattern	Drill diam. (µm)	Pad diam. (µm)	Clearance diam. (µm)	Via edge to plane (µm)
	IPC C1	350	none	640	145
	IPC C2	350	none	700	175
	IPC C3	350	none	850	250
	IPC C4	350	none	960	305

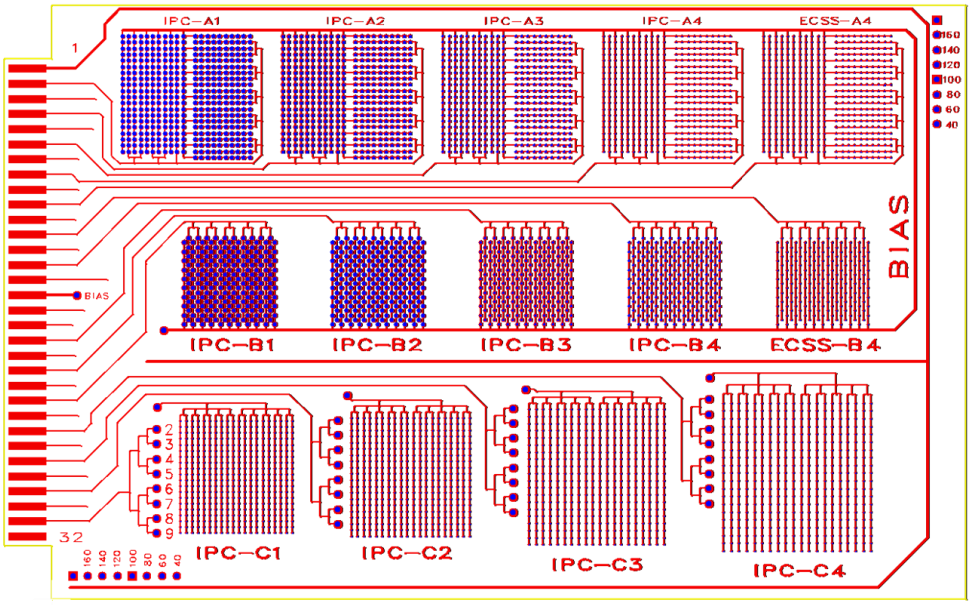


Figure 9-14: Lay-out of CAF pattern

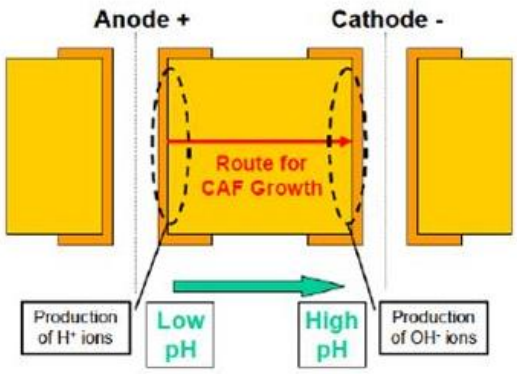


Figure 9-15: Schematic for CAF growth

9.7.3.3 Test method

ECSS-Q-ST-70-60_1390515

a. The sample preparation method shall be as follows:
   1. measurement of registration on electrical test coupons;
   2. bake-out in conformance with clause 9.2.2;
   3. six times reflow simulation in conformance with clause 9.8.3;
   4. ultrasonic cleaning followed by bake-out in conformance with clause 9.2.2.

ECSS-Q-ST-70-60_1390516

b. The CAF test method shall be as follows:
   1. Ambient phase using the parameters: 24h, 25°C, 50% RH, 0V;
   2. Preconditioning phase using the parameters: 96h, 85°C, 75% RH, 0V;
   3. CAF phase using the parameters: 500h, 85°C, 75% RH, 50V;
   4. Ambient phase using the parameters: 24h, 25°C, 50% RH, 0V.

      NOTE 1 CAF is relevant for HDI which can use voltages up to 30 V in conformance with ECSS-Q-ST-70-12. The guidelines in IPC-9691B recommend a margin of x2. For practical considerations of the test equipment this is limited to 50 V.

      NOTE 2 It is good practice to control the environmental chamber such that no condensation or rain occurs. This can be achieved during the transition from the ambient phase to the pre-conditioning phase by increasing temperature at a controlled rate, implementing a dwell time, after which the humidity can be increased at a controlled rate. This can be achieved during the transition from the CAF phase to the ambient phase by decreasing the humidity at a controlled rate, implementing a dwell time, after which the temperature can be decreased at a controlled rate.

      NOTE 3 It is good practice to clean the environmental chamber and the electrical test rack and to perform a dry run at a temperature and humidity level higher than the set points during the CAF test.

ECSS-Q-ST-70-60_1390517

c. During the CAF test method insulation resistance of all patterns shall be measured periodically using an electrometer capable of measuring high resistances combined with a switchbox, while maintaining the bias voltage if applicable.

   NOTE The AutoSIR equipment can perform this task. It is good practice to have current limiting resistors of 1 MΩ to avoid fusing the CAF and damage to the laminate. This is foreseen in the AutoSIR.

ECSS-Q-ST-70-60_1390518

d. Acquisition rate during the CAF phase shall be at least once in 15 minutes.

NOTE A faster acquisition rate is good practice to be able to detect transient changes.

ECSS-Q-ST-70-60_1390519

e. During the ambient and preconditioning phases, only a few acquisitions of insulation resistance shall be done.

NOTE This is specified because bias voltage is applied during measurement, in phases that are specified to be without bias stress.

ECSS-Q-ST-70-60_1390835

f. After the CAF test method, the location of breach of insulation should be determined on each pattern by electrical insulation of sections of the pattern.

NOTE Localisation in A and B pattern comprises of determining the x, y location, which can be achieved by insulation of sections of the surface pattern. Localisation in C pattern comprises of determining the layer, which can be achieved by insulation of the interconnections to the planes that are designed on the surface.

ECSS-Q-ST-70-60_1390836

g. After localisation samples should be microsectioned to determine the cause of a breach of insulation resistance.

NOTE It is good practice to perform visual inspection on test rack, PCB sample connector footprint and test pattern surface area to verify that breach of insulation is not caused by surface effects, such as dendritic growth. To mitigate this risk, it is possible to apply a coating on the test pattern surface layers, such as conformal coating, solder mask or potting. On the connector footprint this risk is mitigated by only using every second connector.

9.7.3.4 Acceptance criteria

ECSS-Q-ST-70-60_1390520

a. A sudden drop in resistance by an order of magnitude shall be breach of insulation.

NOTE 1 Breach of insulation can occur intermittent or continuous. Examples of stable insulation and breach of insulation are shown in Figure 9-12. Breach of insulation during the first ambient phase or the pre-conditioning phase are considered early failures for which CAF cannot be the failure mechanism.

NOTE 2 An insulation threshold below 0,1 GΩ is typically considered a breach of insulation. However, such absolute threshold depends on the sensitivity of the sample design.

ECSS-Q-ST-70-60_1390521

b. Nonconformances caused by breach of insulation shall be evaluated by the qualification authority and by the procurement authority for the HDI technology under evaluation.

NOTE The test patterns have an increasingly complex design. Failure of a specific pattern can be attributed to the small spacing or the specific via configuration. It is good practice to evaluate the representativity of the failed pattern to the used HDI design. For instance, the ECSS A4 and ECSS B4 patterns are considered to be most representative to HDI designs for space and are not expected to fail. In contrast, IPC pattern A1 is designed with significantly less insulation distance than specified in ECSS-Q-ST-70-12 and can therefore be expected to show failures.

9.8 Group 6 – Assembly and life test - short

9.8.1 Overview

Group 6 includes a lower number of 200 thermal cycles with a higher temperature range of 200 °C. It does not include electrical testing and peel strength. This thermal cycling method is quicker to perform and has heritage from ECSS-Q-ST-70-10. The group 6 is performed for delta qualification or project qualification, in case it is not necessary to cover the general assembly verification.

The test levels for thermal cycling are not only driven by space environment. Thermal cycling to the levels specified in clauses 9.6.2 and 9.8.2 provide reference to the heritage test levels that assess robustness of the PCB construction.

To avoid nonconformances after group 6 for inherently weaker PCB technology, it is good practice to use group 4 test flow.

See clause 9.6.1 for an overview of group 4.

9.8.2 Test flow for group 6

ECSS-Q-ST-70-60_1390522

a. The test vehicle for group 6 shall include the PCB.

NOTE A PCB with a nonconformance on external layers identified by visual inspection can be selected as test vehicle. In case the nonconformance to visual inspection criteria is not associated to thermal stress and clearly identified on the test vehicle prior to the test, it can be evaluated as a conform test result.

ECSS-Q-ST-70-60_1390837

b. The test vehicle for group 6 may include additional coupons.

ECSS-Q-ST-70-60_1390523

c. The following test steps shall be performed for group 6 in this order:

1. bake-out in conformance with clause 9.2.2;
2. reflow simulation in conformance with clause 9.8.3;
3. rework simulation on at least 2 PTH of the PCB in conformance with clause 9.5.4 and requirement 9.5.4.2e;
4. rework simulation on at least 2 via-in-pad on top side and 2 via-in-pad on bottom side of the PCB in conformance with requirement 9.5.4.2f;
5. thermal cycling in conformance with clause 9.8.4;
6. microsectioning in conformance with clause 9.5.2;
7. evaluation of acceptance criteria in conformance with clause 10.

NOTE Via-in-pad can include blind vias or microvias.

ECSS-Q-ST-70-60_1390524

d. Microsectioning and evaluation in conformance with 9.8.2c.6 and 9.8.2c.7 shall be performed on the following:

   1. The PTH and via-in-pad of the PCB that have been subjected to rework simulation;
   2. All technology features under qualification.

ECSS-Q-ST-70-60_1390838

e. In case of project qualification, the reflow simulation and rework simulation may be tailored to be representative of the assembly processes.

ECSS-Q-ST-70-60_1390525

f. In case of project qualification, the reflow simulation and rework simulation shall be representative of the worst-case assembly processes.

   NOTE Assembly processes include initial assembly by hand and machine soldering, as well as rework and repair.

ECSS-Q-ST-70-60_1390839

g. In case of project qualification with specific environmental requirements, the thermal cycling may be tailored.

   NOTE 1 Specific environmental requirements can include operational temperature below -55 °C or above +85 °C, for instance for detector technology that is exposed to planetary environment.

   NOTE 2 It is not good practice to reduce the temperature range or number of cycles because thermal cycling is not only a simulation of space environment. It also simulates equipment on/off cycles and it is considered a general assessment of PCB robustness.

ECSS-Q-ST-70-60_1390840

h. In case of project qualification on a PCB technology with only SMT pads and no PTH, the rework may be tailored to be performed on the SMT pads.

9.8.3 Reflow simulation

ECSS-Q-ST-70-60_1390526

a. Reflow simulation shall be performed using a vapour phase equipment and process that are representative of assembly, except for the case in requirement 9.8.3b.

ECSS-Q-ST-70-60_1390841

b. In case reflow simulation is used for a specific project qualification that uses another assembly method than vapour phase, the test method may be tailored to be representative.

ECSS-Q-ST-70-60_1390527

c. The test board shall be lowered into the vapour phase at a peak temperature and duration that is representative of assembly processes.

NOTE Typical vapour phase processes are using a peak temperature of minimum 215 °C, up to 230 °C. It is good practice to use the reflow profile of IPC-TM-650 test method 2.6.27, in case this is representative.

ECSS-Q-ST-70-60_1390528

d. <<deleted>>

ECSS-Q-ST-70-60_1390529

e. The sample shall be cooled at ambient temperature for at least 10 minutes.

ECSS-Q-ST-70-60_1390530

f. After cool down, the sample shall be exposed to a second reflow by repeating the steps from requirements 9.8.3c, 9.8.3d and 9.8.3e.

9.8.4 Thermal cycling

ECSS-Q-ST-70-60_1390531

a. Thermal cycling shall be performed in a one chamber system with ambient pressure.

ECSS-Q-ST-70-60_1390532

b. A temperature sensor shall be in contact with the test vehicle to monitor its temperature continuously.

ECSS-Q-ST-70-60_1390533

c. The rate of temperature change shall not exceed 10 °C/minute.

ECSS-Q-ST-70-60_1390534

d. The dwell time at minimum and maximum temperature shall be at least 15 minutes.

ECSS-Q-ST-70-60_1390535

e. The cycling programme shall start with the hot cycle first.

ECSS-Q-ST-70-60_1390842

f. The temperature should be minimum -60 °C and maximum +140 °C.

ECSS-Q-ST-70-60_1390536

g. The minimum temperature shall be between -55 °C and -70 °C.

NOTE This covers the assembly verification in conformance with requirement 14.11d. of ECSS-Q-ST-70-61.

ECSS-Q-ST-70-60_1390537

h. The maximum temperature shall be between +130 °C and +145 °C.

NOTE The Tg of laminates is typically higher than this temperature.

ECSS-Q-ST-70-60_1390538

i. The temperature range shall be at least 200 °C.

ECSS-Q-ST-70-60_1390539

j. The number of cycles shall be 200.

10 Acceptance criteria

10.1 Overview

The tables in this clause specify the technological features under evaluation. They include an identification by a reference letter, as specified in clause 4.3. The tables specify "Acceptance criteria" for the "Technological features", as well as the "Procurement inspection sample" and the "Measurement method".

The tables identify which sample is inspected for procurement. In addition other samples can be available for procurement, such as "set 2" in clause 10.2. The acceptance criteria in these tables are also applied to the other samples for procurement and qualification inspection samples.

The inspection sample includes a description of the condition, such as AR, RW, SB. In case this condition is placed in brackets, it indicates that vias with the condition in brackets are present on the coupon and are available for inspection for the technological feature, but the condition in brackets holds no relevance for the evaluation of the technological feature. This is the case for defects associated with PCB manufacture and present in AR condition when these defects are evaluated on a coupon after thermal stress that does not cause alteration of the defect.

Illustrations of measurements methods and acceptance criteria are given in photographs and drawings in the notes of the tables from clauses 10.2 to 10.4.

10.2 Inspection by microsectioning for dimensional verification

ECSS-Q-ST-70-60_1390540

a. For the technological feature internal annular ring, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-1.

ECSS-Q-ST-70-60_1390541

b. For the technological feature external annular ring, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-2.

ECSS-Q-ST-70-60_1390542

c. For the technological feature copper foil thickness, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-3.

ECSS-Q-ST-70-60_1390543

d. For the technological feature copper plating thickness, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-4.

ECSS-Q-ST-70-60_1390544

e. For the technological features etchback and glass fibre protrusion, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-5.

ECSS-Q-ST-70-60_1390545

f. For the technological feature wicking, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-6.

ECSS-Q-ST-70-60_1390546

g. For the technological feature wrap copper, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-7.

ECSS-Q-ST-70-60_1390547

h. For the technological feature dielectric thickness for standard technology. The acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-8.

ECSS-Q-ST-70-60_1390548

i. For the technological feature dielectric thickness for microvia layers, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-9.

ECSS-Q-ST-70-60_1390549

j. For the technological features microvia dimensions and aspect, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-10.

ECSS-Q-ST-70-60_1390550

k. For the technological feature microvia plating voids, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-11.

ECSS-Q-ST-70-60_1390551

l. For the technological features tin-lead thickness and composition, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-12.

ECSS-Q-ST-70-60_1390552

m. For the technological features electrolytic nickel and gold dimensions, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-13.

ECSS-Q-ST-70-60_1390553

n. For the technological feature undercut, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-14.

ECSS-Q-ST-70-60_1390554

o. For the technological feature overhang, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-15.

ECSS-Q-ST-70-60_1390555

p. For the technological feature dimensional verification of the rigid-flex interface the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-16.

ECSS-Q-ST-70-60_1390893

q. For the technological feature dimensional verification of backdrilling the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-17.

ECSS-Q-ST-70-60_1390556

Table 10-1: Annular ring internal

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Inner layer	≥ 50 µm	Location: coupon A/B + Bn Condition: set 1 AR(+RW) + set 2 Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Lighting: bright field Measure as shown in Figure 10-1. Measure at the foot of the pad, except for microvias. Measure innerlayer pad from the hole wall. Measure excluding plated copper.
b.	Inner layer at end of blind via	≥ 50 µm		
c.	Inner layer at end of buried via	≥ 50 µm		
d.	Microvia internal landing pad	≥ 0 µm (tangency) at the top of the pad		
e.	Inner layer in conformance with 10.6.1d	≥ 25 µm	Location: electrical registration in 4 corners Frequency: per panel	

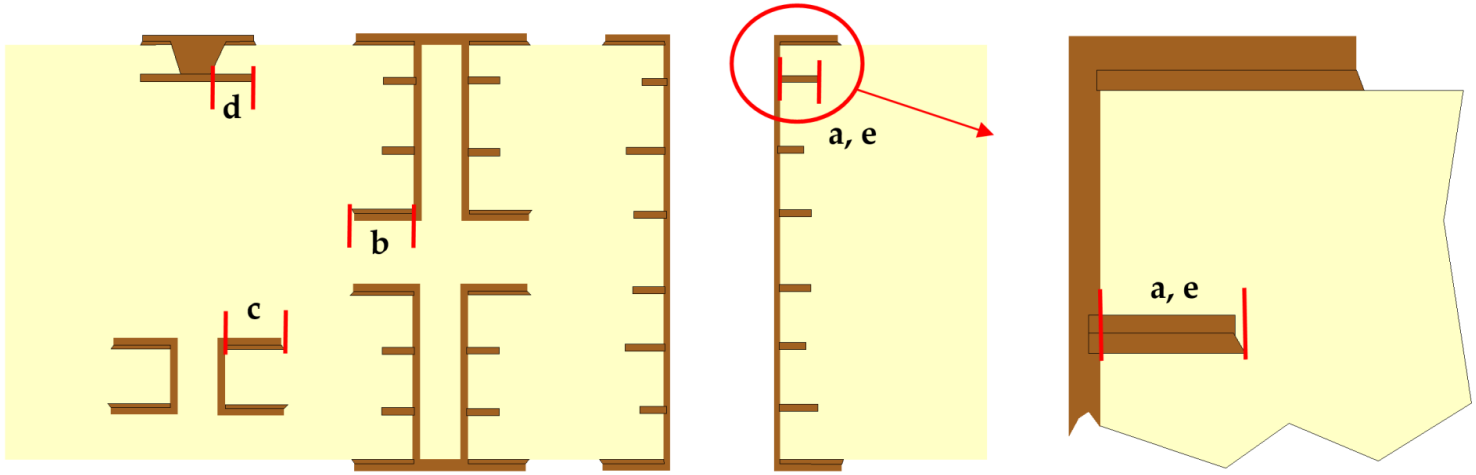


Figure 10-1: Annular ring internal

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method

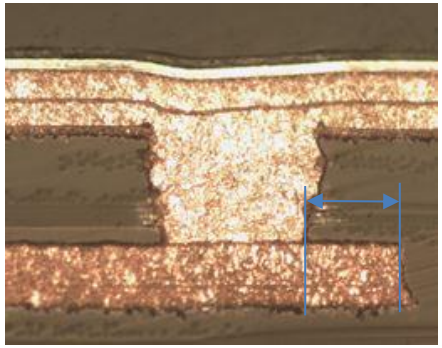


Figure 10-2: Microvia annular ring of internal landing pad

Note: Ref d ensures that the interface between internal landing pad and microvia plating is on the horizontal surface.

Table 10-2: Annular ring external

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Outer layer	≥ 100 µm	Location: coupon A/B + Bn Condition: set 1 AR(+RW) + set 2 Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Lighting: bright field Measure as shown in Figure 10-3. Measure at the foot of the pad. Measure excluding plated copper for Ref. f. For all other references, measure including plated copper.
b.	Outer layer PTH solder side	≥ 200 µm		
c.	Outer layer PTH solder side only for rigid polyimide	≥ 130 µm		
d.	Outer layer PTH only for flex termination	≥ 250 µm on component hole ≥ 100 µm on non-soldering hole		
e.	Outer layer blind via	≥ 100 µm		
f.	(Buried) microvia external capture pad	≥ 10 µm		
g.	Non-plated hole outer layer	≥ 250 µm		
h.	Outer layer PTH solder side for oblong pads	≥ 100 µm		

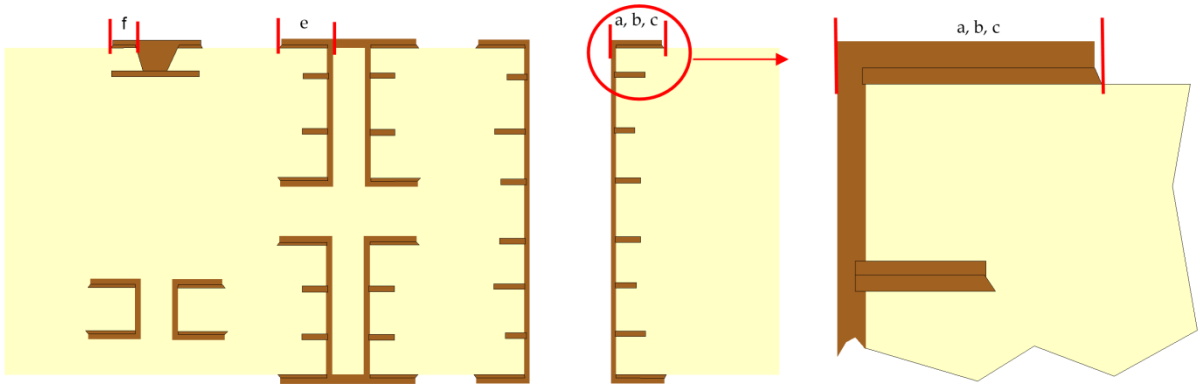


Figure 10-3: Annular ring external

Note 1: Annular ring on outer layer as specified in Ref. a from Table 10-2, includes vias and PTH on component side for rigid, rigid/flex and flex technology.
Note 2: For Ref. g., annular ring is measured similar as for Ref. a., except that no plated copper will be present in the non-plated hole.
Note 3: For Ref h, oblong pads are specified in clause 7.5.3 of ECSS-Q-ST-70-12.

Table 10-3: Copper foil thickness

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
	Nominal copper foil thickness	**Minimum measured copper foil thickness after processing**		
a.	70 µm	≥ 56 µm	Location: coupon A/B + Bn Condition: set 1 AR(+RW) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x for Ref. a, b ≥ 400x for Ref. c, d, e Illumination: bright field Measure as shown in Figure 10-4.
b.	35 µm	≥ 25 µm		
c.	17 µm	≥ 11 µm		
d.	12 µm for HDI	≥ 9 µm		
e.	9 µm for HDI	≥ 6 µm		

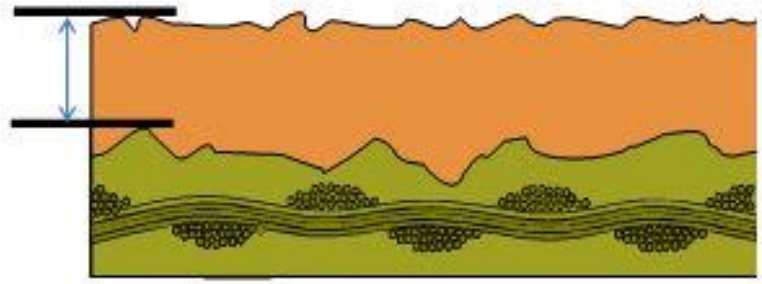


Figure 10-4: Copper foil thickness

The microetching and passivation on the top surface is not subtracted from the thickness measurement.

The treatment on the bottom surface to the laminate is subtracted from the thickness measurement.

Note 1: The equivalent IPC test method is described in IPC-A-600K test method 3.2.4 and IPC-6012F chapter 3.6.2.15

Note 2: This is also specified in Table 7-1 of ECSS-Q-ST-70-12.

Table 10-4: Copper plating thickness

Ref.	Technological feature		Acceptance criteria	Procurement inspection sample	Measurement method
a.	Electroplated copper in PTH, through going vias, blind vias, buried vias	Rigid	≥ 25 µm in zone A on resin ≥ 20 µm in zone B on any local thin area on resin or glass	Location: coupon A/B + Bn Condition: set 1 AR(+RW) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field Measurement in zone A on resin and in zone B on any local thin area on resin or glass are performed as shown in Figure 10-6. The evaluation is performed on 3 locations as shown Figure 10-5.
b.		Flexible	≥ 25 µm in zone A on resin ≥ 20 µm in zone B on any local thin area on resin or glass		
c.		Rigid-flex	≥ 30 µm in zone A on resin ≥ 25 µm in zone B on any local thin area on resin or glass		
d.	Core vias for Polyimide HDI		≥ 30 µm in zone A on resin ≥ 25 µm in zone B on any local thin area on resin or glass See note 6		
e.	Electroplated copper over base copper for layers with plated holes		≥ 25 µm		
f.	Electroplated copper over base copper for internal layers with only microvias		≥ 5 µm		
g.	Electroplated copper in non-filled microvias		≥ 25 µm on resin ≥ 20 µm on any local thin area on glass		

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method

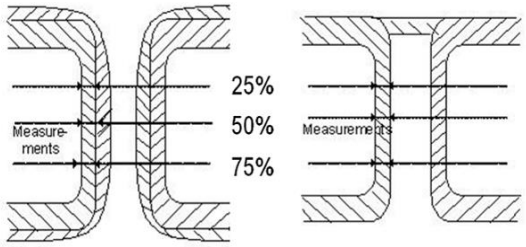


Figure 10-5: Three measurements of copper plating thickness at locations that are at 25 %, 50 % and 75 % of the height of the hole.
The thickness requirements of this table apply to each individual location.

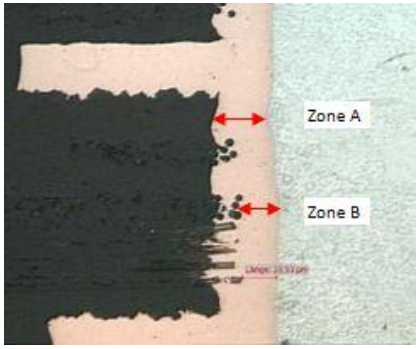


Figure 10-6: Illustration of measurement in zone A on resin and in zone B on any local thin areas on resin or glass.

Note 1: There is no additional requirement for total copper thickness on surface. As an example for Ref. e. min copper foil after processing is 11 µm, plus 25 µm plated copper, results in min 36 µm total copper thickness for standard technology.

Note 2: Ref. e. is specified for the total layer thickness of plated layers. Individual plating sequences can be less than 25 µm, for instance if they are planarized or if several plating steps are performed.

Note 3: Coupon A/B includes the minimum via diameter in conformance with requirement 15.2d.6 from ECSS-Q-ST-70-12 which is verified for copper plating thickness as the inspection from this table.

Note 4: Ref. f. is specified for internal layers only because on external layers plated holes will be present in all cases. The value of 5 µm is derived from the Ref. a. for copper wrap in Table 10-7.

Note 5: The local roughness of the copper plating in zone A caused by surface treatment or hole wall roughness is not accurately measured by this method.

Note 6: For standard polyimide materials the qualified domain at the time of issuing the revision 1 of this standard includes ≥ 35 µm in zone A and ≥ 30 µm in zone B.

Table 10-5: Etchback and glass fibre protrusion

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Etchback	Between negative -13 µm and positive +20 µm	Location: coupon A/B + Bn Condition: set 1 AR(+RW) Frequency: per panel	Microsection and Microscope: Magnification: x200 min Illumination: bright field
b.	Glass fibre protrusion, in case of negative etchback	Glass fibres should protrude into hole wall relative to the resin		
c.	Glass fibre protrusion, in case of positive etchback	Glass fibres should protrude into hole wall relative to the inner layer		
d.	Glass fibre protrusion	Glass fibre protrusion should be limited such that the requirement for minimum Cu plating thickness is achieved.		

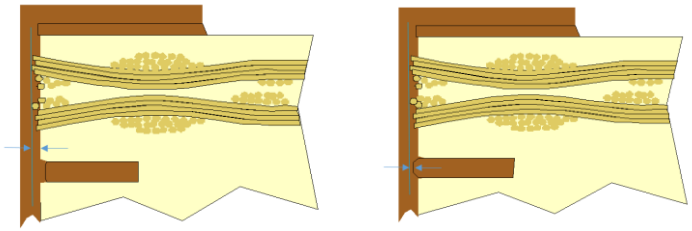


Figure 10-7: Glass fibre protrusion in case of negative etchback (left) and positive etchback (right)

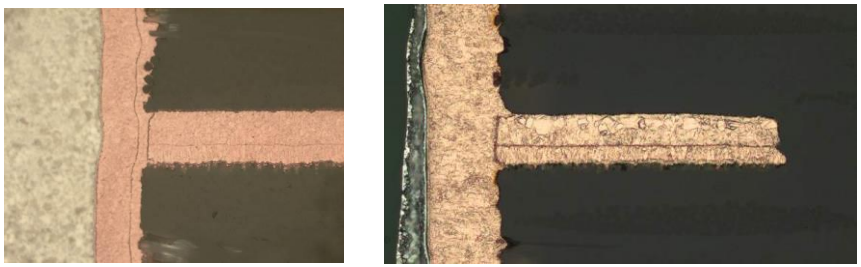


Figure 10-8: Example of negative etchback (left) and approximately neutral etchback (right)

Note 1: Glass fibre protrusion is a qualitative assessment of the general aspect of the hole. A single occurrence outside requirement is not a nonconformance if the general aspect meets the requirement.

Note 2: Etchback is the distance from resin of hole wall to innerlayer foil. It can be both positive or negative depending on the processes used.

Table 10-6: Wicking

Ref.	Technological feature	Acceptance criteria	Sample	Measurement method
a.	Wicking	≤ 50 µm	Location: coupon A/B + Bn Condition: set 1 AR(+RW) Frequency: per panel	Microsection and Microscope: Magnification: x200 min Lighting: bright field Wicking is measured from the resin of the hole wall.
b.	Wicking on reduced annular ring of ≥ 25 µm	≤ Min annular ring measured on that microsection		

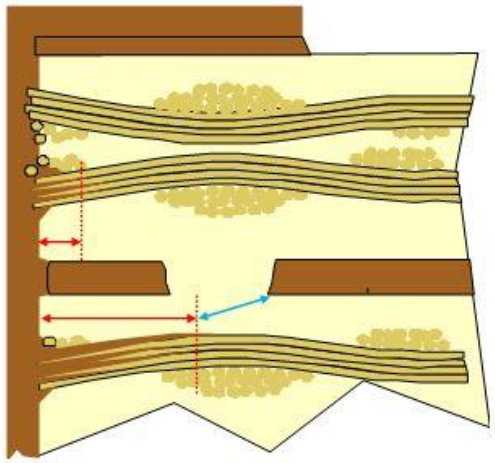


Figure 10-9: Wicking is measured from resin of hole wall (red arrows). In case it exceeds the annular ring, the insulation distance to adjacent circuitry (blue arrow) can be reduced.

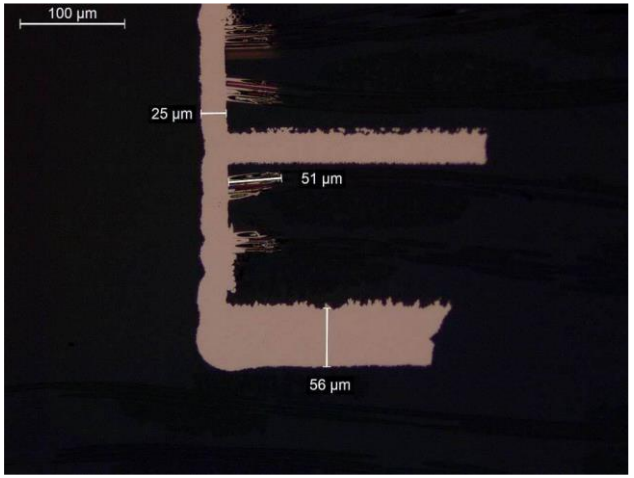


Figure 10-10: Example of wicking

Table 10-7: Wrap copper

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Copper wrap thickness for (micro)vias	≥ 5µm wrap thickness	Location: coupon Bn Condition: set 1 AR (+RW) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field Measure wrap thickness as per red arrows Measure wrap length as per blue arrow
b.	Copper wrap thickness for microvias with copper filling and cap plating	no wrap is acceptable		
c.	Copper wrap length	≥ 25µm for vias ≥ 10 µm for microvias		

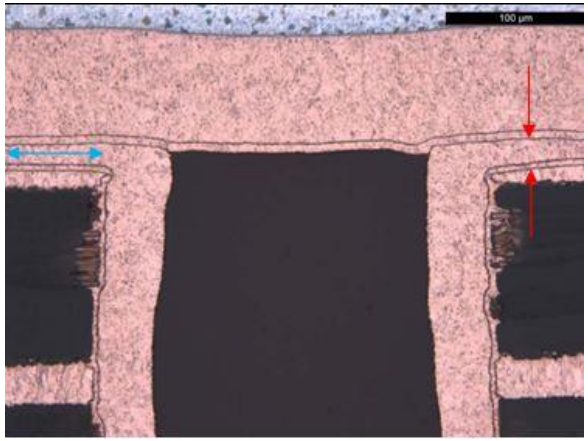


Figure 10-11: Wrap target condition

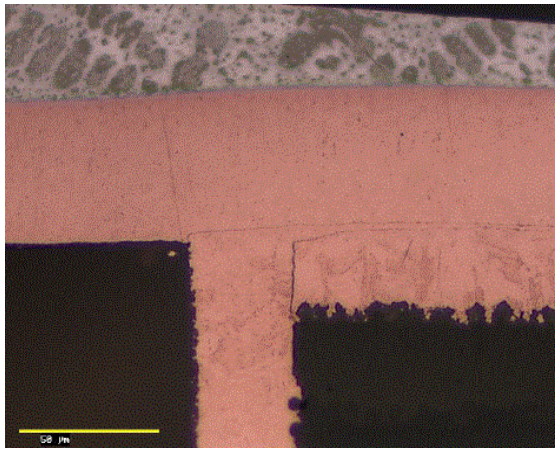


Figure 10-12: Wrap thickness below requirement, not acceptable

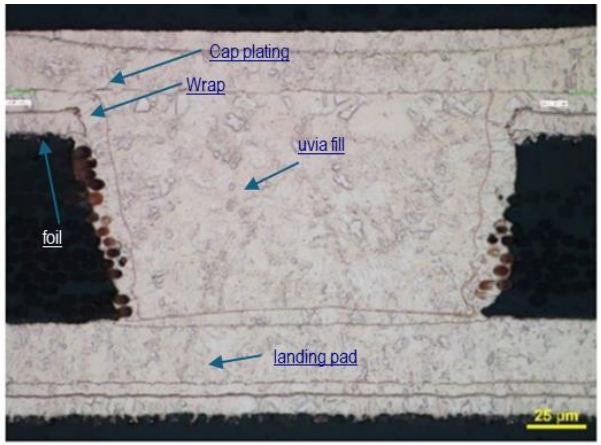


Figure 10-13: Example of microvia wrap, fill and cap plating

Note 1: Planarization or selective plating can be in the PCB manufacturer's PID, if the copper wrap criteria from this table are met. Insufficient wrap copper indicates too much planarization. This can cause separation in plating layers due to lack of mechanical strength.

Note 2: Wrap is important to ensure good adhesion of plated copper to surface foil. In case microvias are button plated and planarized, the wrap can be reduced or absent. Subsequent overplating (cap plating, panel plating) still ensures the reinforcement.

Table 10-8: Dielectric thickness – standard technology

Ref.	technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Insulation between layers	≥ 70 µm for rigid ≥ 22,5 µm for flex	Location: coupon A/B + Bn Condition: set 1 AR(+RW) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field
b.	Number of prepreg between layers	≥ 2		
c.	Number of glass layers in laminate	should be ≥ 2, i.a.w. ECSS-Q-ST-70-12 requirement 7.1.3b.		
d.	Glass fibre compression	not acceptable in case track is compressed into glass bundle and resin starvation occurs		

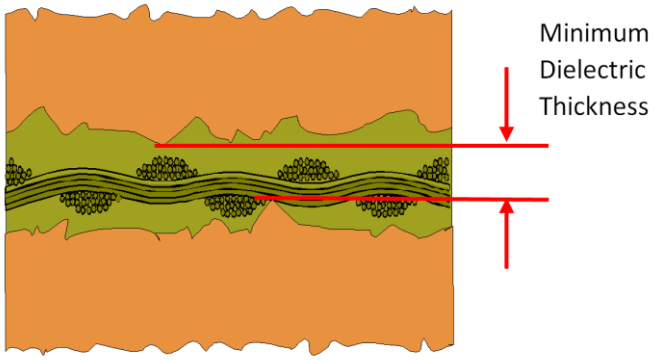


Figure 10-14:Projected-peak-to-peak insulation

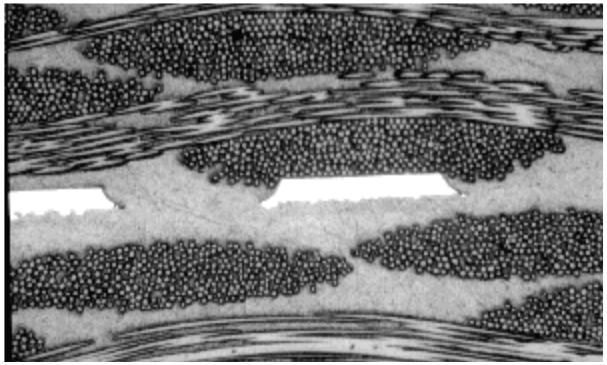


Figure 10-15: Example of glass compression

Table 10-9: Dielectric thickness – microvia layers

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Insulation between layers	≥ 60 µm ≤ 120 µm for microvia diameter of 175 µm	Location: coupon Bn Condition: set 1 AR(+RW) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field
b.	Number of prepreg	2		
c.	Penetration of internal landing pad	Complete penetration through pad not acceptable		

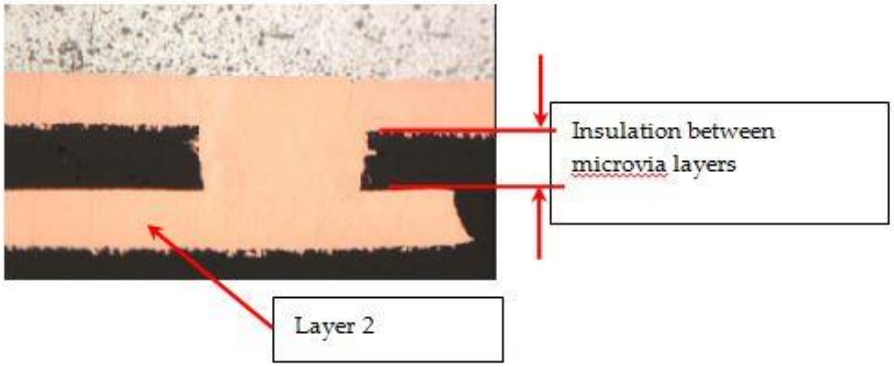


Figure 10-16: Microvia insulation

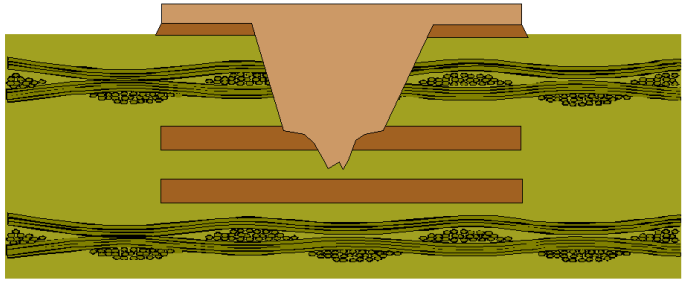


Figure 10-17: Penetration of internal landing pad for µvia, not acceptable

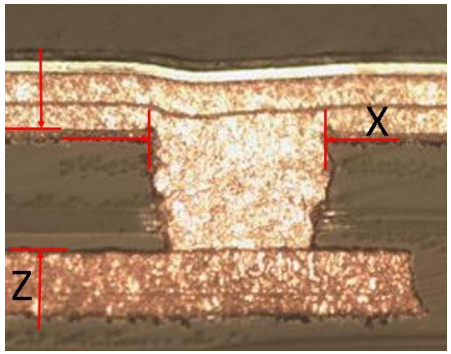
Note 1: Dielectric thickness of approximately 60 µm can create a risk for glass compression. The maximum of 120 µm is used to accommodate 20 % tolerance on the maximum as-designed thickness of 100 µm, in conformance with req 11.4i. from ECSS-Q-ST-70-12. The maximum thickness is in addition limited by the requirement for aspect ratio ≤ 0,8 of microvias, in conformance with Ref. c. from Table 10-10. In case of high dielectric thickness there can be a risk not to meet the contact diameter (e.g. 100 µm) in conformance with Ref. d. from Table 10-10.

Note 2: ECSS-Q-ST-70-12 requirement 11.4.1k states a permission for using 1 sheet of prepreg and a dielectric thickness of ≥ 40 µm. It also states in its note 1 that a qualification has not yet been performed. Therefore, this option is not included as an acceptance criterion in this table.

Table 10-10: Dimension and aspect of microvias

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Dimple on external layer	≤ 30 µm	Location: coupon Bn Condition: set 1 AR(+RW) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field Planarity is measured at the top of the copper surface
b.	Bump on external layer	≤ 15 µm		
c.	Aspect ratio	≤ 0,8 ECSS-Q-ST-70-12 req. 11.4.2a.2		
d.	Contact diameter to internal landing pad	≥ 50% of the drill diameter at internal landing pad, as per IPC-2226 chapter 5.1 and Table 5-1. The contact to internal landing pad shall be continuous.		

See Table 10-29 for interconnect defect and corner cracks in microvias



X=laser drilled diameter in layer 1 base copper, Z=distance from top of layer 1 base copper to top of internal landing pad copper

Figure 10-18: Microvia aspect ratio, X ≥ Z

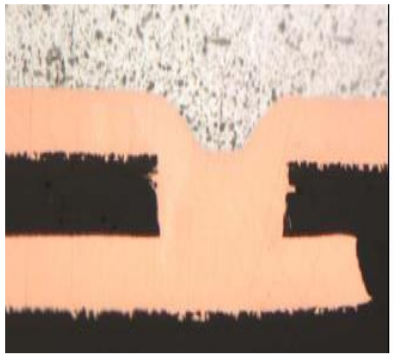


Figure 10-19: Dimple in microvia

Note 1: Microvias can show resin or glass at the bottom edge. This is not considered a defect in case continuous contact is achieved. Presence of dielectric material is not considered ICD.

Note 2: The aspect ratio of max 1 causes a limitation for the maximum thickness of insulation.

Note 3: The dimple and bump feature is not specified for buried staggered microvias. In case of stacked microvias it can be important to have a planar surface. This is not covered by Polyimide HDI technology as per table 11-1 of ECSS-Q-ST-70-12 and therefore not specified.

Table 10-11: Microvia plating voids

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Void inside copper filled microvia	Target condition: no voids. Systematic voids are unacceptable Incidental voids acceptable if all of the following conditions are met: • Less than 25 % of the copper filling area in the cross-section • Minimum copper plating thickness on resin as per ref G of Table 10-4.	Location: coupon Bn Condition: set 1 AR+RW, set 2 SB Frequency: per panel See 10.6.3b for the footprint where this inspection is performed.	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field

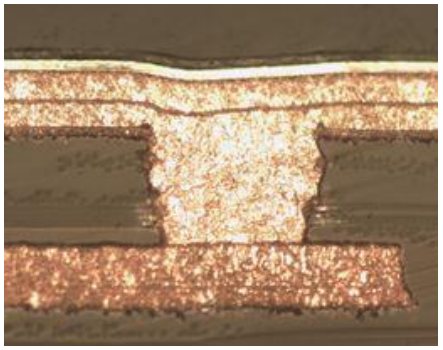


Figure 10-20: Microvia plating, target condition

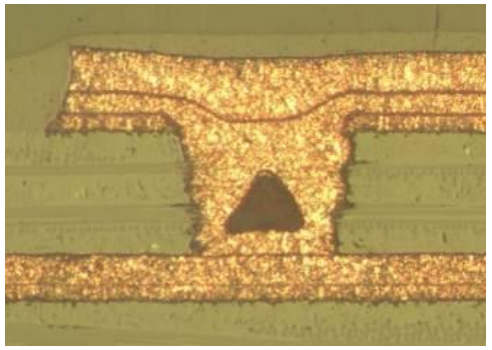


Figure 10-21: Example of void in microvia plating

Note 1: Allowance for voiding is specified in this table for a relatively low sample size as done for procurement. In qualification a larger sample size is taken to verify that the target condition is achieved.

Note 2: Voids in copper filling are typically of spherical or triangular shape.

Note 3: To demonstrate that voids are incidental, the IST coupon with microvias can be microsectioned.

Table 10-12: Tin-lead thickness and composition

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	SnPb composition	Tin content 63±8% by weight	Location: coupon A/B Condition: set 1 AR(+RW) Frequency: per panel	Ref. a: XRF, SEM-EDX, atomic absorption spectrometry on bare PCB Ref. b, c, d, e: Microsection and Microscope: Magnification: ≥ 200x for Ref. b, c, e ≥ 500x for Ref. d Illumination: bright field
b.	SnPb thickness on SMT pads	≥ 5 µm on thickest area		
c.	SnPb thickness on PTH hole wall	≥ 8 µm on thickest area		
d.	SnPb thickness on PTH corners	≥ 1 µm excluding the IMC OR < 1 µm acceptable in case all of the following conditions are met: • SnPb present on top of IMC • acceptable solderability i.a.w. 9.4.11		
e.	SnPb thickness on PTH pads	≥ 5 µm OR < 5 µm acceptable in case all of the following conditions are met: • SnPb present on top of IMC • acceptable solderability i.a.w. 9.4.11		

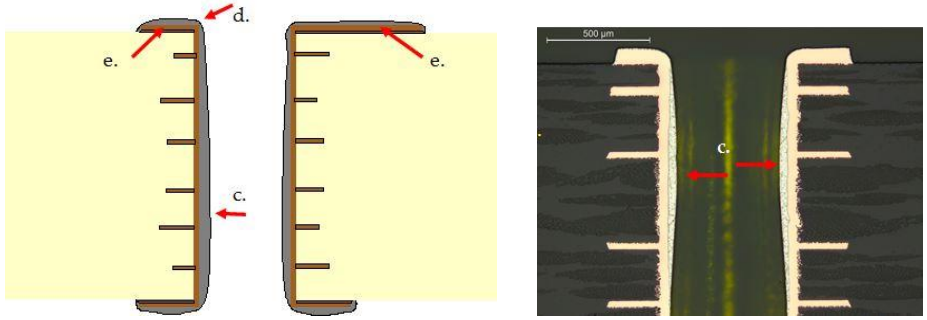


Figure 10-22: Tin-lead thickness in PTH schematic (left) and a typical microsection (right)

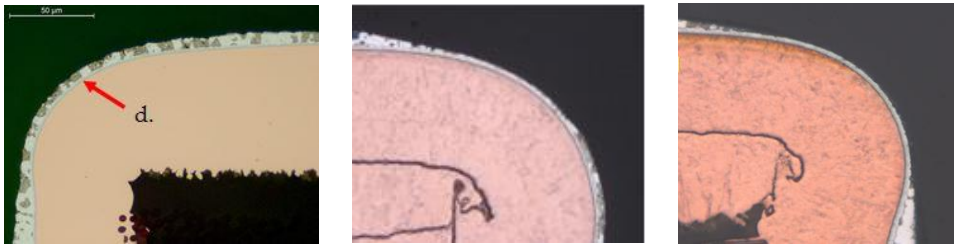
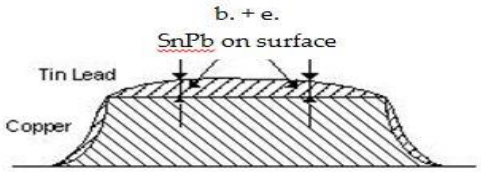


Figure 10-23: Tin-lead thickness on PTH corner – target thickness (left), coverage of less than 1 µm (middle), absence of SnPb on IMC (right)



Measurement is done in centre of pad, at the thickest area.

Figure 10-24: Tin-lead thickness on pad

Note 1: Ref. d allows for less than 1 µm SnPb thickness as long as the IMC is covered by SnPb and acceptable solderability test is obtained.

Note 2: For SMT assembly it can be important to have a SnPb thickness variation of less than 25 µm to ensure planarity. This can be important within the same SMT footprint for dedicated devices, but it is considered less important among different footprints of the PCB. This aspect depends on the design of the footprint that can have SMT pads with or without through-going vias adjacent to it. In case the customer needs to specify planarity of SnPb finish on SMT footprints, it is good practice to include this in the PCB definition dossier.

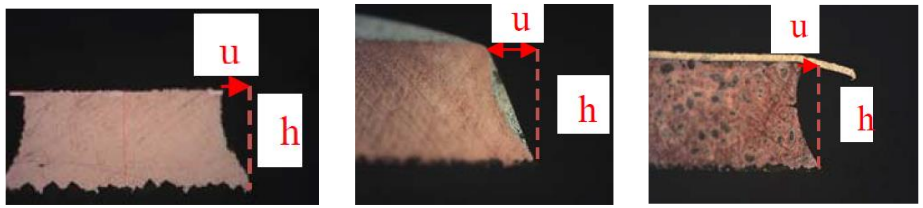
Table 10-13: Dimensional requirements for electrolytic and chemical Ni, Pd, Au

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Electrolytic nickel	≥ 2 µm on all locations, and ≤ 10 µm on hole wall	Location: PCB or coupon A/B or dedicated coupon Condition: AR Frequency: per panel	XRF on PCB, or Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field
b.	Electrolytic gold on nickel	≥ 1 µm		
c.	Electrolytic gold on copper	≥ 3 µm		
d.	Length of tin-lead overlap on Au	≥ 150 µm		
e.	ENIG	Ni 3-6 µm Au 0,04-0,1 µm	1,5x1,5 mm² as per IPC-4552A Frequency: per panel	XRF as per IPC-4552A Frequency: per panel
f.	ENEPIG	Ni 4-6 µm Pd 0,05-0,25 µm Au 0,03-0,08 µm	1,5x1,5 mm² as per IPC-4556 Frequency: per panel	XRF as per IPC-4556 Frequency: per panel
g.	ENIPIG	Ni 3-7 µm Pd 0,01-0,045 µm Au 0,03-0,08 µm	1,5x1,5 mm² as per IPC-4556 Frequency: per panel	XRF as per IPC-4556 Frequency: per panel

Note 1: It is not good practice to use gold as surface finish for soldering as per clause 6.6.2 of ECSS-Q-ST-70-61.
Note 2: Tin-lead overlap as –designed is 200 µm as per see 7.8.1d.1 of ECSS-Q-ST-70-12
Note 3: For Ref. a. no max on surface is specified
Note 4: For Ref. d. and c. no max is specified
Note 5: For Ref. e., f. and g. the thickness values are derived from IPC-4552B, IPC-4556, chemistry supplier recommendations and plating company recommendations.

Table 10-14: Undercut and spurious copper

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Undercut on internal layers	u ≤ h	Location: coupon A/B + Bn Condition: set 1 AR(+RW) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field
b.	Undercut on external layers reflowed Sn/Pb finish	u ≤ h		
c.	Undercut on external layers Electrolytic Ni/Au or Au finish	u ≤ h		
d.	Spurious copper	Incidental occurrence of copper from the rough side of the foil is acceptable if < 10 µm		



Ref. a Ref. b Ref. c

Figure 10-25: Undercut

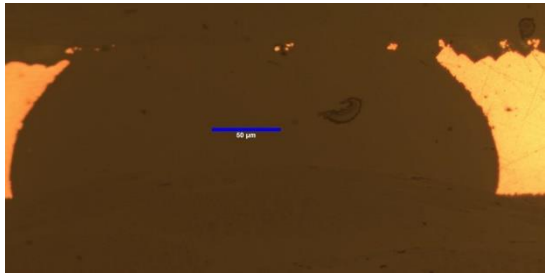


Figure 10-26: Example of spurious copper

Note Spurious copper can be caused by inefficient etching. This is not the same as copper residue as described in Table 10-43.This is not the same as dotted interface line as described in Ref. e of Table 10-34.

Table 10-15: Overhang

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Overhang on reflowed Sn/Pb finish	No overhang	Location: coupon A/B + Bn Condition: set 1 AR Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field
b.	Overhang on electrolytic Ni/Au or Au finish	D ≤ 2x total thickness of copper (h) in case of conformal coating as per 10.6.3j		

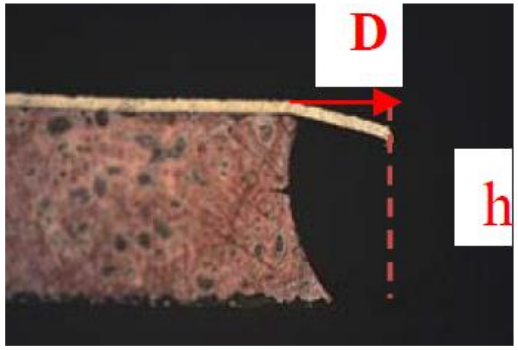


Figure 10-27: Overhang of electrolytic Au

Note: For Tin-lead finish during the reflow operation the overhang of Tin-lead is flowing on the side of the tracks or pads: if the reflow operation has been well conducted there is no overhang left.

Table 10-16: Rigid-flex interface -dimensional verification

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Coverlay and bond-ply insertion into rigid section i.a.w. ECSS-Q-ST-70-12 req. 9.4c.	≥ 1 mm	Location: rigid-flex coupon Condition: set 6 SB Frequency: per panel	Microsection and Microscope Magnification: 50-200x Illumination: bright and dark field
b.	Distance between hole wall and rigid edge of interface, i.a.w. ECSS-Q-ST-70-12 req. 9.5a.	≥ 2mm		
c.	Overlap between coverlay and pad, i.a.w. ECSS-Q-ST-70-12 req. 9.4e.	Not acceptable		

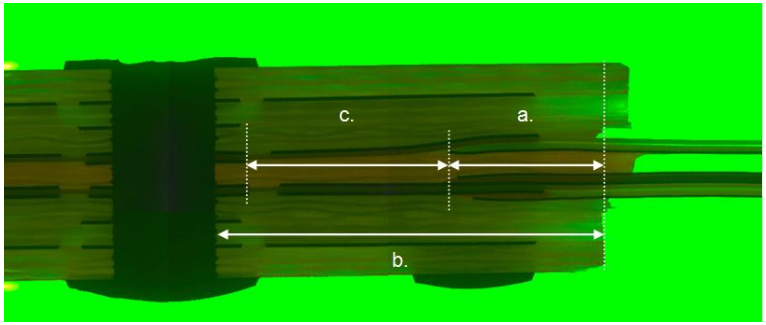


Figure 10-28: Example of dimensional verification of rigid-flex interface

Note 1: In case coverlay insertion into rigid section is 2 mm and distance between hole wall and rigid edge is 2mm then the coverlay overlaps the pad and requirement is not achieved. Requirement 9.4d from ECSS-Q-ST-70-12 specifies that in a multilayer rigid-flex PCB where flex laminates are bonded together with bond-ply, the ends of the coverlay and bond-ply are off- set in the rigid section by 1 mm to prevent a line of weakness.

Note 2: Ref. a. and b. are as-manufactured. Ref. a. is derived from 1,5 mm (from ECSS-Q-ST-70-12) as-designed and allowing for 0,5 mm manufacturing tolerance.

Note 3: To achieve ≥ 2 mm distance in Ref. b., it can be necessary to design a larger distance to allow for manufacturing tolerances. Moreover, for complex build-ups a further increase of this distance by design is good practice because tolerances are larger.

Table 10-17: Backdrilling

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Minimum stub length to target layer	50 µm	Location: dedicated B_n coupon Condition: set 1 AR(+RW) + set 2 Frequency: per panel	Microsection and Microscope Magnification: 50-200x Illumination: bright and dark field
b.	Minimum backdrill diameter	Via diameter + 250 µm		
c.	Maximum misalignment between backdrilled part and the rest of the via hole.	+/- 125 µm		
d.	Drilling burrs, loose debris, plating slivers	Acceptable if incidental and not reducing insulation distance		

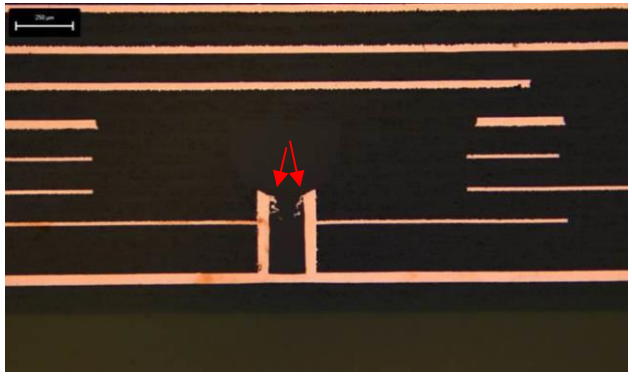


Figure 10-29: Example of backdrilled via with drilling burrs

10.3 Inspection by microsectioning for qualitative aspects

ECSS-Q-ST-70-60_1390572

a. For the technological feature via filling the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-18.

ECSS-Q-ST-70-60_1390573

b. For the technological feature cap lift, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-19.

ECSS-Q-ST-70-60_1390574

c. For the technological feature blind via planarity, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-20.

ECSS-Q-ST-70-60_1390575

d. For the technological features burrs and nodules, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-21.

ECSS-Q-ST-70-60_1390576

e. For the technological features voids and inclusions in copper plating the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-22.

ECSS-Q-ST-70-60_1390577

f. For the technological features wedge voids the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-23.

ECSS-Q-ST-70-60_1390578

g. For the technological feature resin voids, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-24.

ECSS-Q-ST-70-60_1390579

h. For the technological features delamination, blistering, crazing and measling, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-25.

ECSS-Q-ST-70-60_1390580

i. For the technological feature pad lift, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-26.

ECSS-Q-ST-70-60_1390581

j. For the technological feature dielectric cracks, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-27.

ECSS-Q-ST-70-60_1390582

k. For the technological features cracks and separation in copper, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-28.

ECSS-Q-ST-70-60_1390583

l. For the technological feature ICD, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-29.

ECSS-Q-ST-70-60_1390584

m. For the technological feature smear, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-30.

ECSS-Q-ST-70-60_1390585

n. For the technological features hole wall pull away and resin recession, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-31.

ECSS-Q-ST-70-60_1390586

o. For the technological feature nail heading, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-32.

ECSS-Q-ST-70-60_1390587

p. For the technological feature copper-invar-copper, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-33.

ECSS-Q-ST-70-60_1390588

q. For the technological feature inhomogeneity in dielectric, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-34.

ECSS-Q-ST-70-60_1390589

r. For the technological features contamination and foreign inclusions, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-35.

ECSS-Q-ST-70-60_1390590

s. For the technological feature rigid-flex interface delamination between coverlay and prepreg, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-36.

ECSS-Q-ST-70-60_1390591

t. For the technological feature rigid-flex interface adhesive voids in coverlay and bond-ply, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-37.

ECSS-Q-ST-70-60_1390592

u. For the technological feature rigid-flex interface misalignment of prepreg, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-38.

ECSS-Q-ST-70-60_1390895

v. For the technological feature hypercorrosion of ENIG, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-39.

ECSS-Q-ST-70-60_1390896

w. For the technological feature hypercorrosion of ENEPIG and ENIPIG, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-40.

ECSS-Q-ST-70-60_1390897

x. For the technological feature heat sinks and CTE restrictive layers CIC, Molybdenum and ceramic, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-41.

ECSS-Q-ST-70-60_1390593

Table 10-18: Via filling with prepreg resin and plugging paste

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Voids or cracks in the resin of blind , buried or plugged vias inside zone A	Target condition: no voids, no cracks Incidental voids or cracks are acceptable in case the plane of the microsection is filled as follows: • for buried via ≥ 85 % • for plugged via ≥ 85 % • for blind via ≥ 75 % Voids in contact with cap plating, as shown in Figure 10-31, are not acceptable	Location: coupon A/B + Bn Condition: set 1 AR + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field
b.	Voids or cracks in the resin of blind, buried or plugged vias outside zone A	Voids at open ends, as shown in Figure 10-31, are not acceptable.		
c.	Separation between hole wall and resin inside blind and buried via	Not acceptable AR or after SB. Acceptable after group 6 and recorded in PID.		
d.	Voids or cracks in the resin of microvias	Not acceptable		

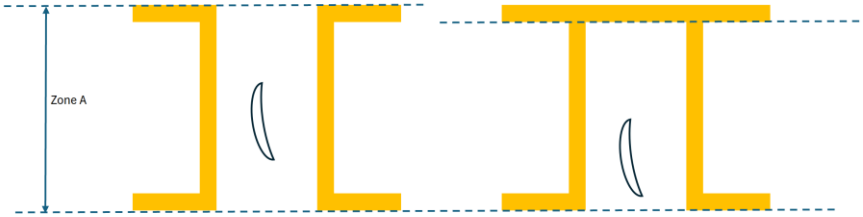


Figure 10-30: Examples of acceptable voids

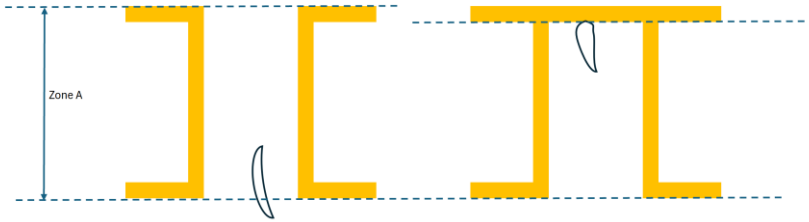


Figure 10-31: Examples of unacceptable voids

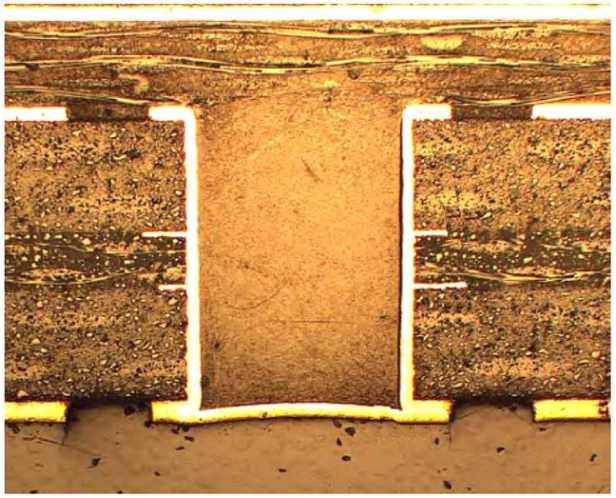


Figure 10-32: Examples of separation between hole wall and resin inside blind via

Note 1: The via filling can be performed by resin flowing from the prepreg or by pre-filling using ink or plugging paste.

Note 2: The figures in this table also apply to cracks.

Note 3: Cracks protruding out of the via are evaluated in conformance with Table 10-27.

Note 4: Voids in zone A can be caused by shrinking. Voids outside zone A can be caused by inadequate filling.

Note 5: Superpositioning of blind vias in PCB is represented in coupons in conformance with requirement 15.2d.5(c) from ECSS-Q-ST-70-12.

Table 10-19: Cap lift on blind via and plugged via

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Cap lift (bulging)	Not acceptable in case via-in-pad are used for soldering as per 6.2.3e	Location: coupon A/B + Bn Condition: set 1 AR + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field
b.	Thin line separation	Acceptable as received and after solder bath float up to 10 µm separation		
c.	Copper surface plating thickness on resin	≥ 25 µm in conformance with Ref. e. from Table 10-4		

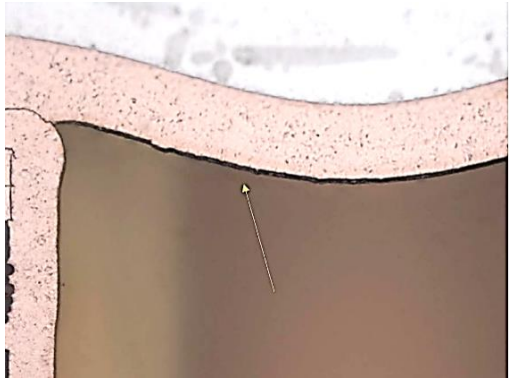


Figure 10-33: Example of acceptable thin line separation

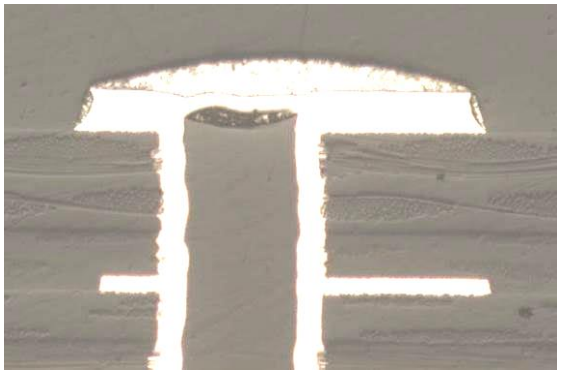


Figure 10-34: Example of non-acceptable bulging

Table 10-20: Blind and plugged via planarity

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Dimple of via on external layers	Depth of dimple ≤ 50 µm Depth of dimple > 50 µm is acceptable in case all of the following conditions are met: • depth of dimple is ≤ 76 µm; • it is a dimple local in the blind or plugged via; • the diameter of the dimple at half of the depth of the dimple is < 10 % of the diameter of the drilled hole. In case the PCB definition dossier specifies that no vias-in-pad are used for soldering in conformance with 6.2.3e, the acceptance criteria for dimple need not to be evaluated.	Location: coupon A/B + Bn Condition: set 1 AR + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field Planarity is measured at the top of the copper surface
b.	Bump on via on external layers	≤ 15 µm		

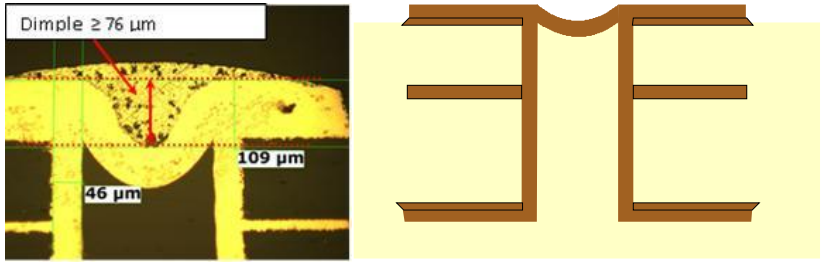


Figure 10-35: Example of dimple on blind via

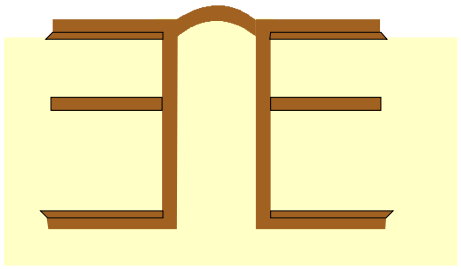


Figure 10-36: Example of bump on blind via

Note 1: Superpositioning of blind vias in PCB is represented in coupons in conformance with requirement 15.2d.5(c) from ECSS-Q-ST-70-12.
Note 2: In case blind vias exceed the requirement on coupons, it is good practice to perform FAI on a PCB in confromance with 15.2b from ECSS-Q-ST-70-12.
Note 3: A drill diameter of ≤ 0,4 mm for blind vias can avoid large dimples.

Table 10-21: Burrs and nodules

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Burrs and nodules	Not acceptable if diameter of plated hole is reduced to below the requirement Not acceptable if detached by probing with a gauge	Location: coupon A/B Condition: set 1 AR+RW, set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field

Figure 10-37: Example of plating nodule

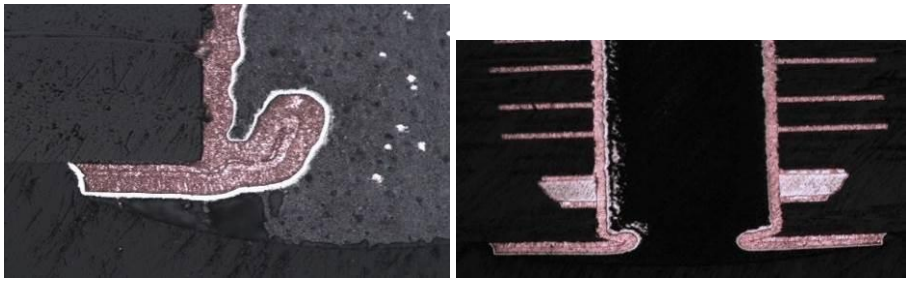


Figure 10-38: Example of burrs reducing hole diameter

Note 1: It is good practice to avoid the presence of burrs and nodules because they can have a negative impact on reliability of the PTH as evaluated in IST.

Note 2: In case the PCB definition dossier does not specify a tolerance of vias, the tolerance of 0,1mm from requirement 6.2.3f.3 is used.

Table 10-22: Voids and inclusions in copper plating

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Voids and inclusions in copper plating	Target condition: no voids, no inclusions Incidental voids and inclusions are acceptable in case: • size ≤ 5 µm • not reducing Cu plating thickness below the requirement of Table 10-4 • embedded within Cu plating layer • not in contact with SnPb	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field
b.	Skip plating	Target condition: no skip plating Incidental skip plating on glass fibres is acceptable. Not acceptable on flex laminate		

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method

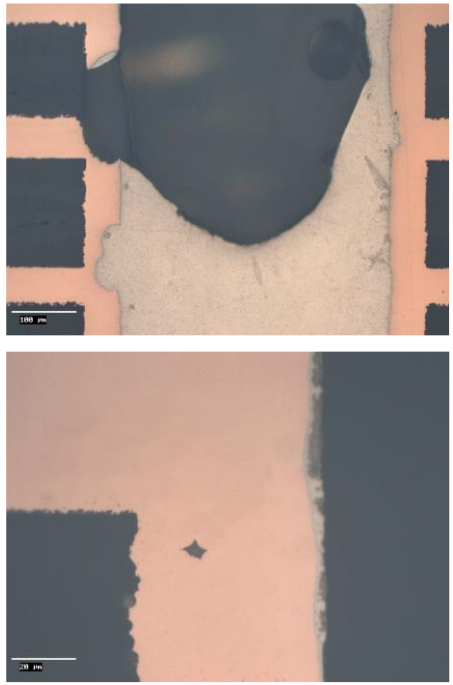


Figure 10-39: Example of voids – top image shows etch-out and bottom image shows an encapsulated void or inclusion

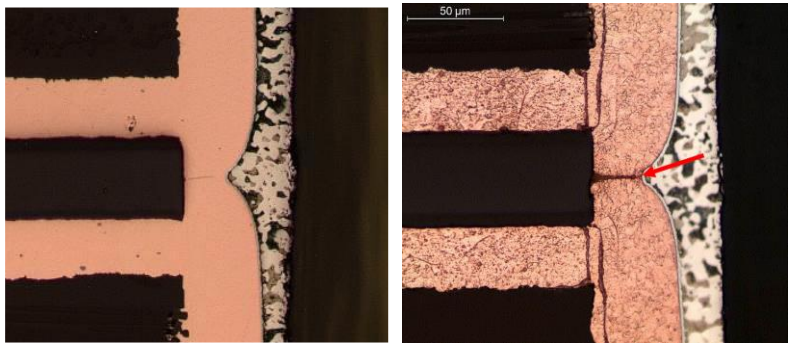


Figure 10-40: Skip plating on flex laminate as-polished (top) and after micro-etch (bottom)

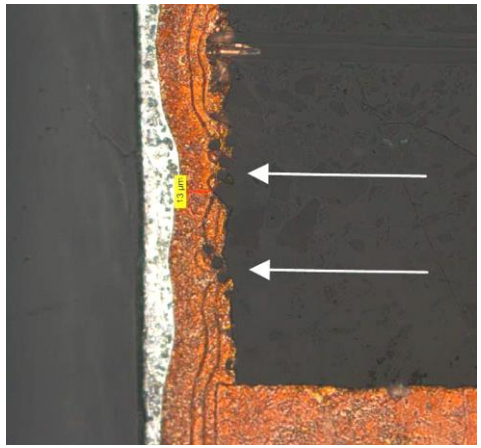


Figure 10-41: Skip plating on glass fibres

Note: Skip plating can be caused by electroless copper that does not cover local areas of the hole wall, such as glass fibres or flex laminate. Subsequent galvanic copper layers can cover up the skip plating, in which case the requirement for minimum copper thickness on local thin areas can be achieved. This can be observed as a plating fold in an etched microsection. On an unetched microsection the copper can seem continuous.

Table 10-23: Wedge voids

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Open wedge void	Not acceptable	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field
b.	Enclosed wedge void	Acceptable on PCB manufacturer copper treatment side of foil in case: Wedge ≤ 13 µm in depth (X-direction) Wedge ≤ 10 µm in height (Z-direction) Void ≤ 5 µm (in X and Y-direction) Copper thickness below void is in conformance with Table 10-3		
c.	Copper filled wedge	Acceptable on PCB manufacturer copper treatment side of foil in case: Wedge ≤ 13 µm in depth (X-direction) Wedge ≤ 10 µm in height (Z-direction)		

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method

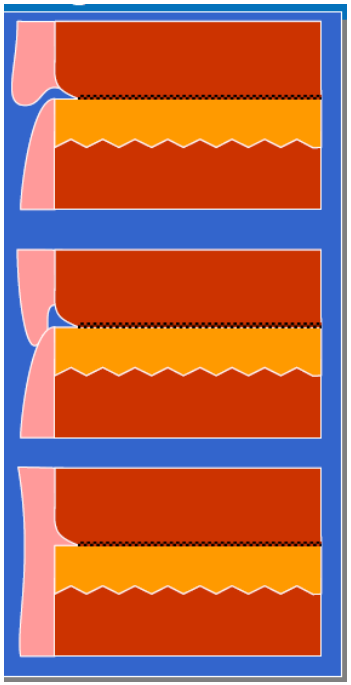
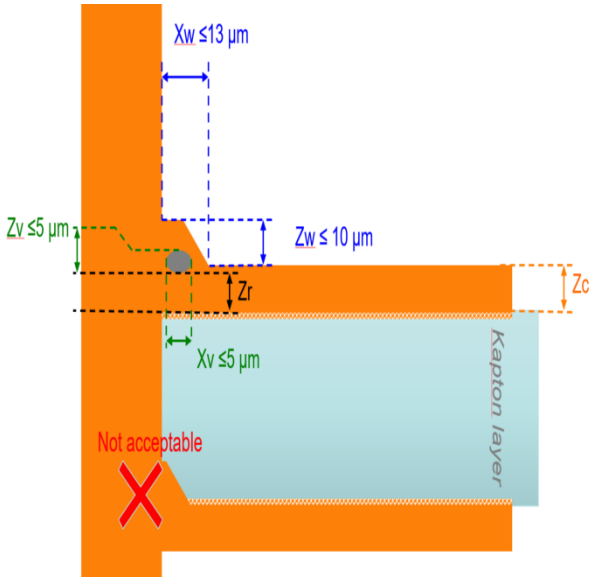


Figure 10-42: Open wedge void (top), enclosed wedge void (middle), copper filled wedge (bottom)



Xw: wedge depth

Zw: wedge height

Xv: void depth

Zv: void height

Zr: copper foil thickness below void

Figure 10-43: Schematic of wedge void dimensions

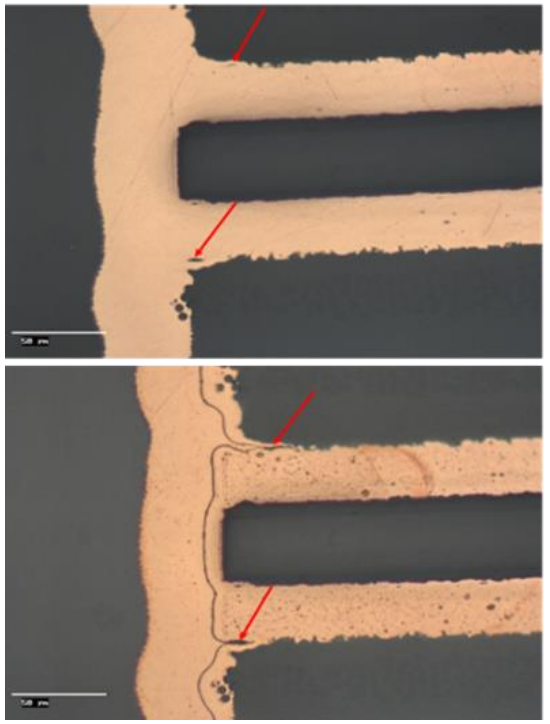


Figure 10-44: Example of wedge voids

Note 1: The height of the copper wedge voids is determined from the copper foil to the point on the hole wall that is aligned with the drilling through the resin.

Note 2: Copper foil of ≤ 12 µm on flex laminate is typically electrodeposited (ED) instead of rolled and annealed (RA). Therefore the desmear process can cause larger wedges. Such thin foils on flex laminate are not within the scope of this standard.

Table 10-24: Resin void

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Resin voids	Target condition: no voids Incidental voids are acceptable if ≤ 80 µm and remaining insulation is in conformance with the PCB definition dossier	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field

Figure 10-45: Example of resin void

Note: Resin voids can occur in prepreg as well as laminate

Table 10-25: Delamination, blistering, crazing, measling

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Delamination, blistering, crazing, measling	Not acceptable	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field

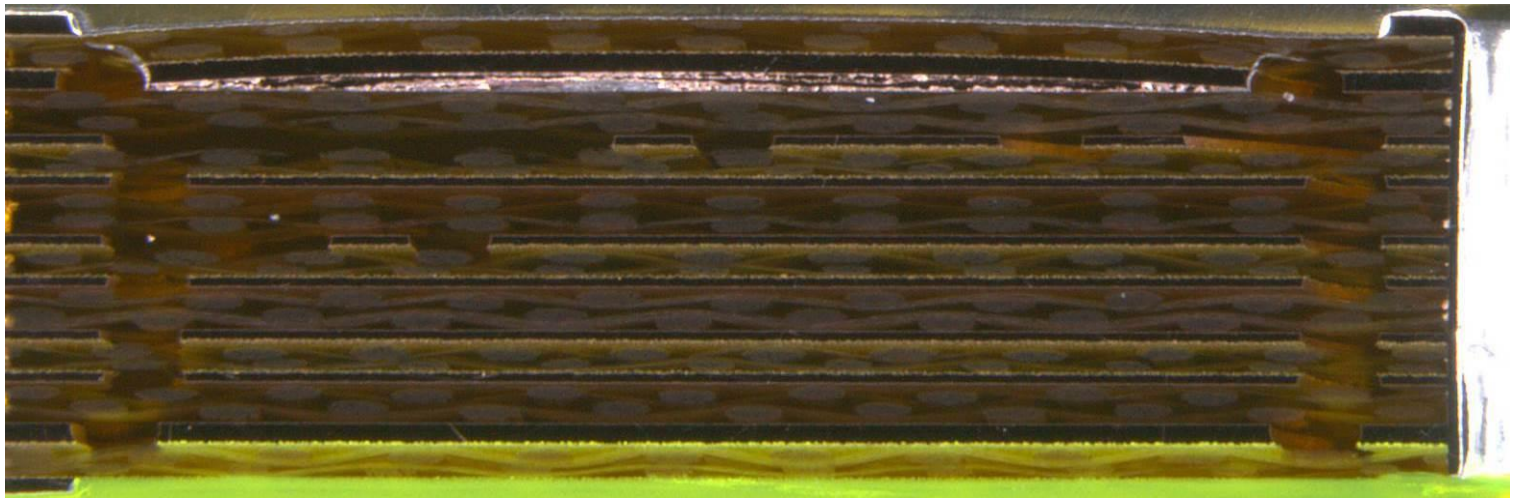


Figure 10-46: Example of delamination

Note : These defects are also evaluated during visual inspection as per Table 10-45.

Table 10-26: Pad Lift

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Pad lift and cracks associated with pad lift	Acceptable if all the following conditions are met: • pads of PTH or via or via-in-pad • after thermal stress • height of pad lift ≤ 40 µm • cracks associated to pad lift do not touch the hole wall • cracks meet requirements of 10.6.2.	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope Magnification: x200 min Lighting: bright and dark field

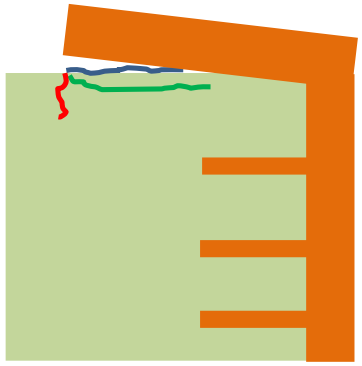


Figure 10-47: Pad lift schematic

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method

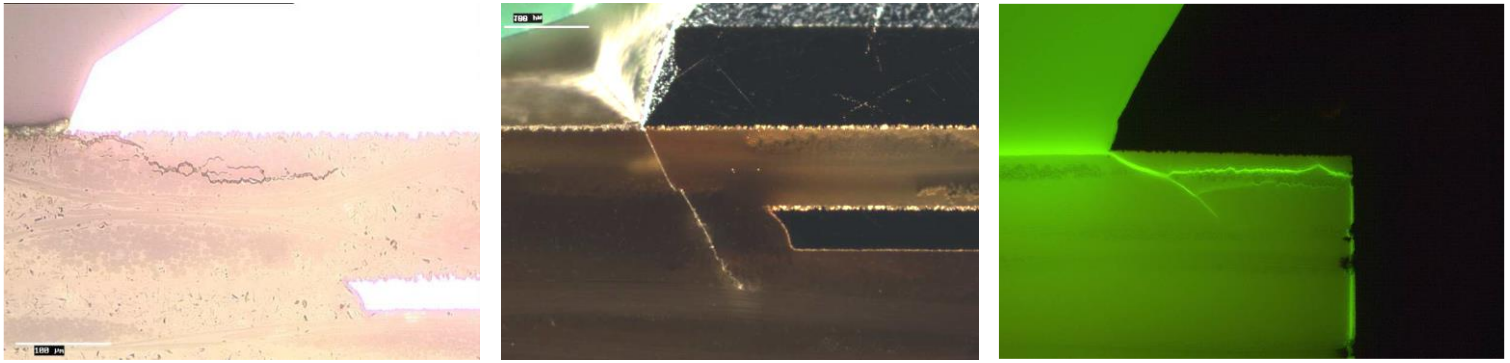


Figure 10-48: Examples of pad lift cracks. The right image is unacceptable because cracks continue until the hole wall

Note 1: The background for pad lift to occur on epoxy technology is because the Tg of the material is below the solidification temperature of solder. Therefore the thermal expansion (above Tg) is high, while the solder has already solidified (during cooling). These conditions are not valid on polyimide laminate, for instance, which has a higher Tg. In case pad lift occurs on polyimide it is considered to be an indicator of an anomaly of the process or the material.

Note 2: Blue line: Adhesive failure between copper and dielectric. This is named “pad lift” or ”lifted lands”. Green line: Horizontal crack or void of any size in dielectric under the pad. This is included as “pad lift”. In case crack protrudes from underneath the pad or into the glass reinforcement, it is evaluated as a “laminate crack” as per Table 10-27. Red line: Vertical crack in dielectric extending from the edge of the pad. This is named “laminate crack” and it is covered in Table 10-27

Table 10-27: Dielectric cracks

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Drilling crack	Standard PCB technology: acceptable if ≤ 80 µm HDI PCB technology: acceptable if ≤ 50 µm and ≤ annular ring And see Ref. d.	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope Perform inspection under dark field to locate any cracks. Perform measurement of crack length in bright field at 500x magnification. Determine remaining insulation distance as per 10.6.3d and 10.6.3e
b.	Crack associated with the end of a conductor pattern	≤ 80 µm and referee test 4 microsections in the spare PCB after SB does not show cracks more than 80 µm, as per 10.6.3c. And see Ref. d.		
c.	Random cracks in the dielectric	≤ 80 µm and referee test 4 microsections in the spare PCB after SB does not show cracks, as per 10.6.3c. Multiple adjacent cracks in the dielectric ≤ 80 µm and evaluated as a single crack And see Ref. d.		
d.	Crack (for Ref. a, b, c)	not crossing glass reinforcement in Z-direction remaining insulation distance is in conformance with the PCB definition dossier		

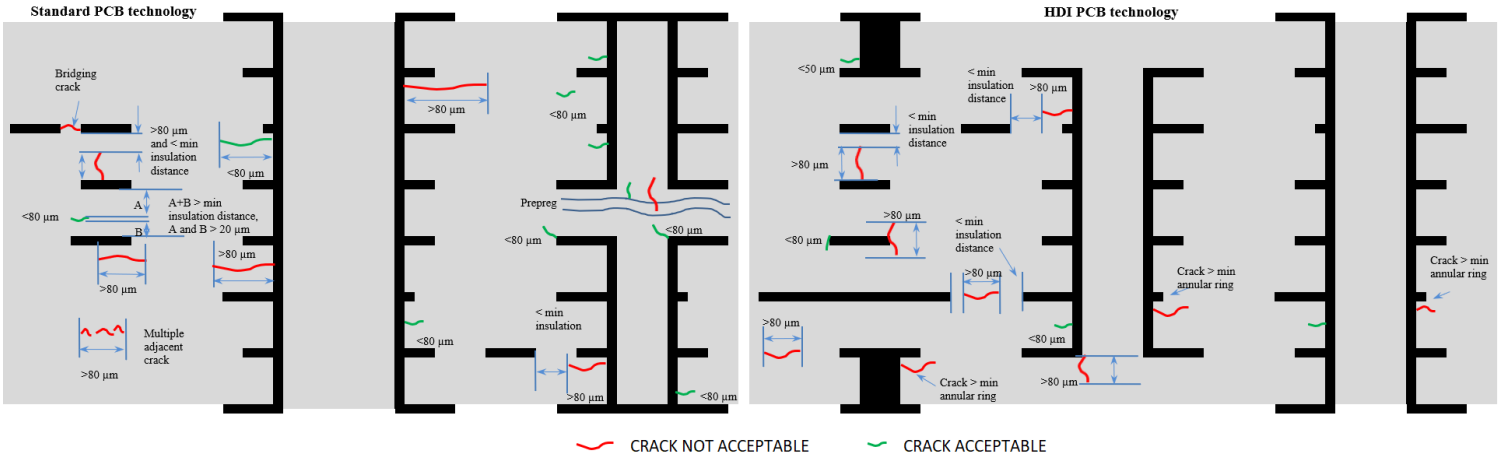


Figure 10-49: Acceptable (green) and non-acceptable (red) dielectric cracks

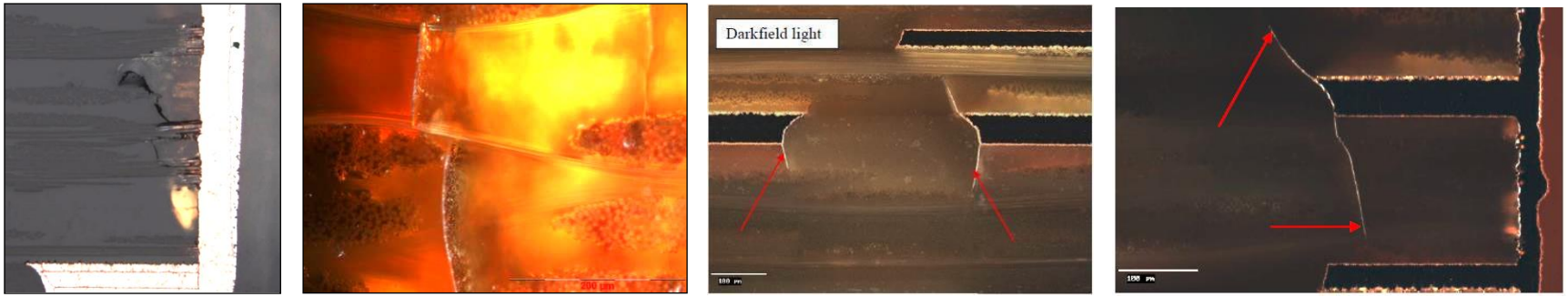


Figure 10-50: Examples of laminate cracks

Note 1: The PCB definition dossier is in conformance with the DRD of ECSS-Q-ST-70-12 Annex A. The insulation distance specified in the PCB definition dossier is in conformance with ECSS-Q-ST-70-12 Table 13-7.

Note 2: Cracks can be observed at the end of conductor patters, in particular when using thick copper profile and resin-rich areas. Random dielectric cracks can be observed in specific prepreg materials.

Note 3: Multiple adjacent cracks are evaluated as a single crack from start of one crack until the end of the adjacent crack, as shown in Figure 10-49.

Note 4: Referee testing is performed by microsectioning and microscopic inspection of a spare PCB in conformance with this table as per 10.6.3c.

Note 5: Drilling cracks are measured in the remaining resin (not taking into account the original drill location).

Note 6: Remaining insulation distance on crack Ref. c. in standard technology shown in Figure 10-49 is determined by adding the intact insulation distance below and above the crack ('A+B') as well as by ensuring a minimum distance of 20 µm on either side.

Table 10-28: Cracks and separation in copper

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Cracks in internal and external copper foil	Not acceptable	Location: coupon A/B + Bn Condition: set 1 AR+RW; set 2 SB Frequency: per panel	Microsection and Microscope Magnification: 200x min Lighting: bright field
b.	Cracks in copper plating including barrel cracks and corner cracks			
c.	Separation between external copper foil and copper plating	Not acceptable AR, RW, SB Acceptable on vertical edge of foil and on horizontal material supplier treatment side of foil in case its evaluation is recorded in the PID.		

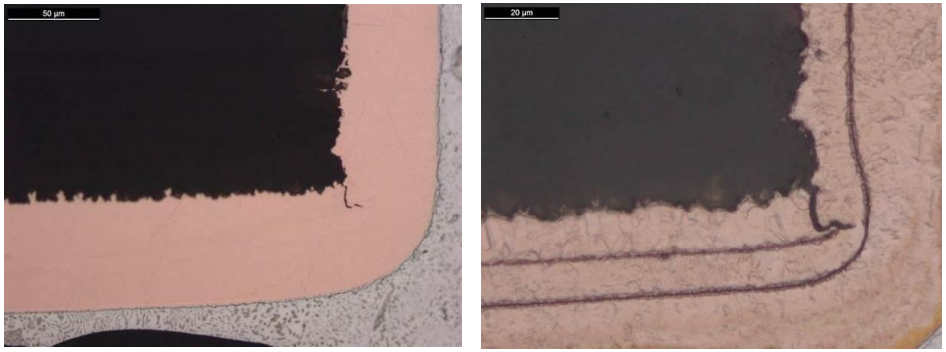


Figure 10-51: Example of C foil separation as-polished and after micro-etch

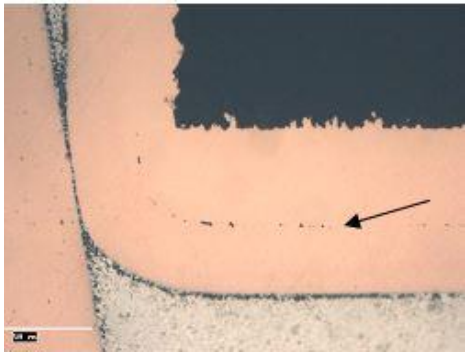


Figure 10-52: Example of interface line between plated copper layers on a non-etched microsection

Note : Interface lines between copper plating layers can occur. ECSS-Q-ST-70-60 does not specify an accept or reject criterion for such feature. It can be justified by group 6 for qualification and described accordingly in the PID.

Table 10-29: Interconnect defect and corner cracks in microvias

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Interconnect defect on standard technology	Not acceptable	Location: coupon A/B and Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: 500x Illumination: bright field
b.	Interconnect defect from microvia to internal landing pad	Not acceptable		
c.	Corner cracks in microvias	Not acceptable (see also note 3)		

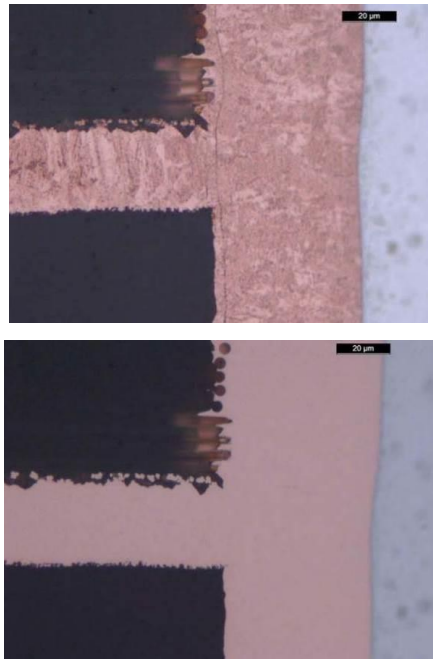


Figure 10-53: Interconnect after stress, target condition, after microetch (top) and as-polished (bottom)

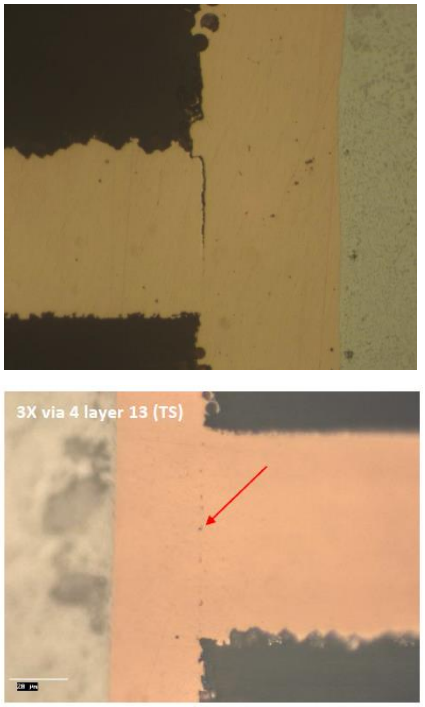


Figure 10-54: Examples of ICD

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method

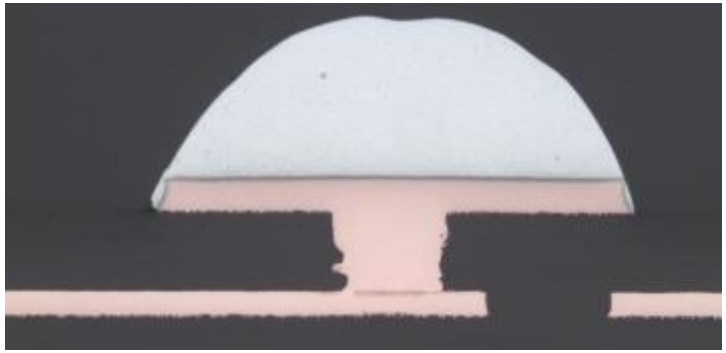


Figure 10-55: ICD on internal landing pad (unetched)

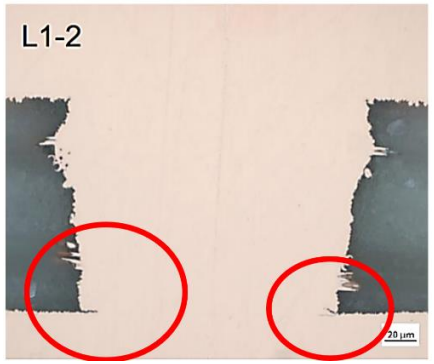


Figure 10-56: Corner cracks on internal landing pad

Note1: It is important for this type of defect that microsections are evaluated in as-polished condition. Microetching can be done to determine the exact interface once a defect has been observed. However, an etched microsection is not suitable for initial evaluation for ICD since it always shows an interface line between foil and plating.

Note 2: ICD is not to be confused with smear.

Note 3: Minor corner cracks can be seen after group 6 testing on the internal landing pad of microvias. In such case, it is good practice to evaluate any corner cracks in combination with the following aspects to justify possible acceptability:
- length of corner cracks,
- number of instances of corner cracks,
- barrel shape, undercut and wedge shape of dielectric at the bottom corners,
- aspect ratio,
- absence of interconnect defect,
- intact contact diameter,
- aspect of microvias that have been subject to IST and after SB.

Table 10-30: Smear

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Smear	Polyimide and Epoxy: no smear accepted ≤ 10 % smear is acceptable on PTFE based resins ≤ 25% smear is acceptable on PTFE based resins in case the additional horizontal microsection shows ≤ 33 % smear in the circumference	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x min Lighting: bright field

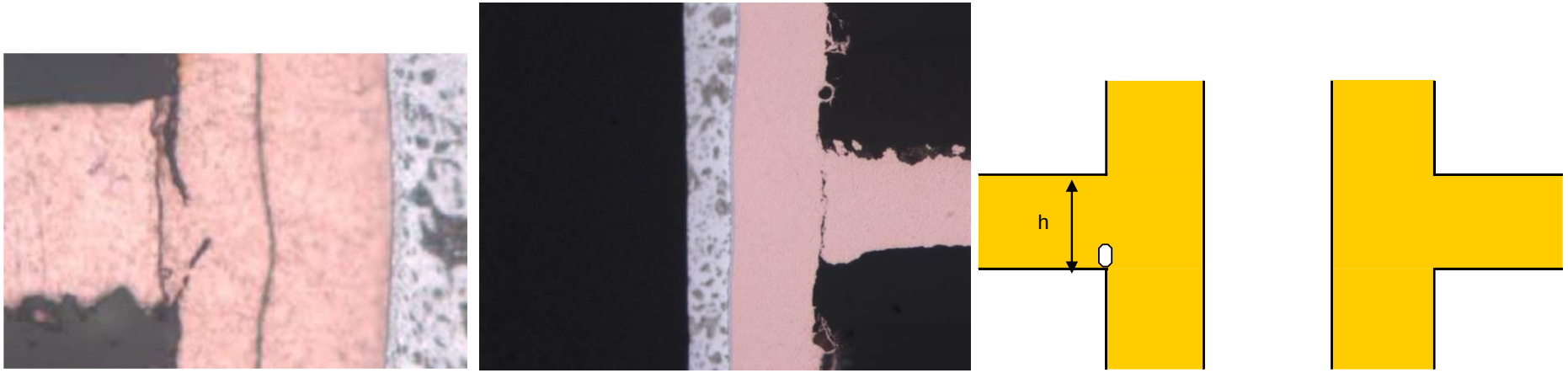


Figure 10-57: Example of smear

Note: In case 10-25 % smear is observed, an additional horizontal microsection is taken to verify the extent of smear around the circumference.

Table 10-31: Hole wall pull away and resin recession

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Hole wall pull away or resin recession	≤ 20 % of the sum of dielectric on standard layers is acceptable Up to 100% is acceptable on specific layers with heat sink or dielectric thickness ≥ 200 µm, in case all of the following conditions are met: • hole wall pull away ≤ 10 µm between hole wall and resin; • resin recession between hole wall and resin is ≤ copper thickness of hole wall; • its evaluation is recorded in the PID.	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope Magnification: x 200 min Illumination: bright field

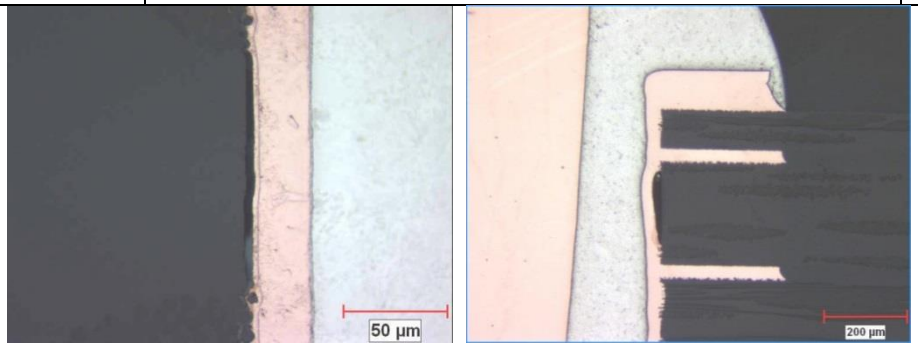


Figure 10-58: Example of hole wall pull away - showing separation of copper in a straight line (left) or slightly bulging outward (right)

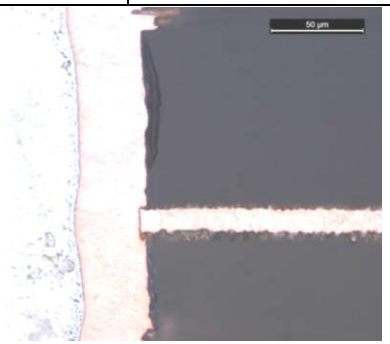


Figure 10-59: Example of resin recession - showing concave retraction of resin

Note 1 Group 6 on hole wall pull away or resin recession is performed to show absence of cracks in copper and separation between hole wall and resin within the requirement.

Note 2: The requirement for plated copper thickness is applicable in case hole wall pull away or resin recession causes thinning of the hole wall.

Note 3: Hole wall pull away can be observed on polyimide resin due to lower adhesion of plated copper to the resin. It can also be observed on epoxy resin. Resin recession can be observed on epoxy resin due to shrinkage of the resin after thermal stress and subsequent separation of the hole wall. Resin recession is not typically observed on polyimide because of the thermal stability of the resin. Hole wall pull away usually appears as a separation of the copper in a straight line or bulging outward from the dielectric. Resin recession usually appears as a concave retraction of the resin.

Note 4: In case of local layers with 100 % HWPA, the other standard layers have HWPA ≤ 20 % of the sum of the dielectric, as specified in this table. The sum of the dielectric is calculated on the remainder of the standard build-up, i.e. not including the layers where 100 % HWPA is permitted.

Table 10-32: Nail heading

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Nail heading	≤ 50 % of inner layer copper thickness	Location: coupon A/B + Bn Condition: set 1 AR(+RW) + set 2 (SB) Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field

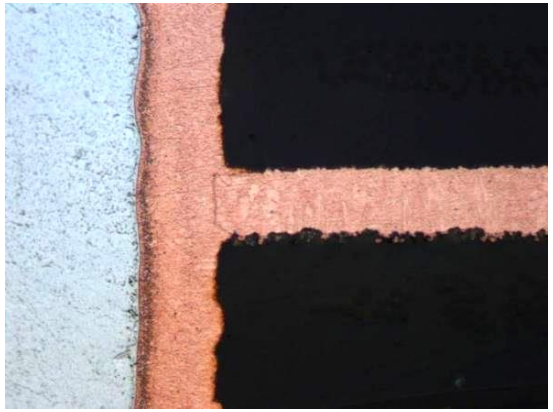


Figure 10-60: Target condition

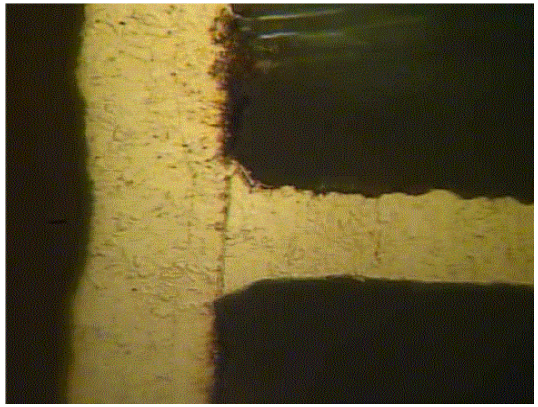


Figure 10-61: Acceptable nail heading

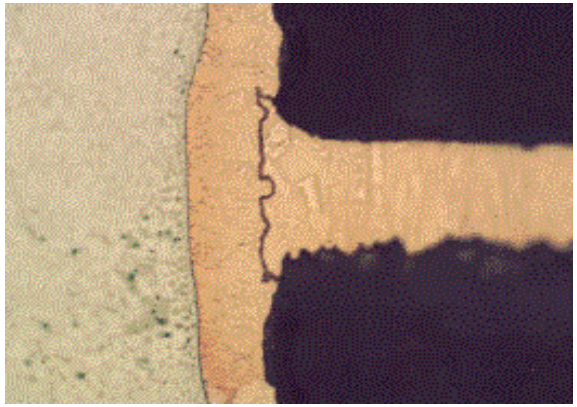


Figure 10-62:Unacceptable nail heading, exceeding 50 % of innerlayer copper thickness

Table 10-33: Cu-Invar-Cu

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Nailheading in CIC layers	≤ 50 % of copper thickness on CIC layer	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 500x Illumination: bright field
b.	Separation or contamination between copper on CIC layer and plated barrel	No separation or contamination allowed		
c.	Separation or contamination between Invar layer and plated barrel	≤ 20 % separation/contamination		

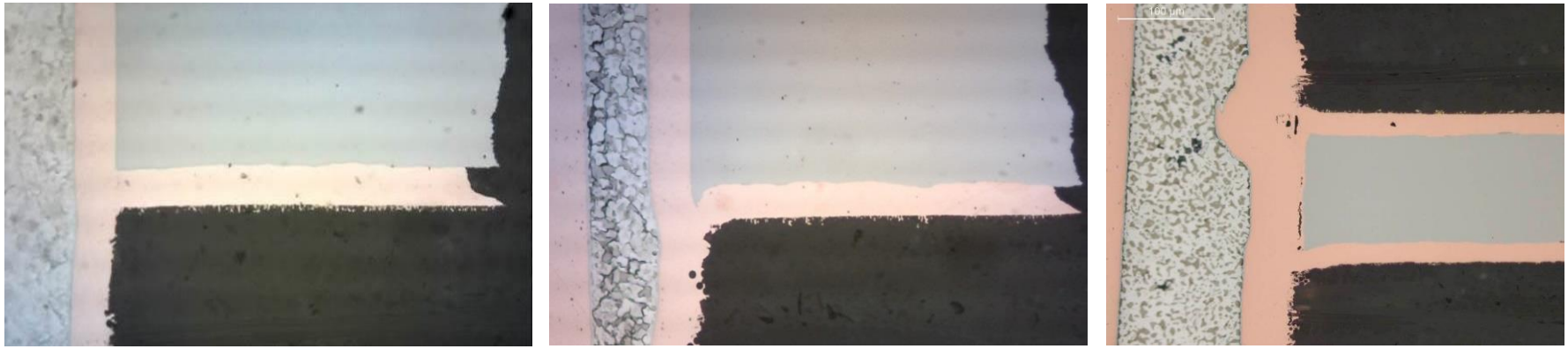


Figure 10-63: Examples of CIC connection, target condition (left), nailheading (middle), separation to CIC (right)

Note 1: Contamination can be Invar smear, seen as a grey substance between copper and plated barrel

Note 2: A (non-mechanical) buried via that connects to the surface of the CIC does not have specific additional features defined in this table.

Table 10-34: Inhomogeneity in dielectric

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Bromine flame retardant	Unacceptable if agglomerated. Random dots are acceptable provided that THB or CAF testing are successful.	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x Illumination: dark field
b.	Agglomeration of filler	Unacceptable in case size is >80 µm on interface between prepreg and laminate		
c.	Swirl or milky appearance in no-flow prepreg	Acceptable in case its evaluation is recorded in the PID.		
d.	Demarcation line in no-flow prepreg	Acceptable in case its evaluation is recorded in the PID.		
e.	Dotted interface line	Acceptable in case all the following conditions are met: • It can only be seen in dark field • Dots are seen as broken dotted line, not a continuous line • Dots within the line are seen at different depths of the microsection • Evaluation of the dots is recorded in the PID.		Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field and dark field and out of focus view

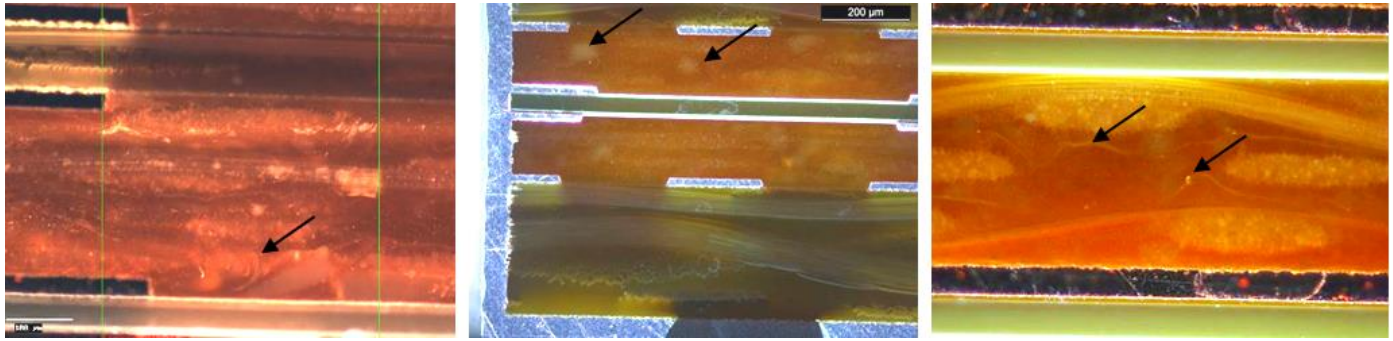


Figure 10-64: Examples of swirl (1st and 2nd image) and demarcation line (3rd). In the 2nd picture the difference between no-flow prepreg (top) and laminate (bottom) is noticeable

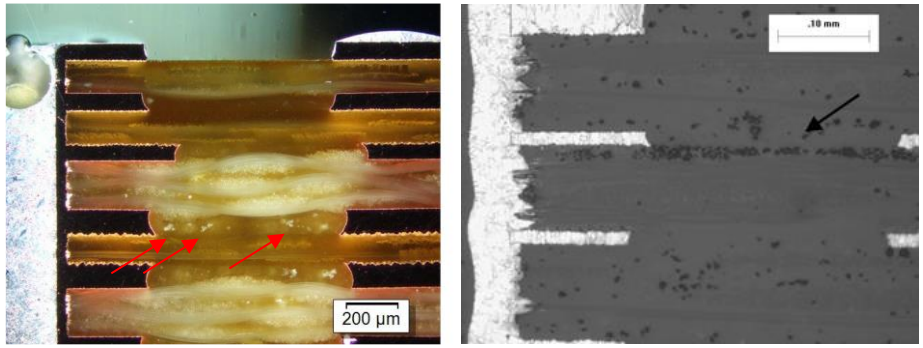


Figure 10-65: Examples of bromine flame retardant observed as random dots (left) and an agglomeration (right)

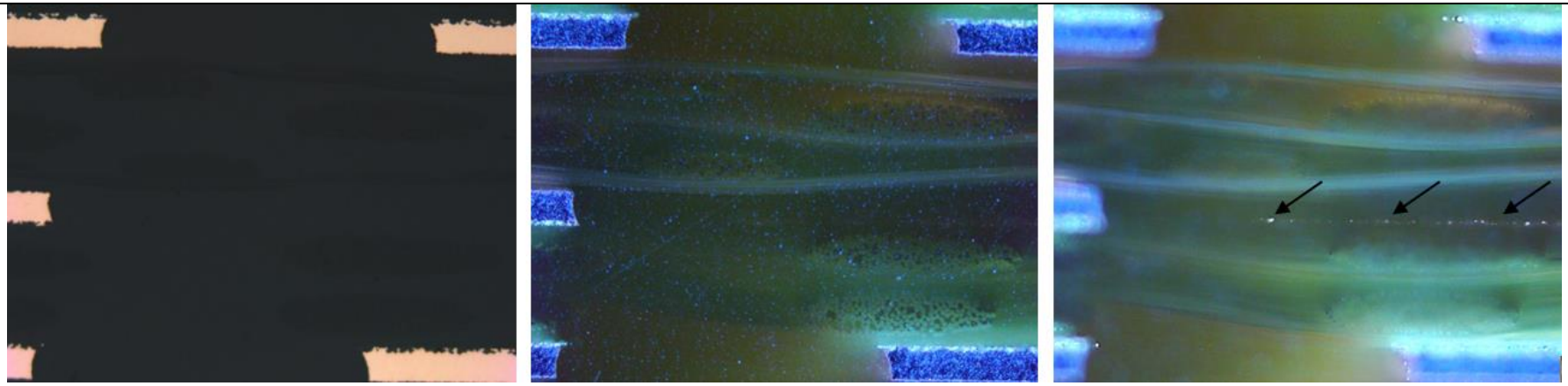


Figure 10-66: Example of dotted interface line observed in dark field out of focus (right), which is not visible in focus (middle) and in bright field (left)

Note 1: Cracks are evaluated in conformance with Table 10-27.

Note 2: Agglomeration of filler is evidenced by the non-wetted aspect of several filler particles in contact with each other. Agglomeration of filler is typically caused by bad mixing during raw material manufacturing. Random filler particles > 80 µm can be embedded in base laminate. Due to the probable presence of resin (butter coat) between copper and filler particle, it does not appear on the interface between prepreg and laminate and is acceptable. Filler particles on external layers observed by visual inspection are evaluated in conformance with Table 10-46.

Note 3: Dotted interface lines is not the same as spurious copper as specified in Table 10-14. Dotted interface line is also known as treatment transfer.

Table 10-35: Contamination or foreign inclusion

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Non-metallic contamination in microsection	Target condition: no contamination Incidental contamination is acceptable if ≤ 80 µm and remaining insulation is in conformance with the PCB definition dossier	Location: coupon A/B + Bn Condition: set 1 AR+RW + set 2 SB Frequency: per panel	Microsection and Microscope: Magnification: ≥ 200x min Illumination: bright field
b.	Metallic contamination	Not acceptable		

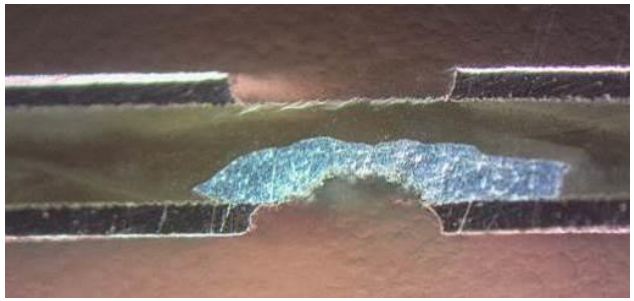


Figure 10-67: Example of metallic contamination in laminate

Note: This is specified to handle all types of contamination. Because of the inspection by cross-sectioning it is most effective at detecting larger inclusions. Small fibre contamination cannot be efficiently evaluated in a cross-section. Instead it can be better evaluated by visual inspection in conformance with Table 10-46 on external layers. Internal layer cleanliness is also specified in clause 6.5 and 6.7.

Table 10-36: Rigid-flex interface - delamination between coverlay and prepreg

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Delamination between coverlay and prepreg	Not accepted	Location: rigid-flex coupon Condition: set 6 SB Frequency: per panel	Microsection and Microscope: Magnification: 50x - 200x Illumination: dark field or UV fluorescent

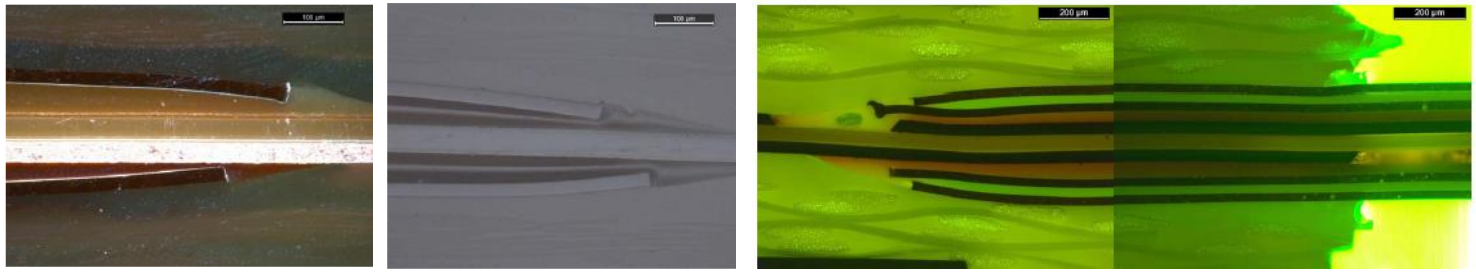


Figure 10-68: Acceptable adhesion between coverlay and prepreg

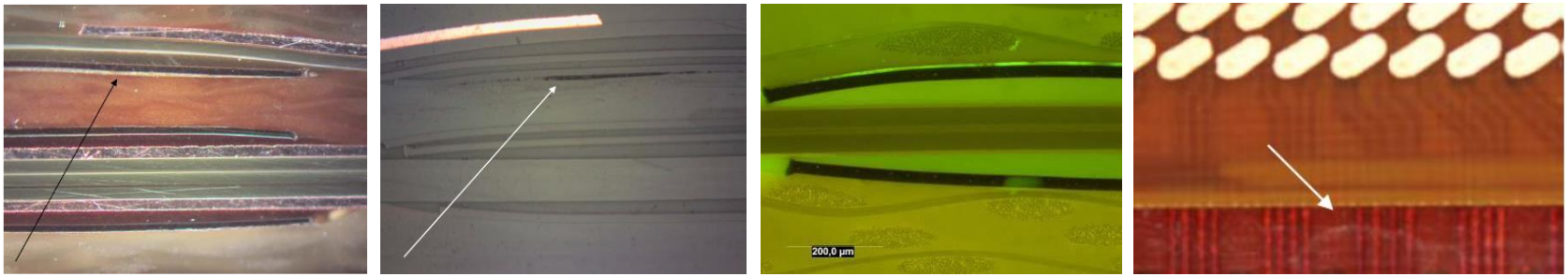


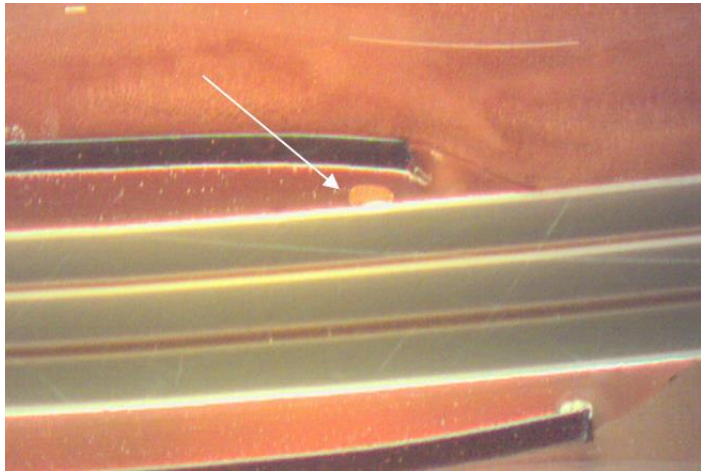
Figure 10-69: Delamination between coverlay and prepreg

Note 1: Preparation of the microsection can create separation between materials due to mechanical stress.

Note 2: Table 10-55 specifies visual inspection criteria for coverlay. Blistering can appear as local delamination in the microsection.

Table 10-37: Rigid-flex interface - adhesive voids in coverlay and bond-ply

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Adhesive void in Rigid-flex interface	Target condition: no voids Incidental voids of ≤ 80 µm are acceptable in case the insulation distance is in conformance with the PCB definition dossier	Location: rigid-flex coupon Condition: set 6 SB Frequency: 1 per panel	Microsection and Microscope: Magnification: 50x - 200x Illumination: dark field or UV fluorescent or bright field



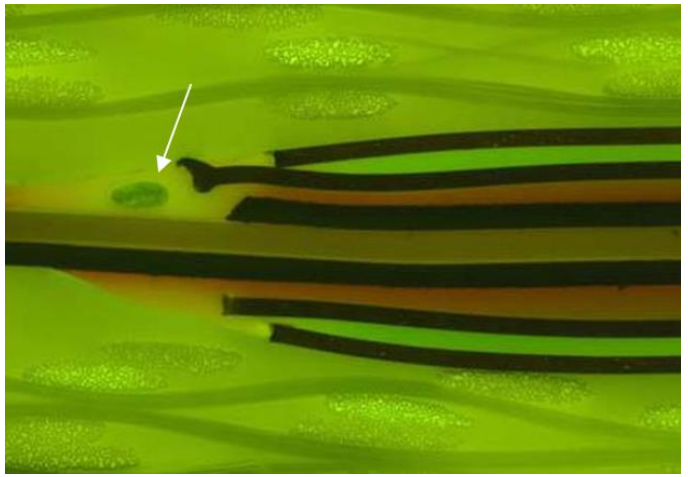


Figure 10-70: Example of voids in acrylic adhesive in rigid-to-flex interface

Note: Bond-ply consist of kapton with adhesive on both sides as indicated in the note of requirement 9.3e of ECSS-Q-ST-70-12. Only adhesive between copper layers does not provide sufficient insulation.

Table 10-38: Rigid-flex interface - misalignment of prepreg

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Resin squeeze out	≤ 1,5 mm	Location: rigid-flex coupon Condition: set 6 SB Frequency: per panel	Microsection under magnification
b.	Adhesive filet recession	≤ 0,5 mm into rigid section		

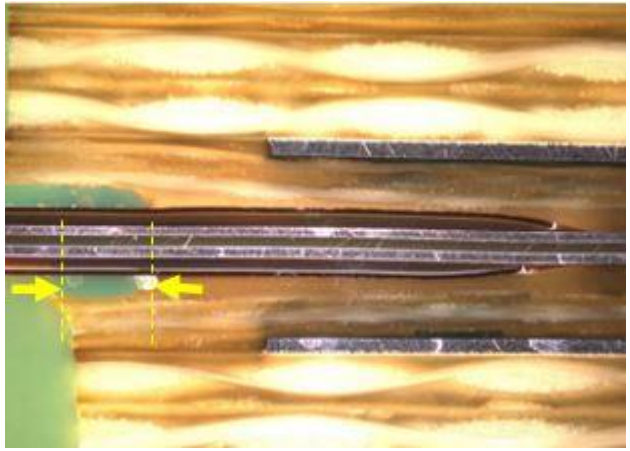


Figure 10-71: Example of adhesive filet recession into rigid section as observed in microsection

Note: These features are also evaluated in visual inspection in conformance with Table 10-52.

Table 10-39: Hypercorrosion of ENIG

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Hypercorrosion of ENIG	Hypercorrosion level 0 is the target condition. Hypercorrosion level 1 is acceptable provided that it is incidental.	Location: coupon A/B or Bn Condition: set 1 AR(+RW) Frequency: pre-screening of one coupon per panel, followed by in-depth hypercorrosion assessment on the worst-case coupon of the batch.	Corrosion level definition as per 3.6.2 of IPC-4552B applies. Corrosion level evaluation as per 3.6.3 of IPC-4552B applies. Product rating as per 3.6.3.8 of IPC-4552B is disregarded. Microsection and Microscope: Magnification: 1000x Illumination: bright field or Nomarski DIC

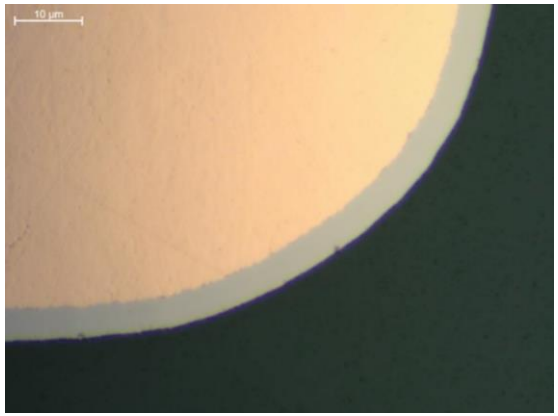


Figure 10-72: Example of ENIG hypercorrosion level 1 (incidental)

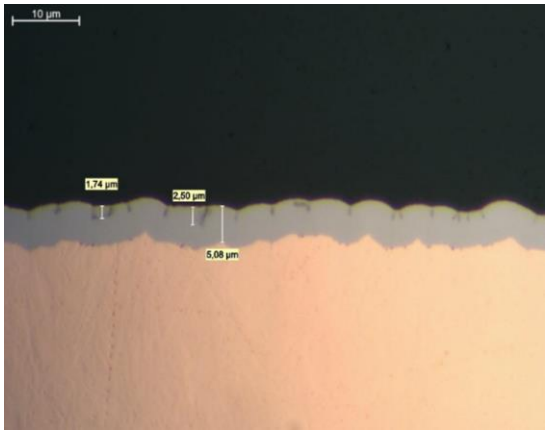


Figure 10-73: Example of ENIG hypercorrosion level 2

Note 1: Hypercorrosion occurs in the Nickel layer.

Note 2: IPC-4552B permits for <10 hypercorrosion spikes per inspection area to be classified under level 1. However, ECSS-Q-ST-70-60 describes that hypercorrosion spikes are only acceptable if incidental. This is a significant reinforcement of the IPC specification.

Note 3: It is important for this evaluation that microsections are evaluated in as-polished condition, without microetch. Coupon A/B or Bn will subsequently be microetched by the PCB manufacturer for other assessments and eventually delivered to the customer. It is good practice for the customer to repolish the microsection to remove the microetch and oxidation prior to the evaluation of hypercorrosion as part of their incoming inspection. In case the customer does not have the capability to repolish, it can be specifically requested to the PCB manufacturer during the MRR.

Table 10-40: Hypercorrosion of ENEPIG and ENIPIG

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
b.	Hypercorrosion of ENEPIG	Hypercorrosion is not acceptable.	Location: coupon A/B or Bn Condition: set 1 AR(+RW) Frequency: pre-screening of one coupon per panel, followed by in-depth hypercorrosion assessment on the worst-case coupon of the batch.	Microsection and Microscope: Magnification: 1000x Illumination: bright field or Nomarski DIC
c.	Hypercorrosion of ENIPIG	Level I$_{ENIPIG}$ acceptable, as below		

Level I$_{ENIPIG}$ acceptable:

- ≤ 50 spike type defects and some spreader/spikes defects observed on most pads, and
- Corrosion spike depth <2 micron and no more than 30% of the nickel deposit thickness (≥ 3µm Ni thickness is achieved)

Level II$_{ENIPIG}$ not acceptable:

- > 50 spike type defects and some spreader/spikes defects observed on most pads. At this activity level, more than 99% of the solder surface has not degraded.
- Corrosion spike depth is <3 microns and no more than 50% of the nickel deposit thickness (≥ 3µm Ni thickness is achieved).
- Standard preparation methods are not always sufficient to discriminate level I and level II. As a referee method it is good practice to perform ion beam milling and polishing or evaluation after SB. In addition, it is good practice to perform a solderability test in case referee investigation is needed.

Level III$_{ENIPIG}$ not acceptable:

- Black band defects observed on most pads.
- Corrosion spike depth is ≥ 3 microns or ≥ 50% of the nickel deposit thickness (i.e. 3µm Ni thickness is not achieved), whichever is greater.

Note 1: Hypercorrosion occurs in the Nickel layer.

Note 2: IPC-4556 does not specify hypercorrosion levels for ENEPIG. No hypercorrosion is considered to occur due to the nature of the processes and the type of finish.

Note 3: It is important for this evaluation that microsections are evaluated in as-polished condition, without microetch. Coupon A/B or Bn will subsequently be microetched by the PCB manufacturer for other assessments and eventually delivered to the customer. It is good practice for the customer to repolish the microsection to remove the microetch and oxidation prior to the evaluation of hypercorrosion as part of their incoming inspection. In case the customer does not have the capability to repolish, it can be specifically requested to the PCB manufacturer during the MRR.

Table 10-41: Heat sinks and CTE restrictive layers CIC, Molybdenum and ceramic

Ref.	technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Cracks in ceramic	Not acceptable	Location: coupon A/B + Bn or special coupon Condition: set 2 SB Frequency: per batch	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright field
b.	Lack of adhesion of resin (resin recession)	Not acceptable		
c.	Burrs	Not acceptable		
(no example pictures available)				

10.4 Visual inspection

ECSS-Q-ST-70-60_1390614

a. For the technological feature conductor width, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-42.

ECSS-Q-ST-70-60_1390615

b. For the technological feature conductor spacing, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-43.

ECSS-Q-ST-70-60_1390616

c. For the technological feature surface metallisation the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-44.

ECSS-Q-ST-70-60_1390617

d. For the technological features measling, crazing, blistering and delamination the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-45.

ECSS-Q-ST-70-60_1390618

e. For the technological features contamination and inhomogeneity, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-46.

ECSS-Q-ST-70-60_1390619

f. For the technological feature scratches, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-47.

ECSS-Q-ST-70-60_1390620

g. For the technological features weave exposure, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-48.

ECSS-Q-ST-70-60_1390621

h. For the technological feature haloing the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-49.

ECSS-Q-ST-70-60_1390622

i. For the technological feature tin-lead surface quality the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-50.

ECSS-Q-ST-70-60_1390623

j. For the technological feature marking the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-51.

ECSS-Q-ST-70-60_1390624

k. For the technological features rigid-flex interface misalignment of prepreg, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-52.

ECSS-Q-ST-70-60_1390625

l. For the technological feature rigid-flex interface fibre protrusion the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-53.

ECSS-Q-ST-70-60_1390626

m. For the technological feature rigid-flex interface haloing the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-54.

ECSS-Q-ST-70-60_1390627

n. For the technological features rigid-flex interface aspect of flex laminate and coverlay the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-55.

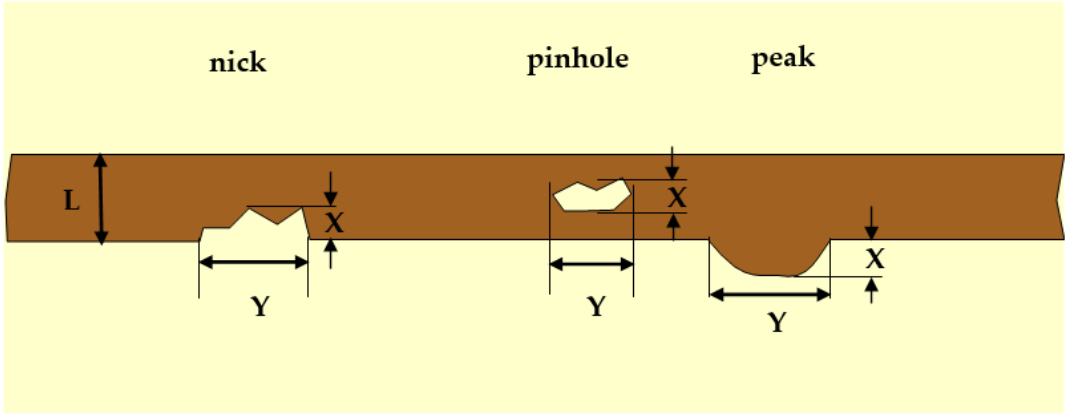
ECSS-Q-ST-70-60_1390898

o. For the technological features for solder mask the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-56.

ECSS-Q-ST-70-60_1390628

Table 10-42: Conductor width

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Peak, nick, pinhole	Acceptable if all the following conditions are met: X ≤ 20 % of L Y ≤ L minimum conductor width (L – X) ≥ PCB definition dossier	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x X is the as-manufactured conductor width
b.	Conductor width	Tolerance of conductor width is ≤ 20 % in conformance with Table 7-3 from ECSS-Q-ST-70-12		
c.	Peak, nick, pinhole on SMT pad	Not acceptable in pristine area consisting of the middle 80 % of the pad		



X: width of defect
Y: length of defect
L: conductor width

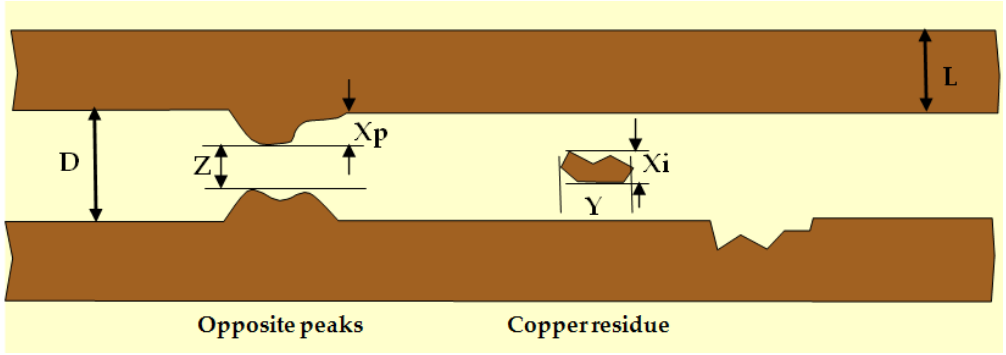
Figure 10-74: Conductor width

Note 1: Intermittent and irregular metallisation defects on conductors include edge roughness caused by peak (synonyms: spike, protrusions , unintentional pattern) or nick (synonyms: indentations, mouse bites, dents) and pinholes (synonyms: voids, pits). Conductors include pads.

Note 2: Probe marks from electrical test are not evaluated as a conductor imperfection.

Table 10-43: Conductor spacing

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Peaks	Acceptable if all the following conditions are met: Opposite peaks: Z ≥ 80 % of D Isolated peaks: Xp ≤ 20 % of L minimum remaining spacing Z ≥ PCB definition dossier	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x D is the as-manufactured spacing
b.	Conducting island	Acceptable if all the following conditions are met: (Xp + Xi) ≤ 20 % of D Xi ≤ 20% of D Y ≤ D Minimum remaining spacing (D – Xi) ≥ PCB definition dossier		
c.	Conductor spacing	Tolerance of conductor spacing is ≤ 20 % in conformance with Table 7-3 from ECSS-Q-ST-70-12		



Xp: width of peak
Xi: width of island
Y: length of defect
L: conductor width
D: insulation distance
Z: remaining insulation distance between defects

Figure 10-75: Conductor spacing

Note: Intermittent and irregular metallisation defects caused by peaks (synonyms: spikes, protrusions , unintentional pattern) or copper residue (synonyms: unintentional pattern, conducting island). Conductors include pads. Copper residue can be caused by a problem in the imaging processes. This is not the same as spurious copper as described in Table 10-14.

Table 10-44: Surface metallization

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Lifting or delamination of conductive pattern from substrate	Not accepted	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Copper or nickel visible on top surface plated areas	Not accepted		
c.	Exposed copper on side of conductor	Acceptable		
d.	Corrosion of exposed copper	Not accepted		

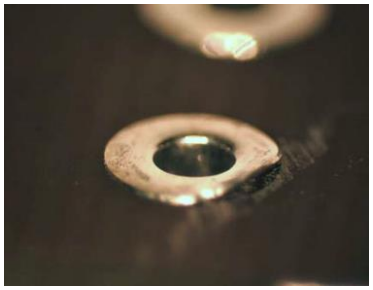


Figure 10-76: Example of lifted land

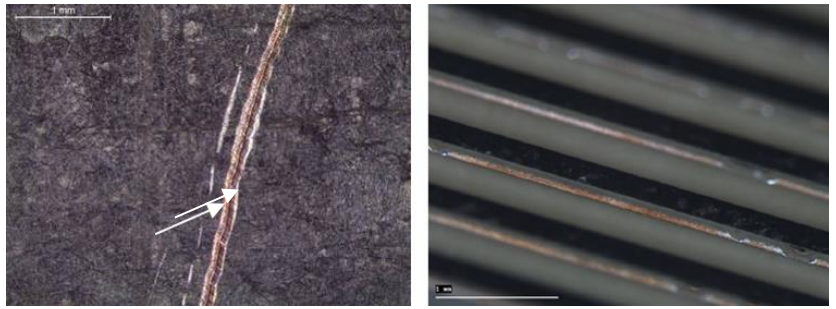


Figure 10-77: Example of visible copper on top surface (left) and on side of track (right)

Table 10-45: Measling, crazing, blistering, delamination

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Measling, crazing, blistering, delamination	Not accepted	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

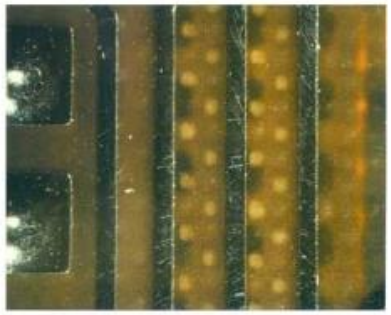


Figure 10-78: Example of measling

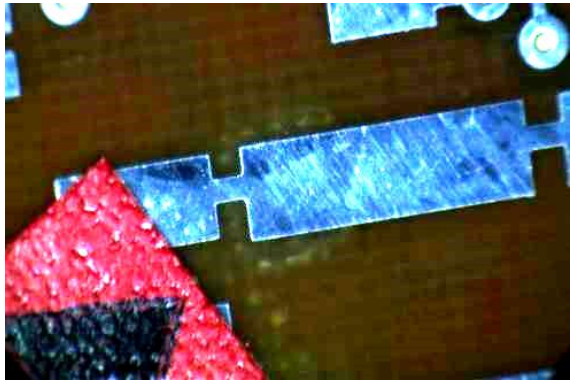


Figure 10-79: Examples of crazing

Note: An isolated white spot is not typical for measling or crazing. Instead, this can be a dry spot, which is not associated with thermal stress, and can be evaluated as inhomogeneity. Measling can be caused by soldering and inadequate bake-out.

Table 10-46: Contamination, inhomogeneity

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Non-metallic contamination or inhomogeneity	Accepted with traceability in CoC in case the remaining insulation distance is in conformance with the PCB definition dossier. Numerous inclusions indicate poor workmanship and is not accepted.	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Metallic contamination	Not accepted		
c.	Discoloured copper oxide on underlying layer	Accepted in case it does not originate from via holes		

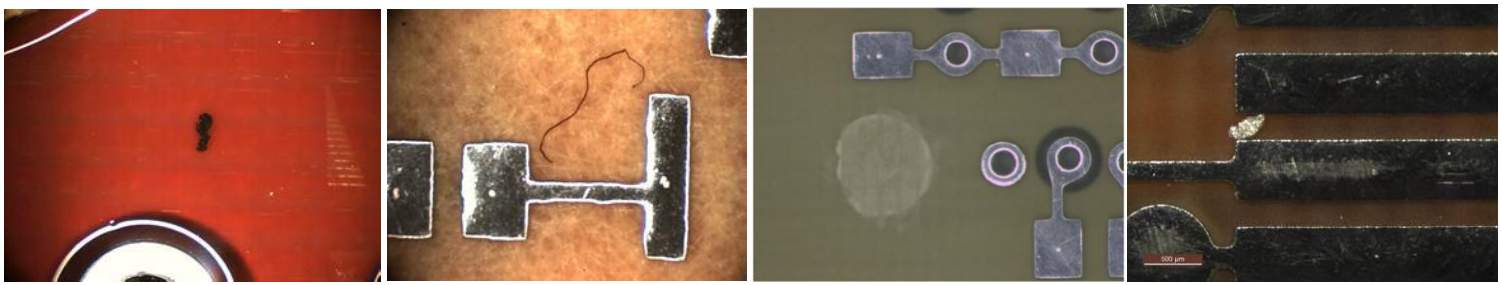


Figure 10-80: Examples of contamination and inhomogeneity

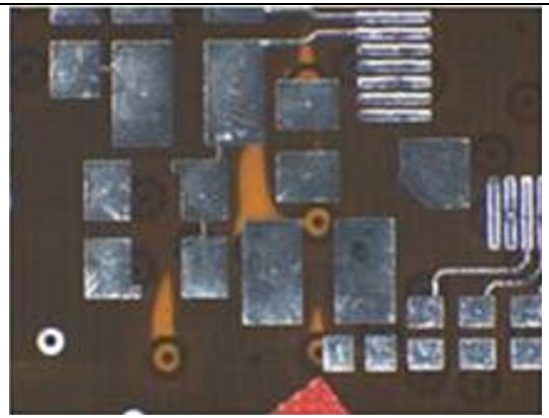


Figure 10-81: Examples of unacceptable discoloured copper oxide originating from a via

Note 1: The term inhomogeneity is used to describe a different aspect (such as colour) of dielectric material that can be intrinsic to the material, instead of caused by a foreign substance. Discoloured copper oxide is not an inhomogeneity in the dielectric.

Note 2: Occurrence of contamination is a process indicator of raw materials and PCB processes as described in clause 6.7.1.

Note 3: Random particles of filler material on external layers are evaluated as non-metallic contamination (Ref. a).

Note 4: Discoloured copper oxide that originates from the via holes indicates the release of chemistry that subsequently prevents efficient microetch of the surface.

Table 10-47: Scratches

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Scratches on conductors	Target condition: no scratches Incidental superficial scratches are acceptable. Numerous superficial scratches indicating poor workmanship are not acceptable. Scratches exposing copper are not acceptable. Scratches causing smear of SnPb are not acceptable.	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Scratches on dielectric	Target condition: no scratches Incidental superficial scratches are acceptable. Numerous superficial scratches indicating poor workmanship are not acceptable. Scratches causing a sharp indentation or exposure of glass fibres (weave exposure) are not acceptable.		

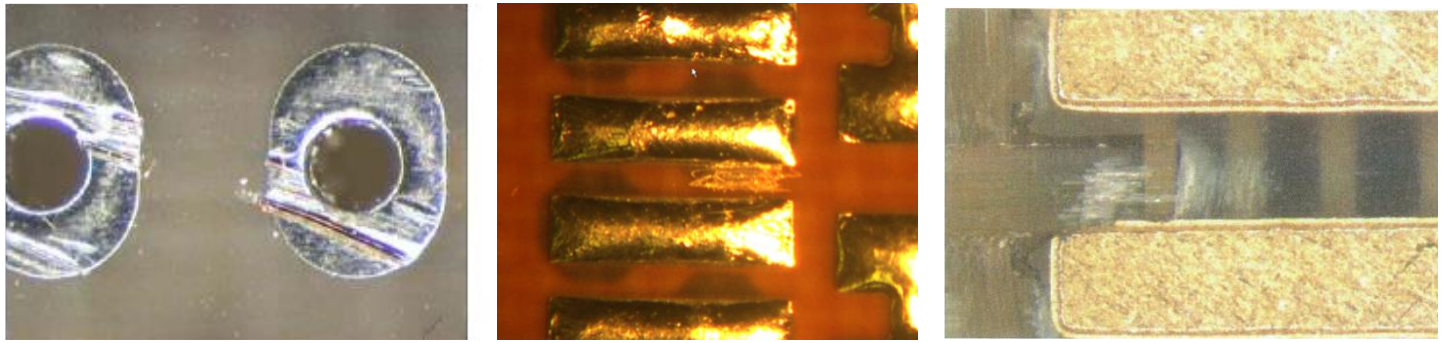


Figure 10-82: Example of scratches on conductors and dielectric

Note: The term scratch refers also to dents and indentations. A cut of conductors is evaluated as a scratch exposing copper. Intentional scratches caused by repair are covered by the clause 6.10. Exposed glass or re-enforcement in laminate not accepted, due to risk for moisture absorption.

Table 10-48: Weave exposure

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Weave exposure	Not acceptable in external layers Acceptable in depth controlled milling or drilling	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Weave texture	Acceptable		
no example pictures available				

Note 1: It can be difficult to distinguish weave texture from weave exposure. See IPC-A-600K clause 2.2.2.

Note 2: Weave exposure is accepted in depth controlled milling and drilling for cavities or countersink or counterbore holes. This is permitted because it is intentional and controlled by design and process.

Table 10-49: Haloing at PCB edge and non-plated holes

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Haloing adjacent to tracks, pads and planes	≤ 1,5mm into rigid section, and ≤ 50% of the insulation between edge of rigid section to pattern on external layer and the underlying layer.	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Haloing adjacent to footprint for stiffener	≤ 90% of the insulation between edge of rigid section to pattern on external layer, and ≤ 50% of the insulation between edge of rigid section to pattern on the underlying layer		

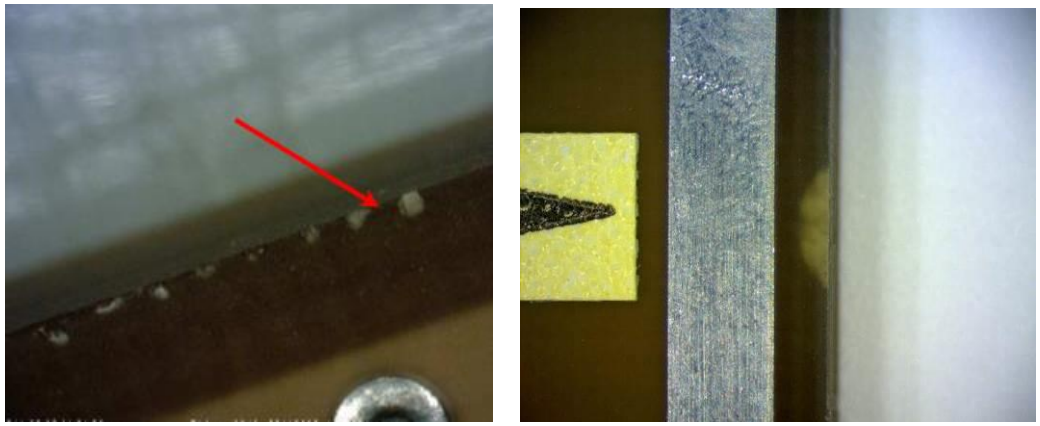


Figure 10-83: Haloing at edge

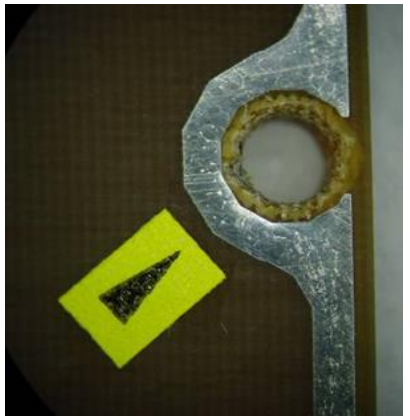


Figure 10-84: Haloing from non-plated hole to footprint for stiffener

Note 1: Depanelisation by cutting of support tabs can cause haloing.

Note 2: PCB edge can also include the edge of non-plated mechanical holes, cut-outs and depth-controlled milling.

Note 3: In case the minimum allowed insulation distance from conductor to PCB edge from clause 14.3.1 of ECSS-Q-ST-70-12 is used, there is almost no allowance for haloing. This is not considered reliable design and is typically indicated as risk factor during MRR.

Note 4: Any haloing at via holes and PTH is handled as a dielectric crack, or possibly measling, crazing, delamination.

Table 10-50: Tin-lead surface quality

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Dewetting and non-wetting	Not accepted on solder pads	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Granular aspects in tin-lead	Accepted in case sample with granular aspect pass solderability test		

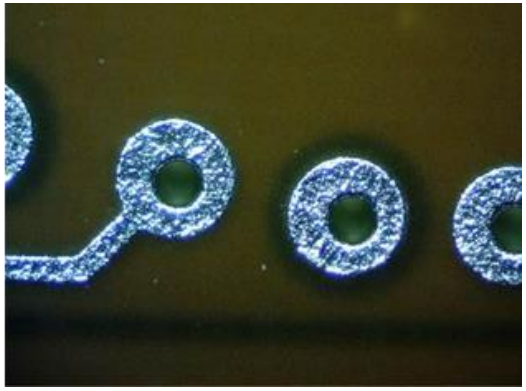


Figure 10-85: Granular aspect

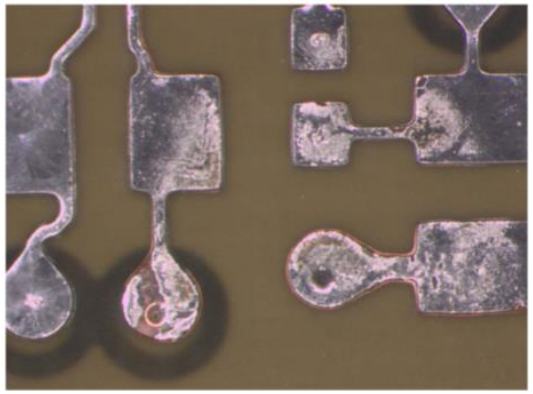


Figure 10-86: Dewetting

Note: Granular tin-lead is caused by the temperature profile during reflow.

Table 10-51: Marking, identification

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Marking quality	Clear and legible marking	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

Figure 10-87: Example of unclear marking

Table 10-52: Rigid-flex interface - misalignment of prepreg

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Resin squeeze out	≤ 1,5 mm	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	adhesive filet recession	≤ 0,5 mm into rigid section		

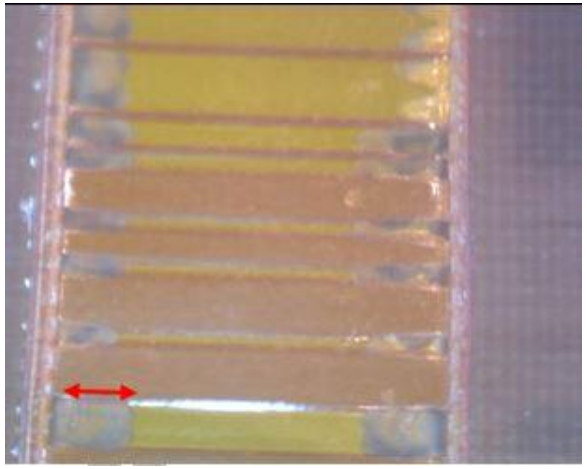


Figure 10-88: Example of resin squeeze out

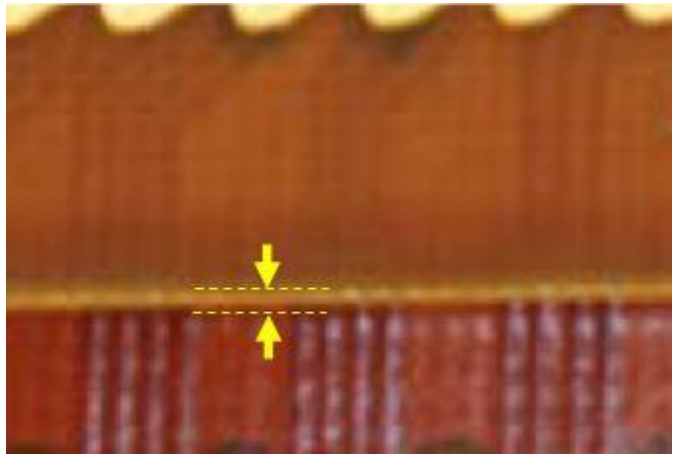


Figure 10-89: Example of adhesive filet recession into rigid section as observed in visual inspection

Note: Resin can be squeezed out of the prepreg during lamination and flow onto the coverlay of the flex section.

Table 10-53: Rigid-flex interface - fibre protrusion

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Fibre protrusion	Target condition: smooth edge incidental fibre protrusion ≤ 1,5 mm is acceptable	Location: PCB, rigid-flex coupon Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

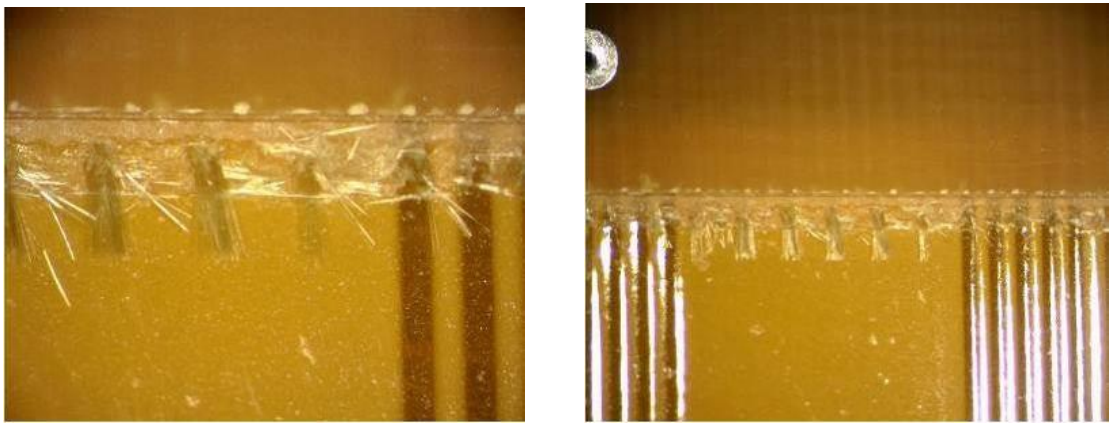


Figure 10-90: Examples of fibre protrusion

Note: Fibre protrusion can be caused by milling when resin is removed but fibres are not cut cleanly.

Table 10-54: Rigid-flex interface - haloing

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Haloing	≤ 1,0 mm into rigid section, and ≤ 50 % of the insulation between edge of rigid section to pattern on external layer and the underlying layer.	Location: PCB, rigid-flex coupon Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

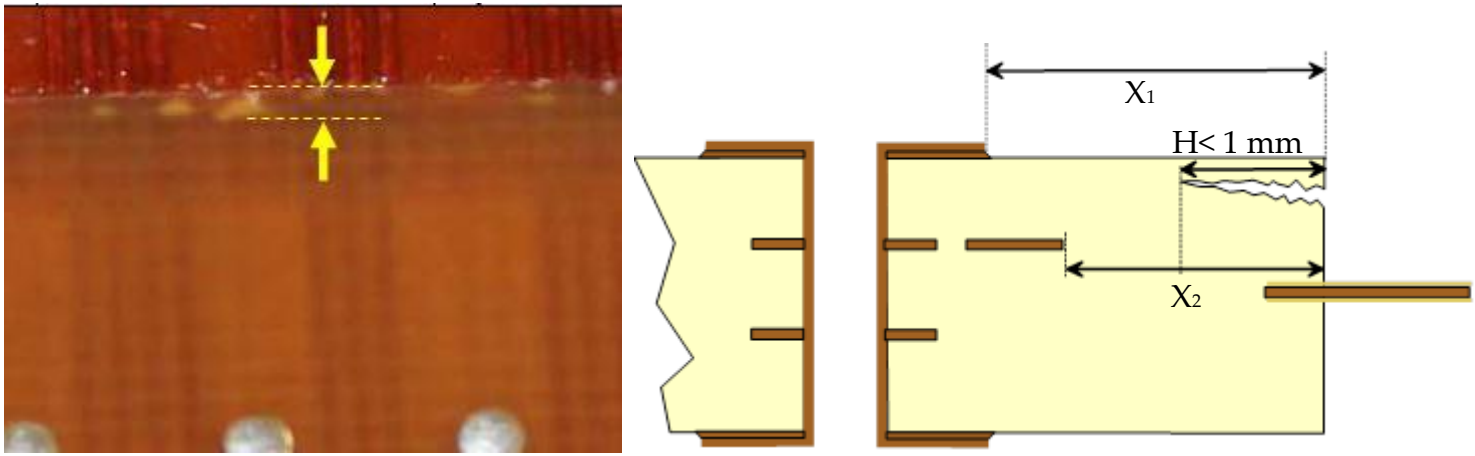


Figure 10-91: Example of acceptable incidental haloing ≤ 1 mm into rigid section

Note 1: Haloing can be seen on all rigid edges. At the rigid-flex interface haloing can be caused by the unsupported milling process. It is good practice to allow for haloing on rigid-to-flex interface and other PCB edges when designing insulation distance from the pattern on external layer and the underlying layer to the edge.

Note 2: Smallest distance of via to rigid-flex-interface is 2 mm, thus X1 is 1,9 mm, thus H can be up to 1,0 mm, which leaves 0,9 mm remaining insulation distance. Smallest distance X2 of internal layer to rigid-flex interface is as for conductor to hole wall which is 154 µm as manufactured (180 as designed), which gives almost no allowance for haloing. It is needed that the design does not include any conductor (plane of track) closer to the rigid-flex interface than the nearest via.

Table 10-55: Rigid-flex - aspect of flex laminate and coverlay

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Scratches, folding marks, blistering, nicks, contamination, voids, white spots	Target condition of coverlay is without defect. An incidental defect is acceptable in accordance with the criteria specified hereunder.	Location: PCB, rigid-flex coupon Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Scratches, cuts	Accepted if superficial scratch Not accepted if a cut causes a sharp indentation or exposed copper		
c.	Folding marks	Accepted if remaining insulation distance is in conformance with PCB definition dossier.		
d.	Blistering (bubbles)	Accepted if remaining insulation distance is in conformance with PCB definition dossier.		
e	Delamination	not acceptable		
f.	Nicks and burrs on flex edge	acceptable if ≤ 50 % of the insulation between edge of flex section to pattern		
g.	Tear on flex edge	not acceptable		
h.	Voids or pinhole in the kapton of the coverlay	Voids or pinholes are acceptable in case: They are not above or exposing the copper circuit. They are not reducing insulation distance below the requirement specified in the PCB definition dossier.		
i.	Contamination below coverlay	Accepted if remaining insulation distance is in conformance with PCB definition dossier.		
j.	Voids in adhesive from coverlay	Voids of ≤ 80 µm are acceptable in case the insulation distance is in conformance with the PCB definition dossier		
k.	White spots below coverlay	Accepted if remaining insulation distance is in conformance with PCB definition dossier.		
l.	Resin spots on coverlay	Accepted if incidental and well adhered to coverlay.		

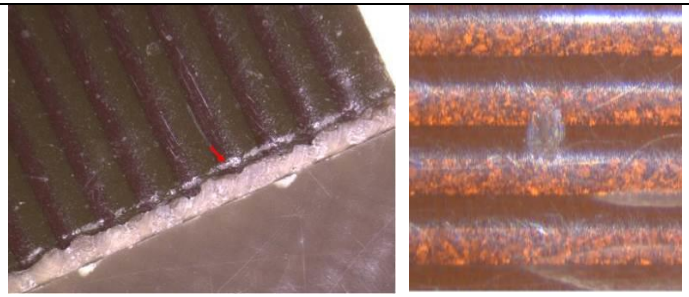


Figure 10-92: Example of an acceptable superficial scratch (left) and a resin spot on coverlay (right)

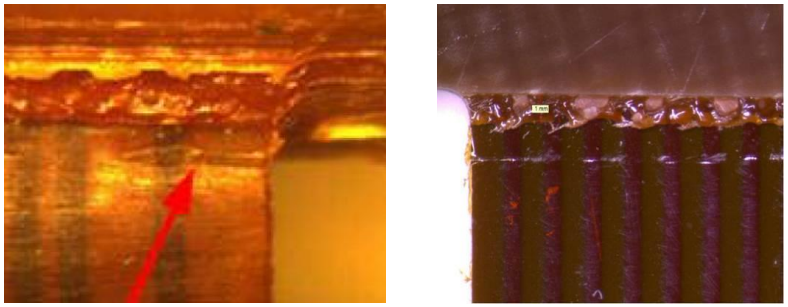


Figure 10-93: Examples of non-acceptable cut and blister, evident by a sharp indentation

Figure 10-94: Examples of burrs on edge of flex

Note 1: The PCB definition dossier is in conformance with the DRD of ECSS-Q-ST-70-12 Annex A. The insulation distance specified in the PCB definition dossier is in conformance with ECSS-Q-ST-70-12 Table 13-7.

Note 2: The procurement specification for coverlay is IPC-4203. Chapter 3.5.4. of this specification allows voids up to 75 µm. It is the PCB manufacturer's responsibility to meet the requirement of this table.

Note 3: Voids in coverlay can be caused by the PCB manufacturer due to mechanical stress.

Note 4: See requirement B.2.1.1c.

Table 10-56: Solder mask

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Solder mask in vias and PTH	Not accepted	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Solder mask on pads	Not accepted for NSMD pads		
c	Voids, missing solder mask	Incidental missing solder mask and voids are acceptable on laminate provided that it does not reduce insulation distance below the specification from the PCB definition dossier. Incidental missing solder mask and voids are acceptable on conductive elements provided that bare copper is not exposed.		
d.	Inclusions	Incidental inclusions are acceptable provided that it does not reduce insulation distance below the specification from the PCB definition dossier.		
e.	Blistering	Not acceptable		
(no example pictures available)				
Note 1: Ref A in this table meets the conditions of requirement 7.8.2.2a of ECSS-Q-ST-70-12, which forbids the use of tented vias. Note 2: Solder mask is hampering visual inspection of the dielectric material on outer layers.				

10.5 Visual inspection of sculptured flex PCB

ECSS-Q-ST-70-60_1390642

a. For the technological feature misregistration of holes for sculptured flex PCB the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-57.

ECSS-Q-ST-70-60_1390643

b. For the technological feature aspect of coverlay for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-58.

ECSS-Q-ST-70-60_1390644

c. For the technological feature tin-lead infiltration for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-59.

ECSS-Q-ST-70-60_1390645

d. For the technological feature bare copper for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-60.

ECSS-Q-ST-70-60_1390646

e. For the technological feature misregistration between pads for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-61.

ECSS-Q-ST-70-60_1390647

f. For the technological feature annular ring for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-62.

ECSS-Q-ST-70-60_1390648

g. For the technological features conductor width and spacing for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-63.

ECSS-Q-ST-70-60_1390649

h. For the technological feature adhesive in plated holes for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-64.

ECSS-Q-ST-70-60_1390650

i. For the technological feature aspect of pads for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-65.

ECSS-Q-ST-70-60_1390651

j. For the technological features copper wrinkle for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-66.

ECSS-Q-ST-70-60_1390652

k. For the technological features aspect of mechanical holes and edge of coverlay for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-67.

ECSS-Q-ST-70-60_1390653

l. For the technological feature scratch on coverlay for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-68.

ECSS-Q-ST-70-60_1390654

m. For the technological feature aspect of finger after bending for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-69.

ECSS-Q-ST-70-60_1390655

n. For the technological feature marking adhesion strength for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-70.

ECSS-Q-ST-70-60_1390656

o. For the technological feature microsection for sculptured flex PCB, the acceptance criteria, the inspection samples and the measurement method shall be in conformance with Table 10-71.

ECSS-Q-ST-70-60_1390657

Table 10-57: Sculptured flex - misregistration of holes

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Misregistration of coverlayers	Acceptable if hole diameter is in conformance with PCB definition dossier	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Misregistration of hole to conductor	Acceptable if distance D between hole and conductor is ≥ 0,4 mm		

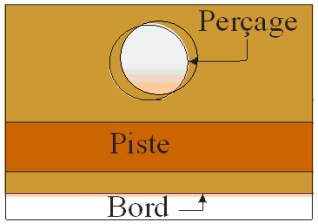


Figure 10-95: Misregistration of top and bottom coverlay

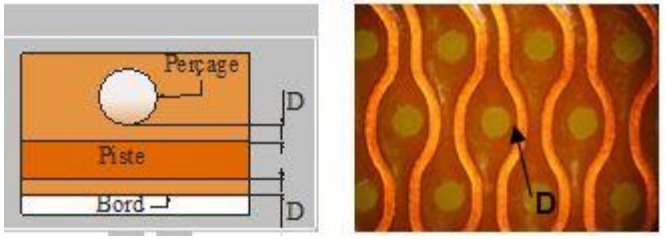
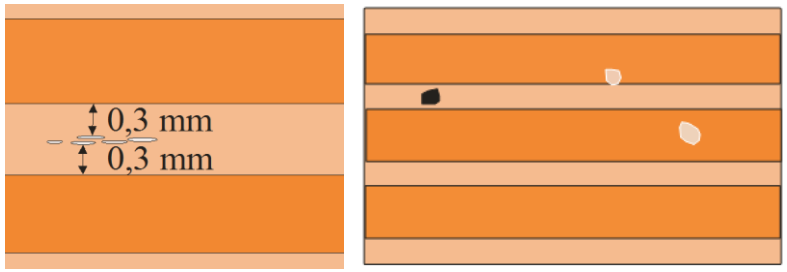


Figure 10-96: Misregistration of hole in coverlay to the conductor

Table 10-58: Sculptured flex - aspect of coverlay that insulates copper tracks

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Scratches, folding marks, blistering, nicks, contamination, voids, white spots	Target condition of coverlay is without defect. An incidental defect is acceptable in accordance with the criteria specified hereunder.	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Scratches, cuts	Accepted if superficial scratch Not accepted if a cut causes a sharp indentation or exposed copper		
c.	Folding marks	Accepted if remaining insulation distance is in conformance with PCB definition dossier.		
d.	Blistering (bubbles)	not acceptable		
e	Delamination	not acceptable		
f.	Nicks and tears	≤ 50 % of the insulation between edge of flex section to pattern		
g.	Voids or pinhole in coverlay	Voids or pinholes are acceptable in case: They are not above or exposing the copper circuit. They are not reducing insulation distance below the requirement specified in the PCB definition dossier.		
h.	Black spot contamination below coverlay	acceptable if: • remaining insulation distance in conformance with PCB definition dossier • maximum two black spots per PCB		
i.	Fibre contamination below coverlay	acceptable if remaining insulation distance in conformance with PCB definition dossier		
j.	Voids in adhesive	Incidental voids of ≤ 80 µm are acceptable in case the insulation distance is in conformance with the PCB definition dossier		
k.	White spots below coverlay	Acceptable if: • remaining insulation distance is in conformance with PCB definition dossier • distance to the edge of a conductor is ≥ 0,3 mm • maximum two white spots per PCB		



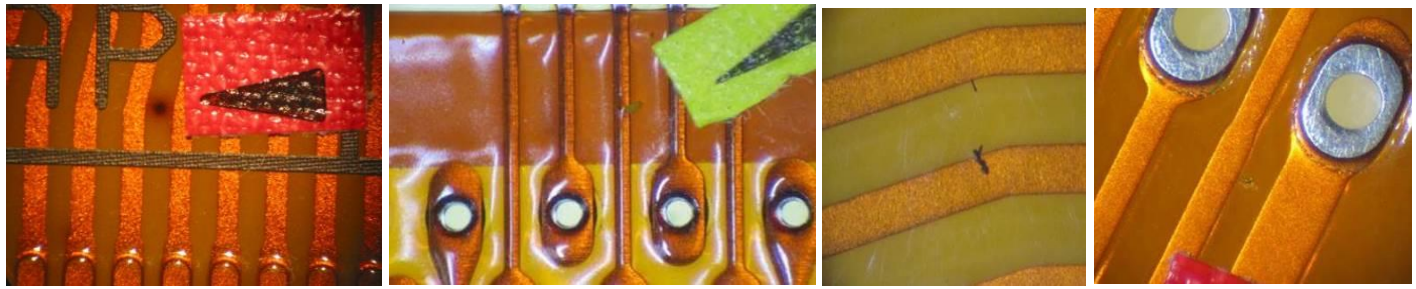


Figure 10-97: Examples of white spot configurations and black spot contamination

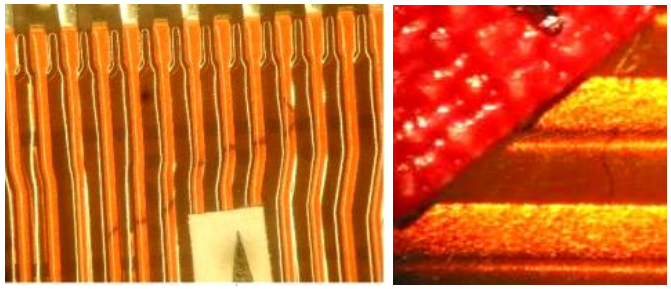


Figure 10-98: Examples of fibre contamination

Note: A second coverlay can be used as mechanical reinforcement, applied on a first coverlay for electrical insulation of tracks. The title of this table clarifies that these requirements apply only to the first coverlay, and not to the second.

Table 10-59: Sculptured flex - SnPb infiltration

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	SnPb infiltration below coverlay	Not acceptable	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

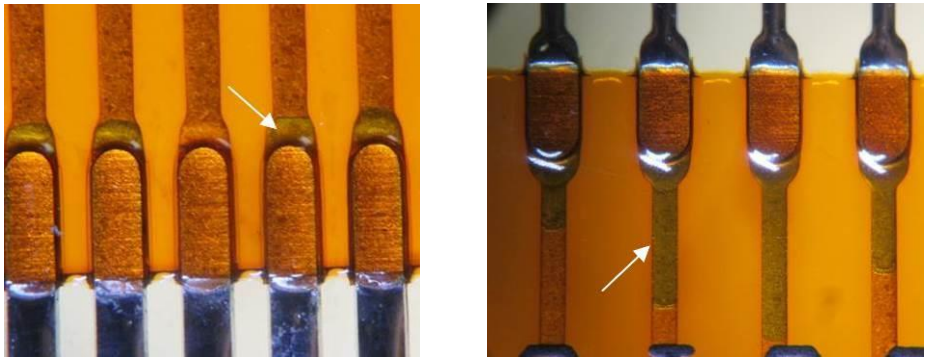


Figure 10-99: Examples of SnPb infiltration on sculptured pad (left) and on tracks (right)

Table 10-60: Sculptured flex - bare copper on fingers and pads

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Bare copper on fingers and pads	Not acceptable	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

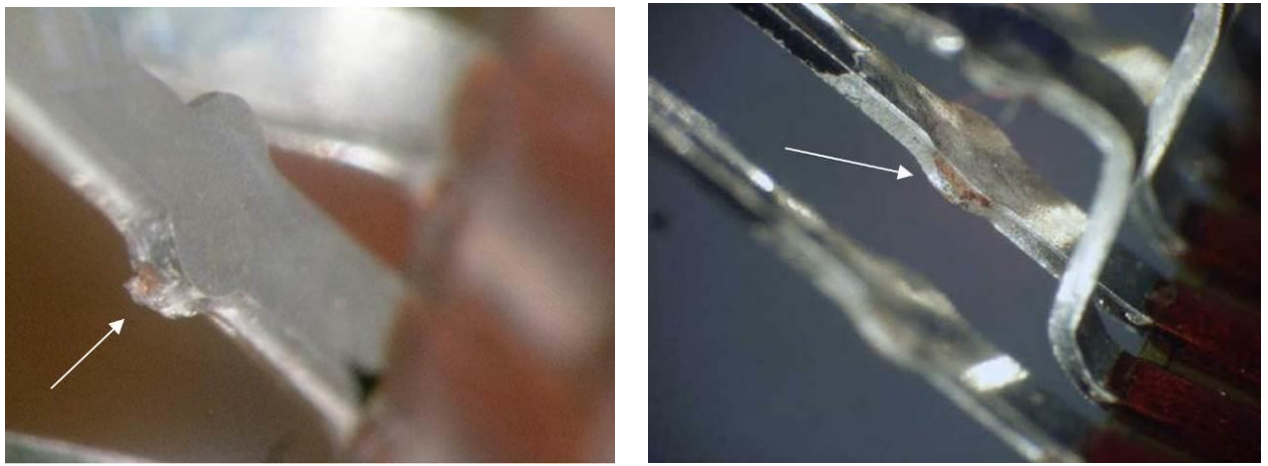


Figure 10-100: Bare copper on fingers

Table 10-61: Sculptured flex – misregistration between pads

Ref.	technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Misregistration between top and bottom pads	Acceptable if • misregistration ≤ 100 µm • insulation distance D between pad and conductor in conformance with PCB definition dossier	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

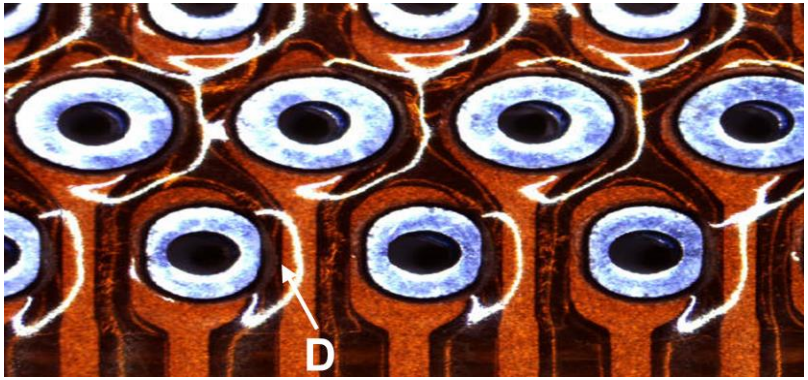


Figure 10-101: Misregistration of pads

Table 10-62: Sculptured flex – annular ring

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Annular ring on oblong pad on solder side	≥ 150 µm on smallest side ≥ 250 µm on largest side	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Annular ring on circular pad on solder side	≥ 250 µm		
c.	Annular ring on component side	Tangency acceptable in case no adhesive inside the hole, in conformance with 8.7.5e of ECSS-Q-ST-70-12		

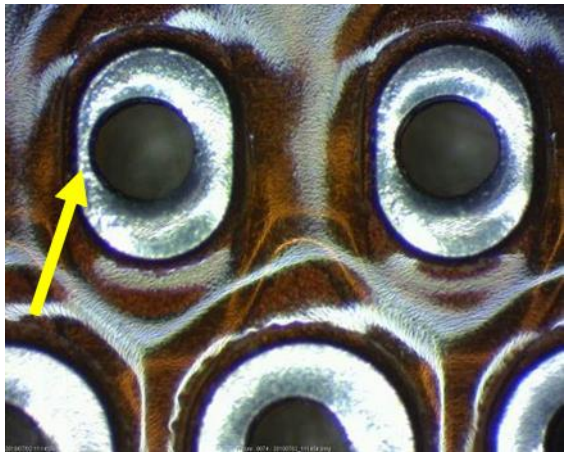
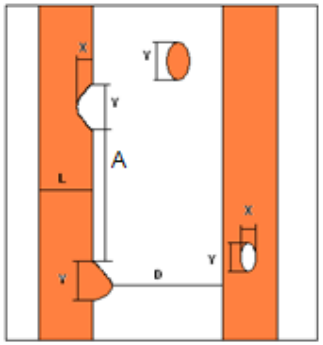


Figure 10-102: Hole misregistration causing reduced annular ring

Table 10-63: Sculptured flex - copper conductor width and spacing

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Nicks, peaks and pinholes on conductors	Acceptable if all the following are met For designed conductor width ≤ 0,8 mm • X ≤ 25 % of L • Y ≤ 0,5 mm • Z ≤ 50 % of designed conductor thickness • distance A between two defects is ≥ 5 mm For designed conductor width ≥ 0,8 mm • X ≤ 20 % of L • X ≤ 0,25 mm • Y ≤ 1 mm • Z ≤50 % of designed conductor thickness • distance A between 2 defects is ≥ 5 mm	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.	Peaks and copper residue	Acceptable if For designed conductor thickness ≥ 250 µm • insulation distance D ≥ 300µm For designed conductor thickness ≥ 200µm • insulation distance D ≥ 250µm For designed conductor thickness ≥ 150µm • insulation distance D ≥ 200µm		
c.	Copper residue to the edge of the flex	Acceptable if insulation distance D ≥ 400µm between residue and edge of flex		
d.	Bump on conductor due to local insufficient etching	Acceptable		

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
e.	Conductor width and spacing	Tolerance of conductor width and spacing is ≤ 20 % in conformance with Table 7-3 from ECSS-Q-ST-70-12		



X: width of defect
Y: length of defect
L: conductor width
D: insulation distance
Z: depth of pinhole
A: distance between

Figure 10-103: Schematic of conductor width and spacing and local defects

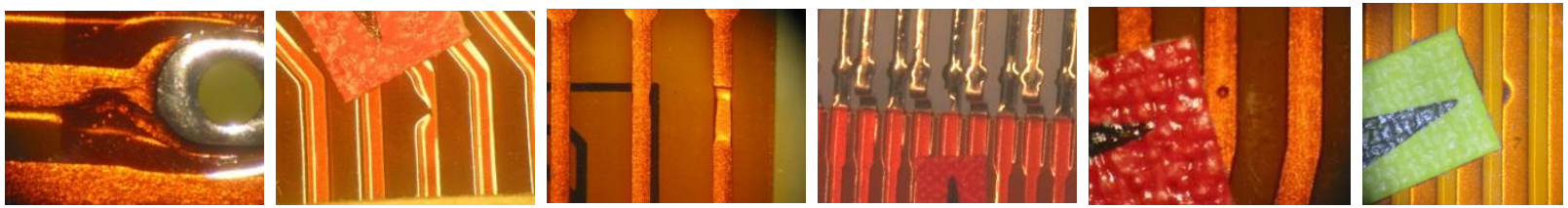


Figure 10-104: Examples of nick near pad, nick on conductor, overetching reducing thickness of conductor, nick on finger, pinhole and local reduced track width (left to right)

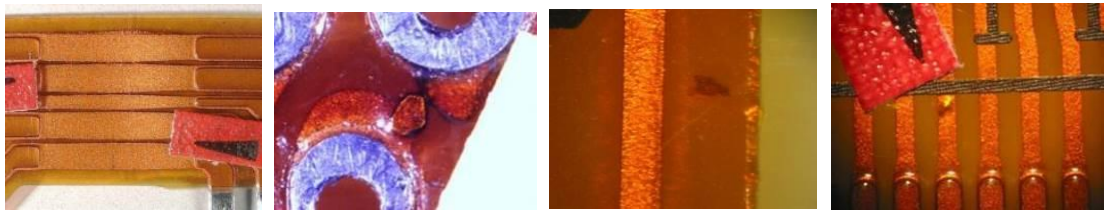


Figure 10-105: Examples of insufficient spacing between conductors, copper residue between pads, copper residue to edge of flex, bump on conductor (left to right)

Table 10-64: Adhesive in plated holes

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Adhesive in plated holes	Acceptable if hole diameter is in conformance with PCB definition dossier	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

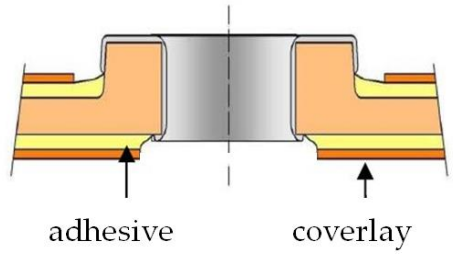
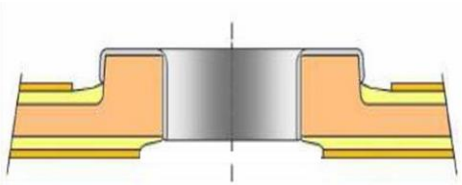
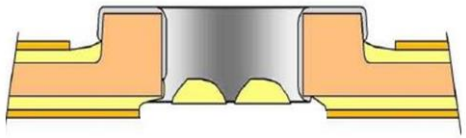
PREFERRED	ACCEPTED	REJECT
No adhesive on the edge of the hole  	Flow of adhesive on the edge of the hole, not reducing its diameter below the requirement 	Flow of adhesive in the hole, reducing its diameter below the requirement 

Figure 10-106: Adhesive in plated holes

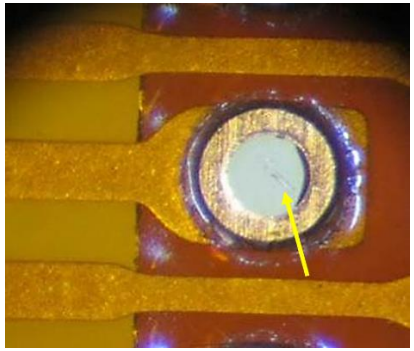


Figure 10-107: Example of adhesive in plated holes

Table 10-65: Sculptured flex – aspect of pads on solder side

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Absence of SnPb on pads; Pad diameter reduction due to coverlay or adhesive	Remaining circular pad width ≥ 250 µm Remaining pad width on smallest side of oblong pad ≥ 150 µm Remaining pad width on largest side of oblong pad ≥ 250 µm	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

PREFERRED	ACCEPTED	REJECT
Full coverage of SnPb on pads	Partial coverage of SnPb on pads. Remaining pad width: ≥ 250 µm	Partial coverage of SnPb on pads. Remaining pad width: < 250 µm

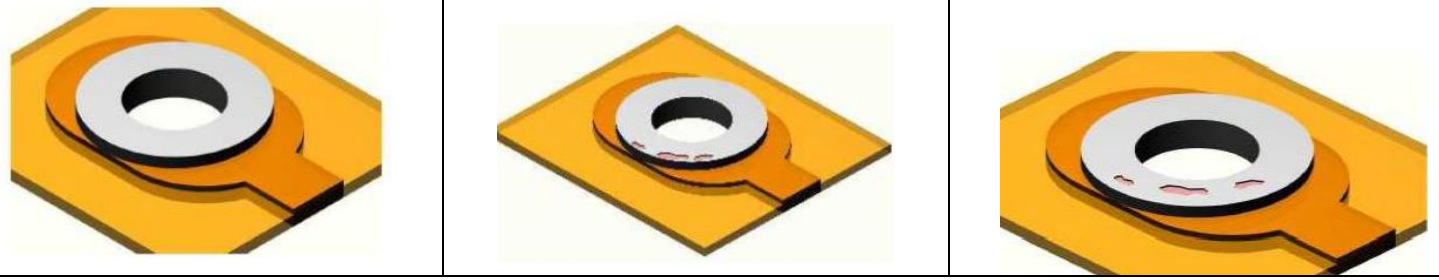


Figure 10-108: SnPb coverage on pads

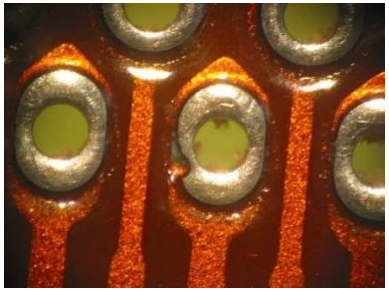


Figure 10-109: Pad diameter reduction due to local coverage by coverlay or resin squeeze out

Table 10-66: Sculptured flex - copper wrinkle

Ref.	technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Copper wrinkle	Not acceptable	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

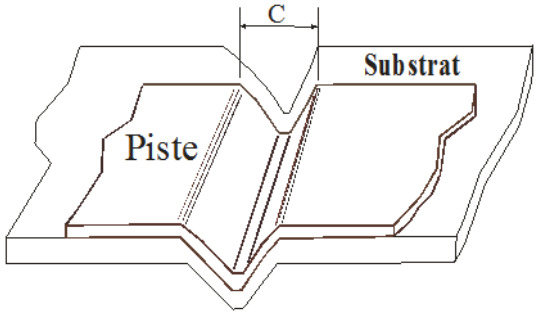


Figure 10-110: Copper wrinkle

Table 10-67: Sculptured flex – aspect of mechanical holes and edge of coverlay

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	nick, burr, tear in mechanical hole in coverlay or on edge of coverlay	Tear not acceptable.	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x
b.		Target condition: no burrs Incidental burr on hole acceptable in case diameter meets PCB definition dossier.		
c.		Target condition: no nicks Incidental nick on edge acceptable in case remaining insulation distance to copper ≥ 0,4 mm		

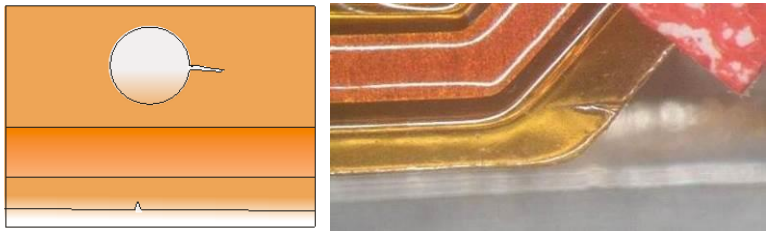


Figure 10-111: Tear in hole and edge of coverlay

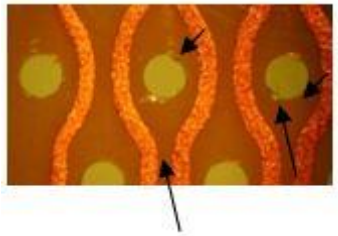


Figure 10-112: Burrs on holes

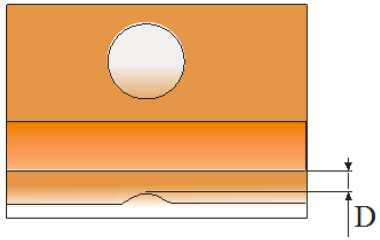


Figure 10-113: Nick on edge of coverlay

Table 10-68: Sculptured flex – scratch on coverlay

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Scratches, cuts	Accepted if superficial scratch Not accepted if a cut causes a sharp indentation or exposed copper	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

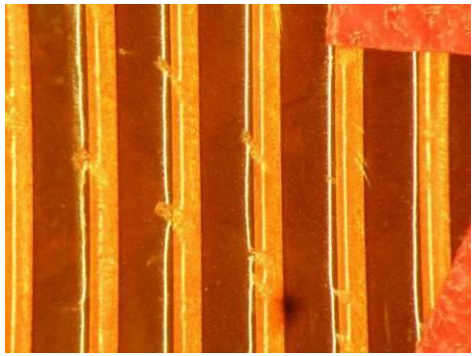


Figure 10-114: Coverlay scratch – Non acceptable

Table 10-69: Sculptured flex - aspect of finger after bending

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Aspect of finger after bending and SnPb coverage	Exposed copper not acceptable Copper crack not acceptable	Location: PCB Condition: AR Frequency: 100 %	Visual inspection magnification ≥ 10x

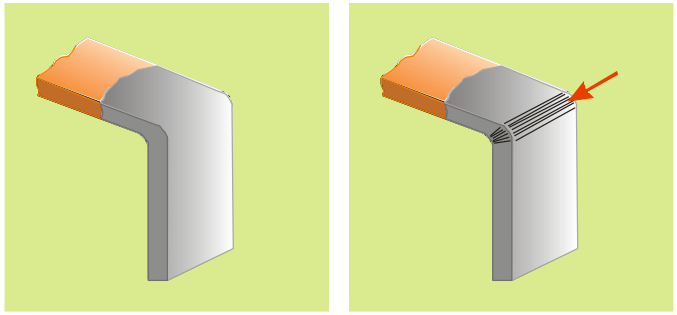


Figure 10-115: Acceptable aspect of finger after bending

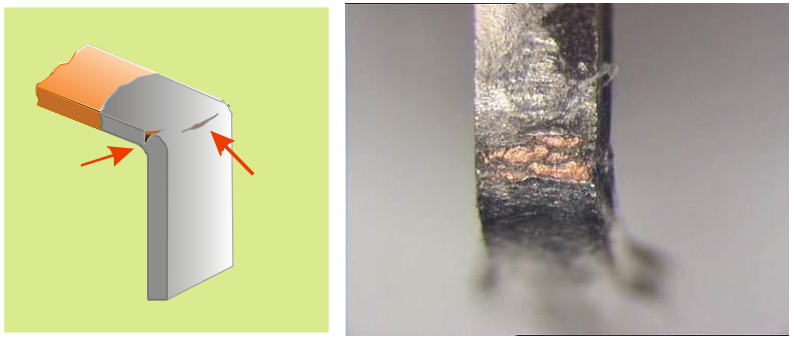


Figure 10-116: Unacceptable aspect of finger after bending

Table 10-70: Sculptured flex - marking adhesion strength

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Marking adhesion strength	No lift of marking	Location: PCB Condition: AR Frequency: 1 per batch	See clause 9.4.5

Table 10-71: Sculptured flex - microsection

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method
a.	Bulk Copper Thickness	As per PCB definition dossier with a tolerance of ± 25 µm	Location: coupon Condition: AR Frequency: 1 per batch	Microsection and Microscope: Magnification: ≥ 200x Illumination: bright and dark field
b.	Copper Conductor Thickness	As per PCB definition dossier with a tolerance of ± 25 µm		
c.	Kapton Base and Coverlay Thickness	25 µm ± 5µm		
d.	Overall Assembly Thickness (No Conductor)	Calculated		
e.	Overall Assembly Thickness (With Conductor)	Calculated		
f.	Tin-Lead Thickness on Surface	7 µm minimum		
g.	Tin-Lead Thickness in Hole	5 µm minimum		
h.	Tin-Lead Thickness on Corners	1 µm minimum		
i.	Tin-Lead infiltration	infiltration under coverlay layer not acceptable	Location: coupon / PCB Condition: AR+RW 3 heating cycles at 330°C See Note 2 Frequency: 1 per panel	
j.	Annular ring is inspected as per Table 10-62			
"Calculated" indicates the addition of individual elements of the build-up.				

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method

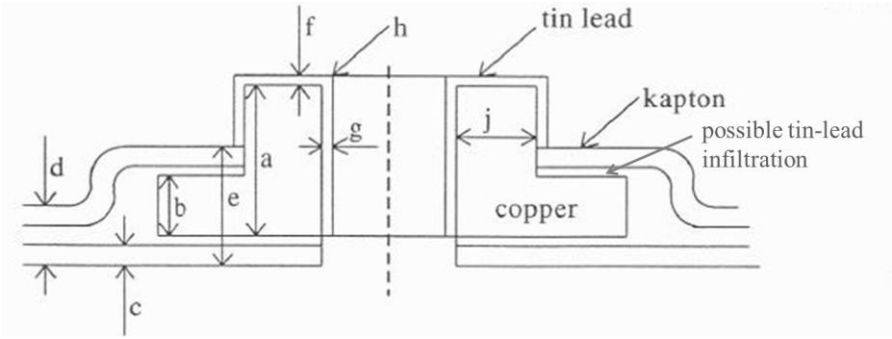


Figure 10-117: Cross-section of hole: Copper conductor shown

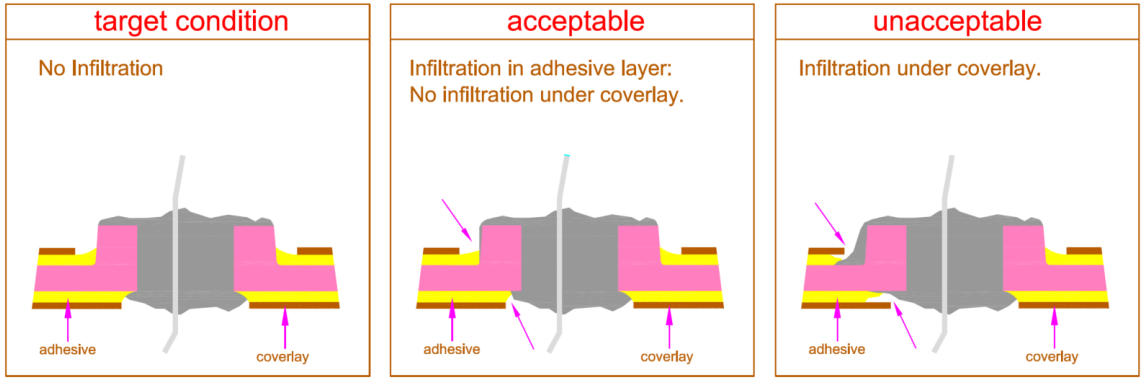


Figure 10-118: Tin-lead infiltration

Ref.	Technological feature	Acceptance criteria	Procurement inspection sample	Measurement method

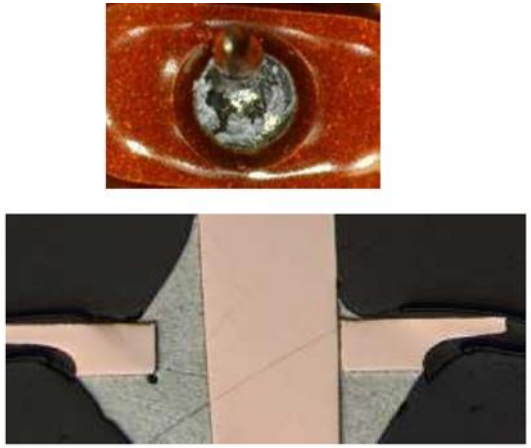


Figure 10-119: Target condition

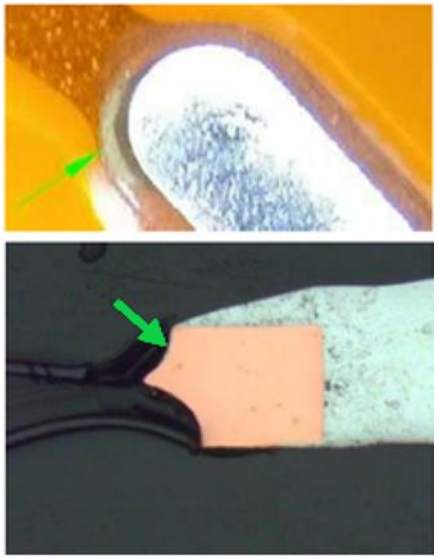


Figure 10-120: Acceptable infiltration of Tin-Lead in adhesive layer but not under coverlay layer

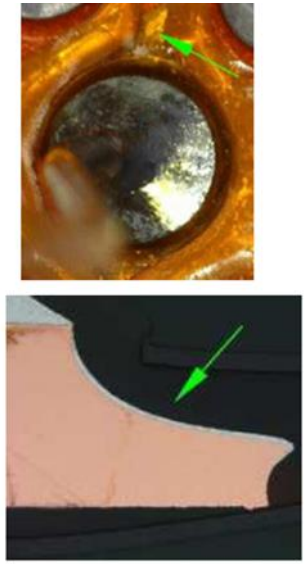


Figure 10-121: Unacceptable Tin-Lead infiltration under coverlay layer

Note 1: Ref. d. and e. have been derived to ensure full encapsulation of conductors and total air exclusion from the bond interface by the allowance of use of additional thickness of acrylic adhesive applied on a case by case basis dependent on circuit.

Note 2: Requirement 9.5.4.2d is tailored using a temperature at 330°C and the requirement 9.5.4.3l is tailored using 3 heat cycles in total.

10.6 Additional requirement to the tables

10.6.1 Annular ring

ECSS-Q-ST-70-60_1390672

a. Annular ring shall be measured excluding the copper plating, except in the case of requirement 10.6.1b.

ECSS-Q-ST-70-60_1390673

b. Annular ring on external layers shall be measured including the Cu plating.

NOTE The measurement method for annular ring is indicated in Table 10-1 and Table 10-2. The reason to include Cu plating in annular ring measurement on external pads is to enable annular ring measurement by visual inspection, whereas the other type of annular ring measurements are performed using microsectioning.

ECSS-Q-ST-70-60_1390674

c. On layers without non-functional pad, the distance between the hole wall and the adjacent circuitry shall be in conformance with requirement 13.8.2g from ECSS-Q-ST-70-12.

NOTE This limits the misregistration of that layer, which cannot be measured without the presence of a pad.

ECSS-Q-ST-70-60_1390843

d. The internal annular ring may be ≥ 25 µm in case the panel includes registration coupons on all four corners for verification of annular ring in conformance with 8.2.3c of ECSS-Q-ST-70-60 and 7.5.3l of ECSS-Q-ST-70-12.

NOTE 1 The electrical coupon R from IPC-2221C allows for such verification. The IST coupon also includes a pattern for electrical registration. Alternatively the verification can be done by X-ray. Microscopic inspection of cross-sections only verifies in one direction and does not assess the full circumference.

NOTE 2 Requirement 7.5.3l of ECSS-Q-ST-70-12 includes teardrop reinforcement and identification of the review item for the PCB definition dossier. The requirement is specified for HDI technology. Therefore a PCB without microvias falls within the HDI technology in case it uses reduced annular ring.

NOTE 3 Table 10-6 and Table 10-27 specify that cracks and wicking cannot be more than the minimum annular ring.

NOTE 4 This requirement is valid for rigid and flex laminate. Larger movement of flex layers causes higher tolerances for annular ring. Therefore the requirement of 50 µm is reduced to 25 µm. However, this margin cannot be used to justify a design with a smaller pad diameter. The pad diameter is designed as if the annular ring was 50 µm, in conformance with the requirement 7.5.2h from ECSS-Q-ST-70-12.

NOTE 5 It is preferred to implement the electrical registration coupon on all corners of the panel, which is deemed a more efficient verification of annular ring compared to microsectioning on 2 opposite corners. To accommodate the recurrent designs without electrical registration coupons, the annular ring requirement of 50 µm is maintained for that technology.

10.6.2 Pad lift and associated laminate cracks

ECSS-Q-ST-70-60_1390675

a. Pad lift shall not be acceptable except for the case specified in Table 10-26.

NOTE In addition to the selected laminate material, the risk of pad lift further increases by the combination of thick PCBs with high layer count, small annular ring and a high amount of heat cycles representative of hand soldering, as performed by rework simulation. On technology prone to pad lift, it is good practice to design with large annular ring or to take other risk mitigations.

ECSS-Q-ST-70-60_1390676

b. Cracks in the laminate underneath SMT pads without via-in-pad shall be evaluated as dielectric cracks, in conformance with the Table 10-27.

NOTE SMT pads without via-in-pad are not included on coupons.

ECSS-Q-ST-70-60_1390677

c. The height of the pad lift shall be in conformance with Table 10-26.

ECSS-Q-ST-70-60_1390678

d. The height of the pad lift shall include adhesive separation between pad and resin as well as cracks or voids due to cohesive separation inside the dielectric.

ECSS-Q-ST-70-60_1390844

e. In case cohesive or adhesive separations are not clearly identifiable, the angle of the pad may be used to calculate the height of the pad lift.

ECSS-Q-ST-70-60_1390679

f. The parts of cracks or voids protruding from underneath the pad shall be evaluated as dielectric cracks in conformance with the Table 10-27.

ECSS-Q-ST-70-60_1390680

g. In case cracks associated with pad lift are observed on the coupon for procurement, conformance to Table 10-26 shall be evaluated after group 6 test for representative technology and recorded in the PID.

NOTE This provides an evaluation that the cracks associated with pad lift do not propagate until the hole wall after group 6, as done for qualification. Propagation of cracks until the hole wall increases the risk of further propagation along the hole wall and potential rupture of innerlayer connections.

ECSS-Q-ST-70-60_1390681

h. Cracks associated with pad lift shall not reach the hole wall before or after thermal stress.

ECSS-Q-ST-70-60_1390682

i. The parts of cracks or voids underneath the pad associated with pad lift shall not reduce the insulation distance to adjacent circuitry below the values specified by the PCB definition dossier, in the DRD of ECSS-Q-ST-70-12 Annex A.

NOTE 1 The insulation distance specified in the PCB definition dossier is in conformance with ECSS-Q-ST-70-12 Table 13-7.

NOTE 2 It is good practice that technology prone to pad lift is designed with margin such that the potential pad lift does not reduce the insulation between component holes and adjacent circuitry.

ECSS-Q-ST-70-60_1390683

j. Adjacent circuitry as specified in requirement 10.6.2i shall include the worst-case in the PCB.

NOTE In case tracks are routed in the PCB on layer 2 or layer N-1 underneath the external pad that can show pad lift or associated cracks, it is important to represent this in the coupon in conformance with requirement 15.2a from ECSS-Q-ST-70-12. In case such design is not represented on the coupon, the potential crack on the coupon cannot easily be assessed by the PCB manufacturer for its remaining insulation

distance to adjacent circuitry. In this case, it is important to perform FAI in conformance with requirement 15.2b from ECSS-Q-ST-70-12 and to include the theoretical worst-case adjacent circuitry of the PCB in the assessment from requirement 10.6.2j.

ECSS-Q-ST-70-60_1390684

k. A specific evaluation of possible anomalies of materials or processes shall be performed by the PCB manufacturer in case pad lift and associated cracks are observed on polyimide PCBs.

NOTE 1 This is specified because polyimide PCB have high Tg and are considered robust to thermal stress. Therefore it is not expected to see this defect and it can be an indicator of a process or material anomaly.

NOTE 2 Polyimide rigid-flex PCBs that use many layers of no-flow prepreg can be prone to pad lift due to high thermal expansion in Z-direction and low Tg of the material. Alternative processes or materials can be investigated with the PCB manufacturer to avoid pad lift.

10.6.3 Miscellaneous

ECSS-Q-ST-70-60_1390685

a. Any defects that are specified within ECSS-Q-ST-70-60 to be acceptable after group 6, shall also be acceptable after group 4.

ECSS-Q-ST-70-60_1390686

b. The plating in microvias shall be evaluated in conformance with Table 10-11 in high density and low density footprint.

NOTE Microvias in low density footprint are included in coupons from set 1 and set 2. Microvias in high density footprint are included in the IST coupon, which can be microsectioned after IST test.

ECSS-Q-ST-70-60_1390687

c. In case cracks are observed in microsections for procurement in conformance with Table 10-27 within the dimensional limitation specified for Ref. b and Ref. c, a referee test shall be performed by taking 4 additional microsections from a spare PCB from the same batch and by evaluation of conformance to Table 10-27.

ECSS-Q-ST-70-60_1390688

d. Remaining insulation distance shall be the sum of insulation distances to conductors that are not affected by cracks.

ECSS-Q-ST-70-60_1390689

e. Insulation from crack to adjacent conductor of less than 20 µm shall not be included in the calculation of remaining insulation distance for Ref. g from Table 10-27.

NOTE This is specified because cracks closer than 20 µm to a conductor are at risk to be in contact with the conductor out-of-plane from the microsection. In case the crack is further separated from adjacent conductors than 20 µm, the remaining insulation distance can be calculated by addition of the insulation on both sides of the crack to adjacent conductors. An example is shown in Figure 10-122, which is a zoom from Figure 10-49. In case both a) and b) are > 20 µm, the remaining insulation distance equals c) minus the length of the crack. In case a) is < 20 µm, the remaining insulation distance equals b).

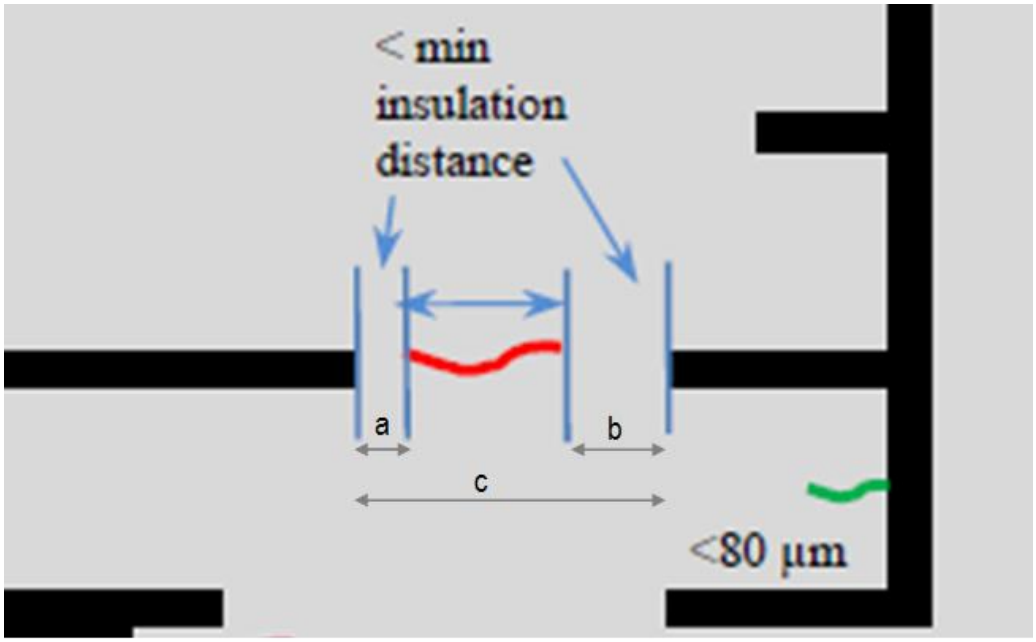


Figure 10-122: Calculation of remaining insulation distance

ECSS-Q-ST-70-60_1390690

f. PTH with a diameter of ≥ 0,6 mm shall meet the requirement for finished hole diameter from the PCB definition dossier.

NOTE These hole diameters cannot be reduced by a bulb of SnPb.

ECSS-Q-ST-70-60_1390845

g. Plated holes with a diameter < 0,6 mm may have a reduced diameter due to blocking with SnPb.

NOTE In some applications, such as for nano-D connectors, PTH are used with a diameter < 0,6 mm with SnPb surface finish. In this case it is

important to review the finished hole diameter. It is the responsibility of the PCB manufacturer in case such design is specified in the PCB definition dossier and accepted in the MRR, in which case it is good practice to raise it as a review item. Blocking with SnPb can also be a review item for larger hole diameters.

ECSS-Q-ST-70-60_1390846

h. Coverlay and its adhesive may partly cover the pad of flexible PCBs in case the annular ring is in conformance with clause 8.5.1 from ECSS-Q-ST-70-12 and Ref. d from Table 10-2.

NOTE Minimum annular ring is 250 µm on a component hole and 100 µm on a non-soldering hole.

ECSS-Q-ST-70-60_1390847

i. The customer may specify a requirement for maximum copper thickness in the PCB definition dossier.

NOTE ECSS-Q-ST-70-60 and ECSS-Q-ST-70-12 do not specify a maximum copper thickness for plated layers. This could be important for HDI layers, thermal performance of PCBs or for RF applications. Copper thickness on plated layers (internal/external) can be influenced by pattern design and value above maximum are acceptable in case all other requirements like dielectric thickness, undercut, conductor width/space are achieved.

ECSS-Q-ST-70-60_1390691

j. In case of overhang of Au or Ni/Au in conformance with Table 10-15, the assembled PCB shall be conformal coated.

NOTE Overhang occurs when Au or Ni/Au is plated before etching. To avoid overhang, the plating can occur after etching, in which case the circuit to be plated is designed to enable electrical connection. Brushing of overhang is not allowed in conformance with requirement 6.10.2n and its note. Other surface finishes, such as ENEPIG, are available that do not cause any overhang. This is necessary on RF PCBs in case conformal coating is not desired.

Annex A (normative) Qualification letter – DRD

A.1 DRD identification

A.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60, requirement 5.12a.

A.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the qualification letter.

A.2 Expected response

A.2.1 Scope and content

ECSS-Q-ST-70-60_1390692

a. The qualification letter shall contain the following:
   1. Date of issue;
   2. Contact details of PCB manufacturer and qualification authority;
   3. Reference to request of qualification;
   4. Reference to evaluation test report;
   5. Reference to audit report;
   6. Reference to qualification test report;
   7. Qualified technology;
   8. PID reference;
   9. Qualification period.

A.2.2 Special remarks

None.

Annex B (normative) CoC for PCB – DRD

B.1 DRD identification

B.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60, requirement 8.3a.

B.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the CoC and its lab reports.

B.2 Expected response

B.2.1 Scope and content

B.2.1.1. CoC for PCB

ECSS-Q-ST-70-60_1390693

a. The CoC shall contain the following:
   1. Declaration of conformance, in conformance with B.2.1.2;
   2. Lab report for visual inspection of PCBs for qualitative aspects, in conformance with B.2.1.3;
   3. Lab report for visual inspection of PCBs for dimensional verification, in conformance with B.2.1.4;
   4. Lab report for microsection of coupons for qualitative aspects, in conformance with B.2.1.5;
   5. Lab report for microsection of coupons for dimensional verification, in conformance with B.2.1.6;
   6. Lab report for additional tests, in conformance with B.2.1.7.

ECSS-Q-ST-70-60_1390694

b. The CoC shall cover the batch or a subset.

ECSS-Q-ST-70-60_1390695

c. The CoC shall record the presence of the following:
   1. Microvia plating voids in conformance with Table 10-11;
   2. Voids or cracks in the resin of blind and buried vias inside zone A in conformance with Table 10-18;
   3. Dimple in blind via in conformance with Table 10-20;
   4. Voids and inclusions in copper plating and skip plating in conformance with Table 10-22;
   5. Resin voids in conformance with Table 10-24;

6. Pad lift and cracks associated with pad lift in conformance with Table 10-26;
7. Dielectric cracks in conformance with Table 10-27;
8. Separation between external copper foil and copper plating in conformance with Table 10-28;
9. Smear in conformance with Table 10-30;
10. Hole wall pull away or resin recession in conformance with Table 10-31;
11. Swirl or milky appearance in no flow prepreg and demarcation line in no flow prepreg and dotted interface line in conformance with Table 10-34;
12. Non-metallic contamination in microsection in conformance with Table 10-35;
13. Adhesive voids in rigid-flex interface in conformance with Table 10-37;
14. Non-metallic contamination or inhomogeneity in conformance with Table 10-46;
15. Scratches on conductor and scratches on dielectric in conformance with Table 10-47;
16. Granular aspect in tin-lead in conformance with Table 10-50;
17. Fibre protrusion in conformance with Table 10-53;
18. Aspect of flex laminate and coverlay in conformance with Table 10-55;
19. Voids, omissions or inclusions of solder mask in conformance with Table 10-56;
20. Aspect of coverlay for sculptured flex in conformance with Table 10-58;
21. Aspect of mechanical holes and edge of coverlay for sculptured flex in conformance with Table 10-67;
22. Scratch of coverlay for sculptured flex in conformance with Table 10-68.

NOTE 1 This is recorded in the CoC even if it is in conformance with the requirements from the tables to provide traceability. See column "present?" in Table B-2, Table B-4 and Table B-5. More details can be specified in the "comments" field of the tables.

NOTE 2 For example, this is important for KIP/MIP after assembly to ensure that blistering or voids in coverlay adhesive did not propagate.

B.2.1.2. Declaration of conformance

ECSS-Q-ST-70-60_1390696

a. The declaration of conformance shall include the following:

1. Declaration of conformance to ECSS-Q-ST-70-60;
2. Declaration of conformance to the PCB definition dossier;
3. Traceability reference to the PCB definition dossier from procurement authority including revision and issue number;
4. MRR reference;
5. In case of partial or noncompliance to B.2.1.2a1 or B.2.1.2a2 reference to waiver request;
6. Purchase order number from procurement authority;
7. Traceability reference from PCB manufacturer;
8. Date code, as per the following format: YYWW;
9. Quantity of delivered PCBs in the batch;
10. Serial numbers of delivered PCBs in the batch;
11. Signature from PCB manufacturer.

NOTE 1 Note to item 3: This traceability reference can be named ‘part number’.

NOTE 2: Note to item 7: This traceability reference can be named ‘batch code’.

NOTE 3 Note to item 8: YYWW indicates a two digit reference to year followed by a two digit reference to week number.

B.2.1.3. Lab report for visual inspection of PCBs for qualitative aspects

ECSS-Q-ST-70-60_1390697

a. Lab report for visual inspection of PCBs for qualitative aspects shall include the following:

1. Arbitrary defects of conductors and pads (mouse bites, dents, nicks, pinhole, unintentional pattern) in conformance with Table 10-42 and Table 10-43;
2. Lifting of conductor pattern in conformance with Table 10-44;
3. Copper or nickel visible on top surfaces in conformance with Table 10-44;
4. Corrosion of copper in conformance with Table 10-44;
5. Blistering or air bubbles in conformance with Table 10-45;
6. Delamination in conformance with Table 10-45;
7. Crazing and measling in conformance with Table 10-45;
8. Surface contamination or inclusion of foreign matter in conformance with Table 10-46;

9. Non-homogeneous colour of innerlayer copper in conformance with Table 10-46;
10. Scratches in conformance with Table 10-47;
11. Weave exposure in conformance with Table 10-48;
12. Haloing in conformance with Table 10-49;
13. SnPb surface quality in conformance with Table 10-50;
14. Marking in conformance with Table 10-51;
15. Coverlay registration and annular ring of terminations on flexible PCB in conformance with Ref. d from Table 10-2;
16. Rigid-to-flex interface, alignment of prepreg in conformance with Table 10-52;
17. Rigid-to-flex interface, fibre protrusion in conformance with Table 10-53;
18. Rigid-to-flex interface, haloing in conformance with Table 10-54;
19. Rigid-to-flex interface, aspect of flex laminate and coverlay in conformance with Table 10-55.

ECSS-Q-ST-70-60_1390698

b. The visual inspection of qualitative aspects shall include the review items from the MRR.

ECSS-Q-ST-70-60_1390699

c. The acceptance criteria for visual inspection for qualitative aspects shall cover all PCBs in the batch by providing a pass/fail evaluation.

NOTE Inspection and evaluation of requirements is performed on all PCBs in the batch, whereas the reporting provides a summary.

B.2.1.4. Lab report for visual inspection of PCBs for dimensional verification

ECSS-Q-ST-70-60_1390700

a. The sampling plan for performing visual inspection of PCBs for dimensional aspects shall be as specified in Table 8-1.

ECSS-Q-ST-70-60_1390701

b. The lab report for visual inspection for dimensional verification shall include the following:

1. the PCB thickness is a representative measurement;
2. the PCB length and width are representative measurements;
3. specific dimensional features from the PCB definition dossier are representative measurements;
4. the warp and twist are the maximum measurements recorded on the worst-case PCB;

5. diameter of plated and non-plated holes for all diameters is a pass/fail evaluation, except for < 0,6mm holes with SnPb in conformance with 10.6.3g;
6. external annular ring for all plated-hole types is a pass/fail evaluation;
7. external conductor width and spacing is a pass/fail evaluation for minimum width and spacing;
8. comparison of lay-out to the drawing for the presence of plated and non-plated holes and milling is a pass/fail evaluation.

NOTE 1 Comparison of lay-out to the drawing is performed as in-process inspection in conformance with 6.3g.

NOTE 2 Pass/fail evaluations provide an assessment of dimensions with respect to their tolerances specified in the PCB definition dossier.

NOTE 3 In case an external conductor is indicated as critical in the PCB definition dossier it can be inspected on all PCBs.

NOTE 4 Specific dimensional features can include cut-out or radius of PCB edge.

B.2.1.5. Lab report for microsection of coupons for qualitative aspects

ECSS-Q-ST-70-60_1390702

a. The lab report for microsection for qualitative aspects shall include the following:
   1. Via filling in conformance with Table 10-18;
   2. Cap lift and planarity in conformance with Table 10-19 and Table 10-20;
   3. Burrs and nodules in conformance with Table 10-21;
   4. Voids or inclusions in copper plating in conformance with Table 10-22;
   5. Wedge voids in conformance with Table 10-23;
   6. Resin voids in conformance with Table 10-24;
   7. Delamination, blistering, crazing, measling in conformance with Table 10-25;
   8. Pad lift in conformance with Table 10-26;
   9. Dielectric cracks in conformance with Table 10-27;
   10. Cracks and separation in copper in conformance with Table 10-28;
   11. ICD in conformance with Table 10-29;
   12. Smear in conformance with Table 10-30;
   13. HWPA and resin recession in conformance with Table 10-31;
   14. Nail heading in conformance with Table 10-32;
   15. CIC in conformance with Table 10-33;

16. Inhomogeneity in dielectric in conformance with Table 10-34;
17. Contamination or inclusion in conformance with Table 10-35;
18. Delamination between coverlay and prepreg in conformance with Table 10-36;
19. Adhesive voids in coverlay and bond-ply in conformance with Table 10-37;
20. Misalignment of prepreg in rigid-flex-interface in conformance with Table 10-38.

ECSS-Q-ST-70-60_1390703

b. The lab report for microsection for qualitative aspects shall include the review items from the MRR.

ECSS-Q-ST-70-60_1390704

c. The acceptance criteria for microsection for qualitative aspects shall cover all microsections of coupons in the batch by providing a pass/fail evaluation.

NOTE Inspection and evaluation of requirements is performed on all microsections of coupons in the batch, whereas the reporting provides a summary.

ECSS-Q-ST-70-60_1390705

d. The lab report for microsection for qualitative aspects shall include the following representative pictures of microsections covering the batch, except in case this is specifically waived by the customer in the PCB definition dossier:
   1. Overview of PTH after SB in dark field showing laminate integrity, build-up;
   2. 500x magnification after SB in bright field showing interconnect and absence of ICD;
   3. 500x magnification as received in bright field showing SnPb on corner;
   4. Overview of rigid-to-flex interface after SB in dark field showing laminate integrity and absence of delamination.

B.2.1.6. Lab report for microsection of coupons for dimensional verification

ECSS-Q-ST-70-60_1390706

a. The microsection of coupons for dimensional verification shall be performed for all panels.

ECSS-Q-ST-70-60_1390707

b. The summary in the lab report shall be for a representative measurement covering all panels.

ECSS-Q-ST-70-60_1390708

c. The lab report for visual inspection for dimensional verification shall include the following:
   1. Annular ring internal and external in conformance with Table 10-1 and Table 10-2;
   2. Copper foil thickness in conformance with Table 10-3;
   3. Copper plating thickness in conformance with Table 10-4;
   4. Etchback in conformance with Table 10-5;
   5. Wicking in conformance with Table 10-6;
   6. Wrap copper in conformance with Table 10-7;
   7. Dielectric thickness in conformance with Table 10-8 and Table 10-9;
   8. Microvias dimensions and plating voids in conformance with Table 10-10 and Table 10-11;
   9. SnPb thickness in conformance with Table 10-12;
   10. Electrolytic Ni and Au dimensions in conformance with Table 10-13;
   11. Undercut and overhang in conformance with Table 10-14 and Table 10-15;
   12. Dimensions of rigid-flex-interface in conformance with Table 10-16.

B.2.1.7. Additional tests

ECSS-Q-ST-70-60_1390709

a. The lab report for additional tests shall include the following:
   1. Solderability in conformance with 9.4.11 in case this is applicable as specified in Table 10-12;
   2. High resistance electrical test and continuity test in conformance with 9.3.7.2 and 9.3.8, including serial numbers of accepted PCBs;
   3. IST in conformance with 9.5.5.

B.2.2 Special remarks

The example test reports in Table B-1 to Table B-7 can be used.

Table B-1: Example of a declaration of conformance

Declaration of Conformance:	
☐ In conformance with ECSS-Q-ST-70-60	
☐ In conformance with PCB definition dossier	
Reference to waiver request, if applicable:	
MRR reference:	
Report reference number:	
Issue date of report:	
Purchase order:	
PCB Manufacturer & location:	
Customer Part Number (PCB definition dossier)	
PCB definition dossier and issue nr	
Batch code from PCB manufacturer	
Date code of PCB manufacture (YYWW)	
Serial number (S/N):	
Quantity ordered	
Quantity delivered	
Signature	

Table B-2: Example of a lab report for visual inspection of PCBs for qualitative aspects

Lab report for visual inspection of PCBs for qualitative aspects	Sampling	Requirement references	Value	Pass/ Fail	Present? as per B.2.1.1c
Arbitrary defects of conductors, and pads (mouse bites, dents, nicks, pinhole, unintentional pattern)	100%	Table 10-42 + Table 10-43	-		-
Lifting of conductor pattern	100%	Table 10-44	-		-
Copper or nickel visible on top surface	100%	Table 10-44	-		-
Corrosion of copper	100%	Table 10-44	-		-
Blistering or air bubbles	100%	Table 10-44	-		-
Delamination	100%	Table 10-45	-		-
Crazing and measling	100%	Table 10-45	-		-
Surface contamination or inclusion of foreign matter	100%	Table 10-46	-		-
Non-homogeneous colour (oxidation of innerlayer copper, white spots)	100%	Table 10-46	-		
Scratches	100%	Table 10-47	-		
Weave exposure	100%	Table 10-48	-		-
Haloing	100%	Table 10-49	-		-
SnPb surface quality	100%	Table 10-50	-		
Marking	100%	Table 10-51	-		-
Coverlay registration and annular ring of terminations on flexible PCB	100%	Table 10-2	-		-
Rigid-to-flex interface, alignment of prepreg	100%	Table 10-52	-		-
Rigid-to-flex interface, fibre protrusion	100%	Table 10-53	-		
Rigid-to-flex interface, haloing	100%	Table 10-54	-		-
Rigid-to-flex interface, aspect of flex laminate and coverlay	100%	Table 10-55	-		
Solder mask	100%	Table 10-56			
Review items from MRR	100%	B.2.1.3b	-		-
Comments:					

Table B-3: Example of a lab report for visual inspection of PCBs for dimensional verification

Lab report for visual inspection of PCBs for dimensional verification	**Sampling 1 PCB/panel**	**Requirement references**	**Value**	**Pass/ Fail**
PCB thickness, ☐ over laminate, ☐ over surface finish	s/n:	9.3.3.1b		
	Sampling 1 PCB/batch	**Requirement references**	**Value**	**Pass/ Fail**
PCB length	s/n:	9.3.3.1c		
PCB width	s/n:	9.3.3.1c		
specific dimensional features from the PCB definition dossier (e.g. cut-out, radius)		B.2.1.4b3		
Warp and twist (maximum measurements recorded on the worst-case PCB)	s/n:	9.3.3.2-9.3.3.3		
Diameter of plated and non-plated holes for all diameters ≥0,6mm	s/n:	9.3.3.1d	-	
Diameter of plated holes <0,6mm if specified in PCB definition dossier	100%	10.6.3g	-	
External annular ring for all plated-hole types	s/n:	10.6.1b	-	
External conductor width and spacing on minimum dimensions	s/n:	9.3.3.1g, 9.3.3.1h, 9.3.3.1i, 9.3.3.1j	-	
External conductor width and spacing fine pitch on minimum dimensions	100%	9.3.3.1g, 9.3.3.1h, 9.3.3.1i, 9.3.3.1j	-	
Comparison of lay-out to the drawing (presence of plated and non-plated holes and milling)	s/n:	6.3g	-	
Comments:				

Table B-4: Example of a Lab report for microsection of coupons for qualitative aspects

Lab report for microsection of coupons for qualitative aspects	Inspection	Requirement references	as per flow from Figure 8-1	
			Pass/ Fail	Present? as per B.2.1.1c
Via filling, voids or cracks	each panel	Table 10-18		
Cap lift	each panel	Table 10-19		-
Planarity, dimple	each panel	Table 10-20		
Burrs and nodules	each panel	Table 10-21		-
Voids in copper plating	each panel	Table 10-22		
Wedge voids	each panel	Table 10-23		-
Resin voids	each panel	Table 10-24		
Delamination, blistering, crazing, measling	each panel	Table 10-25		-
Pad lift	each panel	Table 10-26		
Dielectric cracks	each panel	Table 10-27		
Cracks and separation in copper	each panel	Table 10-28		
ICD	each panel	Table 10-29		-
Smear	each panel	Table 10-30		
HWPA and resin recession	each panel	Table 10-31		
Nail heading	each panel	Table 10-32		-
CIC	each panel	Table 10-33		-
Inhomogeneity in dielectric	each panel	Table 10-34		
Contamination or inclusion	each panel	Table 10-35		
Delamination between coverlay and prepreg	each panel	Table 10-36		-
Adhesive voids in coverlay and bond-ply	each panel	Table 10-37		
Misalignment of prepreg in rigid-flex-interface	each panel	Table 10-38		-
Review items from MRR	each panel	B.2.1.5b		-
Comments:				
Pictures of microsections in conformance with B.2.1.5d.				

Table B-5: Example of a lab report for microsection of coupons for dimensional verification

Lab report for microsection of coupons for dimensional verification	Requirement references	Pass/ Fail	Present? as per B.2.1.1c		Requirement references	Measured value
	covers 100%			measure 1 per batch		
Annular ring internal	Table 10-1		-	s/n:	50 µm	
Annular ring internal reduced	Table 10-1		-	s/n:	Ref. e, 25 µm	
Annular ring microvia internal landing pad	Table 10-1		-	s/n:	Ref. d, 10 µm	
Annular ring external blind via	Table 10-2		-	s/n:	Ref. e, 100 µm	
Annular ring external microvia	Table 10-2		-	s/n:	Ref. f, 10 µm	
Copper foil thickness	Table 10-3		-	s/n:		build-up report
Copper plating thickness, PTH and via	Table 10-4		-	s/n:	Ref. a, b, c	
Copper plating thickness, blind and buried via	Table 10-4		-	s/n:	Ref. d	
Etchback	Table 10-5		-	s/n:	Ref. a	
Wicking	Table 10-6		-	s/n:		
Wrap copper	Table 10-7		-	s/n:		
Dielectric thickness	Table 10-8 + Table 10-9		-	s/n:		build-up report
Dielectric thickness - number of prepreg	Table 10-8 + Table 10-9		-	s/n:	Ref. b	
Microvias dimple and bump	Table 10-10		-	s/n:	Ref. a, b	
Microvias aspect ratio	Table 10-10		-	s/n:	Ref. c	
Microvias diameter to internal landing pad	Table 10-10		-	s/n:	Ref. d	
Microvias plating voids	Table 10-11			s/n:		
SnPb thickness PTH hole wall	Table 10-12		-	s/n:	Ref. c	
SnPb thickness PTH corner	Table 10-12		-	s/n:	Ref. d	
SnPb thickness PTH pads	Table 10-12		-	s/n:	Ref. e	
Electrolytic Ni	Table 10-13		-	s/n:	Ref. a	
Electrolytic Au	Table 10-13		-	s/n:	Ref. b, c	
Undercut	Table 10-14		-	s/n:		
Overhang	Table 10-15		-	s/n:	Ref. b	
Dimensions of rigid-flex-interface	Table 10-16		-	s/n:	Ref. a, b	
Comments:						

Table B-6: Example of a build-up report

Layer	Layer stacking	Thickness requirements			Measured value (µm) on s/n: ……..	Pass / Fail
		Nominal (µm)	Tolerances (µm)			
			min	max		
1	copper					
	dielectric					
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						
18						
19						
20						
21						
22						

Table B-7: Example of a lab report for additional tests

Lab report for additional tests		Pass	Fail	
Solderability	9.4.11			
High resistance electrical test	9.3.7			list of s/n:
Continuity test	9.3.8			list of s/n:
IST	9.5.5			report reference:
Comments:				

Annex C (normative) Qualification test report – DRD

C.1 DRD identification

C.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60 requirement 5.10c.

C.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the qualification test report.

C.2 Expected response

C.2.1 Scope and content

ECSS-Q-ST-70-60_1390710

a. The qualification test report shall include:
   1. Description and history of the samples.
   2. Reference to the approved qualification test plan.
   3. All results from the qualification tests in conformance with requirements from clause 7.2.
   4. Photographic documentation of results obtained from microsectioning.

ECSS-Q-ST-70-60_1390711

b. The photographic documentation of microsections from the qualification test report shall use magnification level, lighting, micro-etchant and surface preparation in conformance with clauses 9.5.2 and 10.

C.2.2 Special remarks

ECSS-Q-ST-70-60_1390712

a. The qualification test report shall be maintained under configuration control.

Annex D (normative) Process Identification Document (PID) for PCB manufacturing – DRD

D.1 DRD identification

D.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60 requirement 5.9c.1.

D.1.2 Purpose and objective

The purpose of the PID is to specify the manufacturing processes, materials and equipment of the qualified PCB technology. It also specifies the technological parameters of the qualified design.

The PID consist of a general part and specific parts. A general part of the PID describes the company, whereas specific parts of the PID describe each qualified technology.

D.2 Expected response

D.2.1 Scope and content

D.2.1.1. General part of the PID

ECSS-Q-ST-70-60_1390713

a. The general part of the PID shall include the following information:
   1. Description of the company: history in business, products, staff, customers and the qualified site, in case of multiple sites;
   2. Technology road map;
   3. Organization chart with names and functions of key personnel;
   4. Quality certifications;
   5. Description of the process flow for order treatment, including the following:
      (a) Design review in conformance with the clause 5.2 of ECSS-Q-ST-70-12;
      (b) MRR in conformance with the clause 5.2 of ECSS-Q-ST-70-12;
      (c) Outgoing inspection and CoC in conformance with the clause 8;

6. List of main equipment for the production of PCBs, including type and brand name;
7. List of test and control equipment with their capabilities;
8. List of work instructions for manufacture and control of PCBs, with document numbers and issue references.

NOTE 1 For D.2.1.1a.7, examples of test capabilities are metallographic examination, chemical analysis, failure analysis, mechanical and electrical test including functional testing of PCBs.

NOTE 2 For D.2.1.1a.8, the work instructions include the process description.

D.2.1.2. Specific parts of the PID

ECSS-Q-ST-70-60_1390714

a. Specific parts of the PID shall include:
   1. Manufacturing and quality control flow charts with reference to applicable work instructions;
   2. List of base materials and chemicals with brand name, type, and supplier;
   3. Production flow-chart, including in-process inspections and reference to work instructions in conformance with D.2.1.1a8;
   4. Description of qualified domain in conformance with the items specified in requirement G.2.1b;
   5. Description of any review items that have been specifically qualified, as specified in clause <7>a of Annex A of ECSS-Q-ST-70-12;
   6. Subcontracted processes.

D.2.2 Special remarks

ECSS-Q-ST-70-60_1390848

a. If several technologies are qualified, the general part of the PID may be a separate document to avoid duplication in the PIDs for each technology.

ECSS-Q-ST-70-60_1390715

b. All PIDs shall have an identification of the issue, revision number and date, and a page showing the modifications introduced at each revision.

ECSS-Q-ST-70-60_1390716

c. The modifications introduced since the previous revision of a PID shall be identified with specific marks or font.

NOTE It is good practice to include in the PID the following:

- in-process inspection as per 6.3f;
- approach for TMA as per 6.3h;

- etchback as per 6.3i;
- selection, test and inspection of prepreg, laminate, flex laminate, coverlay, bond-ply, copper foil, heat sinks and metal core as per 6.5g;
- repair operations as per 6.10.2a;
- specification of solderability test for procurement as per 8.2.4i;
- planarization and selective plating processes as per Table 10-7;
- group 6 evaluation of separation between hole wall and resin inside blind/buried via as per Table 10-18 Ref. c;
- group 6 evaluation of separation between external copper foil and copper plating as per Table 10-28 Ref. c;
- group 6 evaluation of >20% HWPA or RR as per Table 10-31;
- evaluation of swirl or milky appearance as per Table 10-34 Ref. c;
- evaluation of demarcation line as per Table 10-34 Ref. d;
- evaluation of dotted interface line as per Table 10-34 Ref. e;
- group 6 evaluation of pad lift and associated laminate cracks as per 10.6.2g and Table 10-26;
- group 6 evaluation of interface lines between Cu plating as per the Note of Table 10-28.

Annex E (normative)
Process change notice (PCN) – DRD

E.1 DRD identification

E.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60, requirement 5.13f and F.2.1a.1.

E.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the process change notice (PCN).

E.2 Expected response

E.2.1 Scope and content

ECSS-Q-ST-70-60_1390717

a. Process changes shall include process parameters, chemistry, material, equipment, process flow and inspections.

ECSS-Q-ST-70-60_1390718

b. The PCN shall contain the following:
   1. Categorisation of process change as “major” or “minor”;
   2. Justification for categorisation;
   3. Description of old and new process;
   4. Justification for change;
   5. Reference to work instruction in PID;
   6. In case of minor process change, results of verification tests and inspections;
   7. Request for major process change including qualification test plan;
   8. Request for approval of implementation of the major process change including qualification test report;
   9. Optional approval from procurement authority for major process change in conformance with requirement 5.13h.

E.2.2 Special remarks

None.

Annex F (normative)
QA report – DRD

F.1 DRD identification

F.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60, requirement 5.14a.

F.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the QA report.

F.2 Expected response

F.2.1 Scope and content

ECSS-Q-ST-70-60_1390719

a. The QA report shall contain the following:
   1. Status of process changes, including associated process change notices in conformance with the DRD in Annex E;
   2. Overview of internal nonconformances, scrap, cause, yield and corrective action;
   3. Overview of external nonconformances, cause and corrective action;
   4. Overview of KPIs including OTD;
   5. Overview of planned and implemented investments;
   6. Changes in personnel and organigram;
   7. Overview of major visits by procurement authority, qualification authority or by certification bodies;
   8. Action list with status.

F.2.2 Special remarks

ECSS-Q-ST-70-60_1390849

a. Nonconformances and KPIs should be expressed per month in absolute numbers and relative to the production in accordance with applicable PIDs for each technology.

Annex G (normative)
PCB approval sheet – DRD

G.1 DRD identification

G.1.1 Requirement identification and source document

This DRD is called from ECSS-Q-ST-70-60 requirement 6.14h for the PCB approval sheet part 1 and is called from ECSS-Q-ST-70-60 requirement 6.14j for the PCB approval sheet part 2.

G.1.2 Purpose and objective

The purpose of the DRD is to describe the content of the PCB approval sheet part 1 and part 2.

G.2 Expected response

G.2.1 Scope and content

ECSS-Q-ST-70-60_1390720

a. The PCB approval sheet part 1 shall contain the following information:
   1. Identification of the PCB reference;
   2. PCB manufacturer and country;
   3. Backup PCB manufacturer and country;
   4. PCB technology as specified in requirement 5.11b;
   5. PCB procurement specification in conformance with 6.2.2a;
   6. Listing of the qualification status of PCB manufacturer on public web portal;
   7. Identification of the PID reference;
   8. Associated delta qualification and RFA.

      NOTE 1 The customer can be the prime contractor, space agency or the next industry in the contractual chain.

      NOTE 2 The public web portal can be www.escies.org.

ECSS-Q-ST-70-60_1390721

b. The PCB approval sheet part 2 shall contain the following information
   1. PCB technology as specified in requirement 5.11b;
   2. Number of rigid layers;
   3. Number of flex layers;
   4. Number of plating sequences;
   5. Number of lamination sequences;

6. Length and width of PCB and manufacturing panel;
7. Thickness of PCB;
8. Thickness of outer layer copper foil and copper plating;
9. Minimum and maximum copper thickness of internal layers;
10. Identification of material reference for:
    (a) Epoxy;
    (b) Polyimide;
    (c) Flexible layers;
    (d) RF materials;
    (e) Mixed materials;
    (f) Metal core;
11. Identification of the used surface finishes, including but not limited to the following:
    (a) Hot oil reflowed tin-lead;
    (b) Electroplated hard gold and soft gold with possible nickel underplating;
    (c) Solder mask;
    (d) Tin diffusion layer;
    (e) ENIG, ENEPIG, ENIPIG;
12. Minimum external and internal track width;
13. Minimum external and internal insulation distance;
14. Minimum insulation distance in Z-direction;
15. Minimum finished holes sizes and maximum aspect ratio for:
    (a) PTH;
    (b) Blind via;
    (c) Buried via;
    (d) Microvia;
16. List of review items from MRR in conformance with clause A.2<7> of ECSS-Q-ST-70-12.

ECSS-Q-ST-70-60_1390722

c. The PCB approval sheet part 2 shall provide confirmation for each aspect in conformance with requirements from G.2.1b that it is within the qualified domain from the PID of the PCB manufacturer.

ECSS-Q-ST-70-60_1390723

d. The PCB approval sheets part 1 and part 2 shall contain the approval signatures from the procurement authority and customer

NOTE The customer can be the prime contractor, space agency or the next industry in the contractual chain.

G.2.2 Special remarks

Examples of a PCB approval sheet part 1 and part 2 are given in the Table G-1 and Table G-2.

Table G-1: Example of a PCB approval sheet part 1

PCB Approval sheet part 1	
PCB reference	
Manufacturer / country	
Backup manufacturer	
PCB technology description	Polyimide sequential rigid Polyimide sequential rigid/flex Epoxy sequential rigid Epoxy multilayer rigid/flex HDI with microvias RF PCBs Flex and sculptured flex Low expansion materials
Generic specification ECSS-Q-ST-70-60?	(Y/N)
Approval status of PCB manufacturer	
PCB manufacturer listed on ESCIES.org?	(Y/N)
PID reference	
Delta qualification required?	(Y/N)
If yes, reference of the RFA	
Approval signature	
Procurement authority approval	Date
Customer approval	Date

Table G-2: Example of a PCB approval sheet part 2

PCB approval sheet part 2			
PCB summary drawing sheet			
PCB reference(s)			
		Actual value worst case as designed	PID qualified domain
Number layers/sequence	Rigid		
	Flex		
	Plating sequences		
	Lamination sequences		
Thickness/size	PCB Size (mm)		
	PCB Thickness (mm)		
	External Cu thickness foil and plating (µm)		
	Internal min Cu thickness (µm)		
	Internal max Cu thickness (µm)		
Material (Commercial reference Manufacturer name)	Epoxy		
	Polyimide		
	Flexible		
	RF materials		
	Mixed materials		
	Metal core		
	other		
Surface finish	Sn/Pb hot oil reflow		
	Ni/Au electroplated (hard/soft)		
	Solder mask		
	Tin diffusion layer		
	ENIG, ENIPIG, ENEPIG		
	other		
Minimum design features (µm)	External track width		
	External insulation distance		

	Internal track width		
	Internal insulation distance		
	Insulation distance in Z-direction		
Minimum finished hole size (µm)	PTH		
	Blind		
	Buried		
	Microvia		
Aspect ratio	PTH		
	Blind		
	Buried		
	Microvia		
Review items from MRR	(Y/N)		
as per clause A.2<7> of ECSS-Q-ST-70-12	If yes, provide list of review items from MRR and verify against PID when applicable		

Approval signature

Procurement authority approval Date

Customer approval Date

Annex H (informative) Example of plated-through hole microsection

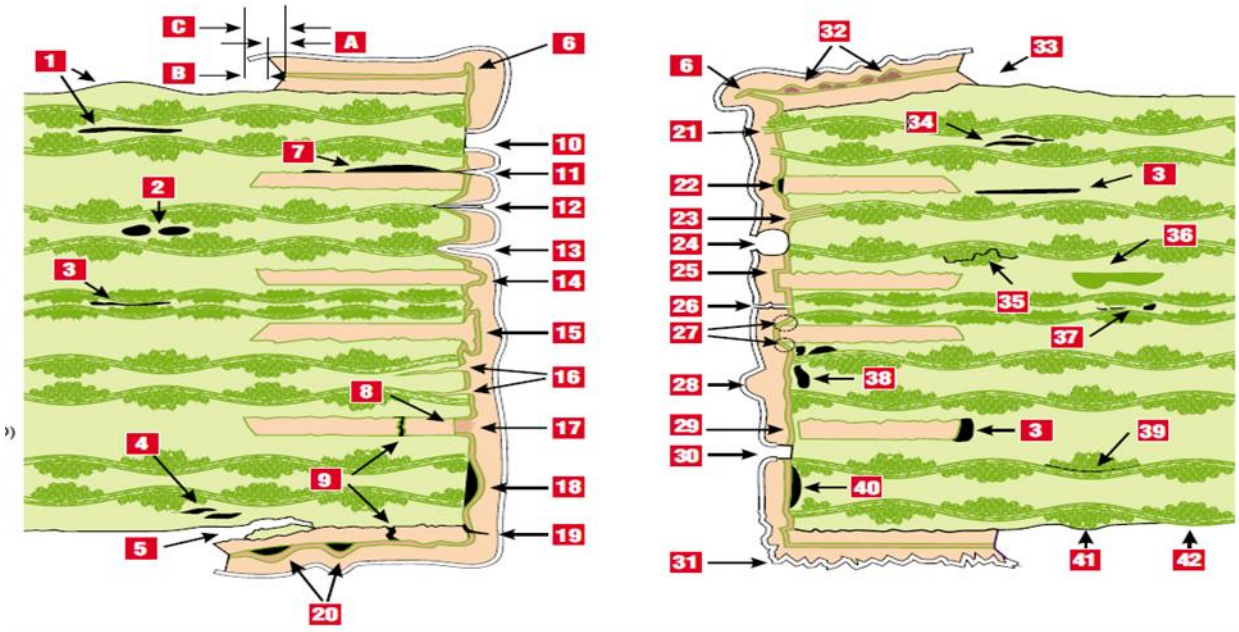


Figure H-1: Typical phenomena in cross-section of PTH. Not all phenomena are specified in ECSS-Q-ST-70-60 in the same way.

Annex I (informative) Cleanliness requirements for laminate and prepreg

I.1 Introduction

The text from this annex is cited from Appendix A from IPC-4101E and was originally drafted by European space industry. The text is provided for information. The full standard and any future revisions can be obtained from IPC.

I.2 Citation of Appendix A from IPC-4101E

APPENDIX A from IPC-4101E supplemental inspection requirements if required in purchase order or master drawing.

A.1 - SCOPE

This Appendix A defines supplemental requirements to this standard [IPC-4101E] with the purpose to define a high quality for base materials to be used for high reliability PWBs for critical applications. PWBs designed with small spacing or used in high voltage applications can be subject to failure of insulation resistance due to breakdown or inclusion of foreign material.

Printed boards that meet the requirements of IPC-6012DS ‘‘Space and Military Avionics Applications Addendum, Section 0.1.1 Purpose,’’ are not allowed to have foreign inclusions that reduce dielectric spacing to below the minimum requirement. The requirements on base materials in this appendix aim to prevent and to detect such nonconformance earlier in the supply chain.

If the user of material wishes to acquire laminate, prepreg or both that meet the requirements of this Appendix A, then this Appendix A shall be specifically called out in the purchase order or the master drawing. Further, this Appendix A shall not be assumed to be in force if it is not specifically called out in the purchase order or the master drawing.

A.2 - PREPREG

A.2.1 Acceptance Criteria for Prepreg Requirements 3.8.3.2.1 and 3.8.3.2.2 shall apply for inclusions and imperfections in prepreg.

A.2.2 Test Method for Prepreg Prepreg shall be tested in accordance with Table 3-2 for visual properties, with the following modification:

a. – Conformance testing of visual properties shall be performed on 100% of the units in a lot using IPC-TM-650, Method 2.1.5, or an equivalent method AABUS. Modify Method 2.1.5 by changing the particulate inspection magnification to 50X.

b. A.2.3 Rejection Criteria for Prepreg Section 4.4.3 shall be discarded for rejected lots. The following modification shall apply:

c. – Material with nonconformances shall be discarded from the batch. The remainder of the batch shall be compliant with this Appendix A.

A.3 - LAMINATE

A.3.1 Acceptance Criteria for Laminate The requirements of 3.8.3.1.6 shall apply for imperfections on laminate, with the following modification:

– Requirement 'f' shall be deleted and the following shall apply: Opaque foreign matter shall not exceed 0.50 mm [0.019 in]. Opaque foreign inclusions <0.13 mm [0.005 in] shall not be counted. Opaque foreign inclusions sized between 0.13 mm [0.005 in] and ≤0.50 mm [0.019 in] shall average no more than two spots per 300 mm x 300 mm [11.81 in x 11.81 in] area inspected.

A.3.2 Test Method for Laminate Laminate shall be tested in accordance with Table 3-1 for surface and sub-surface imperfections, with the following modification:

– The conformance testing of surface and sub-surface imperfections shall be performed on ≥2% of the total area of the lot.

A.3.3 Rejection Criteria for Laminate Section 4.4.3 shall be discarded for rejected lots. The following modification shall apply:

– All base material in the lot shall be non-compliant to this Appendix A if non-conformances are observed in the lot.

A.3.4 In-Process Requirement for Laminate For the manufacture of copper clad laminate, the base material supplier shall use prepreg that is inspected and evaluated in accordance with A.2 or AABUS.

A.3.5 Hi-Pot Test for Laminate Hi-Pot testing as per IPC-TM-650, Method 2.5.7.2, can be performed AABUS on 100% of the copper clad laminate with a nominal thickness of ≤0.119 mm [0.0047 in]. The preparation of edges of the laminate, the bake out, the electrical test parameters and the acceptance criteria are AABUS.

A.4 - APPLICABILITY

Section 4.2 shall apply for the responsibility of conformance testing performed by the base material manufacturer, with the following modification:

– The procurement authority has the right to perform inspections set forth in this Appendix A to verify acceptability of the lot, in which case the requirements of this Appendix A shall apply.

A.5 - CERTIFICATE OF CONFORMANCE

Section 4.4.5 shall apply for the certificate of conformance, with the following modification:

– The certificate of conformance shall include a statement of compliance to this Appendix A.

A.6 - QUALITY CONFORMANCE INSPECTION AND FREQUENCY

Sections 4.4 and 4.4.1 shall apply for quality conformance inspection and frequency with the following modification:

– The manufacturer's quality system shall not take precedence over the requirements in Appendix A.

Table A-1 Summary Table of Modifications in Appendix A

Tests	Requirement paragraph IPC-4101E	Test Method	Qualification Testing	Conformance Testing	Conformance Testing Frequency	Inspected specimens
Visual properties for prepreg	3.8.3.2	2.1.5 or AABUS	✓	✓	Lot	100% of the lot as per A.2.2
Surface and Sub-Surface Imperfections for laminate	3.8.3.1.6 and A.3	2.1.5 or AABUS	✓	✓	Lot	≥2% of the lot as per A.3.2
Hi-Pot electrical test on laminate	A.3.5	2.5.7.2 or AABUS	AABUS	AABUS	-	100% or AABUS

Annex J (informative)
Example qualification programme

Test vehicle ID as per figure 7-1	Group	Clause or req. in ECSS-Q-ST-70-60	Test description (initial test as received)	Clause or req. in ECSS-Q-ST-70-60	Test description (subsequent test after stress)	Nr of samples	Running item nr
PCB 1-3	group 1	9.3.2	visual inspection for qualitative aspects	-	-	3	1
PCB 1-3	group 1	9.3.3	visual inspection for dimensional verification	-	-	3	2
PCB 1-3	group 1	9.3.3.2	warp	-	-	3	3
PCB 1-3	group 1	9.3.3.3	twist	-	-	3	4
3 coupons	group 1	9.3.4	impedance test	-	-	3	5
3 coupons	group 1	9.3.5	dielectric constant and loss tangent	-	-	3	6
PCB 1	group 1	9.3.6	cleanliness	-	-	1	7
PCB 1-3	group 1	9.3.7.2	high resistance electrical test	-	-	3	8
PCB 1-3	group 1	9.3.8	continuity test	-	-	3	9
1 coupon	group 2	9.4.2	peel test	-	-	1	10
2 coupons	group 2	9.4.3	flexural fatigue	-	-	2	11
2 coupons	group 2	"	"	9.4.3h	resistance before and after test	2	12
2 coupons	group 2	"	"	9.3.2, 10.4	visual inspection	2	13
2 coupons	group 2	"	"	9.5.2, 10.3	microsectioning for qualitative aspects	2	14
1 coupon or 1 PCB sample	group 2	9.4.4	bending test	-	-	1	15
1 coupon or 1 PCB sample	group 2	"	"	9.4.3h	resistance before and after test	1	16
1 coupon or 1 PCB sample	group 2	"	"	9.3.2, 10.4	visual inspection	1	17

Test vehicle ID as per figure 7-1	Group	Clause or req. in ECSS-Q-ST-70-60	Test description (initial test as received)	Clause or req. in ECSS-Q-ST-70-60	Test description (subsequent test after stress)	Nr of samples	Running item nr
2 locations	group 2	"	"	9.5.2, 10.3	microsectioning for qualitative aspects	2	18
1 coupon	group 2	9.4.5	coating adhesion - tape test	-	-	1	19
1 coupon	group 2	9.4.6	analysis of SnPb	-	-	1	20
1 coupon	group 2	9.4.7	outgassing	-	-	1	21
1 coupon	group 2	9.4.8b	TGA: Td	-	-	1	22
1 coupon	group 2	9.4.8d	DSC: Tg	-	-	1	23
1 coupon	group 2	9.4.8c, 9.4.8e, 9.4.8f	TMA: T288, Tg, CTE	-	-	1	24
1 coupon	group 2	9.4.11	solderability, without microsectioning	-	-	1	25
3 coupons and 1 PCB sample	group 3	9.5.2, 10.2, 10.3	microsectioning for qualitative aspects, dimensional verification	-	-	4	26
3 coupons and 1 PCB sample	group 3	9.5.3	solder bath float	-	-	4	27
3 coupons and 1 PCB sample	group 3	"	"	9.3.2, 10.4	visual inspection	4	28
3 coupons and 1 PCB sample	group 3	"	"	9.5.2, 10.3	microsectioning for qualitative aspects	4	29
3 coupons	group 3	9.5.4	rework simulation	-	-	3	30
3 coupons	group 3	"	"	9.5.2, 10.3	microsectioning for qualitative aspects	3	31
3 coupons	group 3	9.5.5	IST test	-	-	3	32
3 coupons	group 3	"	"	9.5.2, 10.3	microsectioning for qualitative aspects	3	33
2 PCB samples	group 4	9.6.2c.2	intralayer insulation resistance DC as per 9.6.3	-	-	2	34
2 PCB samples	group 4	"	interlayer insulation resistance DC as per 9.6.3	-	-	2	35
2 PCB samples	group 4	9.6.2c.3	intralayer dielectric withstanding voltage DC as per 9.6.4	-	-	2	36
2 PCB samples	group 4	"	interlayer dielectric withstanding voltage DC as per 9.6.4	-	-	2	37
2 PCB samples	group 4	9.6.2c.4	reflow simulation as per 9.8.3	-	-	2	38
2 PCB samples	group 4	9.6.2c.5 + 6	rework simulation on 2 PTH and 2+2 via-in-pad as per 9.5.4	-	-	2+2+2	39
2 PCB samples	group 4	9.6.2c.7	thermal cycling as per 9.6.2c.7 (500x, from -55 to +100 degC)	-	-	2	40
2 PCB samples	group 4	"	"	9.6.2c.8	intralayer insulation resistance DC as per 9.6.3	2	41

Test vehicle ID as per figure 7-1	Group	Clause or req. in ECSS-Q-ST-70-60	Test description (initial test as received)	Clause or req. in ECSS-Q-ST-70-60	Test description (subsequent test after stress)	Nr of samples	Running item nr
2 PCB samples	group 4	"	"	"	interlayer insulation resistance DC as per 9.6.3	2	42
2 PCB samples	group 4	"	"	9.6.2c.9	intralayer dielectric withstanding voltage DC as per 9.6.4	2	43
2 PCB samples	group 4	"	"	"	interlayer dielectric withstanding voltage DC as per 9.6.4	2	44
2 PCB samples	group 4	"	"	9.6.2c.10	peel test	2	45
10 microsections	group 4	"	"	9.6.2c.11, 9.6.2c.12	microsectioning for qualitative aspects	10	46
4 coupons	group 5	9.7.2	THB	-	-	4	47
4 coupons	group 5	"	"	9.5.2	microsectioning	4	48
10 coupons	group 5	9.7.3	CAF	-	-	10	49
10 coupons	group 5	"	"	9.5.2	microsectioning	10	50
1 PCB sample	group 6	9.8.2c.2	reflow simulation as per 9.8.3	-	-	1	51
1 PCB sample	group 6	9.8.2c.3 + 4	rework simulation on 2 PTH and 2+2 via-in-pad as per 9.5.4	-	-	2+2+2	52
1 PCB sample	group 6	9.8.2c.5	thermal cycling as per 9.8.4 (200x, from -60 to +140 degC)	-	-	1	53
10 microsections	group 6	"	"	9.8.2c.6	microsectioning for qualitative aspects	10	54

Annex K (informative) Checklist for MPCB

K.1 Introduction

This checklist provides guidelines for the review and approval of PCB technology during Materials and Processes Control Boards (MPCB).

The checklist is intended for:

a. the equipment supplier to self-assess compliance with the requirements from the applicable standards;

b. the customer chain to identify if expert support is required to conclude on the review;

c. the MPCB to use as a guide during the review process.

It is the intention of the checklist to provide sufficient detail for a robust approval process of the PCB technology, while also maintaining a reasonably short review process. It is the intention that Materials and Process (M&P) Engineers who are not expert in PCB technology can conduct this review with confidence, using this checklist, with the following outcome:

- Approval of qualified PCB technology;
- Identification of any non-qualified technology or any deviation to requirements;
- Preparation of the contents of RFAs.

Non-qualified technology, deviation to requirements and RFx are recommended to be reviewed, and eventually approved, by PCB experts, not only by M&P Engineers.

K.2 Checklist for MPCB

Question nr	Reference from ECSS-Q-ST-70-60	Assessment	Contractor response: (compliant, partial or non-compliance with justification)
Statement	6.14s	The approval of the item in the DML is based on the review of PCB approval sheets of all PCBs covered by the item of the DML. NOTE: Approval by RFA in the DML is indicated by 'X' with the RFA reference number as described in Table A-4 of ECSS-Q-ST-70.	Statement, for information
Statement	6.14o	Customer approval of PCB approval sheets is based on the compliance of technology parameters to the PID, as declared on the PCB approval sheet part 2.	Statement, for information
Q1	6.14g	The procurement authority specifies in the DML for each PCB technology the following: 1. PCB manufacturer; 2. PCB procurement specification; 3. PCB technology description as per 6.14e (see Q3 below); 4. traceability to individual PCBs and their PCB approval sheet. NOTE 1: The name of the selected PCB manufacturer(s) is declared in DML and approval sheets. NOTE 2: The acronym or name of the PCB in the DML can provide the traceability to the PCB approval sheet.	Response 1:
Q2	6.14a 6.2.2a	ECSS-Q-ST-70-60 is used for procurement of PCBs for flight models and for qualification models. NOTE 1: ECSS-Q-ST-70-60 is declared as "procurement standard" in the appropriate column of the DML, as per req. 6.14g.2. NOTE 2: It is not good practice to use another procurement specification that is (declared to be) in compliance with ECSS-Q-ST-70-60, as described in 6.2.2a.	Response 2:
Q3	6.14e	The procurement authority lists in the DML each PCB technology as a separate item: 1. Polyimide rigid 2. Polyimide rigid/flex 3. Epoxy rigid 4. Epoxy rigid/flex	Response 3:

Question nr	Reference from ECSS-Q-ST-70-60	Assessment	Contractor response: (compliant, partial or non-compliance with justification)
		5. HDI 6. RF 7. Flexible 8. Sculptured flex 9. Low thermal expansion materials	
Q4	6.14f	The PCB technology is listed as a single line item in the DML covering all materials and processes for its manufacture. Individual raw materials and PCB manufacturing processes are not listed in the DML and DPL as separate items. NOTE 1: Details of raw materials and processes included in the single declared line item of the DML, are given in the PID of the qualified PCB manufacturer or in the RFA for a non-qualified PCB. NOTE 2: The single declared line item in the DML can include several PCB types/designs within that technology category. Traceability to all PCB types/designs and their PCB approval sheets is provided in the DML line item as per 6.14g.4.	Response 4:
Q5	6.14h, l, m	The procurement authority completes a PCB approval sheet part 1 for each individual PCB type as per the DRD in Annex G and submit it for approval by the MPCB prior to the PDR. NOTE: The procurement authority can reuse PCB approval sheets part 1 and part 2 from previous procurement in case the PCB design is 'recurrent', as per clause 4.1 of ECSS-Q-ST-70-12.	Response 5:
Q6	6.14j, k, m	The procurement authority completes a PCB approval sheet part 2 for each individual PCB type as per the DRD in Annex G and submit it for approval by the MPCB prior to the CDR.	Response 6:
Q7	-	The PCB approval sheet includes evidence of the qualified status. This can be obtained from the public web portal www.escies.org/pcb/.	Response 7:
Q8	6.14d	The procurement authority ensures that all procured PCBs meet the project requirements. NOTE: Examples of applications for projects with specific requirements are human spaceflight, long-term storage, detector technology, planetary exploration.	Response 8:
Q9	5.1b	In case of operational use of PCB (and assemblies) below -55 °C and/or above +85 °C, the technology is subject to project specific qualification under RFA.	Response 9:

Question nr	Reference from ECSS-Q-ST-70-60	Assessment	Contractor response: (compliant, partial or non-compliance with justification)
Q10	6.14b, c	It is good practice to use the same PCB manufacturer for flight models and qualification models. In case a different PCB manufacturer or different PCB material is used for flight models compared to qualification models, the procurement authority analyses in a technical note the impact on the following items: 1. Electrical performance of the equipment; 2. Mechanical performance of the equipment; 3. Thermal performance of the equipment; 4. Assembly approval status; 5. Any modifications of the PCB definition dossier done by the previous PCB manufacturer.	Response 10:
Q11	6.14n, r	The following documentation is available for possible review during MPCB: 1. FAI (First Article Inspection) on PCB as per clause 8.5; 2. PCB definition dossiers. NOTE: Any confidential drawings can be removed from the PCB definition dossier.	Response 11:
Q12, if applicable	6.14p, q 7.7.2d 7.7.2n	In case of non-compliance of a technology parameter to the PID, an RFA part 1 with the project qualification plan and RFA part 2 with project qualification results are submitted to the customer for review by technology experts as part of the MPCB process. NOTE 1: Clauses 7.6 and 7.7 specify requirements of tests, inspections and specimen for delta qualification and project qualification under RFA. NOTE 2: Clause 7.7.2p specifies conditions for procurement as per IPC standards.	Response 12:

Bibliography

ECSS-S-ST-00	ECSS system – Description, implementation and general requirements
ECSS-Q-ST-70-07	Space product assurance — Verification and approval of automatic machine wave soldering
ECSS-Q-ST-70-28	Space product assurance — Repair and modification of printed circuit board assemblies for space use
IEC 60068-2-3 (1969-01)	Environmental testing. Part 2: Tests. Test Ca: Damp heat, steady state
IEC 60068-2-14-am 1 (1986-01)	Environmental testing. Part 2: Tests. Test N: Change of temperature
IEC 60068-2-20-am 2 (1987-01)	Environmental testing. Part 2: Tests. Test T: Soldering
IEC 60249-1-am 4 (1993-05)	Base materials for printed circuits. Part 1: Test methods
IEC 60326-5-am 1 (1989-10)	Printed boards. Part 5: Specification for single and double sided printed boards with plated-through holes
IEC 60326-8 (1981-01)	Printed boards. Part 8: Specification for single and double sided flexible printed boards with through connections
IEC 60326-11 (1991-03)	Printed boards. Part 11: Specification for flex-rigid multilayer printed boards with through connections
IEC 62326-4 (1996-12)	Printed boards. Part 4: Rigid multilayer printed boards with interlayer connections - Sectional specification
MIL-P-50884C (1984)	Printed wiring, flexible and rigid-flex
IPC-J-STD-003D (2023)	Solderability test for printed boards
IPC-1602A (2024)	Standard for Printed Board Handling and Storage
IPC-2221C (2023)	Generic standard on printed board design
IPC-5703 (2013)	Cleanliness guidelines for printed board fabricators
IPC-5704 (2009)	Cleanliness requirements for unpopulated printed boards
IPC-6011A (2025)	Generic performance specification for printed boards
IPC-6013ES (to be issued)	Space and military avionics applications addendum to IPC-6013E
IPC-9252B (2016)	Requirements for electrical testing of unpopulated printed boards
IPC-9691B (2016)	User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance and Other Internal Electrochemical Migration Testing