# INTEGRATED CIRCUITS, SILICON MONOLITHIC, 32-BIT ARM® CORTEX®-M7 MICROCONTROLLER

## BASED ON TYPE SAMRH707

## ESCC Detail Specification No. 9512/008


| | |
|---|---|
| Issue 1 | June 2025 |


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## DOCUMENTATION CHANGE NOTICE

(Refer to https://escies.org for ESCC DCR content)

| DCR No. | CHANGE DESCRIPTION |
|---|---|
| | |

**TABLE OF CONTENTS**

# 1 GENERAL

## 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics and test and inspection data for the component type variants and/or the range of components specified below. It supplements the requirements of, and shall be read in conjunction with, the ESCC Generic Specification listed under Applicable Documents.

## 1.2 APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

(a) ESCC Generic Specification No. 9000.

(b) MIL-STD-883, Test Method Standard for Microcircuits.

## 1.3 TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply.

## 1.4 THE ESCC COMPONENT NUMBER AND COMPONENT TYPE VARIANTS

### 1.4.1 The ESCC Component Number

The ESCC Component Number shall be constituted as follows:

Example: 951200x01R

- Detail Specification Reference: 951200x
- Component Type Variant Number: 01
- Total Dose Radiation Level Letter: R (as applicable)

### 1.4.2 Component Type Variants

The component type variants applicable to this specification are as follows:

| Variant Number | Based on Type | Case | Terminal Material and Finish | Weight max g | Total Dose Radiation Level Letter (Notes 2, 3) |
|---|---|---|---|---|---|
| 01 | SAMRH707 | CQFP-164 | D2 (Note 1) | 18 | E [20krad(Si)] or R [100krad(Si)] |

**NOTES:**

1. The terminal material and finish shall be in accordance with the requirements of ESCC Basic Specification No. 23500.
2. Total dose radiation level letters are defined in ESCC Basic Specification No. 22900. If an alternative radiation test level is specified in the Purchase Order the letter shall be changed accordingly.
3. The Total Dose Radiation Level Letter shall be validated as follows:
   - For letter E: Tested up to 30krad(Si) with non-volatile memory selected (i.e. in read mode)
   - For letter R: Tested up to 150krad(Si) with non-volatile memory unselected

1.5 MAXIMUM RATINGS

The maximum ratings shall not be exceeded at any time during use or storage. Functional performance for extended periods at the maximum ratings may adversely affect device reliability.

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in the Test Methods and Procedures of the applicable ESCC generic specification.

| Characteristics | Symbols | Maximum Ratings | Units | Remarks |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$<br>$V_{CC}$ | -0.3 to 2<br>-0.3 to 4 | V | Notes 1, 2, 3 |
| I/O Input Voltage Range | $V_{IN}$ | -0.3 to 2.25 | V | Note 1, 3 |
| Operating Temperature Range | $T_{op}$ | -55 to +125 | °C | Note 1<br>$T_{amb}$ |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C | |
| Junction Temperature | $T_j$ | +175 | °C | |
| Thermal Resistance, Junction-to-Case | $R_{th(j-c)}$ | 1 | °C/W | |
| Soldering Temperature | $T_{sol}$ | +345 | °C | Note 4 |

**NOTES:**

1. The following operating conditions also apply. Device performance beyond these operating conditions is not guaranteed:

| Characteristics | Symbols | Maximum Rated Operating Conditions | Units | Remarks |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$<br>$V_{CC}$ | 1.65 to 1.95<br>3 to 3.6 | V | Notes 2, 3 |
| I/O Input Voltage Range | $V_{IN}$ | As per Maximum Ratings table | | Note 3 |
| Operating Temperature Range | $T_{op}$ | As per Maximum Ratings table | | $T_{amb}$ |

2. $V_{DD}$ is for Core and $V_{CC}$ is for I/O.
3. With reference to $V_{SS}$ = 0V.
4. Duration 10 seconds maximum at a distance of not less than 1.6 mm from the device body and the same terminal shall not be re-soldered until 3 minutes have elapsed.

1.6 HANDLING PRECAUTIONS

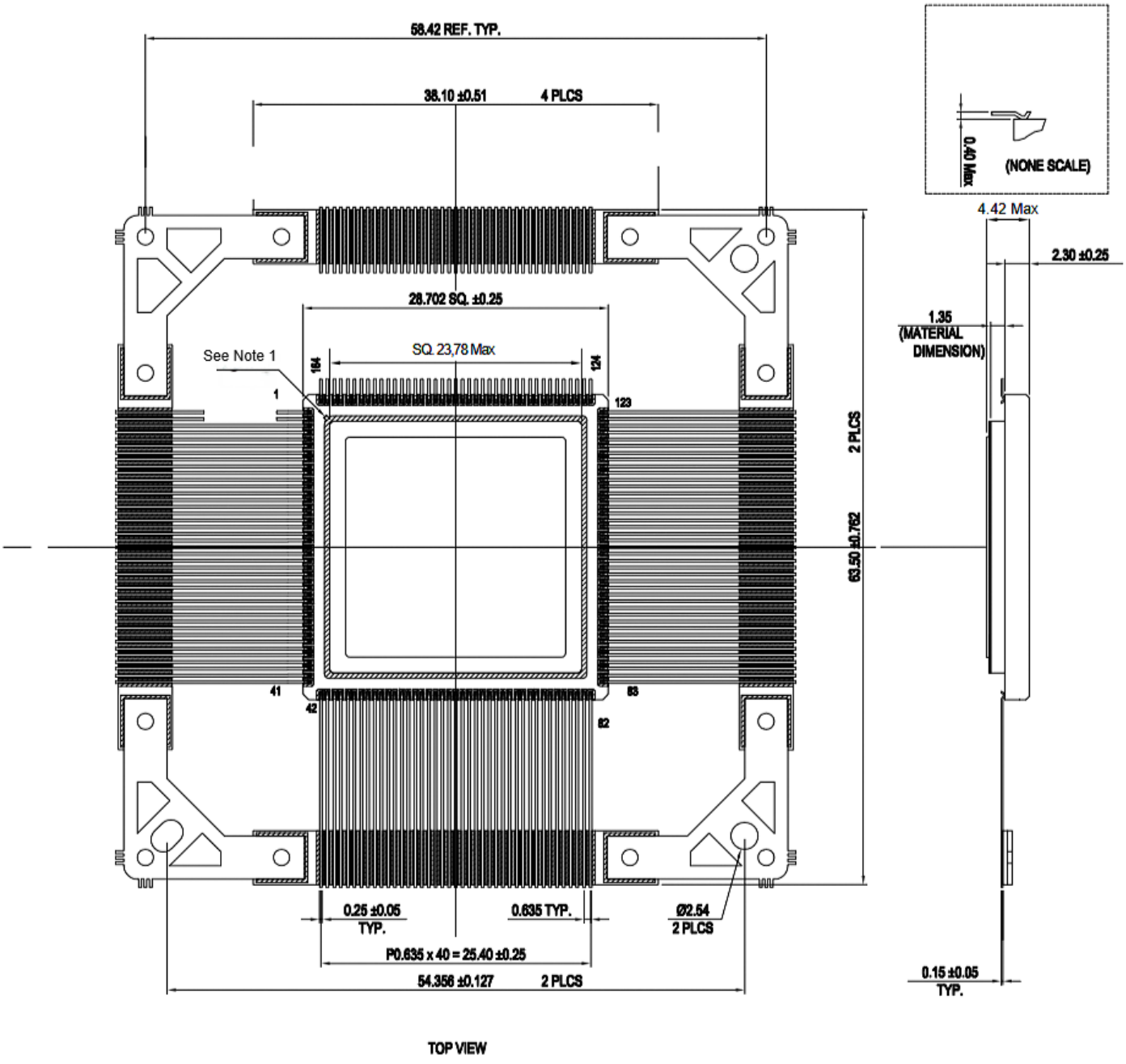
These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 per ESCC Basic Specification No. 23800 with a Minimum Critical Path Failure Voltage of < 250 Volts.

(Note: < 250V applies for pins PA0 to PA15 and PD28 to PD31. Other pins level is < 1000V).

1.7 PHYSICAL DIMENSIONS AND TERMINAL IDENTIFICATION

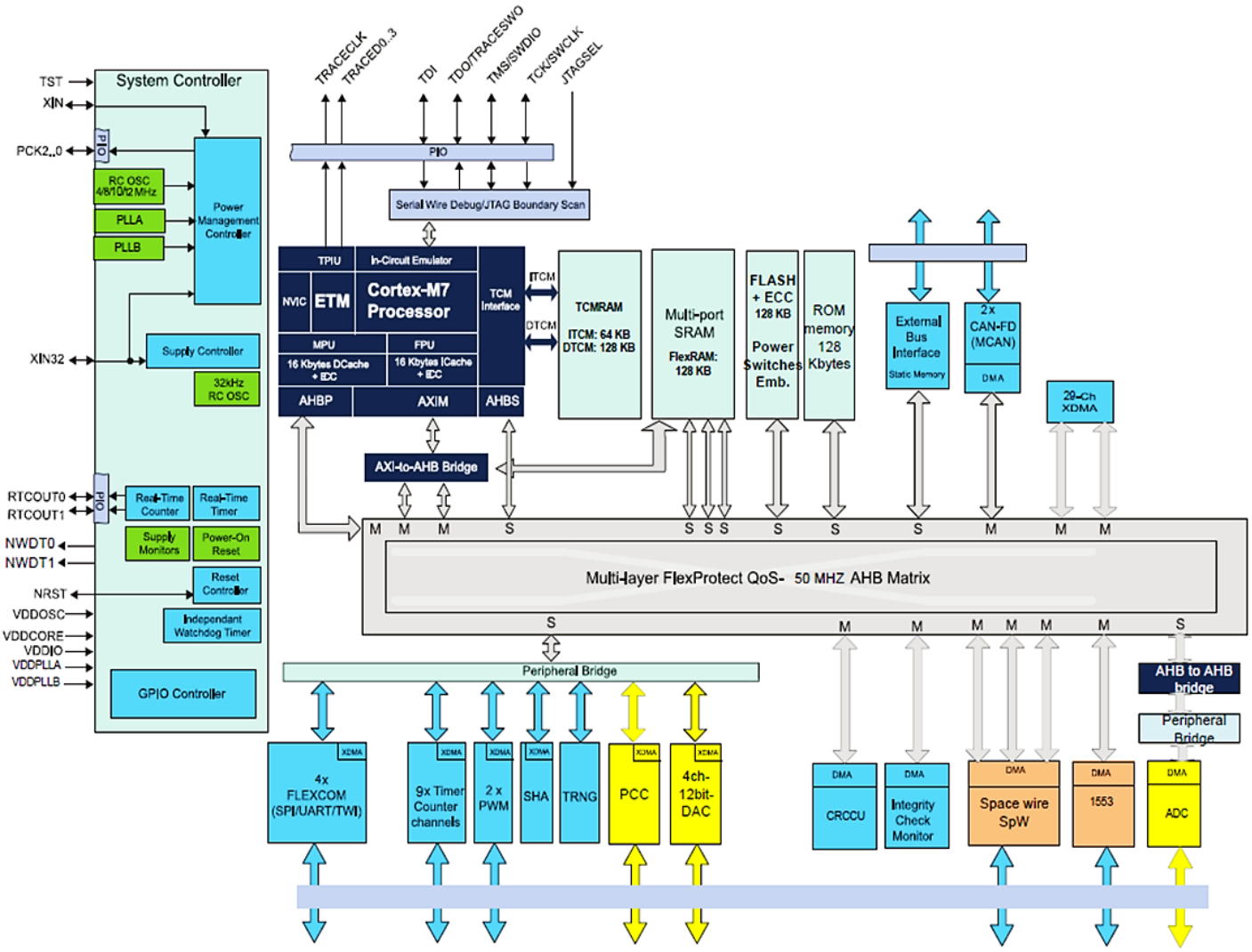
Ceramic Quad Flat Package (CQFP-164) – 164 Tied Leads




**NOTES:**

1. Terminal identification is specified by reference to the index mark.
2. Dimensions in mm.

1.8 FUNCTIONAL DIAGRAM

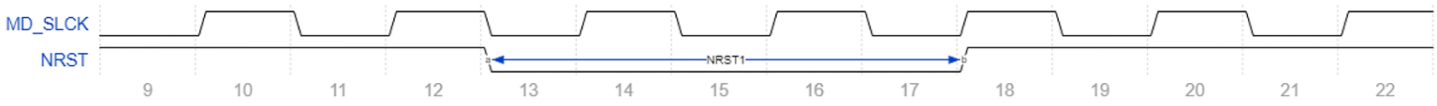



1.9 PIN ASSIGNMENT

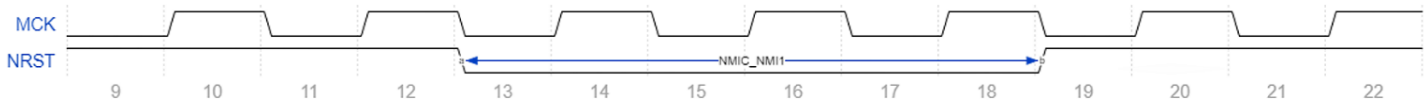
| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | GND_CORE | 42 | GND_CORE | 83 | GND_CORE | 124 | GND_CORE |
| 2 | VDD_CORE | 43 | VDD_CORE | 84 | VDD_CORE | 125 | VDD_CORE |
| 3 | PA20 | 44 | PB20 | 85 | PC12 | 126 | PD28 |
| 4 | PA21 | 45 | PB21 | 86 | PC13 | 127 | PD29 |
| 5 | PA22 | 46 | PB22 | 87 | PC14 | 128 | PD30 |
| 6 | PA23 | 47 | PB23 | 88 | PC15 | 129 | PD31 |
| 7 | PA24 | 48 | PB24 | 89 | PC16 | 130 | VDDIO_DAC |
| 8 | PA25 | 49 | PB25 | 90 | PC17 | 131 | GNDIO_DAC |
| 9 | PA26 | 50 | PB26 | 91 | PC18 | 132 | AD_DAC_GNDREF |
| 10 | PA27 | 51 | PB27 | 92 | PC19 | 133 | AD_DAC_VREFIN |
| 11 | PA28 | 52 | PB28 | 93 | PC20 | 134 | ANA_GND |
| 12 | PA29 | 53 | PD0 | 94 | PC21 | 135 | ANA_3V3 |

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 13 | PA30 | 54 | PD1 | 95 | PC22 | 136 | VDDIO_ADC |
| 14 | PA31 | 55 | PD2 | 96 | PC23 | 137 | GNDIO_ADC |
| 15 | PB0 | 56 | PD3 | 97 | PC24 | 138 | PA0 |
| 16 | PB1 | 57 | TST | 98 | PC25 | 139 | PA1 |
| 17 | PB2 | 58 | JTAGSEL | 99 | PC26 | 140 | PA2 |
| 18 | VDD_PLLA/B | 59 | NMIC_NMI | 100 | PC27 | 141 | PA3 |
| 19 | GND_PLLA/B | 60 | NRST | 101 | PC28 | 142 | PA4 |
| 20 | XIN | 61 | VDDIO | 102 | VDDIO | 143 | VDDIO |
| 21 | PB3 | 62 | GNDIO | 103 | GNDIO | 144 | GNDIO |
| 22 | PB4 | 63 | PD4 | 104 | PD10 | 145 | PA5 |
| 23 | PB5 | 64 | PD5 | 105 | PD11 | 146 | PA6 |
| 24 | PB6 | 65 | PD6 | 106 | PD12 | 147 | PA7 |
| 25 | VDDIO | 66 | PD7 | 107 | PD13 | 148 | PA8 |
| 26 | GNDIO | 67 | PC0 | 108 | SPWREF0 | 149 | PA9 |
| 27 | PB7 | 68 | PC1 | 109 | PD14 | 150 | PA10 |
| 28 | PB8 | 69 | PC2 | 110 | PD15 | 151 | PA11 |
| 29 | PB9 | 70 | PC3 | 111 | PD16 | 152 | PA12 |
| 30 | PB10 | 71 | PC4 | 112 | PD17 | 153 | PA13 |
| 31 | PB11 | 72 | PC5 | 113 | PD18 | 154 | PA14 |
| 32 | PB12 | 73 | PC6 | 114 | PD19 | 155 | PA15 |
| 33 | PB13 | 74 | PC7 | 115 | PD20 | 156 | PA16 |
| 34 | PB14 | 75 | PC8 | 116 | PD21 | 157 | XIN32 |
| 35 | PB15 | 76 | PC9 | 117 | SPWREF1 | 158 | PC29 |
| 36 | PB16 | 77 | PC10 | 118 | PD22 | 159 | PC30 |
| 37 | PB17 | 78 | PC11 | 119 | PD23 | 160 | PA17 |
| 38 | PB18 | 79 | PD8 | 120 | PD24 | 161 | PA18 |
| 39 | PB19 | 80 | PD9 | 121 | PD25 | 162 | PA19 |
| 40 | VDD_CORE | 81 | VDD_CORE | 122 | VDD_CORE | 163 | VDD_CORE |
| 41 | GND_CORE | 82 | GND_CORE | 123 | GND_CORE | 164 | GND_CORE |

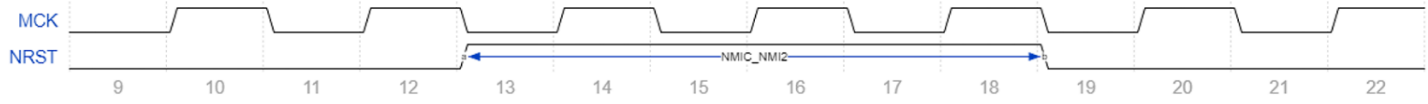
1.10 INSTRUCTION SET AND TIMING DIAGRAMS



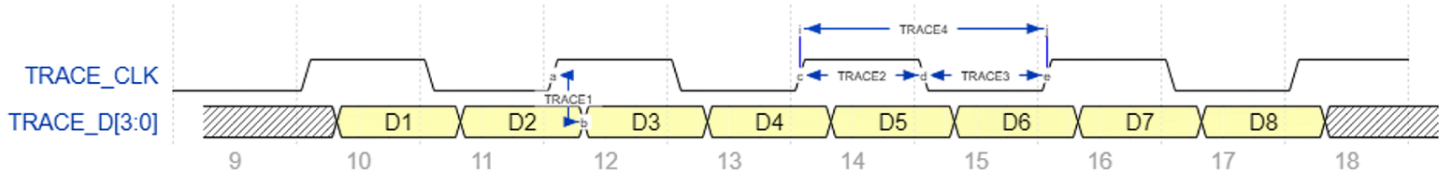

*NRST Characteristics*



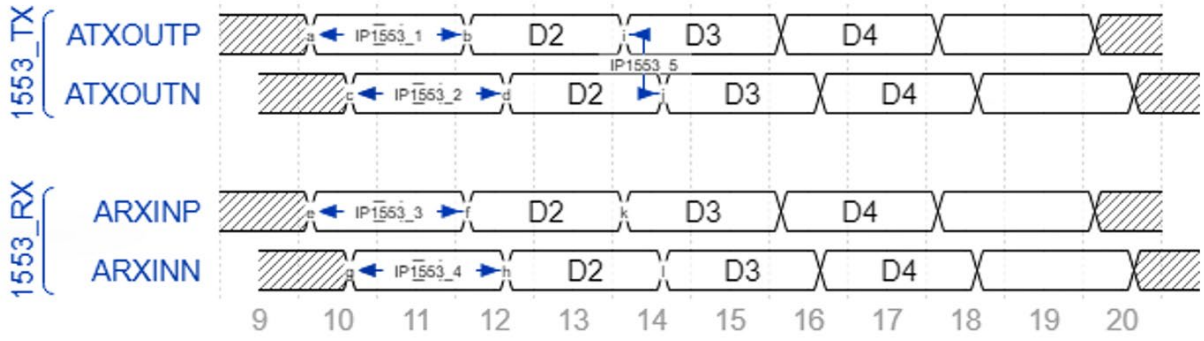

*NMIC_NMI Characteristics (Active Level Low)*



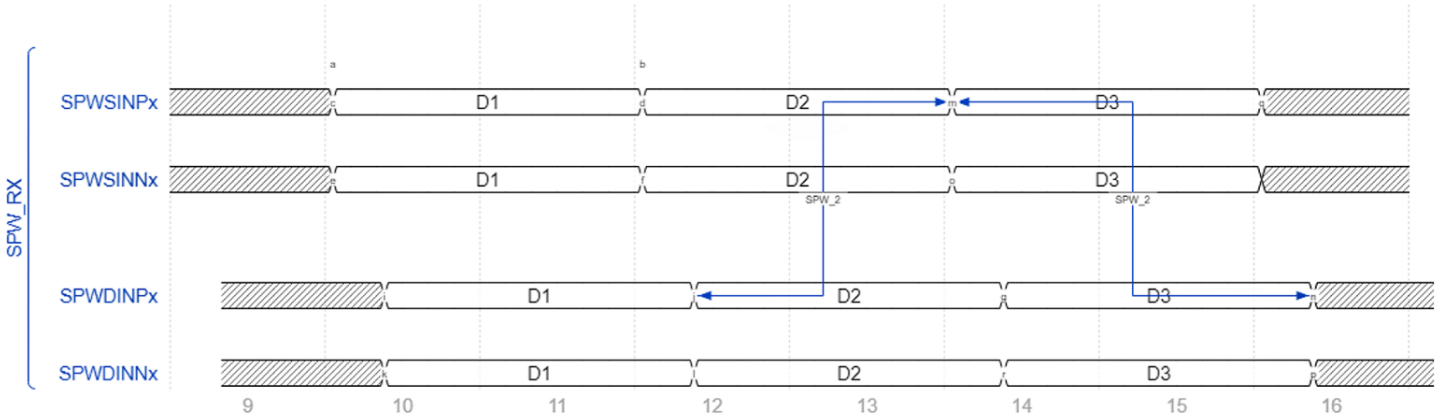

*NMIC_NMI Characteristics (Active Level High)*



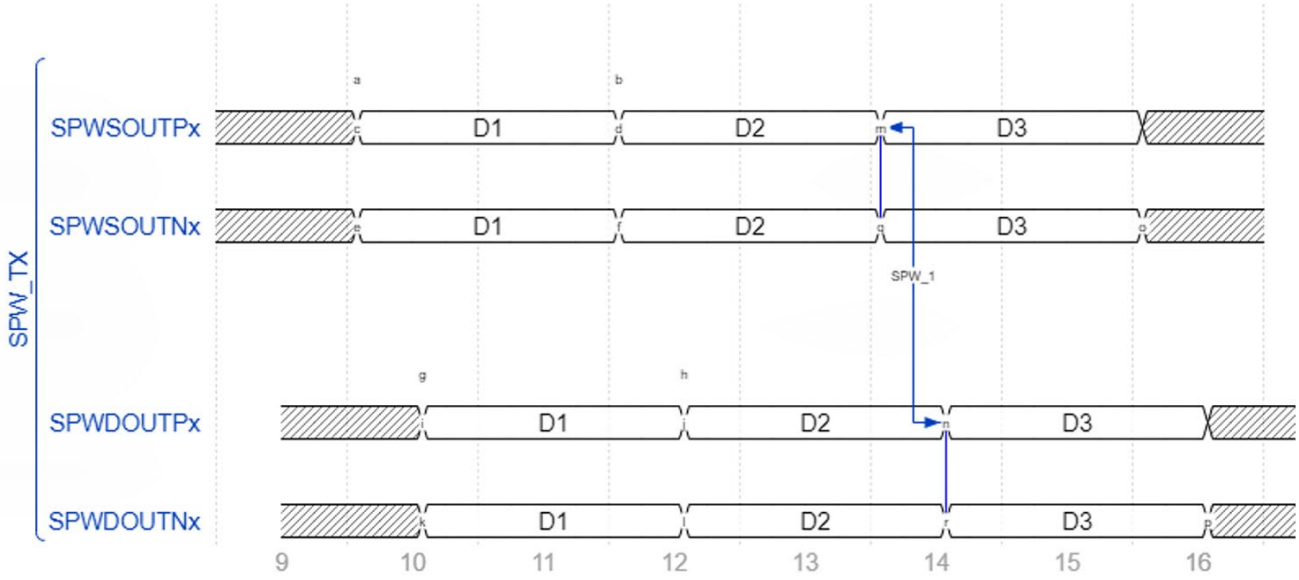

*TRACE Characteristics*



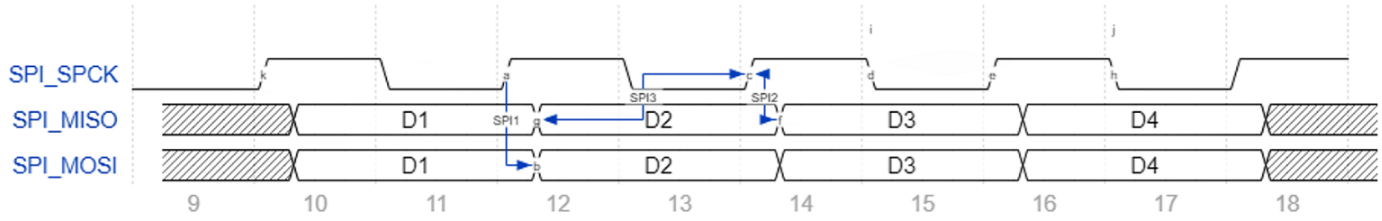

*1553 Characteristics*



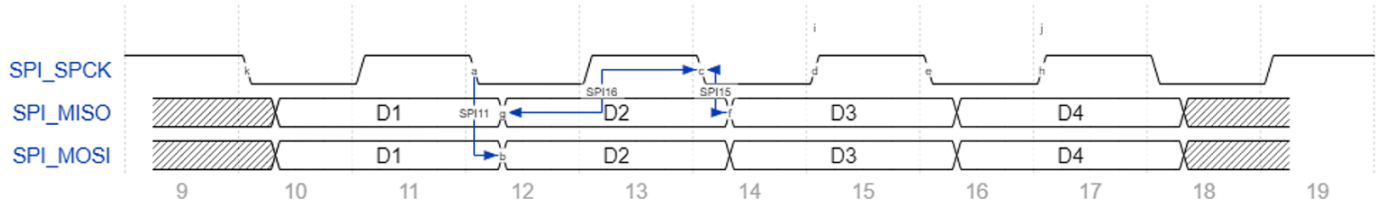

*SPW RX Characteristics*



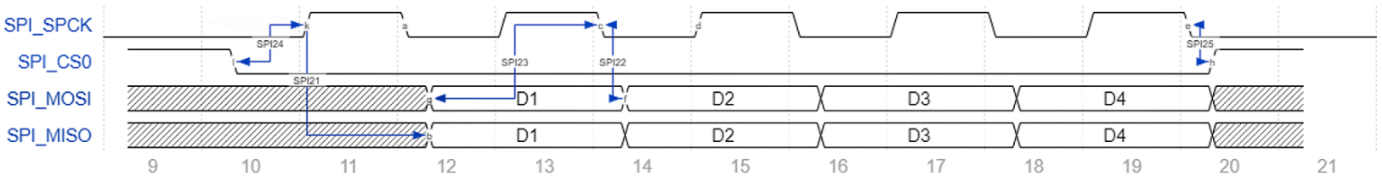

*SPW TX Characteristics*



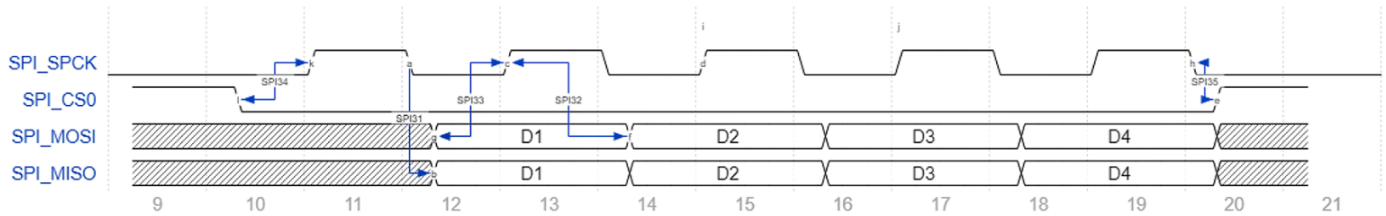

*FlexCOM SPI Characteristics Master Mode (CPOL=0 and NCPHA=0) or (CPOL=1 and NCPHA=1)*



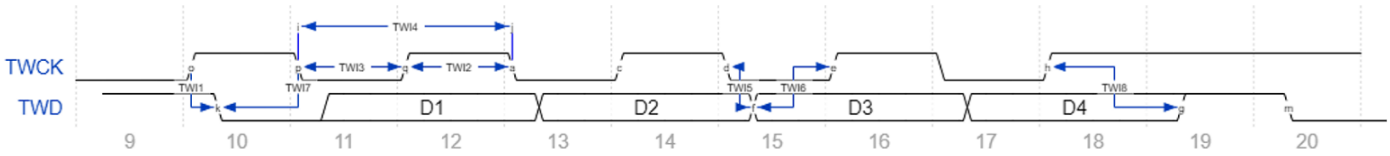

*FlexCOM SPI Characteristics Master Mode (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)*



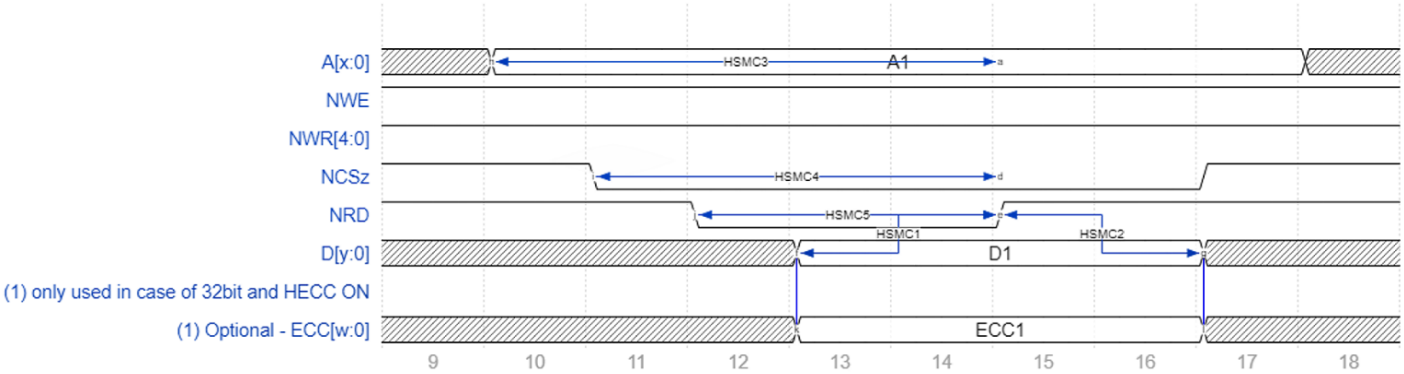

*FlexCOM SPI Characteristics Slave Mode (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)*



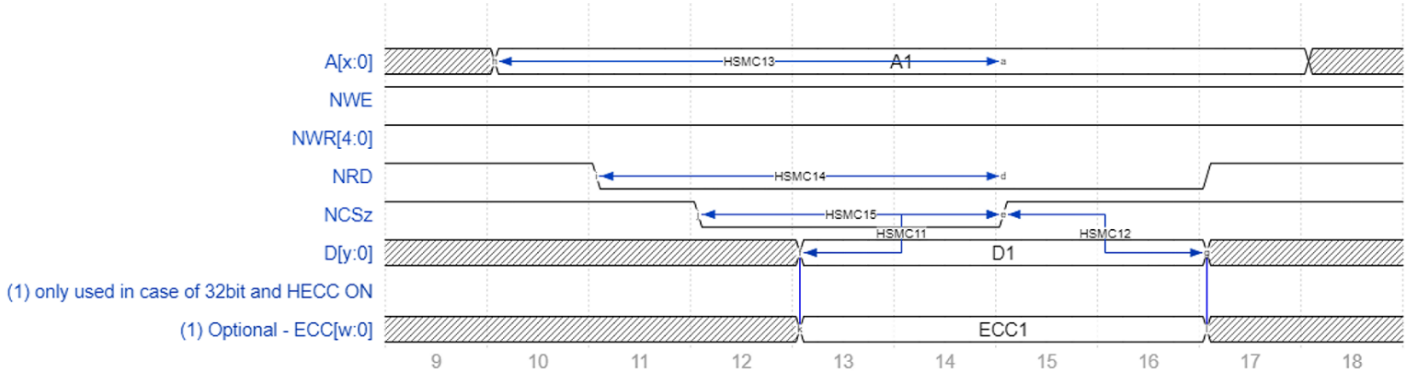

*FlexCOM SPI Characteristics Slave Mode (CPOL=0 and NCPHA=0) or (CPOL=1 and NCPHA=1)*



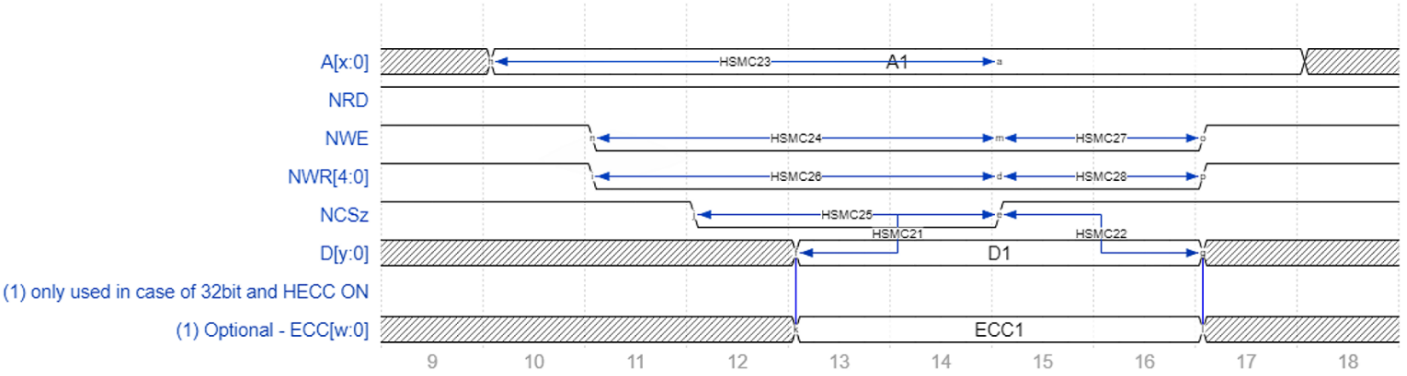

*FlexCOM TWI Characteristics*



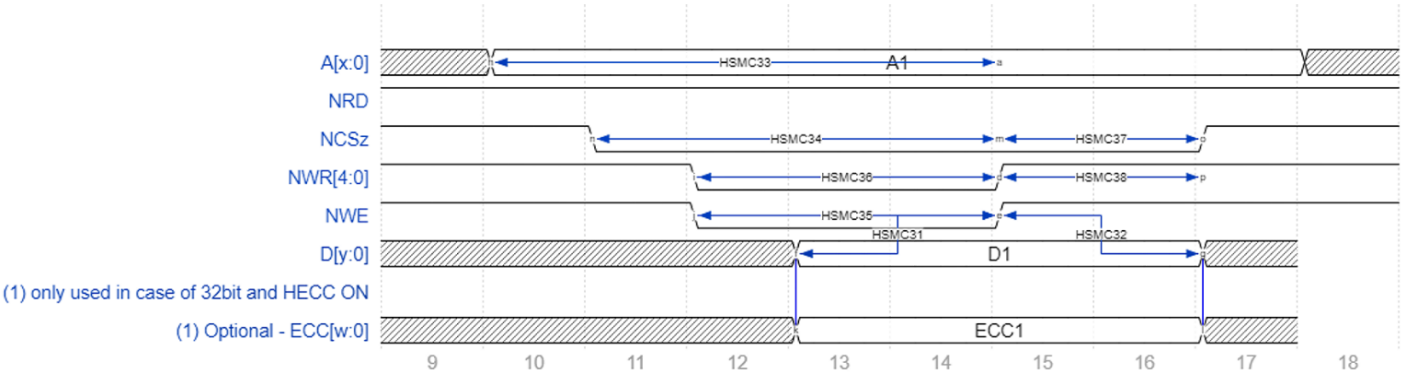

*HSMC Read Data - NRD Controlled - x=[27] ; y=[31,15,7] ; z=[0:5] ; w=[11:7]*



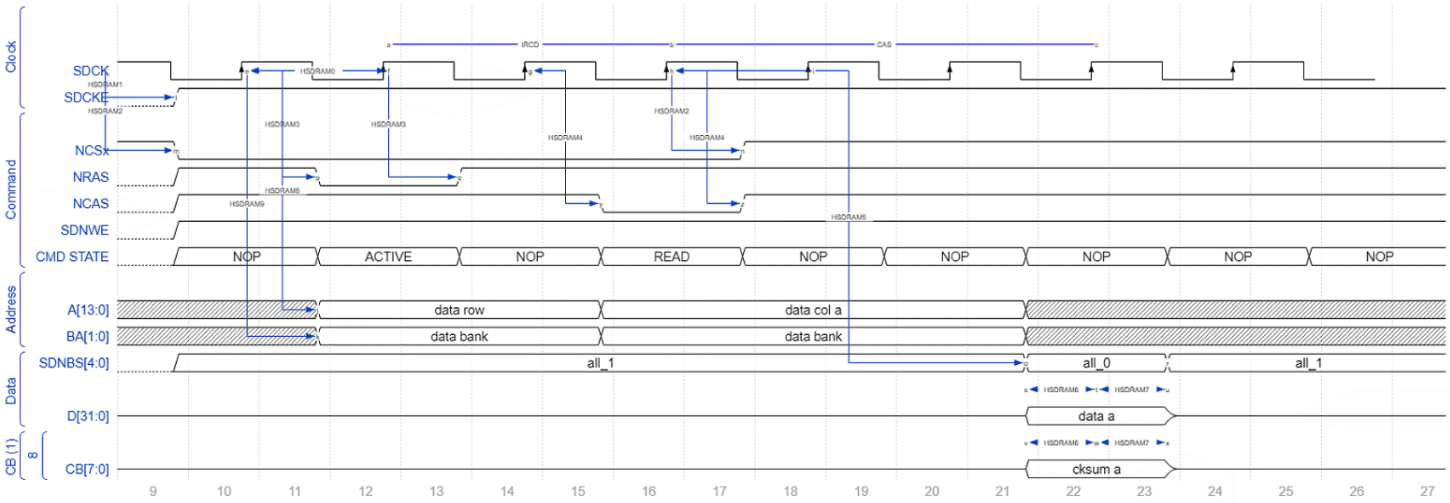

*HSMC Read Data - NCS Controlled - x=[27] ; y=[31,15,7] ; z=[0:5] ; w=[11:7]*



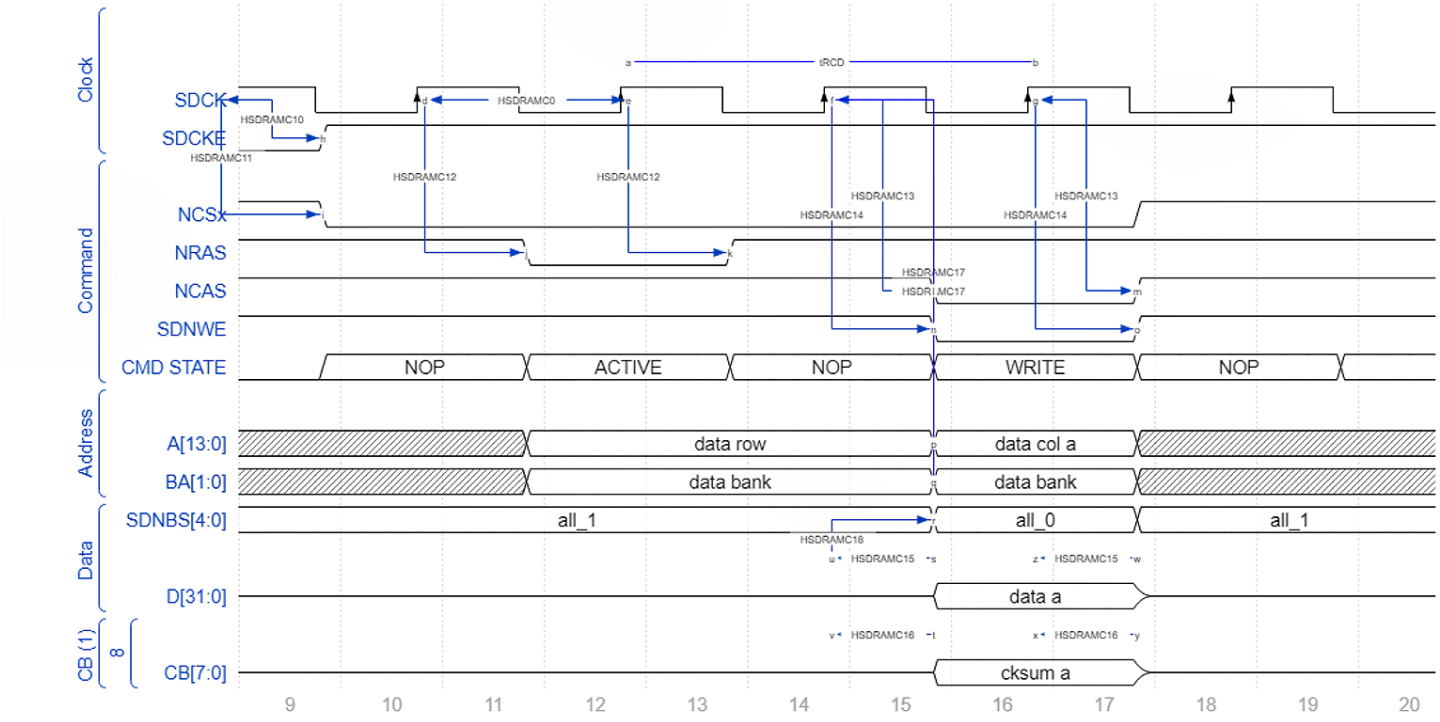

*HSMC Write Data - NCS Controlled Mode - x=[27] ; y=[31,15,7] ; z=[0:5] ; w=[11:7]*



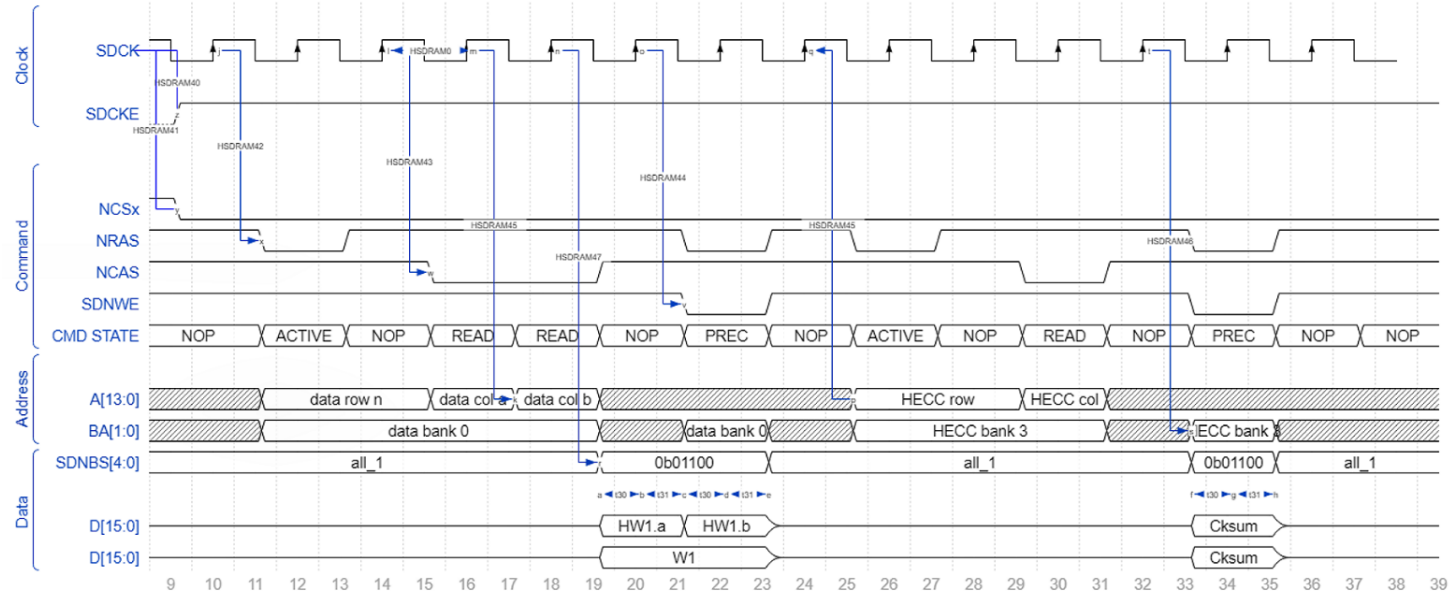

*HSMC Write Data - NWE Controlled - x=[27] ; y=[31,15,7] ; z=[0:5] ; w=[11:7]*



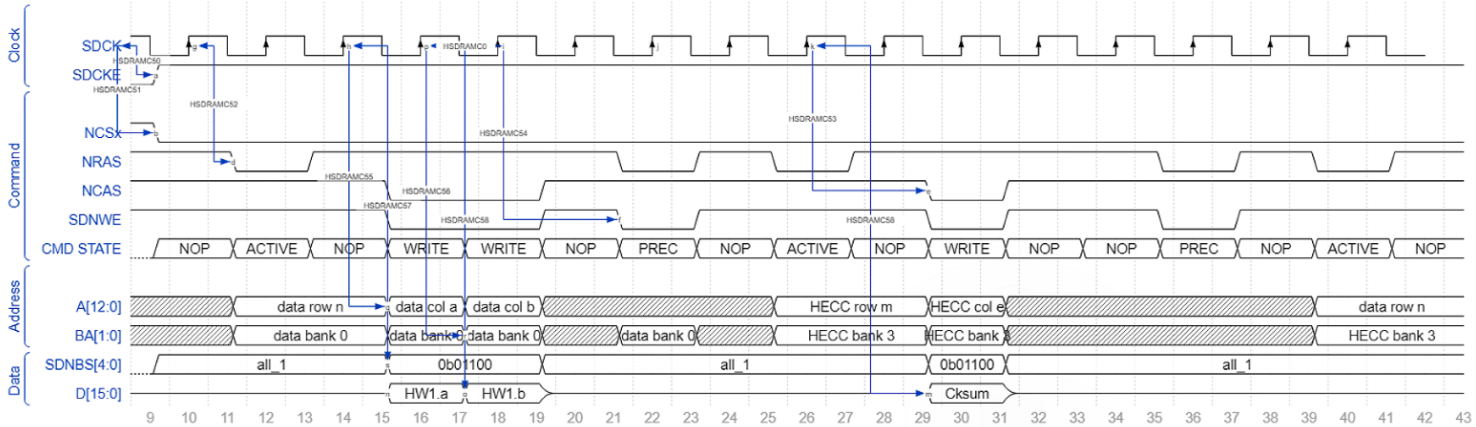

*Read Word Access - 32-bit Memory - HECC ON, HECC OFF*




*Write Word Access - 32-bit Memory - HECC ON, HECC OFF*

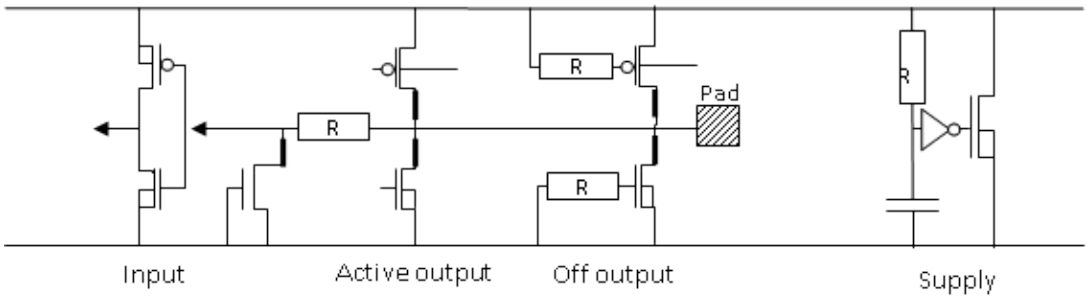



*Read Word Access - 16-bit Memory - HECC ON*




*Write Word Access - 16-bit Memory - HECC ON*

## 1.11 PROTECTION NETWORK




**NOTES:**

1. The ratio of Active Output to Off Output determines the output strength.
2. Resistors R are approximately 400Ω each.
3. Transistors with a snapback mechanism are symbolised by a bold line on the drain side.

## 2 REQUIREMENTS

### 2.1 GENERAL

The complete requirements for procurement of the components specified herein are as stated in this specification and the ESCC Generic Specification. Permitted deviations from the Generic Specification, applicable to this specification only, are listed below.

Permitted deviations from the Generic Specification and this Detail Specification, formally agreed with specific manufacturers on the basis that the alternative requirements are equivalent to the ESCC requirements and do not affect the component's reliability, are listed in the appendices attached to this specification.

#### 2.1.1 Deviations from the Generic Specification

None.

### 2.2 MARKING

The marking shall be in accordance with the requirements of ESCC Basic Specification No. 21700 and as follows.

The information to be marked on the component shall be:

(a) Terminal identification (see Para. 1.7).
(b) The ESCC qualified components symbol (for ESCC qualified component only).
(c) The ESCC Component Number (see Para. 1.4.1).
(d) Traceability information.

### 2.3 ELECTRICAL MEASUREMENTS AT ROOM, HIGH AND LOW TEMPERATURES

Electrical measurements shall be performed at room, high and low temperatures.

#### 2.3.1 Room Temperature Electrical Measurements

The measurements shall be performed at $T_{case}$ = +25(+3 -5)°C.

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions $1.65V < V_{DD} < 1.95V$ $3V < V_{CC} < 3.6V$ (Note 1) | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Functional Tests (Min.) | - | 3014 | $V_{DD}$ = 1.65V<br>$V_{CC}$ = 3V<br>$V_{IH}$ = $V_{DD}$<br>$V_{IL}$ = $V_{SS}$ | - | - | - |
| Functional Tests (Typ.) | - | 3014 | $V_{DD}$ = 1.8V<br>$V_{CC}$ = 3.3V<br>$V_{IH}$ = $V_{DD}$<br>$V_{IL}$ = $V_{SS}$ | - | - | - |
| Functional Tests (Max.) | - | 3014 | $V_{DD}$ = 1.95V<br>$V_{CC}$ = 3.6V<br>$V_{IH}$ = $V_{DD}$<br>$V_{IL}$ = $V_{SS}$ | - | - | - |
| Low Level Input Voltage | $V_{IL}$ | - | CMOS buffers (Note 2) | - | 700 | mV |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions 1.65V < $V_{DD}$ < 1.95V 3V < $V_{CC}$ < 3.6V (Note 1) | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| High Level Input Voltage | $V_{IH}$ | - | CMOS buffers (Note 2) | 2 | - | V |
| Low Level Output Voltage | $V_{OL}$ | 3007 | CMOS buffers $I_{OL}$= 1.8, 3.6, 7.2, 14.4, 21.6 or 28.8mA depending on P-I/O's config. | - | 400 | mV |
| High Level Output Voltage | $V_{OH}$ | 3006 | CMOS buffers $I_{OH}$ = -1.8, -3.6, -7.2, -14.4, -21.6 or -28.8mA depending on P-I/O's config. | $V_{CC}$-0.4 | - | V |
| Low Level Input Current 1 | $I_{IL1}$ | 3009 | CMOS buffers – analog $V_{IN}$ = $V_{SS}$ | -1 | 1 | µA |
| Low Level Input Current 2 | $I_{IL2}$ | 3009 | CMOS buffers – digital $V_{IN}$ = $V_{SS}$ | -1 | 1 | µA |
| Low Level Input Current with Pull-up | $I_{ILPU}$ | 3009 | CMOS buffers $V_{IN}$ = $V_{SS}$ | -48 | -18 | µA |
| High Level Input Current 1 | $I_{IH1}$ | 3010 | CMOS buffers – analog $V_{IN}$ = $V_{CC}$ max | -1 | 1 | µA |
| High Level Input Current 2 | $I_{IH2}$ | 3010 | CMOS buffers – digital $V_{IN}$ = $V_{CC}$ max | -1 | 1 | µA |
| High Level Input Current with Pull-down | $I_{IHPD}$ | 3010 | CMOS buffers $V_{IN}$ = $V_{CC}$ max | 18 | 48 | µA |
| ColdSparing Leakage Current | $I_{CS}$ | 3010 | ColdSparing buffers $V_{IN}$ = $V_{CC}$ max | -1 | 1 | µA |
| LVDS Differential Output Voltage | VOD | 3006 3007 | | 247 | 454 | mV |
| LVDS Difference of Magnitude of VOD for opposite binary state | ΔVOD | 3006 3007 | | - | 50 | mV |
| LVDS Offset Voltage | VOS | 3006 3007 | | 1.125 | 1.375 | V |
| LVDS Difference of Magnitude of VOS for opposite binary state | ΔVOS | 3006 3007 | | - | 50 | mV |
| Array Stand-by Current | $I_{CCSBA}$ | 3005 | $V_{DD}$ max Output = 0mA | - | 20 | mA |
| Array Operating Current | $I_{CCOP}$ | 3005 | $V_{DD}$ max $V_{CC}$ max Coremark / frequency = 50 MHz | - | 500 | mA |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions $1.65V < V_{DD} < 1.95V$ $3V < V_{CC} < 3.6V$ (Note 1) | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Processor Frequency | Freq | 3003 | TimeCoef, Cases of Coremark run in TCM or of Dhrystone run in FlexRam (Note 3) | - | 1 | -- |
| Input Pin Capacitance | $C_{I33}$ | 3012 | CMOS buffers (Note 4) | - | 7 | pF |
| **POR** | | | | | | |
| POR Threshold | POR | 3003 | $V_{CC}$ = 3.3V | 1.47 | 1.6 | V |
| **RC Oscillators** | | | | | | |
| Operating Period RC 32kHz | $t_{OSC}$ | 3003 | (Note 5) | 25 | 42 | µs |
| Operating Period after calibration RC 4MHz | $t_{ACC4}$ | 3003 | (Notes 5, 6) | 227 | 278 | ns |
| Operating Period after calibration RC 8MHz | $t_{ACC8}$ | 3003 | (Notes 5, 6) | 113 | 139 | ns |
| Operating Period after calibration RC 10MHz | $t_{ACC10}$ | 3003 | (Notes 5, 6) | 90 | 112 | ns |
| Operating Period after calibration RC 12MHz | $t_{ACC12}$ | 3003 | (Notes 5, 6) | 75 | 93 | ns |
| **ADC** | | | | | | |
| Differential Non-linearity | $ADC_{DNL}$ | 3003 | In both Single-Ended & Differential modes | -2 | 2 | LSB |
| Integrated Non-linearity | $ADC_{INL}$ | 3003 | In both Single-Ended & Differential modes | -4 | 4 | LSB |
| Gain Error | $ADC_{GE}$ | 3003 | In both Single-Ended & Differential modes | -3 | 3 | % |
| Offset Error | $ADC_{OE}$ | 3003 | In Single-Ended mode<br>In Differential mode | -50<br>-30 | 50<br>30 | LSB |
| **DAC** | | | | | | |
| Differential Non-linearity | $DAC_{DNL}$ | 3003 | In Single-Ended mode<br>In Differential mode | -4<br>-3 | 4<br>3 | LSB |
| Integrated Non-linearity | $DAC_{INL}$ | 3003 | In Single-Ended mode<br>In Differential mode | -4<br>-3 | 4<br>3 | LSB |
| Gain Error | $DAC_{GE}$ | 3003 | In both Single-Ended & Differential modes | -140 | 140 | LSB |

| Characteristics | Symbols | MIL-STD-883 Test Method | Test Conditions $1.65V < V_{DD} < 1.95V$ $3V < V_{CC} < 3.6V$ (Note 1) | Limits | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Offset Error | $DAC_{OE}$ | 3003 | In Single-Ended mode | -75 | 75 | LSB |
| | | | In Differential mode | -30 | 30 | |

**NOTES:**

1. Unless otherwise specified, all inputs and outputs shall be tested for each characteristic. Inputs not under test shall be $V_{IN} = V_{SS}$ or $V_{CC}$ and outputs not under test shall be open. $V_{SS} = 0V$.
2. Tested through Functional Tests.
3. The maximum frequency of the Cortex-M7 processor is obtained using the following formula: $MaxFreq = \frac{1}{TimeCoef}$
4. Guaranteed, not tested.
5. Test conditions: Tester load = 5pF, $V_{IL} = 0V$, $V_{IH} = V_{DD}$, Input signals dynamic characteristics: $t_r$, $t_f < 10ns$, Threshold voltages: $V_{OL} = V_{OH} = V_{DD/2}$.
6. Tested only at $V_{DD} = 1.8V$. Guaranteed by Electrical Characterisation for the full $V_{DD}$ range.

2.3.2 High and Low Temperatures Electrical Measurements

The measurements shall be performed at $T_{case}$ = +125 ±3°C and $T_{case}$ = -55 ±3°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

2.4 PARAMETER DRIFT VALUES

Unless otherwise specified, the measurements shall be performed at $T_{case}$ = +25(+3 -5)°C.

The test methods and test conditions shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.

The drift values (Δ) shall not be exceeded for each characteristic specified. The corresponding absolute limit values for each characteristic shall not be exceeded.

| Characteristics | Symbols | Limits | | | Units |
|---|---|---|---|---|---|
| | | Drift Value Δ | Absolute | | |
| | | | Min | Max | |
| Low Level Output Voltage | $V_{OL}$ | ±100 | - | 400 | mV |
| High Level Output Voltage | $V_{OH}$ | ±0.1 | $V_{CC}$-0.4 | - | V |
| Low Level Input Current 1 and 2 | $I_{IL1}$, $I_{IL2}$ | ±0.03 | -1 | 1 | µA |
| High Level Input Current 1 and 2 | $I_{IH1}$, $I_{IH2}$ | ±0.03 | -1 | 1 | µA |
| ColdSparing Leakage Current | $I_{CS}$ | ±0.03 | -1 | 1 | µA |
| Array Stand-by Current | $I_{CCSBA}$ | ±0.75 | - | 50 | mA |

2.5 INTERMEDIATE AND END-POINT ELECTRICAL MEASUREMENTS

Unless otherwise specified, the measurements shall be performed at $T_{case}$ = +25(+3 -5)°C.

The characteristics, test methods, conditions and limits shall be the same as specified in Para. 2.3.1, Room Temperature Electrical Measurements.

2.6 POWER BURN-IN CONDITIONS

Prior to submitting the parts to Burn-In or Operating Life, a specific application is loaded in the Flash memory. This application automatically starts after the RESET is released. The correct behaviour of the device can be monitored with an on-board LED.

The specific application will run with internal PLL at 37.5MHz (75% of the maximum frequency) and will exercise the following function blocks:

1/ TCMHECC_ITCM
Description: Write and read ITCM memory

2/ TCMHECC_DTCM
Description: Write and read DTCM memory

3/ FlexRAMECC
Description: Write in FlexRAM memory with ECC enabled (Error Code Correction)

4/ TRNG
Description: Start random generator and copy data when available (interrupt)

5/ DACC_to_ADC
Description: External links between DACC (outputs) and ADC (inputs) to use single ended mode and differential mode

6/ PWM
Description: Use 2 PWM channels to output square signals

7/ RTC_to_TC
Description: External link to connect RTC output to TC input

8/ XDMAC
Description: XDMAC transfers data from FlexRAM to DTCM memory

9/ FLEXCOM_TWI
Description: External link (with pullups) between FLEXCOM1 (master) and FLEXCOM3 (slave)

10/ FLEXCOM_SPI
Description: Internal loop back (LLB) mode to check data from SPI bus

11/ FLEXCOM_USART
Description: External link to connect FLEXCOM0 to FLEXCOM2 in UART mode

12/ CAN
Description: Internal loop (LBCK) mode to check data from CAN0 to CAN1

13/ SPW
Description: External links to connect SPW0 to SPW1 (Space wire bus)

14/ ICM_FLEXRAM
Description: Use ICM (Integrity Check Monitor) to transfer data with data check using SHA

15/ IROM
Description: Read all cells of the ROM memory

16/ CRCCU
Description: Compute and compare CRC

This application program runs in loop during several minutes. Then a SCAN program starts (with a toggle coverage >70%) followed by a BIST program to activate DMA, cache and SpaceWire memories.

The activity of “application” + SCAN + BIST programs represent a toggle coverage estimate of > 70%.

| Characteristics | Symbols | Test Conditions | Units |
|---|---|---|---|
| Ambient Temperature | $T_{amb}$ | +125(+8 -0) | °C |
| Core Supply Voltage | $V_{DD}$ | 1.95 | V |
| I/O Supply Voltage | $V_{CC}$ | 3.6 | V |
| Ref. Voltage | $V_{Ref}$ | 1.25 | V |

**NOTES:**

1. Pin connections shall be as follows, where NC = Not Connected:

| Pin | Signal | Loopback to Pin# | Serial Resistance | Wired To | Pin | Signal | Loopback to Pin# | Serial Resistance | Wired To |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GND_CORE | | Direct | GND | 83 | GND_CORE | | Direct | GND |
| 2 | VDD_CORE | | Direct | VDD | 84 | VDD_CORE | | Direct | VDD |
| 3 | PA20 | PD6 65 | 1k | Tester Pin | 85 | PC12 | | | NC |
| 4 | PA21 | PD9 80 | 1k | Tester Pin | 86 | PC13 | | | NC |
| 5 | PA22 | PD8 79 | 1k | Tester Pin | 87 | PC14 | | | NC |
| 6 | PA23 | | | NC | 88 | PC15 | | | NC |
| 7 | PA24 | | | NC | 89 | PC16 | PA26 9 | 1k | Tester Pin |
| 8 | PA25 | | 1k | Tester Pin | 90 | PC17 | PA28 11 | 1k | Tester Pin |
| 9 | PA26 | PC16 89 | 1k | Tester Pin | 91 | PC18 | | | NC |
| 10 | PA27 | | 1k | Tester Pin | 92 | PC19 | | | NC |
| 11 | PA28 | PC17 90 | 1k | Tester Pin | 93 | PC20 | | 1k | Tester Pin |
| 12 | PA29 | | 1k | Tester Pin | 94 | PC21 | | 1k | Tester Pin |
| 13 | PA30 | | 1k | Tester Pin | 95 | PC22 | | 1k | Tester Pin |
| 14 | PA31 | | | NC | 96 | PC23 | | 1k | Tester Pin |
| 15 | PB0 | | | NC | 97 | PC24 | | 1k | Tester Pin |
| 16 | PB1 | | | NC | 98 | PC25 | | 1k | Tester Pin |
| 17 | PB2 | PC26 99 | 1k | Tester Pin | 99 | PC26 | PB2 17 | 1k | Tester Pin |
| 18 | VDD_PLLA/B | | Direct | VDD | 100 | PC27 | | 1k | Tester Pin |
| 19 | GND_PLLA/B | | Direct | GND | 101 | PC28 | | 1k | Tester Pin |
| 20 | XIN | | 10k pull up / 1k | VCC / Tester Pin | 102 | VDDIO | | Direct | VCC |
| 21 | PB3 | | | NC | 103 | GNDIO | | Direct | GND |
| 22 | PB4 | PB22 46 | 1k pull up | VCC | 104 | PD10 | PD20 115 | 1k | Tester Pin |
| 23 | PB5 | PB21 45 | 1k pull up | VCC | 105 | PD11 | PD21 116 | 1k | Tester Pin |
| 24 | PB6 | | | NC | 106 | PD12 | PD18 113 | 1k | Tester Pin |

| Pin | Signal | Loopback to Pin# | Serial Resistance | Wired To | Pin | Signal | Loopback to Pin# | Serial Resistance | Wired To |
|---|---|---|---|---|---|---|---|---|---|
| 25 | VDDIO | | Direct | VCC | 107 | PD13 | PD19 114 | 1k | Tester Pin |
| 26 | GNDIO | | Direct | GND | 108 | SPWREF0 | | direct | Vref |
| 27 | PB7 | | | NC | 109 | PD14 | PD24 120 | 1k | Tester Pin |
| 28 | PB8 | | | NC | 110 | PD15 | PD25 121 | 1k | Tester Pin |
| 29 | PB9 | | | NC | 111 | PD16 | PD22 118 | 1k | Tester Pin |
| 30 | PB10 | | | NC | 112 | PD17 | PD23 119 | 1k | Tester Pin |
| 31 | PB11 | | 1k | Tester Pin | 113 | PD18 | PD12 106 | 1k | Tester Pin |
| 32 | PB12 | | 1k | Tester Pin | 114 | PD19 | PD13 107 | 1k | Tester Pin |
| 33 | PB13 | | | NC | 115 | PD20 | PD10 104 | 1k | Tester Pin |
| 34 | PB14 | | | NC | 116 | PD21 | PD11 105 | 1k | Tester Pin |
| 35 | PB15 | | | NC | 117 | SPWREF1 | | direct | Vref |
| 36 | PB16 | | | NC | 118 | PD22 | PD16 111 | 1k | Tester Pin |
| 37 | PB17 | | | NC | 119 | PD23 | PD17 112 | 1k | Tester Pin |
| 38 | PB18 | | | NC | 120 | PD24 | PD14 109 | 1k | Tester Pin |
| 39 | PB19 | | | NC | 121 | PD25 | PD15 110 | 1k | Tester Pin |
| 40 | VDD_CORE | | Direct | VDD | 122 | VDD_CORE | | Direct | VDD |
| 41 | GND_CORE | | Direct | GND | 123 | GND_CORE | | Direct | GND |
| 42 | GND_CORE | | Direct | GND | 124 | GND_CORE | | Direct | GND |
| 43 | VDD_CORE | | Direct | VDD | 125 | VDD_CORE | | Direct | VDD |
| 44 | PB20 | | | NC | 126 | PD28 | PA3 141 | 1k | Tester Pin |
| 45 | PB21 | PB5 23 | 1k pull up | VCC | 127 | PD29 | PA0 138 | 1k | Tester Pin |
| 46 | PB22 | PB4 46 | 1k pull up | VCC | 128 | PD30 | PA1 139 | 1k | Tester Pin |
| 47 | PB23 | | 1k | Tester Pin | 129 | PD31 | PA2 140 | 1k | Tester Pin |
| 48 | PB24 | | 1k | Tester Pin | 130 | VDDIO_DAC | | Direct | VCC |
| 49 | PB25 | | | NC | 131 | GNDIO_DAC | | Direct | GND |
| 50 | PB26 | | | NC | 132 | AD_DAC_GNDREF | | | GND |
| 51 | PB27 | | | NC | 133 | AD_DAC_VREFIN | | | VCC |
| 52 | PB28 | | | NC | 134 | ANA_GND | | Direct | GND |
| 53 | PD0 | | | NC | 135 | ANA_3V3 | | Direct | VCC |
| 54 | PD1 | | | NC | 136 | VDDIO_ADC | | Direct | VCC |
| 55 | PD2 | | | NC | 137 | GNDIO_ADC | | Direct | GND |
| 56 | PD3 | | | Tester Pin / Led / VDD for monitoring | 138 | PA0 | PD29 127 | 1k | Tester Pin |
| 57 | TST | | 10k pull down / 1k | GND / Tester Pin | 139 | PA1 | PD30 128 | 1k | Tester Pin |
| 58 | JTAGSEL | | 1k | Tester Pin | 140 | PA2 | PD31 129 | 1k | Tester Pin |

| Pin | Signal | Loopback to Pin# | Serial Resistance | Wired To | Pin | Signal | Loopback to Pin# | Serial Resistance | Wired To |
|---|---|---|---|---|---|---|---|---|---|
| 59 | NMIC_NMI | | 1k | Tester Pin | 141 | PA3 | PD28 126 | 1k | Tester Pin |
| 60 | NRST | | 10k pull up / 1k | VCC / Tester Pin | 142 | PA4 | | 1k | Tester Pin |
| 61 | VDDIO | | Direct | VCC | 143 | VDDIO | | Direct | VCC |
| 62 | GNDIO | | Direct | GND | 144 | GNDIO | | Direct | GND |
| 63 | PD4 | | 1k | Tester Pin | 145 | PA5 | | 1k | Tester Pin |
| 64 | PD5 | | 1k | Tester Pin | 146 | PA6 | | 1k | Tester Pin |
| 65 | PD6 | PA20 3 | 1k | Tester Pin | 147 | PA7 | | 1k | Tester Pin |
| 66 | PD7 | | 1k | Tester Pin | 148 | PA8 | | 1k | Tester Pin |
| 67 | PC0 | | | NC | 149 | PA9 | | 1k | Tester Pin |
| 68 | PC1 | | | NC | 150 | PA10 | | 1k | Tester Pin |
| 69 | PC2 | | | NC | 151 | PA11 | | 1k | Tester Pin |
| 70 | PC3 | | | NC | 152 | PA12 | | 1k | Tester Pin |
| 71 | PC4 | | 1k | Tester Pin | 153 | PA13 | | 1k | Tester Pin |
| 72 | PC5 | | 1k | Tester Pin | 154 | PA14 | | 1k | Tester Pin |
| 73 | PC6 | | | NC | 155 | PA15 | | 1k | Tester Pin |
| 74 | PC7 | | | NC | 156 | PA16 | | | NC |
| 75 | PC8 | | | NC | 157 | XIN32 | | 10k pull up / 1k | VCC / Tester Pin |
| 76 | PC9 | | | NC | 158 | PC29 | | Pull Down 10k / 1k | GND / Tester Pin |
| 77 | PC10 | | | NC | 159 | PC30 | | Pull Down 10k / 1k | GND / Tester Pin |
| 78 | PC11 | | | NC | 160 | PA17 | | | NC |
| 79 | PD8 | PA22 5 | 1k | Tester Pin | 161 | PA18 | | | NC |
| 80 | PD9 | PA21 4 | 1k | Tester Pin | 162 | PA19 | | 1k | Tester Pin |
| 81 | VDD_CORE | | Direct | VDD | 163 | VDD_CORE | | Direct | VDD |
| 82 | GND_CORE | | Direct | GND | 164 | GND_CORE | | Direct | GND |

2.7 HIGH TEMPERATURE REVERSE BIAS BURN-IN (STATIC BURN-IN) CONDITIONS

For the High Temperature Reverse Bias Burn-In, no code needs to be loaded into the Flash. The hardware remains the same as for the Power Burn-In, except for a jumper instead of a 2.2kΩ resistor on pin 28 (NRST).

2.8 OPERATING LIFE CONDITIONS

The conditions shall be as specified in Para. 2.6, Power Burn-in Conditions.

2.9 TOTAL DOSE IRRADIATION TESTING

2.9.1 Bias Conditions and Total Dose Level for Total Dose Radiation Testing

Continuous bias shall be applied during irradiation testing as specified below.

The total dose level applied shall be as specified in Para. 1.4.2 or in the Purchase Order.

| Characteristics | Symbols | Test Conditions | Units |
|---|---|---|---|
| Ambient Temperature | $T_{amb}$ | +22±3 | °C |
| Core Supply Voltage | $V_{DD}$ | 1.95 | V |
| I/O Supply Voltage | $V_{CC}$ | 3.6 | V |

**NOTES:**

1. Pin connections shall be as follows, where NC = not connected:

| Pin | Signal | Serial Resistance | Wired To | Pin | Signal | Serial Resistance | Wired To |
|---|---|---|---|---|---|---|---|
| 1 | GND_CORE | Direct | GND | 83 | GND_CORE | Direct | GND |
| 2 | VDD_CORE | Direct | VDD | 84 | VDD_CORE | Direct | VDD |
| 3 | PA20 | 2.2k | VCC | 85 | PC12 | 5.6k | VCC-GND |
| 4 | PA21 | 2.2k | VCC | 86 | PC13 | 5.6k | VCC-GND |
| 5 | PA22 | 2.2k | VCC | 87 | PC14 | 5.6k | VCC-GND |
| 6 | PA23 | 2.2k | VCC | 88 | PC15 | 5.6k | VCC-GND |
| 7 | PA24 | 2.2k | VCC | 89 | PC16 | 5.6k | VCC-GND |
| 8 | PA25 | Direct | JTAG | 90 | PC17 | 5.6k | VCC-GND |
| 9 | PA26 | 100k | VCC | 91 | PC18 | 5.6k | VCC-GND |
| 10 | PA27 | 2.2k | VCC | 92 | PC19 | 5.6k | VCC-GND |
| 11 | PA28 | 2.2k | VCC | 93 | PC20 | 5.6k | VCC-GND |
| 12 | PA29 | 2.2k | VCC | 94 | PC21 | 5.6k | VCC-GND |
| 13 | PA30 | 2.2k | VCC | 95 | PC22 | 5.6k | VCC-GND |
| 14 | PA31 | 2.2k | VCC | 96 | PC23 | 5.6k | VCC-GND |
| 15 | PB0 | 2.2k | VCC | 97 | PC24 | 5.6k | VCC-GND |
| 16 | PB1 | 2.2k | VCC | 98 | PC25 | 5.6k | VCC-GND |
| 17 | PB2 | 2.2k | VCC | 99 | PC26 | 5.6k | VCC-GND |
| 18 | VDD_PLLA/B | Direct | VDD | 100 | PC27 | 5.6k | VCC-GND |
| 19 | GND_PLLA/B | Direct | GND | 101 | PC28 | 5.6k | VCC-GND |
| 20 | XIN | 2.2k | GND | 102 | VDDIO | Direct | VCC |
| 21 | PB3 | 2.2k | VCC | 103 | GNDIO | Direct | GND |
| 22 | PB4 | 2.2k | VCC | 104 | PD10 | 2.2k | VCC |
| 23 | PB5 | 2.2k | VCC | 105 | PD11 | 2.2k | VCC |
| 24 | PB6 | 5.6k | VCC-GND | 106 | PD12 | 2.2k | VCC |
| 25 | VDDIO | Direct | VCC | 107 | PD13 | 2.2k | VCC |

| Pin | Signal | Serial Resistance | Wired To | Pin | Signal | Serial Resistance | Wired To |
|---|---|---|---|---|---|---|---|
| 26 | GNDIO | Direct | GND | 108 | SPWREF0 | Div. Bridge | VDD |
| 27 | PB7 | 2.2k | VCC | 109 | PD14 | 2.2k | VCC |
| 28 | PB8 | 2.2k | VCC | 110 | PD15 | 2.2k | VCC |
| 29 | PB9 | 2.2k | VCC | 111 | PD16 | 2.2k | VCC |
| 30 | PB10 | 2.2k | VCC | 112 | PD17 | 2.2k | VCC |
| 31 | PB11 | 1k | VCC | 113 | PD18 | 2.2k | VCC |
| 32 | PB12 | 2.2k | VCC | 114 | PD19 | 2.2k | VCC |
| 33 | PB13 | 2.2k | VCC | 115 | PD20 | 2.2k | VCC |
| 34 | PB14 | 2.2k | VCC | 116 | PD21 | 2.2k | VCC |
| 35 | PB15 | 2.2k | VCC | 117 | SPWREF1 | Div. Bridge | VDD |
| 36 | PB16 | 2.2k | VCC | 118 | PD22 | 2.2k | VCC |
| 37 | PB17 | 2.2k | VCC | 119 | PD23 | 2.2k | VCC |
| 38 | PB18 | 2.2k | VCC | 120 | PD24 | 2.2k | VCC |
| 39 | PB19 | 2.2k | VCC | 121 | PD25 | 2.2k | VCC |
| 40 | VDD_CORE | Direct | VDD | 122 | VDD_CORE | Direct | VDD |
| 41 | GND_CORE | Direct | GND | 123 | GND_CORE | Direct | GND |
| 42 | GND_CORE | Direct | GND | 124 | GND_CORE | Direct | GND |
| 43 | VDD_CORE | Direct | VDD | 125 | VDD_CORE | Direct | VDD |
| 44 | PB20 | 2.2k | VCC | 126 | PD28 | 2.2k | VCC |
| 45 | PB21 | 2.2k | VCC | 127 | PD29 | 2.2k | VCC |
| 46 | PB22 | 2.2k | VCC | 128 | PD30 | 2.2k | VCC |
| 47 | PB23 | Direct | JTAG | 129 | PD31 | 2.2k | VCC |
| 48 | PB24 | 100k | VCC | 130 | VDDIO_DAC | Direct | VCC |
| 49 | PB25 | 2.2k | VCC | 131 | GNDIO_DAC | Direct | GND |
| 50 | PB26 | 2.2k | VCC | 132 | AD_DAC_GNDREF | Direct | GND |
| 51 | PB27 | 2.2k | VCC | 133 | AD_DAC_VREFIN | Direct | VCC |
| 52 | PB28 | 2.2k | VCC | 134 | ANA_GND | Direct | GND |
| 53 | PD0 | 2.2k | VCC | 135 | ANA_3V3 | Direct | VCC |
| 54 | PD1 | 2.2k | VCC | 136 | VDDIO_ADC | Direct | VCC |
| 55 | PD2 | 2.2k | VCC | 137 | GNDIO_ADC | Direct | GND |
| 56 | PD3 | 2.2k | VCC | 138 | PA0 | 2.2k | VCC |
| 57 | TST | 2.2k | GND | 139 | PA1 | 2.2k | VCC |
| 58 | JTAGSEL | 2.2k | GND | 140 | PA2 | 2.2k | VCC |
| 59 | NMIC_NMI | 2.2k | GND | 141 | PA3 | 2.2k | VCC |
| 60 | NRST | 100k | (*) | 142 | PA4 | 2.2k | VCC |
| 61 | VDDIO | Direct | VCC | 143 | VDDIO | Direct | VCC |
| 62 | GNDIO | Direct | GND | 144 | GNDIO | Direct | GND |

| Pin | Signal | Serial Resistance | Wired To | Pin | Signal | Serial Resistance | Wired To |
|---|---|---|---|---|---|---|---|
| 63 | PD4 | 2.2k | VCC | 145 | PA5 | 2.2k | VCC |
| 64 | PD5 | 5.6k | VCC-GND | 146 | PA6 | 2.2k | VCC |
| 65 | PD6 | 5.6k | VCC-GND | 147 | PA7 | 2.2k | VCC |
| 66 | PD7 | 5.6k | VCC-GND | 148 | PA8 | 2.2k | VCC |
| 67 | PC0 | 5.6k | VCC-GND | 149 | PA9 | 2.2k | VCC |
| 68 | PC1 | 5.6k | VCC-GND | 150 | PA10 | 2.2k | VCC |
| 69 | PC2 | 5.6k | VCC-GND | 151 | PA11 | 2.2k | VCC |
| 70 | PC3 | 5.6k | VCC-GND | 152 | PA12 | 2.2k | VCC |
| 71 | PC4 | 5.6k | VCC-GND | 153 | PA13 | 2.2k | VCC |
| 72 | PC5 | 5.6k | VCC-GND | 154 | PA14 | 2.2k | VCC |
| 73 | PC6 | 5.6k | VCC-GND | 155 | PA15 | 2.2k | VCC |
| 74 | PC7 | 5.6k | VCC-GND | 156 | PA16 | 2.2k | VCC |
| 75 | PC8 | 5.6k | VCC-GND | 157 | XIN32 | 2.2k | GND |
| 76 | PC9 | 5.6k | VCC-GND | 158 | PC29 | 2.2k | GND |
| 77 | PC10 | 5.6k | VCC-GND | 159 | PC30 | 2.2k | GND |
| 78 | PC11 | 5.6k | VCC-GND | 160 | PA17 | 2.2k | VCC |
| 79 | PD8 | 2.2k | GND | 161 | PA18 | 2.2k | VCC |
| 80 | PD9 | 2.2k | VCC | 162 | PA19 | 2.2k | VCC |
| 81 | VDD_CORE | Direct | VDD | 163 | VDD_CORE | Direct | VDD |
| 82 | GND_CORE | Direct | GND | 164 | GND_CORE | Direct | GND |

*N.B. – to release the RESET, a switch is used on pin 60 (NRST) to connect from GND to $V_{CC}$.

2.9.2 Electrical Measurements for Total Dose Radiation Testing

Prior to, during and on completion of irradiation testing the devices shall have successfully met the Room Temperature Electrical Measurements specified in Para. 2.3.1.

Unless otherwise stated the measurements shall be performed at $T_{case}$ = +25(+3 -5)°C.

The characteristics, test methods, conditions and limits shall be as per the corresponding test defined in Para. 2.3.1, Room Temperature Electrical Measurements.