# ESCC9030 Qualified Space Grade FPGA’s & Processors EU supply chain

STMicroelectronics & CNES

# Agenda

1 Rennes Site

2 Space grade packaging for FPGAs and processors

3 Assembly line qualification

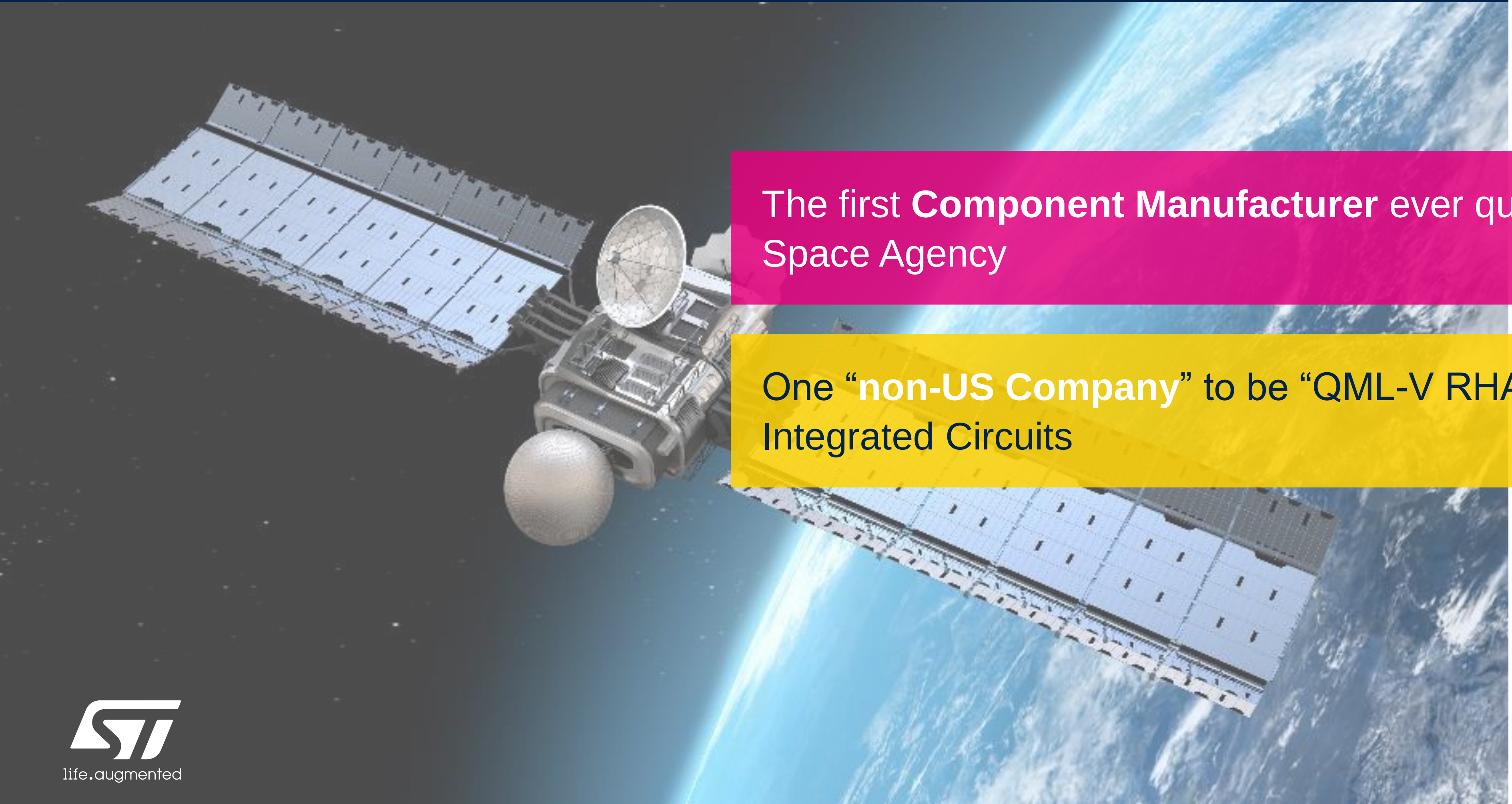
4 ESCC9030 Qualification

5 Conclusion & perspectives

# STMicroelectronics Rennes Space ID Card

45 Years committed to Space Business

The only **Competence Center** within the ST group 100% dedicated to ST’s High-Reliability parts portfolio



The first **Component Manufacturer** ever qualified by the European Space Agency

One “**non-US Company**” to be “QML-V RHA” qualified by DLA for Integrated Circuits

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# STMicroelectronics Rennes Space ID Card

## 45 Years committed to Space Business

### Over 45 years commitment to Space

- Mature ESCC and QML-V qualified products
- State-of-the-art assembly facility
- Range of proprietary rad-capable technologies
- Industry longest product lifetime
- Millions of flying years without failures

### Class 1 Fab

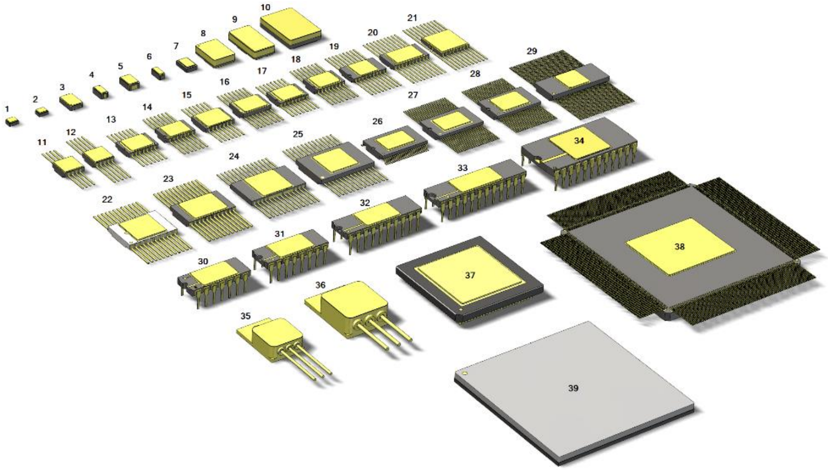
- ISO5 Clean room for assembly
- State of the art equipment
- Upgraded processes and methods
- Strong space class1 packaging knowledge
- Wire bonded and Flip Chip technologies

### Wide range of proprietary technologies

- From planar discrete transistor to CMOS 28nm

### Capacity for small to medium volume

- Fully dedicated to space business
- Total installed capacity : 600 ku / year
- 20 to 24 weeks typical leadime



# STMicroelectronics Rennes Space ID Card

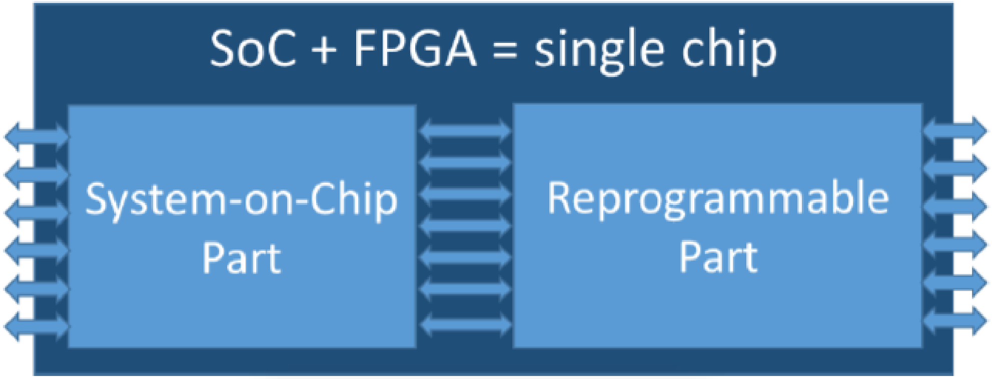
## 45 Years committed to Space Business

# Space Grade FPGAs and Processors


**NG-Ultra**

The European rad-hard SoC + FPGA suitable for future space applications

ESCCON 2023



Initiated by **CNES**, collaboration between Airbus & TAS to develop a European Chip by H2020

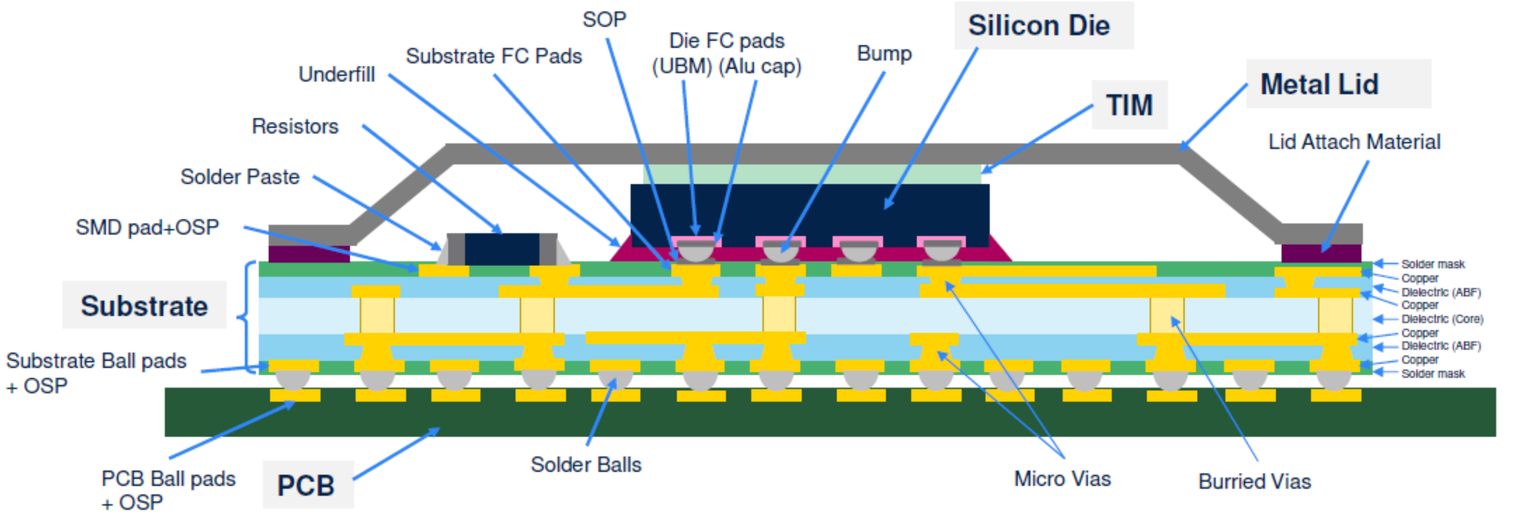
**NanoExplore** owns and commercialize the product manufactured by **STMicroelectronics**

and Qualification is supported by **CNES, ESA** and **EU**

**NG-Ultra = SoC + FPGA**

Horizon 2020 was the EU's research and innovation funding programme from 2014-2020

# Thermally Enhanced Flip Chip BGA EU Supply chain



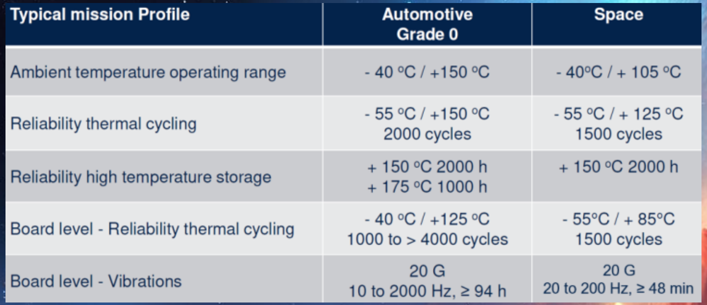
Silicon from Crolles Wafer Fab

EWS and Final test in Grenoble

Assembly in Rennes new dedicated line

# Thermally Enhanced Flip Chip BGA EU Supply chain

## Space packaging challenges similar to Automotive one



| Typical mission Profile | Automotive Grade 0 | Space |
|---|---|---|
| Ambient temperature operating range | - 40 °C / +150 °C | - 40°C / + 105 °C |
| Reliability thermal cycling | - 55 °C / +150 °C<br>2000 cycles | - 55 °C / + 125 °C<br>1500 cycles |
| Reliability high temperature storage | + 150 °C 2000 h<br>+ 175 °C 1000 h | + 150 °C 2000 h |
| Board level - Reliability thermal cycling | - 40 °C / +125 °C<br>1000 to > 4000 cycles | - 55°C / + 85°C<br>1500 cycles |
| Board level - Vibrations | 20 G<br>10 to 2000 Hz, ≥ 94 h | 20 G<br>20 to 200 Hz, ≥ 48 min |

**Electrical Performances** : High count bumps (10 to 20k) and High operating frequency (MHz to 28 GHz)

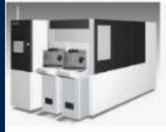
**Thermal Management** : High dissipation (up to 60W)

**Reliability** : Material delamination, Cracks & Voids, Package warpage, Board level reliability

ISO5 Clean room

# BEM&T Rennes – ASIC FC line

| **Main assy steps** | Back Grinding | Laser Groove | Saw | SMD | FC | UF | Lid Attach | Ball Attach |
|---|---|---|---|---|---|---|---|---|
| **Equipment & capability** | 300mm<br>Down to 300µm | 300mm<br>Ablation | 300mm Dual Cut | Screen Printing<br>& Chip Shooter<br>SMD down to 01005 | Pick&Place (+/- 7µm)<br>Reflow<br>Flux Cleaning | Surface preparation<br>Dispense<br>Curing | Double Dispense<br>Pick&Place<br>Curing | Flux & Ball<br>Reflow<br>Flux Cleaning |








**Specific Metrology**


X-Ray


SAM

# Assembly Line Qualification

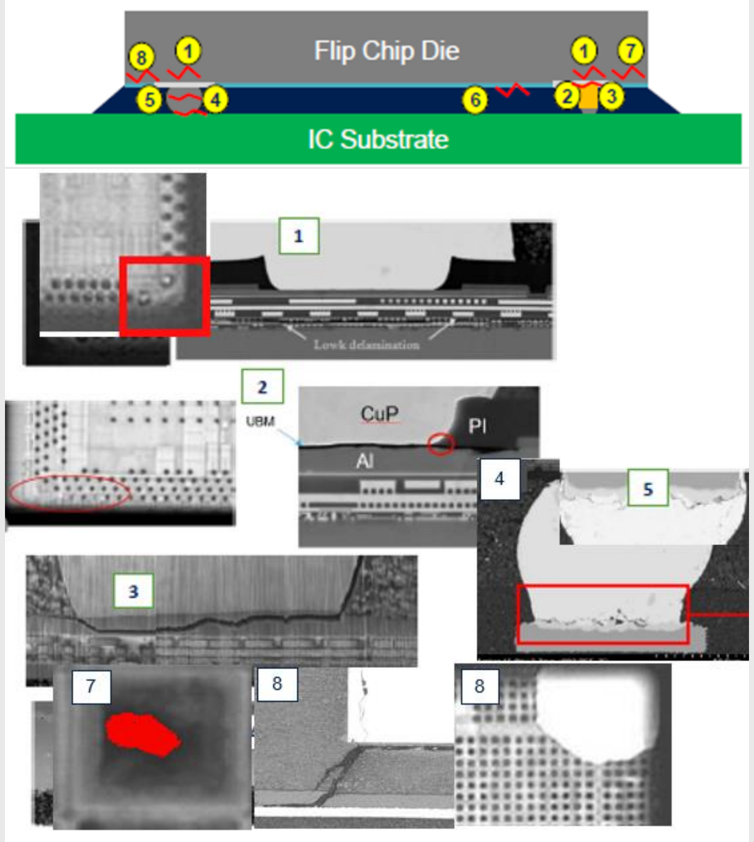
## Qualification program

- Select and set-up robust materials and process parameters (Corner lots)
- Assemble derisking lots with these set-ups and parameters
- Run extended qualification plan to assess package robustness and reliability
- Assess tin whiskers grow risk

## Reliability Test Set

- Temperature Cycling
  (-55°C/+125°C)
- Unbiased Highly Accelerated Stress Test
  (85%RH/85°C/230kPa)
- High Temperature Storage
  (150°C – 500hrs steps up to 2500hrs)
- Mechanical shocks & Vibrations
  (TM 2002 cond. B & TM 2007 cond. A)

## Potential Failure Modes



# Assembly Line Qualification & Monitoring

Material screening

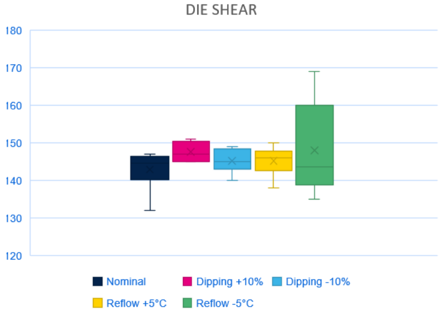
Visual Inspection

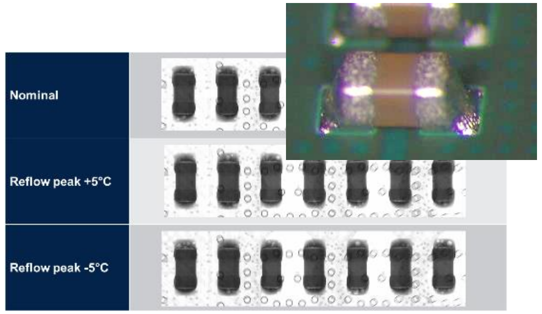
(Hot) Shear Test

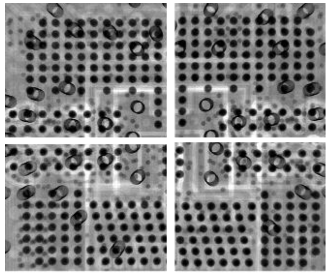
C-SAM

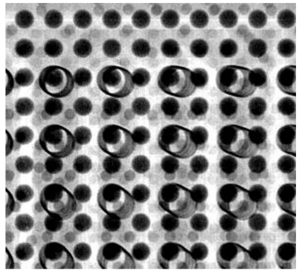
Contact Angle

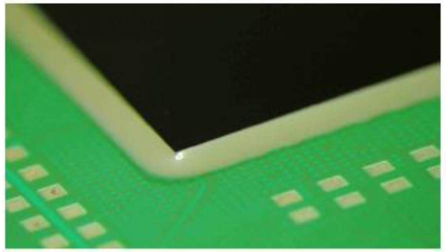
| Flux | Cleaning | LEG | Qty | Process variation | Other Process variation | Optical observations (Bino x30)<br>*2u/leg after shear test*<br>Severity \| location \| type of defect<br>[Refer to annex slide] | T0 (fails) | MSL4+500TC | MSL4+1000TC |
|---|---|---|---|---|---|---|---|---|---|
| A | Water | 1-ULTRA | 7 | PROCESS B (IMPROVED) | | 2 \| Square zone \| Die type C & D | 0/1 | 0/3 | 0/3 |
| | Water | 1b-VT6G | 12 | | | 2 \| Random \| Die type C & D | 0/4 | 0/4 | 0/4 |
| | Water | 1c-VT6G | 11 | | Plasma C | 2 \| Random \| Die type C & D | 0/4 | 0/3 | 0/4 |
| | CL Agent 15% | 3-ULTRA | 12 | | | 0 defect visible @bino_x30<br>@micro_x150 => 2 \| Center \| Type C & D | 0/4 | 0/4 | 0/4 |
| | | 3b VT6G | 8 | | | 2 \| Random \| Type D | 0/2 | 1/3<br>(Xsection => no delam) | 0/3 |
| | CL Agent 25% | 6-ULTRA | 8 | | | 1 \| Square zone \| Type D | 0/2 | 0/3 | 0/3 |
| | | 6b-VT6G | 8 | | | 2 \| Random \| Die type D | 0/2 | 0/3 | 0/3 |
| B | CL Agent 15% | 2-ULTRA | 13 | | | 1 \| Center \| Type E | 1/4<br>(Xsection => Delam + FM) | 1/4<br>Xsection => delam at die edge | 1/5<br>Xsection => delam at die edge |
| | CL Agent 25% | 4-ULTRA | 10 | | Limited staging time | 1 \| Square zone \| Type D | 0/2 | 4/4 | 1/4 |
| | | 5-ULTRA | 12 | | Std 3h30-4h00 out of dry box | 1 \| Square zone \| Type D | 0/2 | 0/3 | 1/7 |
| | CL Agent 25% | 7-ULTRA (REFERENCE) | 9 | PROCESS A (REFERENCE) | | 1 \| Square zone \| Type D | 0/2 | 3/3 | 3/4 |

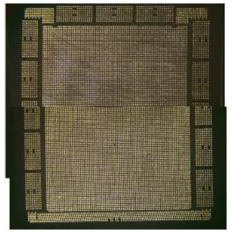


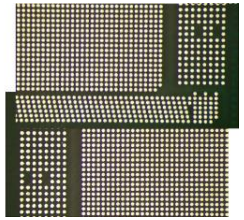


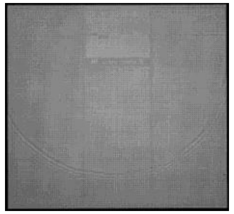

4 corners bump alignment inspection

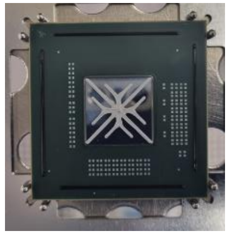

Bump void inspection

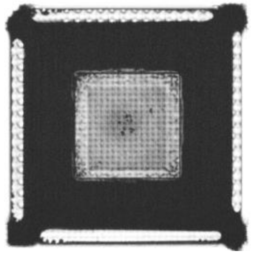


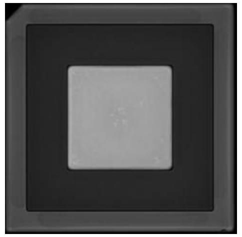












Design Of Experiment

Corner Lots

X-Ray Inspection

Parallel Polishing

Chemical Delid

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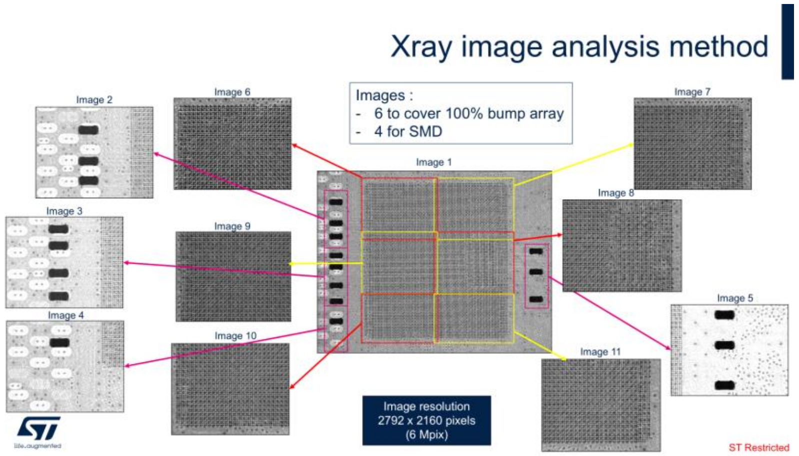
# ULTRA Product Qualification under ESCC9030

- **PID issued**
- **Evaluation and qualification plan agreed with CNES & ESA**
  - Chart F2
    - SAM 100% done on qualification lots instead of sampling
  - Chart F3
    - Reduced Burn-in as anticipated at wafer level
    - Radiography : deep analysis done. Inspection flow modified in agreement with CNES & ESA



Xray image analysis method

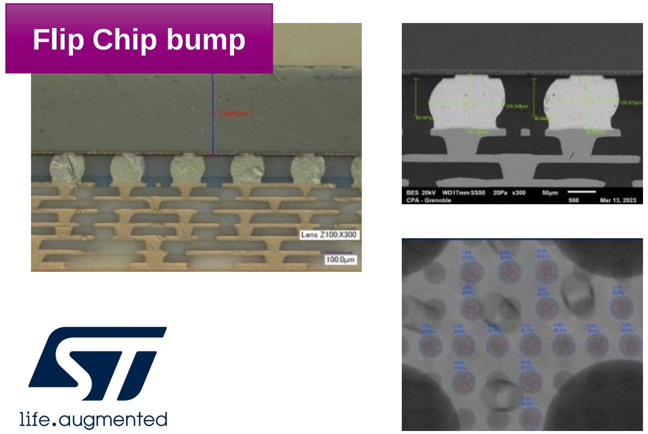
Images :
- 6 to cover 100% bump array
- 4 for SMD

Image resolution
2792 x 2160 pixels
(6 Mpix)

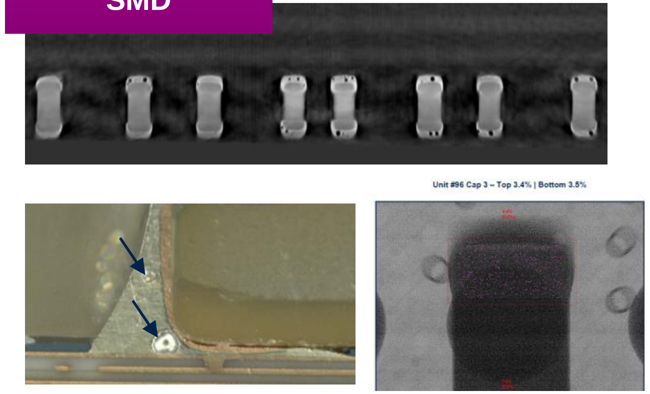
ST Restricted

- **Construction analysis**

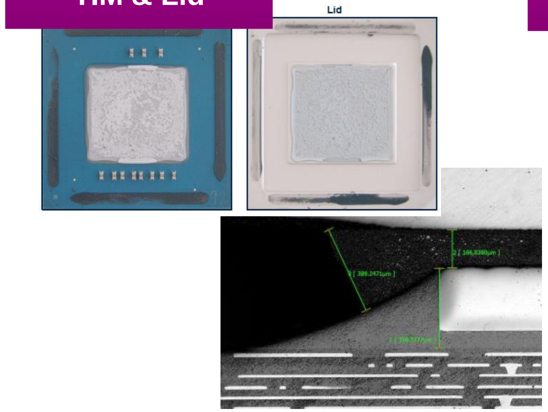
**Flip Chip bump**



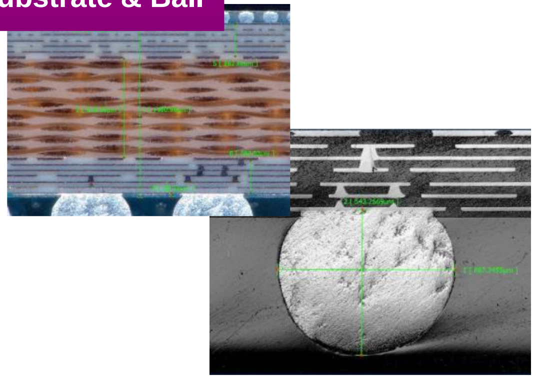
**SMD**



**TIM & Lid**



**Substrate & Ball**

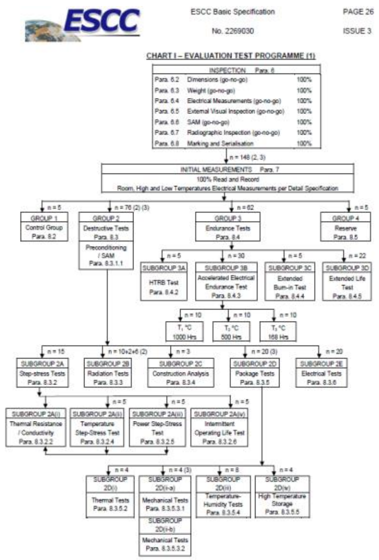


# ULTRA Product Qualification under ESCC9030

## ESCC 2269030 – Evaluation flow

**ESCC 2269030 – Chart I** ✓

- Subgroup 2B – Radiation Tests
- Subgroup 2C – Construction Analysis
- Subgroup 2D (ii)) - Mechanical Tests
- Subgroup 2D (iv) - High Temperature Storage
- Subgroup 2E – ESD



## ESCC 9030 – Qualification Flow

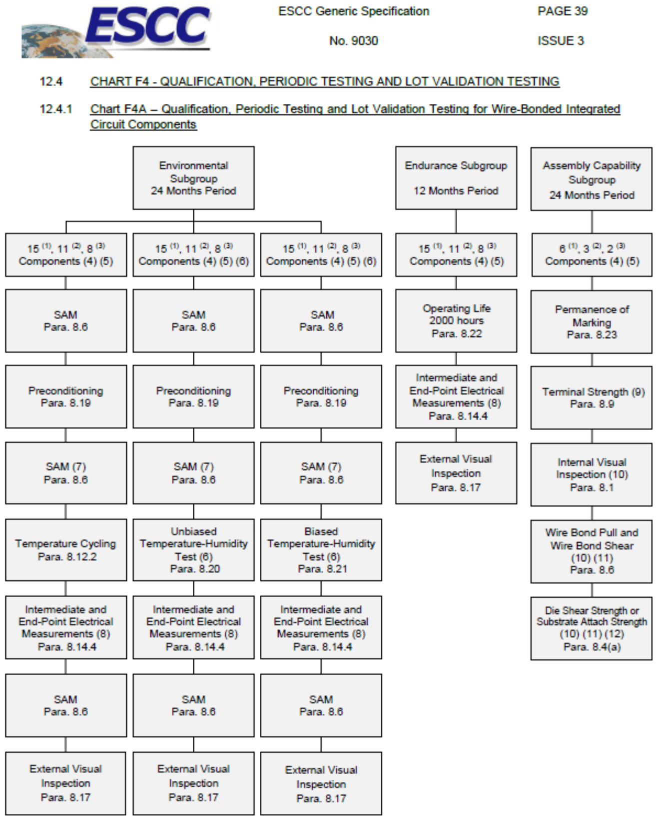
**ESCC 9030 - Chart F4B** ✓

- Temperature Cycling
- Unbiased Temperature-Humidity
- Mechanical Shocks
- Endurance (life test)
- Assembly Capability

## Extended qualification

**2 additional lots testing** ✓

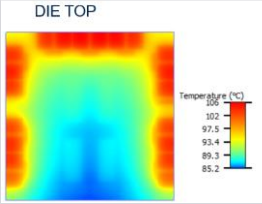
- Temperature Cycling
- UHAST
- Endurance (life test)
- High Temperature Storage

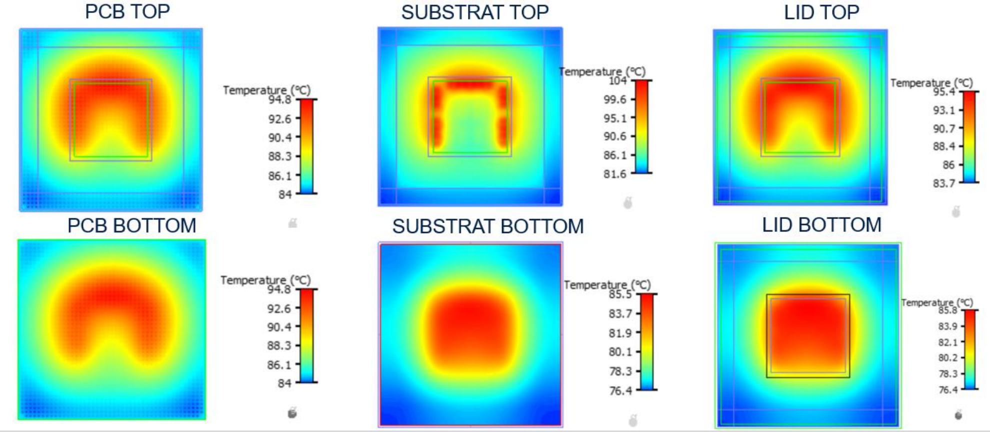


**All criteria fulfilled**

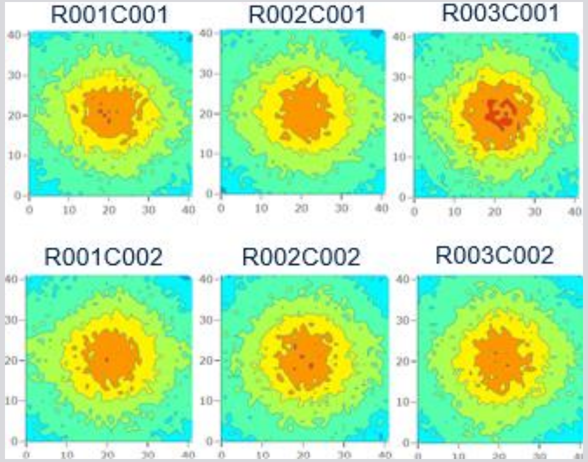
# Thermomechanical challenges

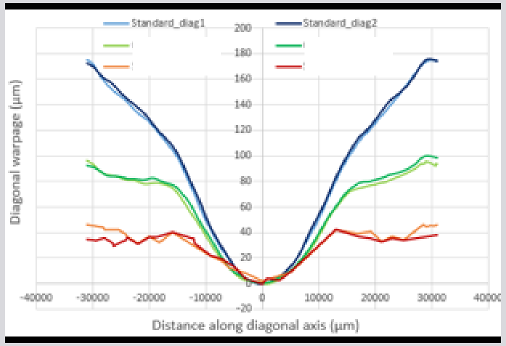
Thermal Management





Coplanarity

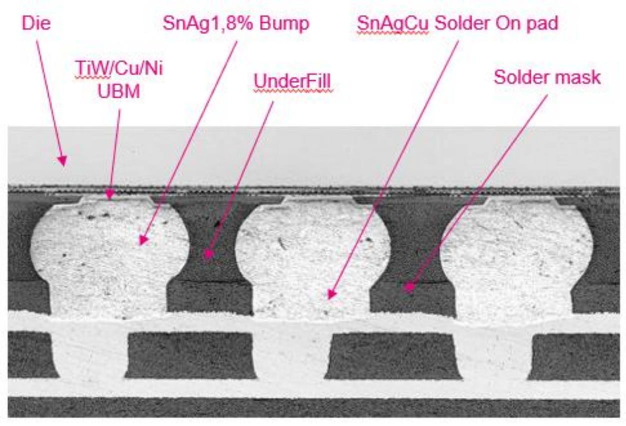




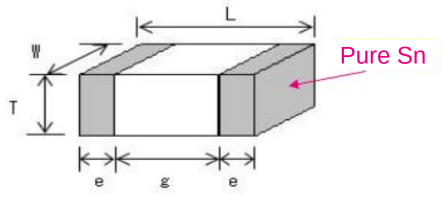
# Tin Whiskers Growth

## Tin usage in ULTRA product

- Solder bumps & Substrate finishing



- Space qualified surface mount capacitors



0603 Capacitors, Miniature, High-Capacity, Surface Mount, Fine Ceramic Dielectric(J2040/M105), High Reliability, Space Use

JAXA

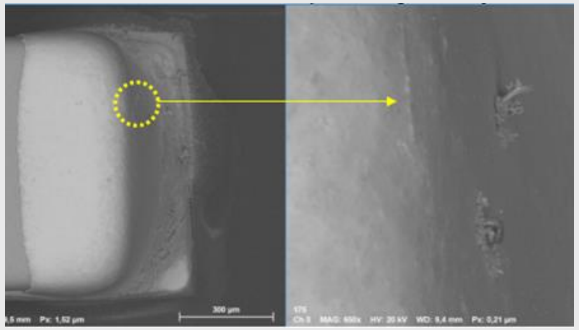
*(JAXA-QTS-2040/M105C)*

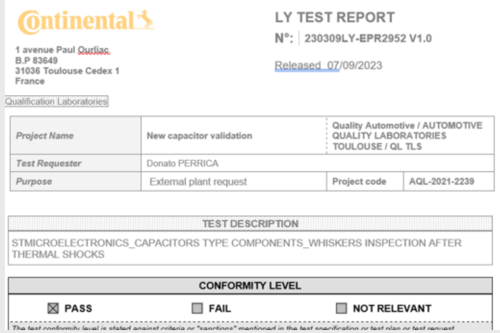
- Balls : Eutectic SnPb

## JESD201 Class2 criteria

| Test | Test duration | Max length (µm) | Result |
|---|---|---|---|
| **Initial state** | - | 26 | **Pass** |
| **Thermal cycling -40/+85°C** | 1000 cycles | 30 | **Pass** |
| | 1500 cycles | 30 | **Pass** |
| **Temperature / humidity storage 30°C / 60%RH** | 2000 hours | No whisker found | **Pass** |
| | 3000 hours | No whisker found | **Pass** |
| | 4000 hours | 10 | **Pass** |
| **High temperature / humidity storage 55°C / 60%RH** | 2000 hours | 26 | **Pass** |
| | 3000 hours | 10 | **Pass** |
| | 4000 hours | 20 | **Pass** |

✓





Continental

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31036 Toulouse Cedex 1
France

Qualification Laboratories

**LY TEST REPORT**
N°: 230309LY-EPR2952 V1.0

Released 07/09/2023

| | | | |
|---|---|---|---|
| *Project Name* | New capacitor validation | Quality Automotive / AUTOMOTIVE QUALITY LABORATORIES TOULOUSE / QL TLS | |
| *Test Requester* | Donato PERRICA | | |
| *Purpose* | External plant request | Project code | AQL-2021-2239 |

TEST DESCRIPTION

STMICROELECTRONICS_CAPACITORS TYPE COMPONENTS_WHISKERS INSPECTION AFTER THERMAL SHOCKS

CONFORMITY LEVEL

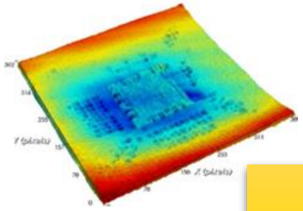
☒ PASS ☐ FAIL ☐ NOT RELEVANT

*The test conformity level is stated against criteria or "sanctions" mentioned in the test specification or test plan or test request*

# Conclusion & Perspectives

Qualified TEFCBGA line

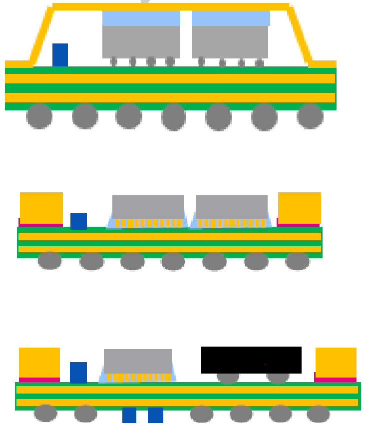
First ESCC9030 Qualified product



Higher Thermomechanical Performances

27x27 & 35x35 TEFCBGAs

SiP assembly capability



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