ACCEDE | ESCCON

2025 Seville - Spain 25 to 27th March

Teledyne e2v System-in-Package Technology for space products

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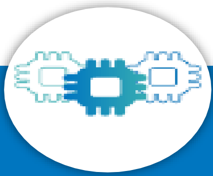
Teledyne e2V Grenoble presentation

A 100% Teledyne subsidiary since 2017

450 employees

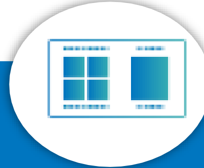
200 engineers



High performance Semiconductors

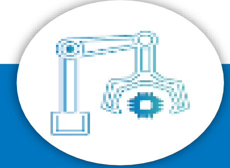
Data Converters

Microprocessors



System in Package

Mixed-Signal



Operation & Manufacturing Services

Assembly & Test

Fully Refurbished Clean Room – ISO7 to ISO4 – Governmental grants

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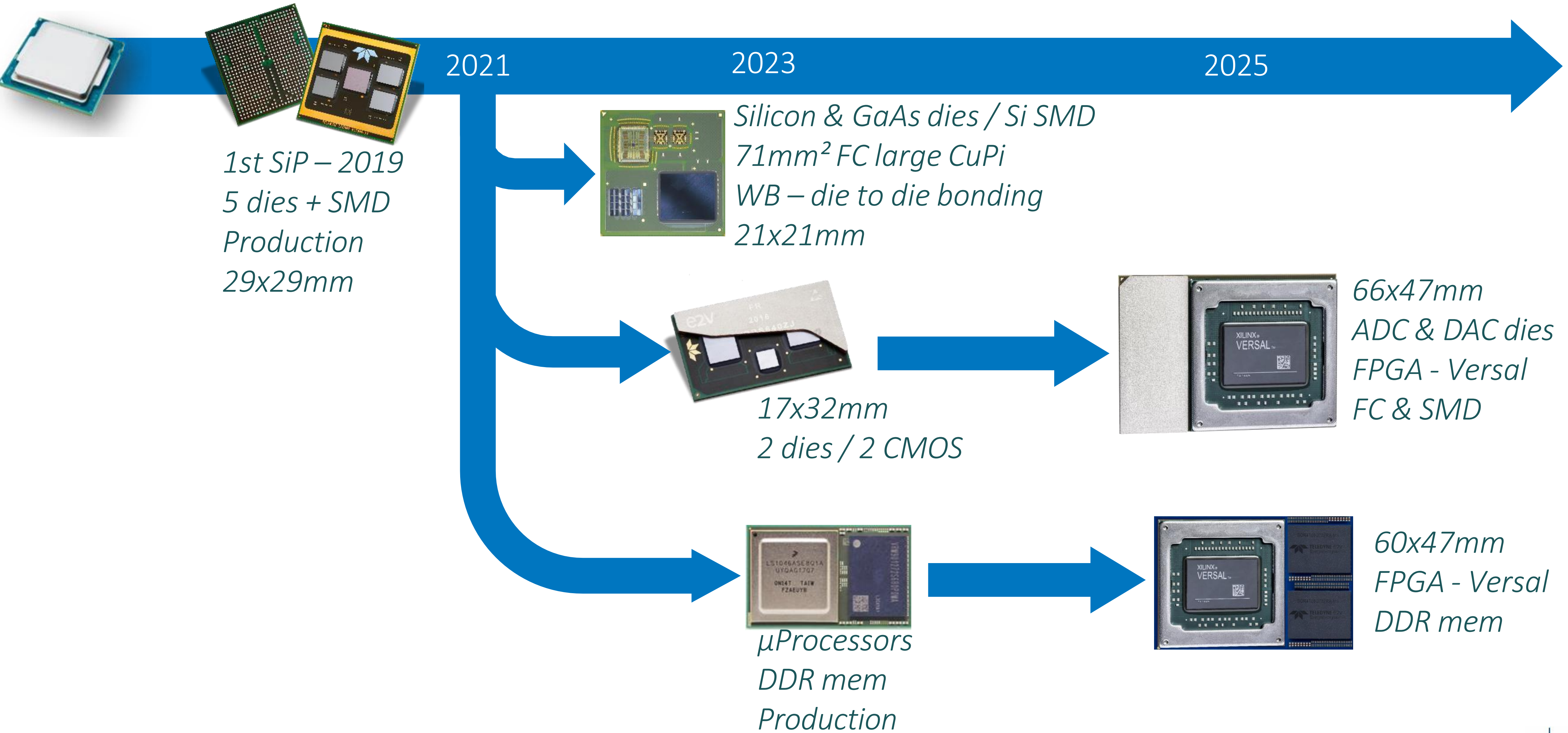
Te2v System-in-Package Trend



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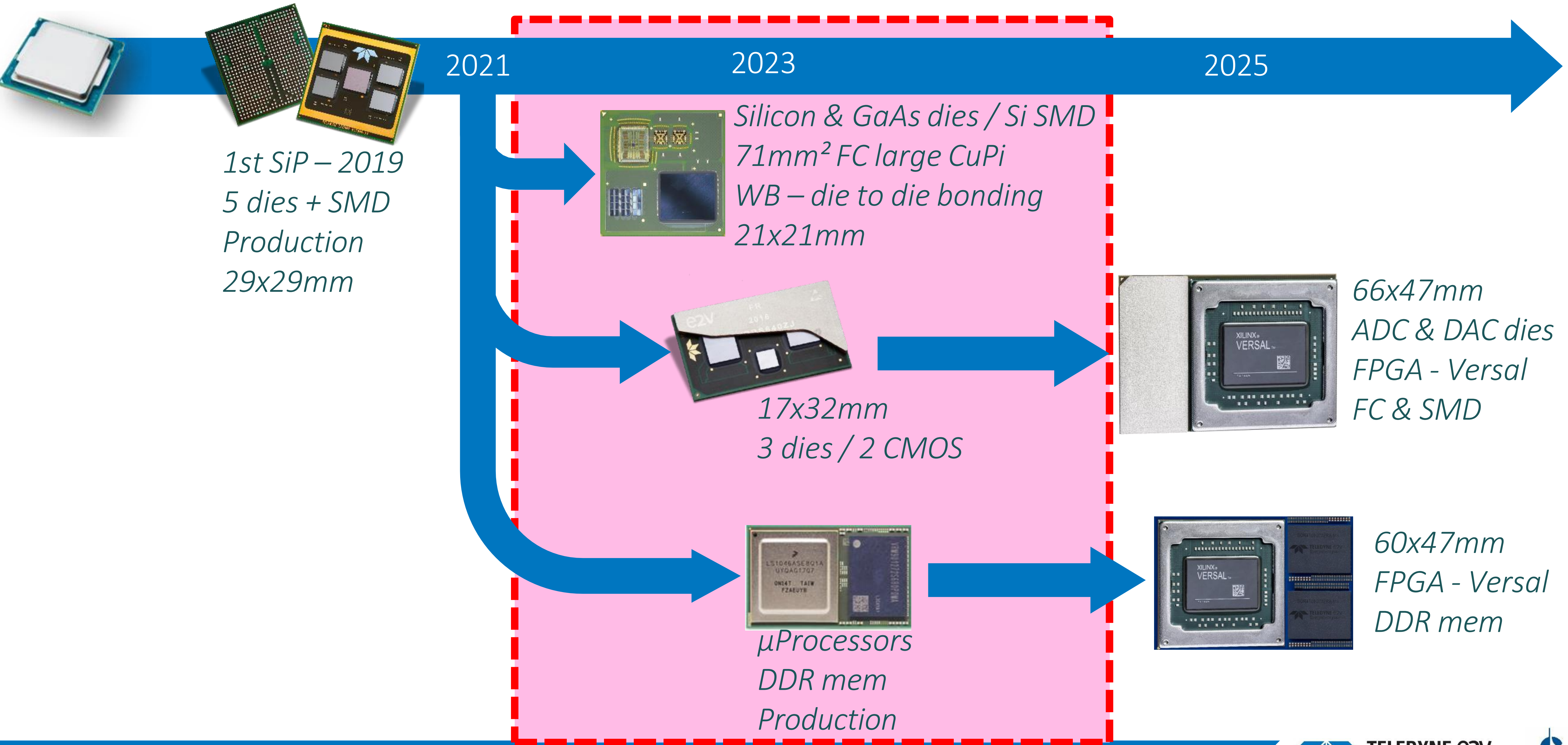
Te2v SiP 1st Challenge – Die to substrate



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SIP: Die to substrate Challenge

- Substrate supplier & Manufacturing
  - Bump & UBM dimension compatibility Vs Design rules manufacturing
- Mix of die technology node
  - Wafer foundries design rules manufacturing
    - Bump pitch
    - UBM size
    - Bump dimension
- Reliability
  - Crack on the interface between Die and bump (Ghost bump & White bump)
  - Crack on the interface between Bump and substrate

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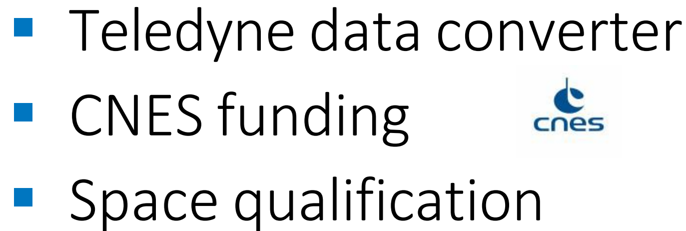
Die to substrate challenge : Teledyne case of study

Project information

- Teledyne data converter
- CNES funding



- Space qualification

Package information

- 17.6X16mm
- Die size:
  - 1st Die: 27mm^2
  - 2nd Die: 15mm^2
- 2 Dies technology nodes
- Bump Pitch (225µm)
- Bump Ø/ Height/UBM Ø
  - 1st Die :135/100/110µm
  - 2nd Die: 92/75/80µm
- SIP with 2 dies
- Bump Metallurgy SnAg1.8
- Substrate techno: SOP
- Substrate SRO Ø
  - 1st Die : 120µm
  - 2nd Die: 100µm

Package reliability mission profile

- HTS : 2000h@125°C
- TMC: 1500 Cycles (-55°C/125°C)
- THB:1000h (85°C/85% Rh)

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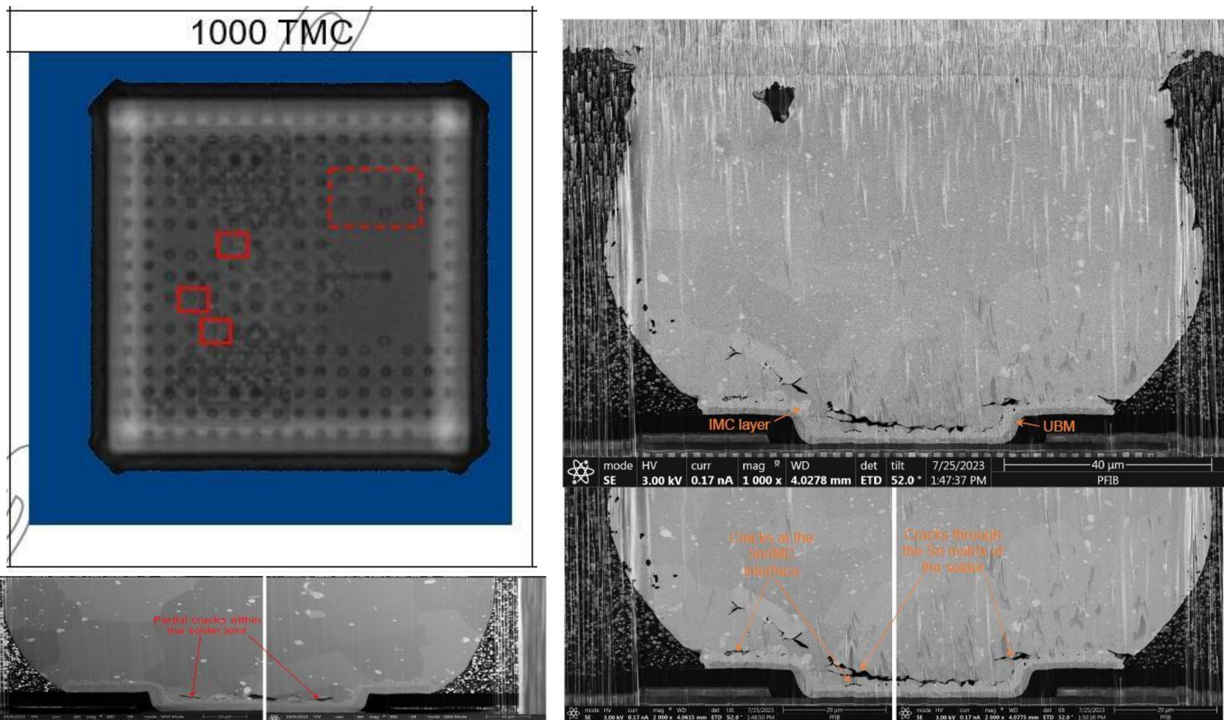
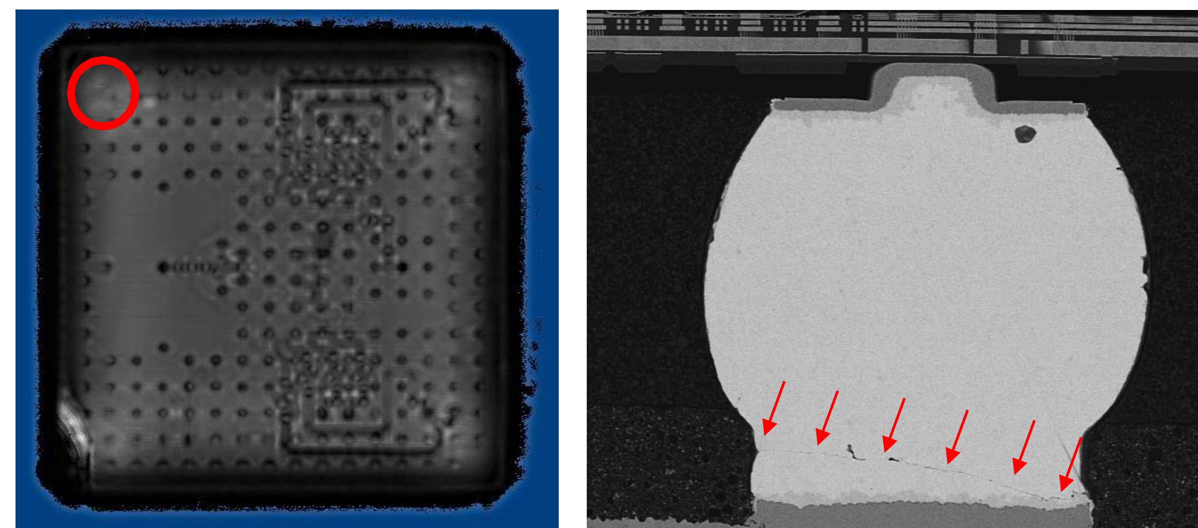
Die to substrate: Challenge faced in package reliability

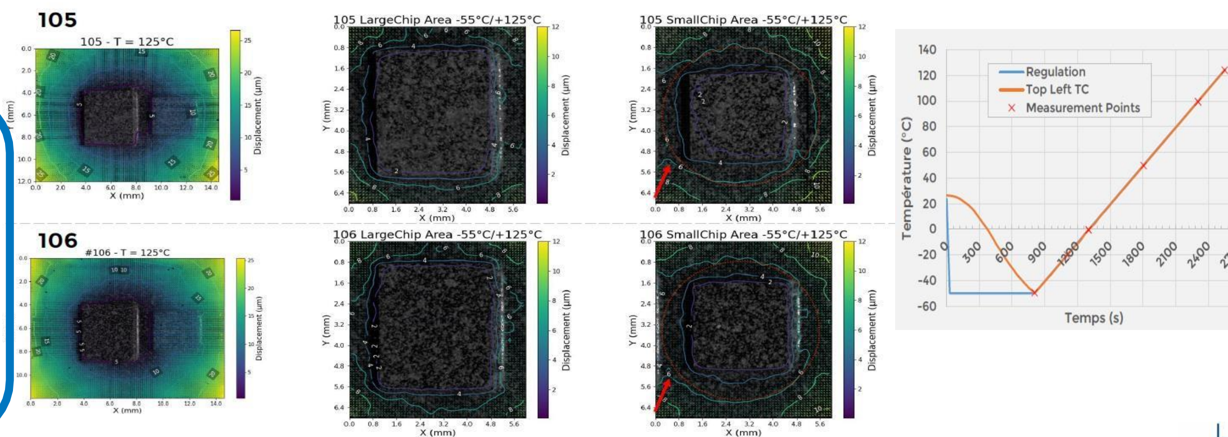
White/ Ghost bump @1000 TMC



Crack at substrate interface@1000 TMC



Thermoire characterization



- No root cause identification by Thermoire characterization
- No improvement with different underfill type
- No correlation with simulation and litterature

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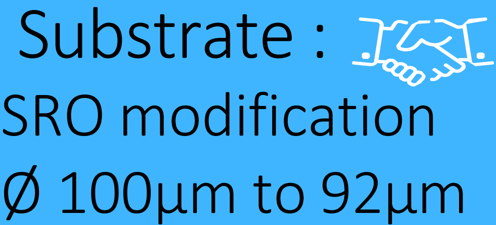
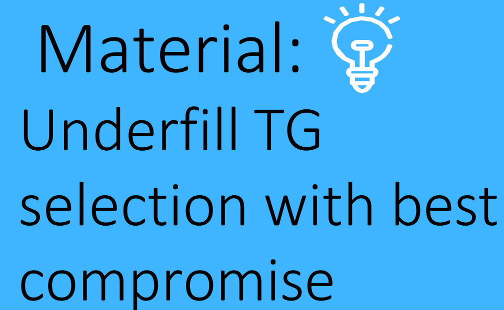
Die to substrate challenge : Teledyne Improvement

Key changes

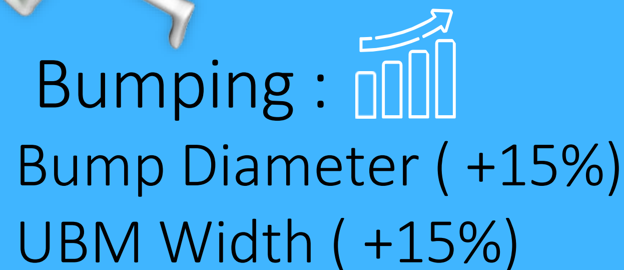


Substrate :
SRO modification
Ø 100µm to 92µm



Material:
Underfill TG selection with best compromise

Die Design :
Bump densification (+63%)
Bump pitch reduction
225µm to 162µm Staggered



Bumping :
Bump Diameter (+15%)
UBM Width (+15%)

Reliability Result

Lot Ref	MSL3+1500 TMC
Target Process Lot	0/30 ✓
Process Corner Lot	0/60 ✓

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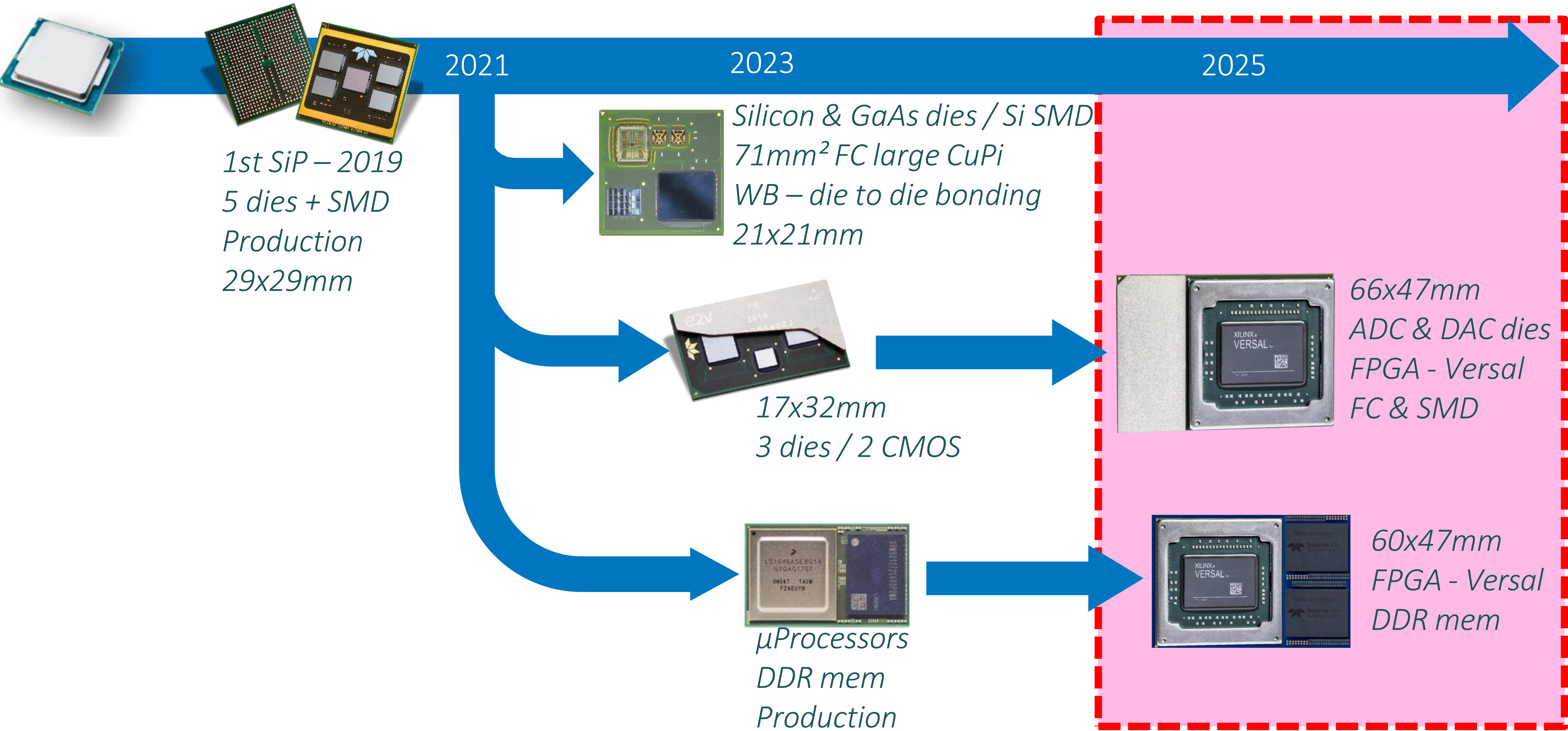
Te2v SiP 2nd Challenge – Substrate to board



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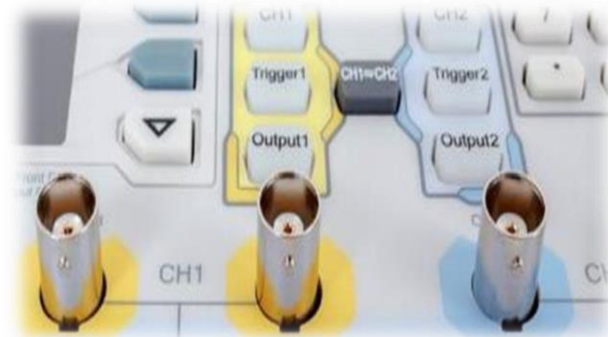
SIP: Substrate to board Challenge



- Large SIP Vs current max size in the space application
  - Current Max size <50x50mm
    ➔ SIP with FPGA targeted > 60X50mm

- Board Level Reliability
  - Crack on the interface Ball to component
  - Shocks & Vibrations high mechanical stress due to weight of large product size

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Substrate to Board challenge : Teledyne case of study

Project information

- Teledyne data converter
- MCM or Mix of Flip chip and FPGA packaged
- Space qualification
  - ECSS-Q-ST-70-61

Package information

- Large SIP up to 66x47mm
  - 50X50mm surface mounting on PCB
- 2 Assembly Technologies
  - FC for data converter and SMD and FPGA packaged
  - Full SIP with packaged component

Board level reliability

- Shocks and vibrations + TMC (-55/ +100°C) to cover a maximum of Customer mission Profile

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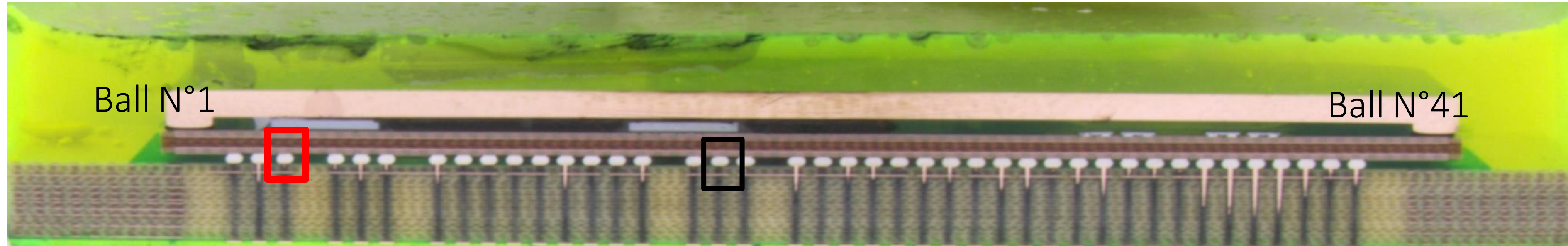
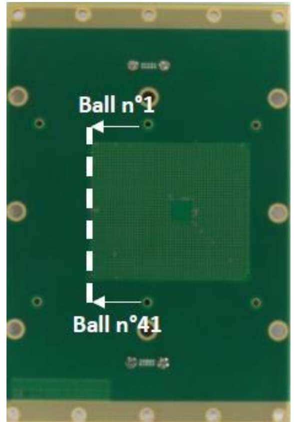
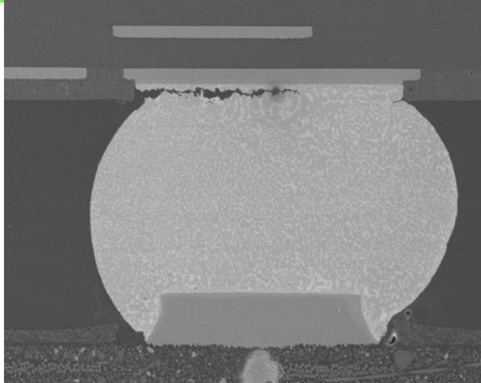
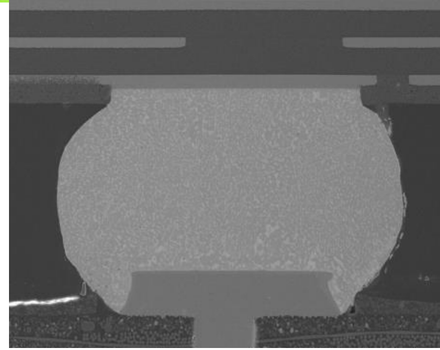
Substrate to board: Challenge faced in package reliability

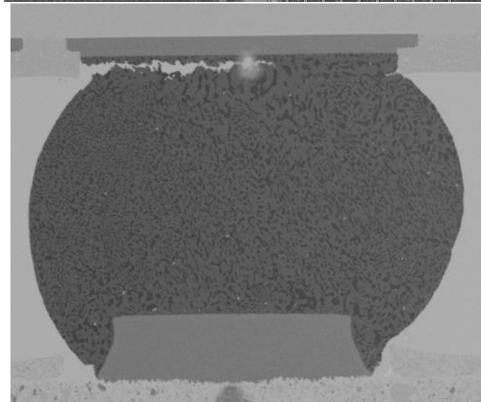
Crack at substrate interface@ Shocks+ Vibrations + TMC

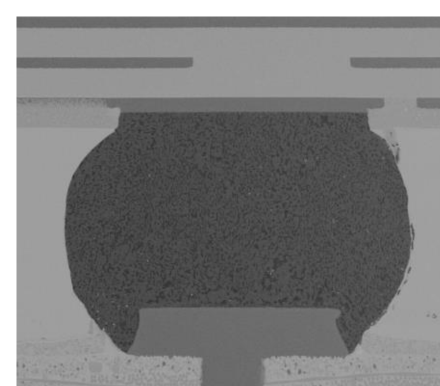












- Crack observed in the corner
- No crack detected in the center
- Early failure after shocks + vibrations
- No crack until 500 cycles (W/o shocks and vibrations)
- Simulation Fit with the result of experiment But without shocks and vibrations

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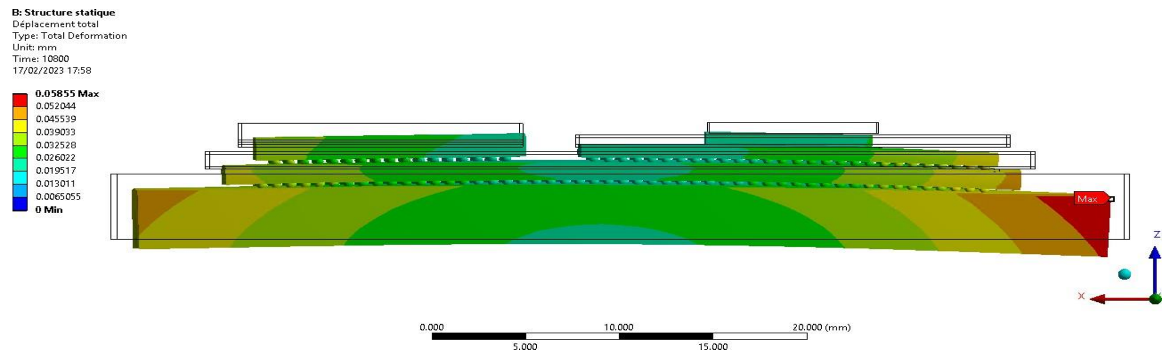
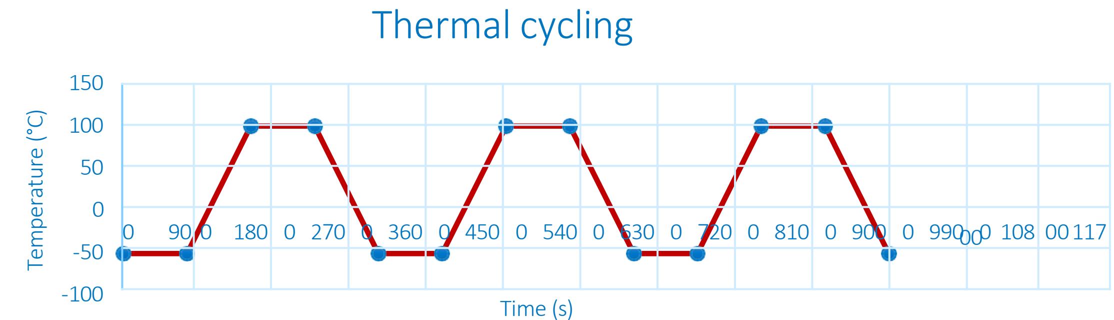
Substrate to board challenge : Teledyne Improvement

- 1st improvement : Simulation on going
  - Development of a simulation model considering shocks and vibrations phases





  - Solder joint weakness identification
  - Define lifetime model
- Verification of the result by experimentation plan
  - Adjust simulation model
  - Adjust lifetime model
- Re-use model of simulation for same SIP family

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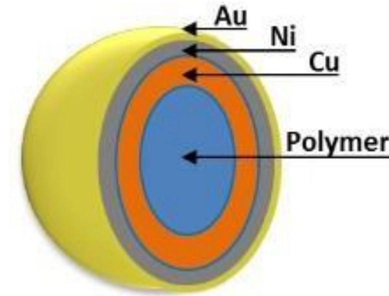
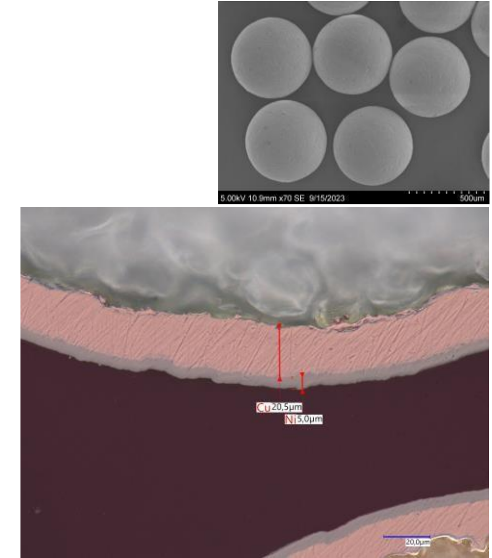
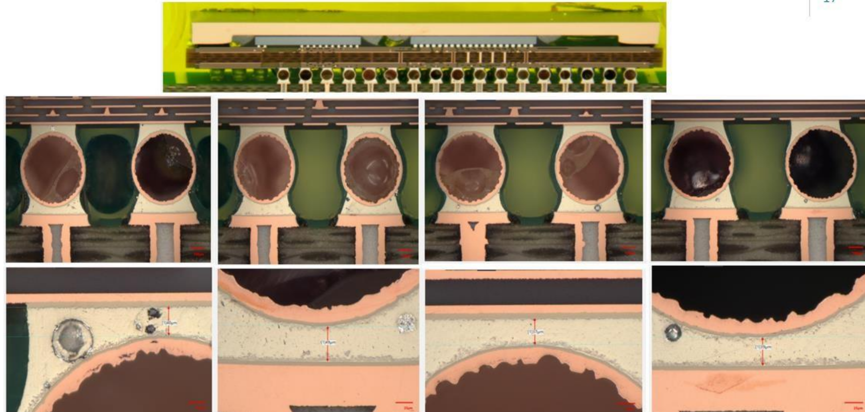
Substrate to board challenge : Teledyne Improvement

- 2nd improvement Exploration : Ball metallurgy
  - Evaluation of new ball materials : Polymer Core solder Ball (PCSB)
  - ➢ Advantage from supplier
    - Lead free material
    - Compatible with solder reflow
    - Improve reliability
    - Controlled stand-off height
  - ➢ Process development and board reliability comparison on SIP (17.6x16mm)





Cross section



1st preliminary Result

	BLR Reliability Test Result (-55/+100°C)			
Ball alloy	Shock & Vibration	Shock & Vibration+1000 TMC	Shock & Vibration+1500 TMC	Shock & Vibration +2500 TMC
SAC305	0/12	0/12	0/12	WK14
Ref A	0/12	0/12	0/12	WK14
PCSB	0/11	0/11	0/11	WK14

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SIP: Summary

- Die to substrate challenge
  - Bump densification ✓
  - UBM optimization ✓
  - Substrate DRM compromise ✓
- Substrate to board challenge
  - Simulation model fit improvement (Target 2026)
  - New ball alloy qualification based on ECSS-Q-ST-70-61 (Target June 2026)

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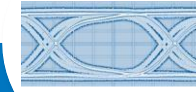
Teledyne e2v Assembly & Test Services Offer

Package Design

- PI/SI Simulations
- EM Simulations
- Thermal Simulations
- Substrate supplier management

Packaging

- Flip Chip & Wire bond
- Organic/ Ceramic
- Transfer Molding
- System-in-Package



Test & Qualification

- Burn-in & Screening
- Reliability Qualification
- Final Test
- Radiations

Supply Chain Management

ISO 9100

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