ACCEDE | ESCCON

2025 Seville - Spain 25 to 27th March

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An exercise of COTS evaluation: Application of Q-60-13 to a complex ADC for class 1 science mission

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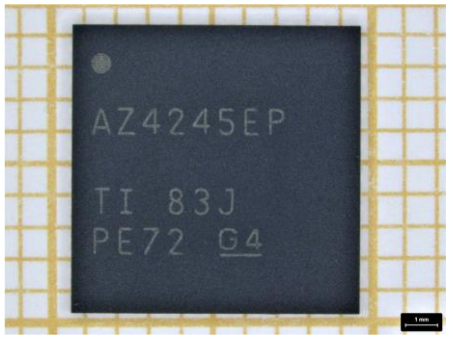
esa beyond gravity

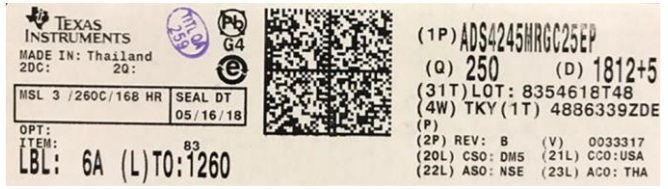
BACKGROUND

In the payload consortia of the “old” Athena in phase B1 before adoption, two COTS components were pre-selected due specific performance :

ADS4245-EP Dual-Channel, 14-Bit, 125MSPS Ultralow-Power ADC:

- achieve high dynamic performance, while consuming extremely low power with 1.8V supply

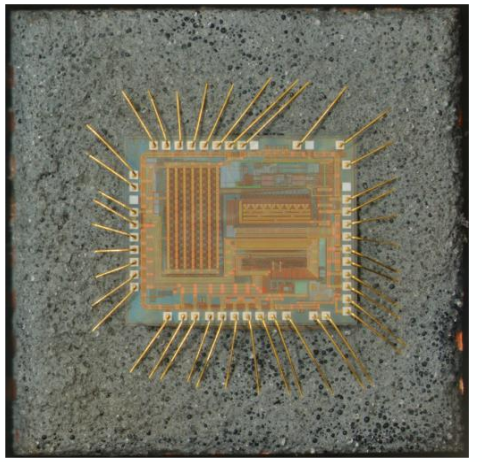




AD9744 14-Bit, 210 MSPS TxDAC®

D/A Converter

- low power CMOS offers exceptional ac and dc performance while supporting rates up to 210 MSPS, is specifically optimized for the transmit signal path of communication systems



BACKGROUND

This evaluation study was part of The Core Technology Programme (CTP) : an integral part of the Science Programme with the prime objective to ensure the development and readiness of critical technologies required for future missions.

This activity was part of a Structuring Measure for Finland with Direct Negotiations with Beyond Gravity (FI).

It had also a more general goal to improve the knowledge of the contractor in evaluating complex COTS components and to build up experience in designing test set-up for SEE test and electrical characterization of commercial microcircuits

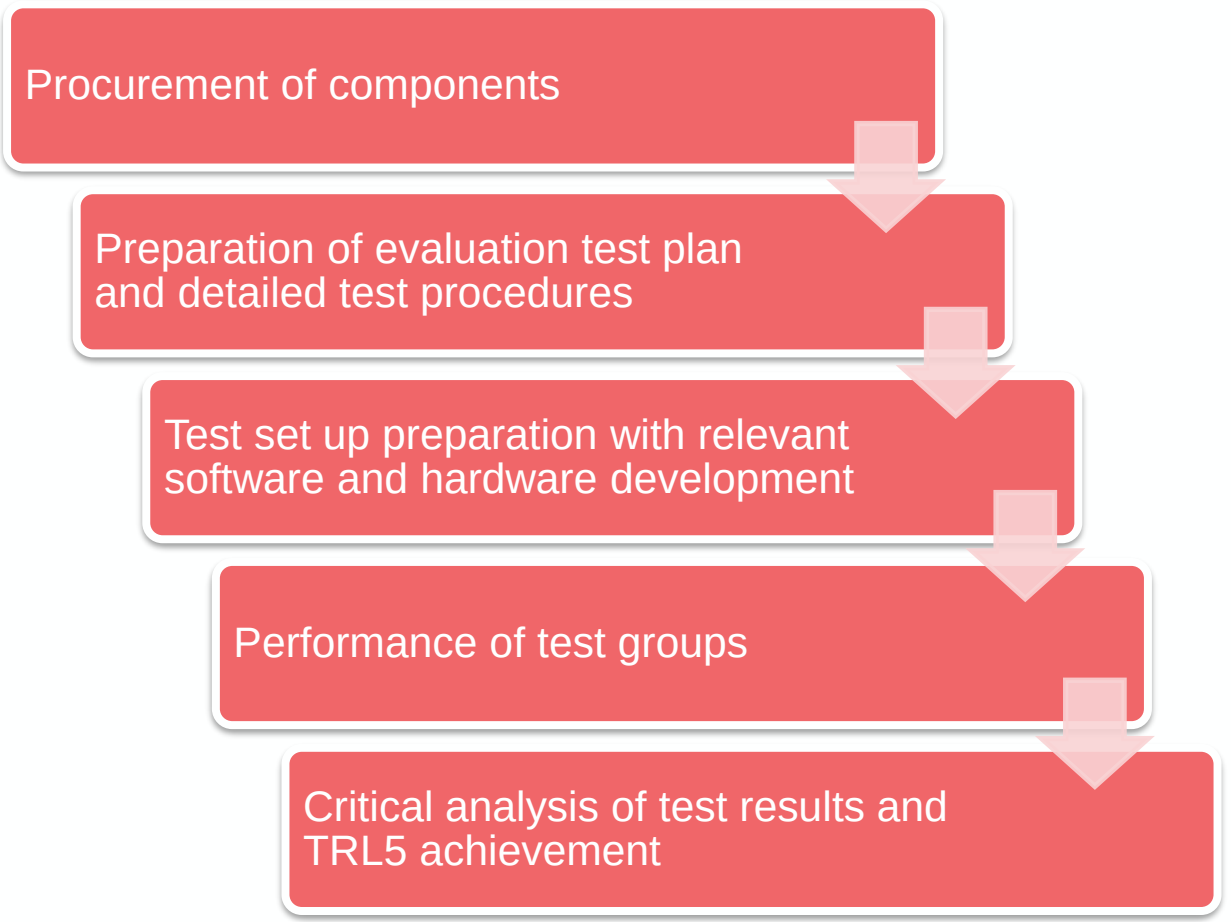
Therefore, the maximum number of testing activities were required to be performed in house

GOALS OF THE ACTIVITY

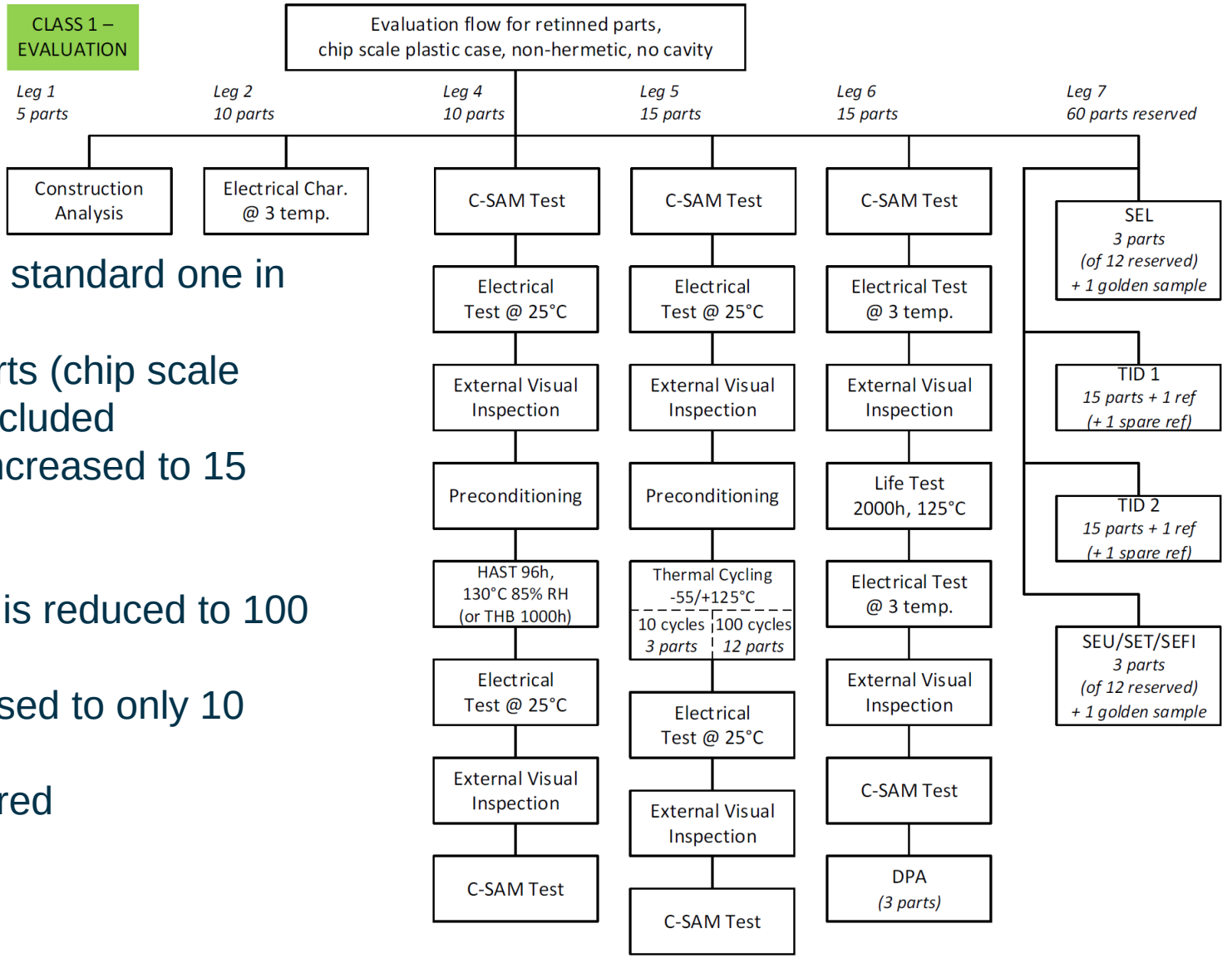
The main objective of this activity was to procure and evaluate a batch of ADC ADS4245-EP and a batch of DAC AD9744 in order to achieve TRL5 before the adoption of the mission and to confirm therefore ADC/DAC baseline of the instrument.

The Workplan reflects the typical evaluation flow.

From schedule perspective the time/effort/man power needed to realise the test set up and to perform the relevant dry run to debug the system was severely underestimated



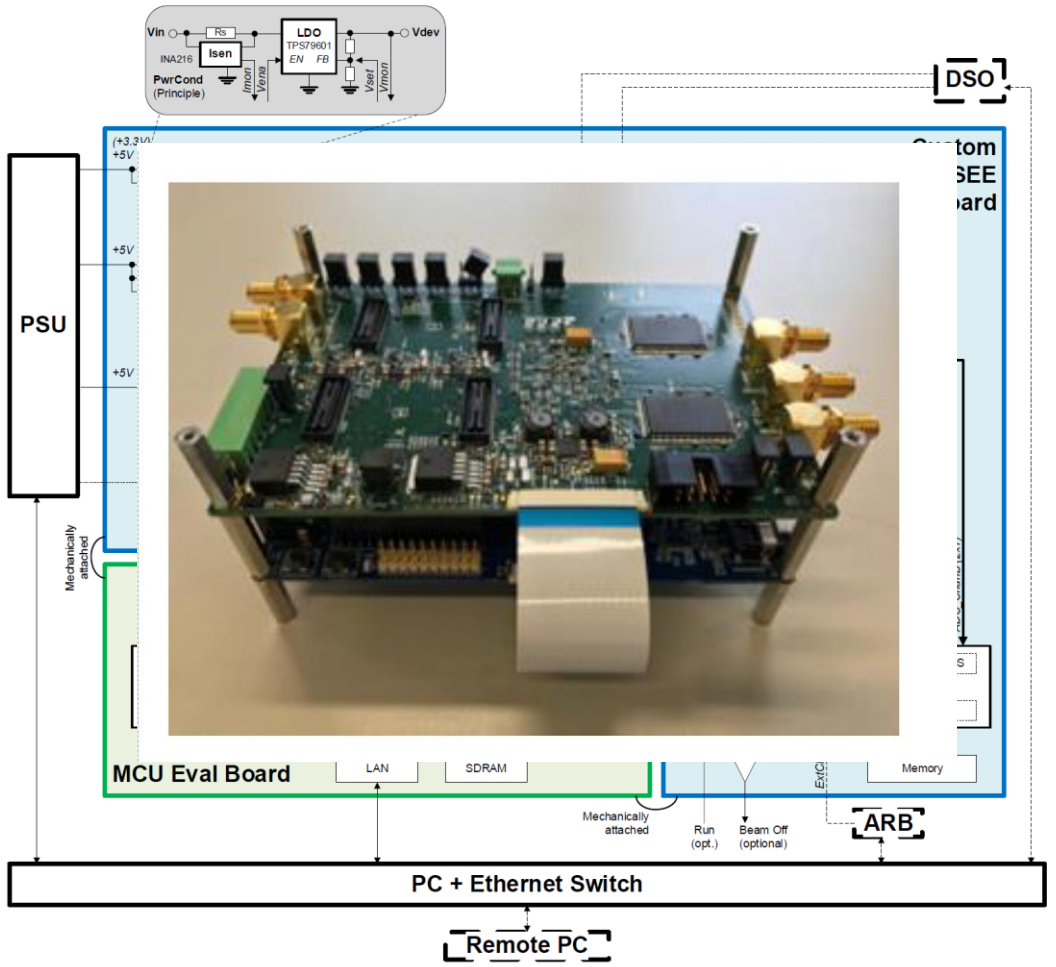
TEST FLOW



The agreed flow deviates from the ECSS standard one in the following details:

- only activities relevant for moulded parts (chip scale plastic, non-hermetic, no cavity) are included
- the number of parts in leg 5 and 6 is increased to 15 (ECSS says minimum 10)
- C-SAM added also to leg 4 and leg 6
- The number of thermal cycles in leg 5 is reduced to 100 (LAT approach was followed)
- A subset of the parts in leg 5 are exposed to only 10 thermal cycles
- The mechanical test were not considered

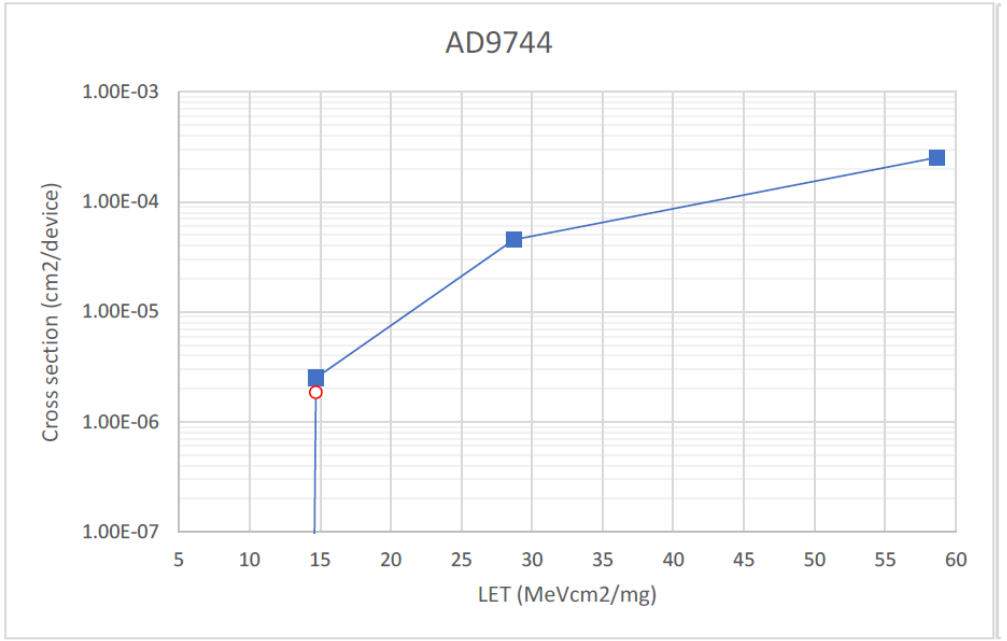
SEL/SEE TEST SET-UP



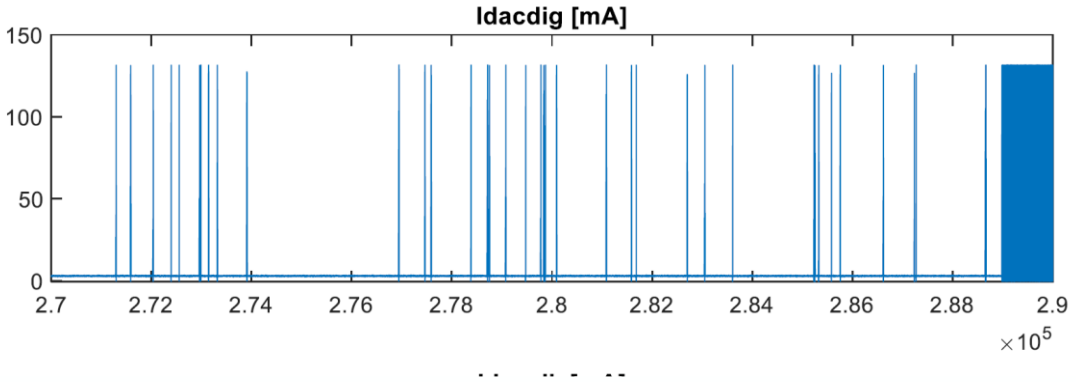
The fundamental design targets of the Custom SEE Board were:

- testing of ADC and DAC using the other as a testing counterpart:
- on-line detection of faults in the signal controlling storage of data
- monitoring of ADC and DAC currents, temperatures and voltages
- on-line detection of overcurrent
- automated sequence of (selectable) recovery actions with adjustable thresholds and delays
- on-line visualization of signals, telemetry and events

SEL RESULTS: AD9744



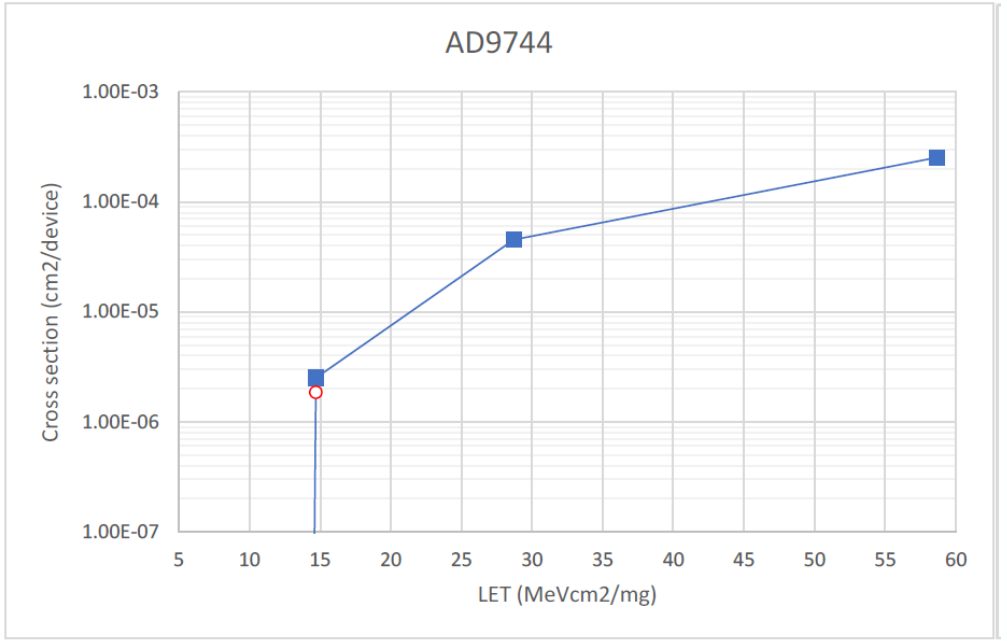
Temperature: +75°C (+10°C / -5°C), reduced per [RD07] from value in [RD05]
Pressure: Ambient (air mode)
Supply Voltage: +3.6 V (applicable for the three DUT supplies)
Reference: Internal reference used
Data mode: Straight binary (MODE pin => DCOM)
Clock mode: Differential clock (CMODE => CLKVDD)
Sleep mode: Not operatively used (used as recovery method)
Fclock: 100 MHz, LVDS based clock driver
Stimuli: Differing from [RD05]: Triangular full-scale waveform pattern with 32 repeats of each code (64 at code extremes), f ~ 97 Hz



Run	DUT	Ion	E MeV	LET_{eff} MeV•cm²/mg	Flux $cm^{-2}\,s^{-1}$	Dur. s	Fluence cm^{-2}	SELs	σ (SEL) cm^2	Cum. TID krad
10	# 6	Xe	2059	58.7	1.46E4	0.8	1.18E4	3	2.55E-4	0.74
11	# 7	Kr	1358	28.7	4.7E4	17.7	8.4E5	38	4.55E-5	1.5
12	# 23	Fe	941	14.7	5.1E4	56.6	2.9E6	3	1.04E-6	0.85
13	# 23	Fe	941	14.7	5.0E4	60	3.0E6	N/A (*)	N/A (*)	1.5
14	# 24	Ar	657	8	6.1E4	100	1.0E7	0	0	1.2
15	# 25	Fe	941	14.7	5.3E3	675	3.6E6	9	2.51E-6	0.86

SELs observed with Kr and Xe ions led to permanently high consumption of the digital section supply voltage by a factor of 10 or more

SEL RESULTS: AD[illegible]4 not suitable for space



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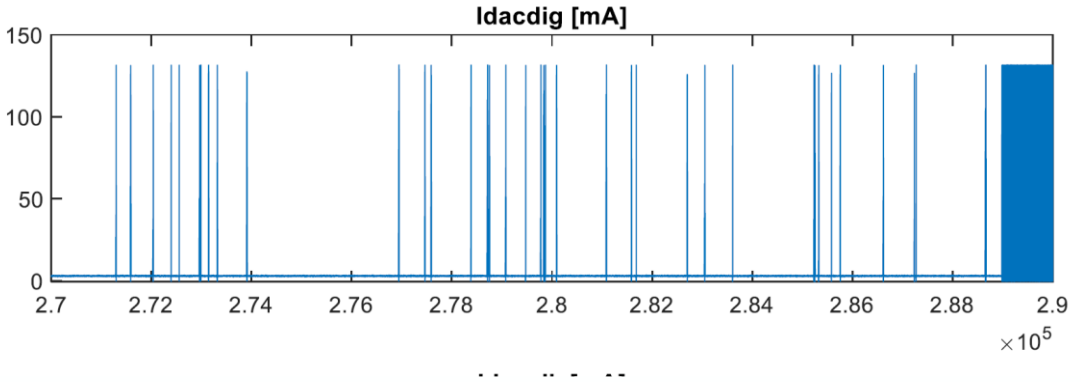

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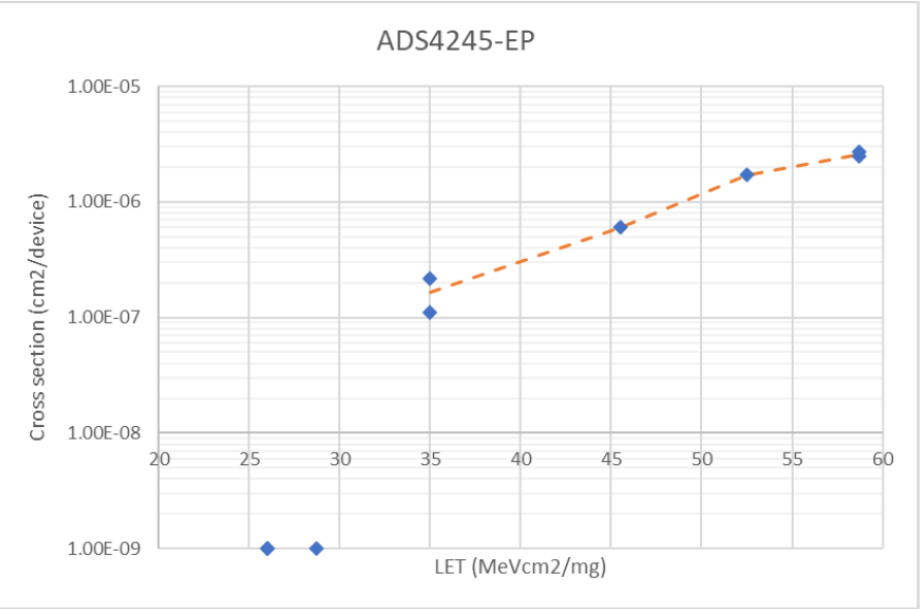
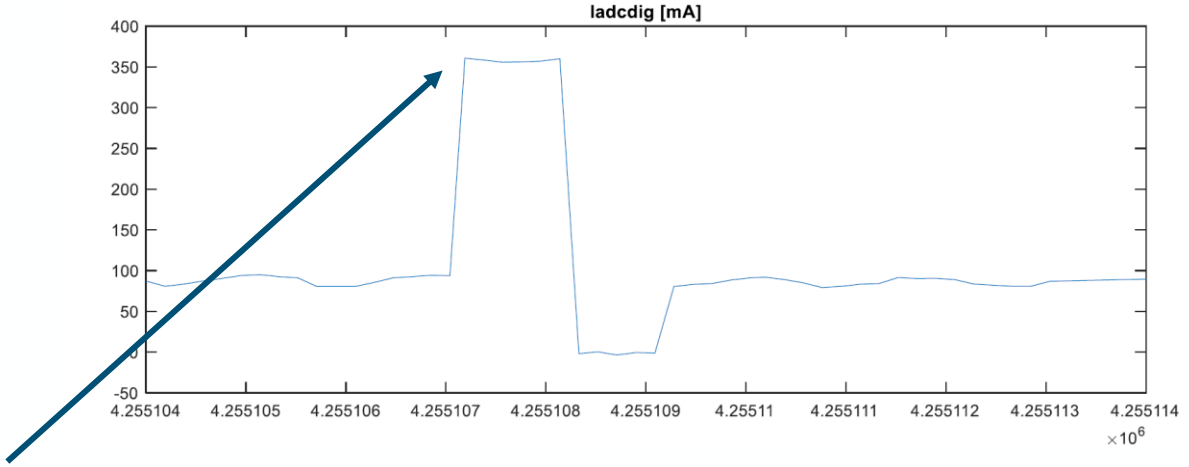
SEL RESULTS : ADS4245-EP



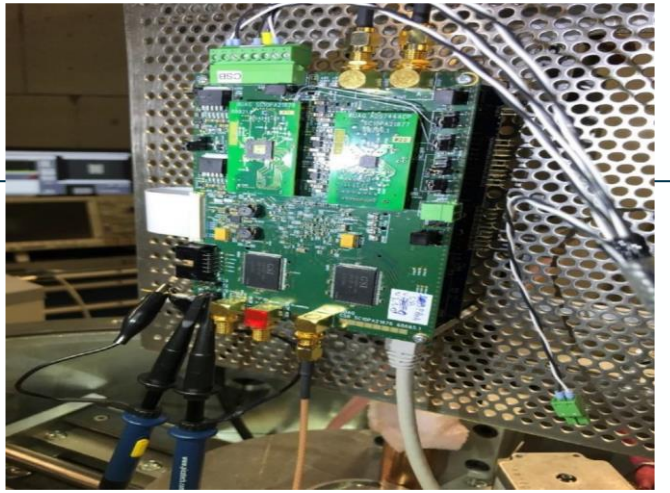


Typical example of recovery from a SEL (amplitude self –limited)

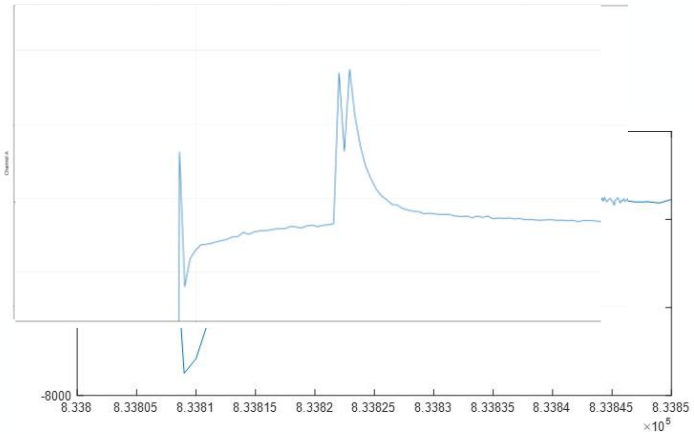
Run	DUT	Ion	E MeV	LET_{eff} MeV•cm²/mg	Flux $cm^{-2}\ s^{-1}$	Dur. s	Fluence cm^{-2}	SELs	σ (SEL) cm^2	Cum. TID krad
2	# 34	Fe	941	14.7	1.0^E3	100	1^E5	0	0	<< 1
3	# 34	Xe	2059	58.7	1.0^E3	100	1^E5	0	0	<< 1
4	# 34	Xe	2059	58.7	1.6^E4	625	1^E7	27	2.7^E-6	8
5	# 35	Ag	1777	45.5	1.0^E4	1000	1^E7	7	7.0^E-7	6
6	# 35	Kr	1358	28.7	1.0^E5	100	1^E7	1	1.0^E-7	10
7	# 33	Kr	1358	28.7	7.8^E4	130	1^E7	0	0	4
8	# 15	Kr	1358	28.7	7.1^E4	140	1^E7	0	0	4
9	# 15	Xe	2059	58.7	2.0^E4	510	1^E7	25	2.5^E-6	12

Xe and Ag beam resulted in events causing current consumption to increase to about 3x of the nominal value. All observations were on the digital supply line. The hard-limit always activate a power cycling, which returned operation to nominal. No permanent damage was observed. Some current events below the hard limit resolved autonomously.

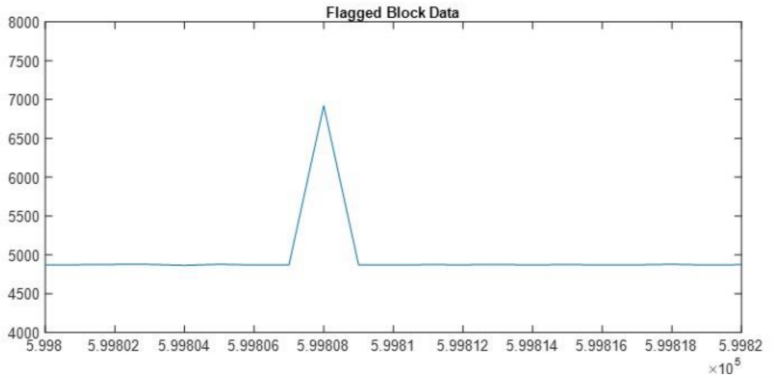
SOFT SEE RESULTS : ADS4245-EP



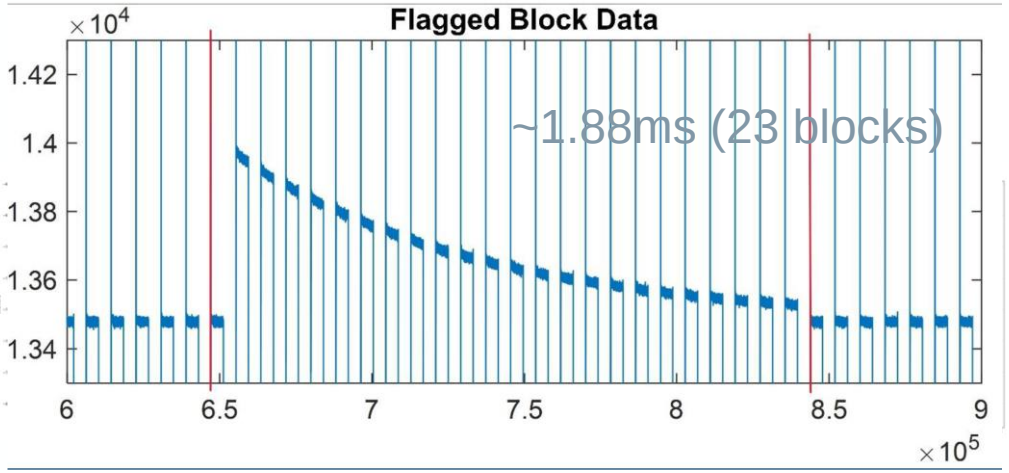
Several different SET were observed.
SEU (register errors), SEFI (several different types), clock errors, small supply current level changes, shifts in Vcm were also observed, but having low cross-sections.



ASET (short analog SET)
LETth = 2.1 MeV•cm2/mg
s = 3.5E-4 cm2
W = 17.8
S = 0.97

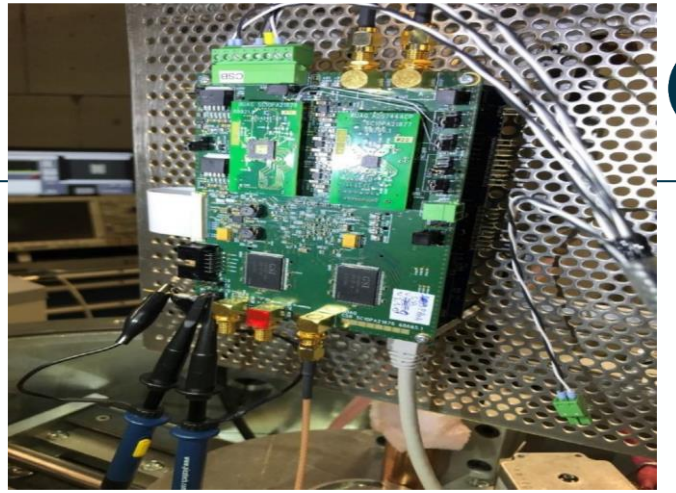


DSET (short digital SET)
LETth = 7.6 MeV•cm2/mg
σ = 1.0E-4 cm2
W = 9.07
S = 1.38

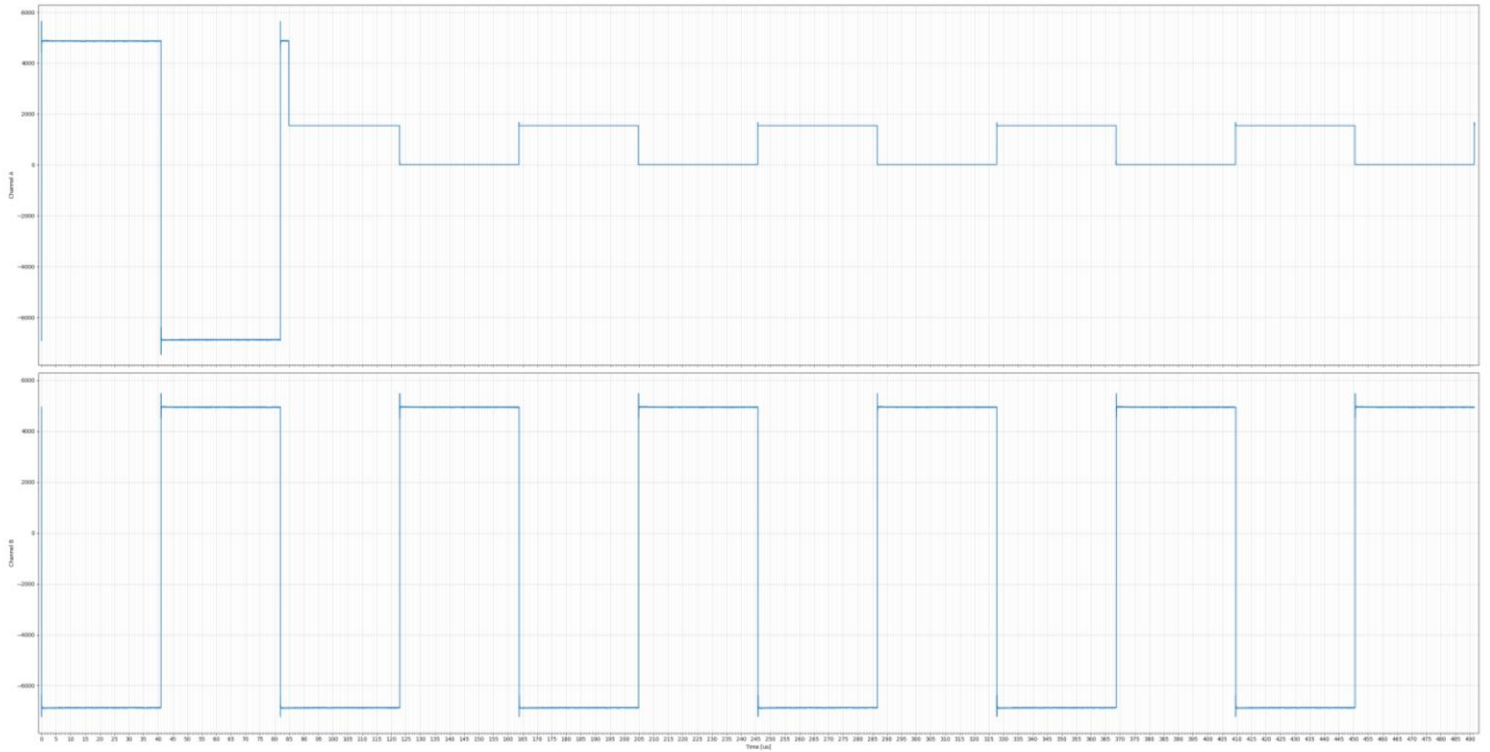


WSET (wide analog SET)
LETth = 7.4 MeV•cm2/mg
σ = 4.2E-5 cm2
W = 9.81
S = 1.77

SOFT SEE RESULTS : ADS4245-EP



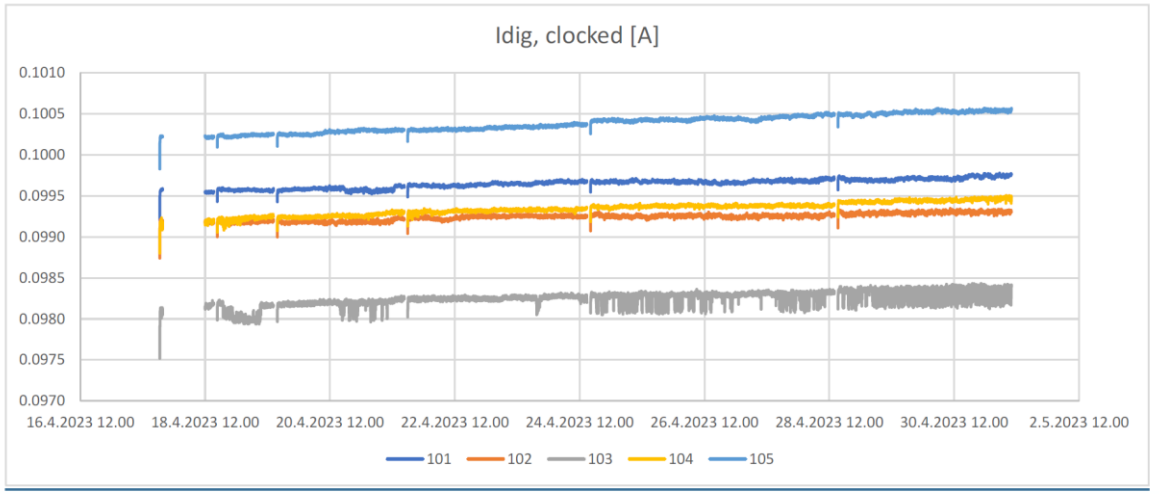
Example of a SEFI affecting only channel A while channel B was nominal.
It was resolved with an hard reset



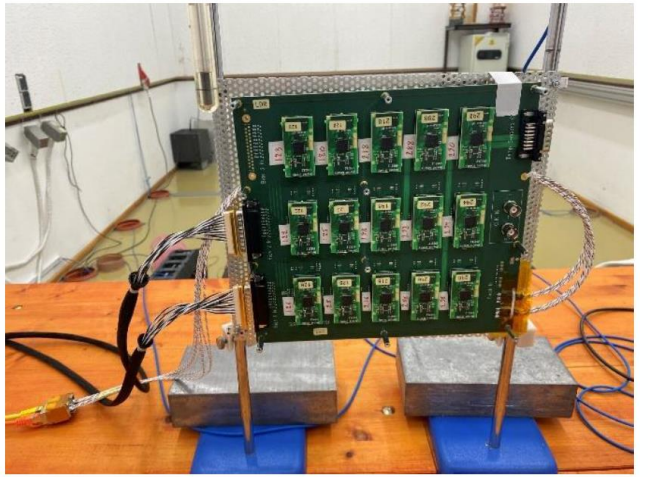
TID RESULTS

TID testing was carried out at the Co60 facility at Estec including annealing at room temperature and accelerated ageing in hot.

- dose rate of about 224.4 rad(Si).
- The intermediate measurement were a reduced set of the electrical characterization list allowing the measurement in less than 2hrs
- Biased and unbiased condition



The characteristics remain stable during the intermediate and final measurements for a TID up 71 krad(Si).



- Dedicated ETB (Environmental Test Board), with mounting provisions for DUT mezzanines and Pt1000 sensor(s)
- Dedicated IFEB (InterFace board for Environmental test Board) providing to each DUT:
  - 100MHz oscillator and dedicated LVDS output stages
  - regulators for analog and digital supplies per DUT
  - current sensors and amplifiers for each supply line
- Data Logger
- Power Supply (for IFEB):

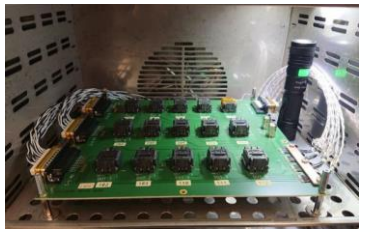
EVALUATION RESULTS

All the test performed in the different test legs were not showing significant drift

Therefore, the evaluation can be declared successful and ADS4245-EP has achieved the TRL5.

Life Test Results

- There is no drift from BOL to EOL over the life test. One part (#308) shows some increase in noise, but contamination was found on the contacts, and after cleaning, recovered

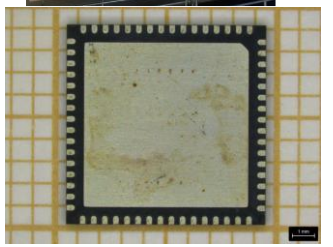


Thermal Cycling Results

- no drift was observed over the thermal cycling.

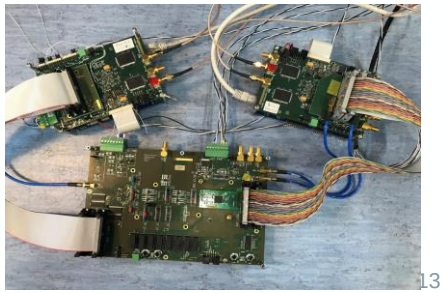
HAST Results

- Very small drifts over HAST, the small changes may be due to residual humidity.
- For one device (#114) some test issues were observed, including an apparent open circuit in SDOUT making readout impossible. This has been explained by contamination.



Electrical Characterisation @3T

- Problems were encountered with the test set-up in performance tests, particularly with the long test cables using a clock frequency of 50MHz. While noise, gain and offset measurements gave credible repeatable results, the linearity test did not reach the high accuracy expectations, particularly regarding INL

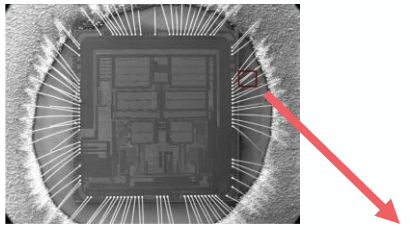


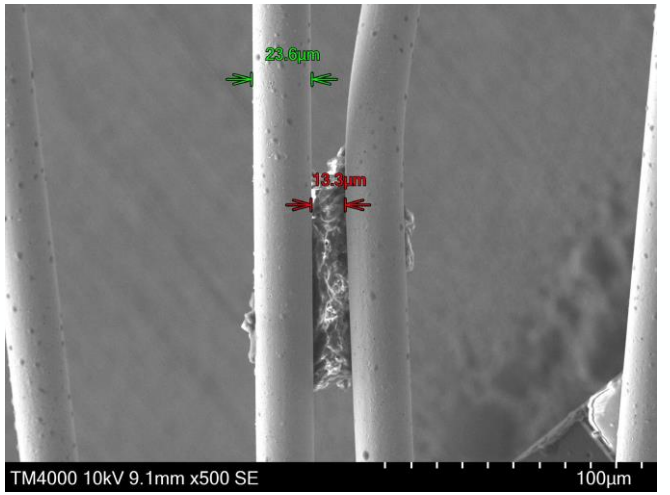
ALL's WELL THAT ENDS WELL?

SOME ANOMALIES / ISSUES DURING TEST CAMPAIGN:

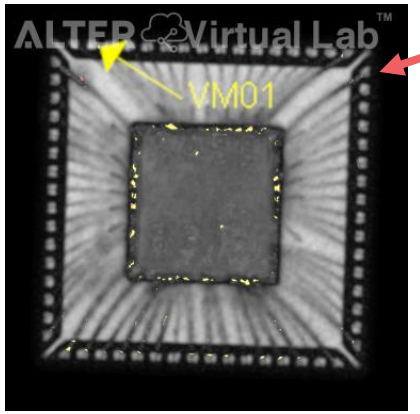
CA Findings:

- several cases of too close internal wires connected to different pads

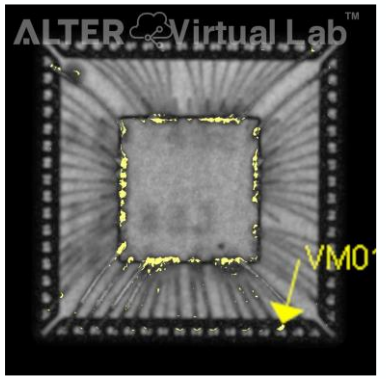




- CSAM anomalies: voids or detection of foreign material in 1 out 5 DUT in CA and in 10 over 43 DUT submitted to CSAM before environmental test



Rejectable void or foreign material intersecting a wire bond.



- the internal plating of terminals including the thermal pad was not listed in data-sheet and materials BOM for the specific package: manufacturer confirmed it was a change not documented.

ALL's WELL THAT ENDS WELL?

PARTICULAR FINDINGS:

The device has a number of control registers accessible via a serial SPI bus.

While the registers were accessible as indicated in the data sheet, the 8 bits address space is only partly specified, and within the specified addresses, part of the 8 bit data registers are undefined.

It was found that the entire 8-bit address space was addressable for read-out (except address 0).

it was found that 20 registers contained one or more bits of data after reset. Some details of these:

- the data pattern was fixed, but the content was different for each tested part
- two of the registers containing such data contained also defined user settable parameters
- for the two registers containing both user settable parameters and initial data at reset, the manufacturer has confirmed that the data relates to calibration, but does not disclose information of registers not specified as user accessible

With the limited data available from the manufacturer, the use of the non-defined registers cannot be recommended in general, but as the data content after reset was unique at least for the number of components tested, these registers were also used as a verification of the correct device being put into the test set-up.

CONCLUSION

MAIN CONCLUSIONS FROM THE STUDY:

The project gave a good understanding of how to carry out the evaluation of COTS components for use in ESA science missions

Carrying out the environmental test revealed some challenges in planning and execution, increasing thus the understanding of the tests beyond what is written in the relevant standards

A few test and inspections outsourcing was needed: HAST, CA, DPA and C-SAM were carried out by Alter

The performance of the Electrical Tester was not sufficient for comparing AC parameters such as SNR and Intermodulation distortion with data sheet values, but functionally the tests were successfully carried out. While noise, gain and offset measurements gave credible repeatable results, the linearity test did not quite reach the high accuracy expectations, particularly regarding INL.

Testing at high and low temperatures may need better cables or routing to the DUT socket

More adequate sockets for high temperature exposure will be needed for future testing to avoid contamination: do not rely on data sheet a dry run is needed

The S/W and H/W development effort/needed competence/cost required to develop electrical tester and SEE test set-up was severely underestimated

CONCLUSION

LAST BUT NOT LEAST:

Around 90 components from the LOT of **ADS4245-EP** that was evaluated will be soon available in ESA stockplace for ESA programme. Summary of the evaluation documentation can be required to ESA through Alter

COTS EVALUATION IS NOT A PIECE OF CAKE