

#4000134677/21/NL/FE

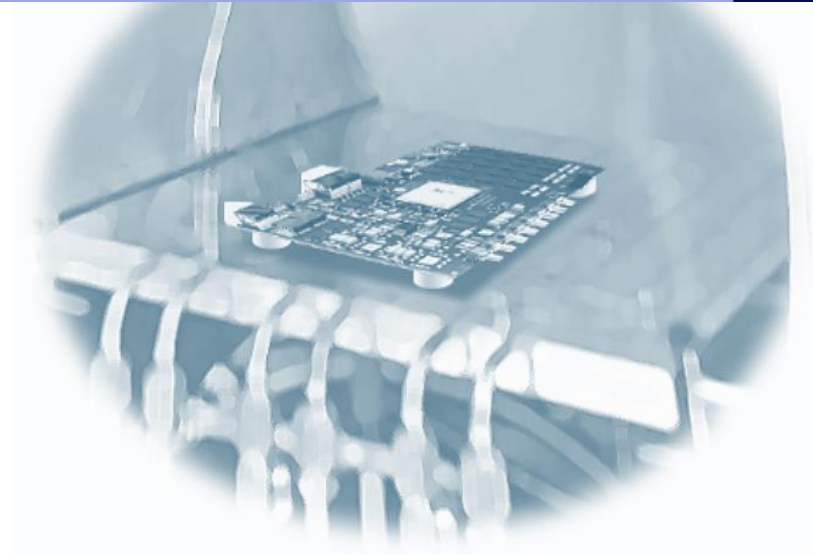


ALTER |  **ACCEDE | ESCCON**  
**2025** Seville - Spain  
25 to 27<sup>th</sup> March

The banner features a blue background with a silhouette of a city skyline and a satellite dish on the right. On the left, there is a red circle and the ALTER logo.

**DSi**  
Aerospace

**ALTER** | 



**ALTER**  
TECHNOLOGY

 **BERNS**  
**ENGINEERS**

SPACE SYSTEMS

**ATCOS GSTP Study: Alternative Test Methods for COTS – Test Results**

We. Create. Space.

# Presentation Overview

- **Study goal**
- **Consortium**
- **Test overview**
- **Test results**
- **Conclusion**

# Study goal

- Compare component level testing with board level testing in order to understand if and how component level testing can be reduced and transferred to board level testing
- Identify suited acceleration means (HALT, HASS) for board level testing to optimize test effort

HALT – Highly Accelerated Life Test

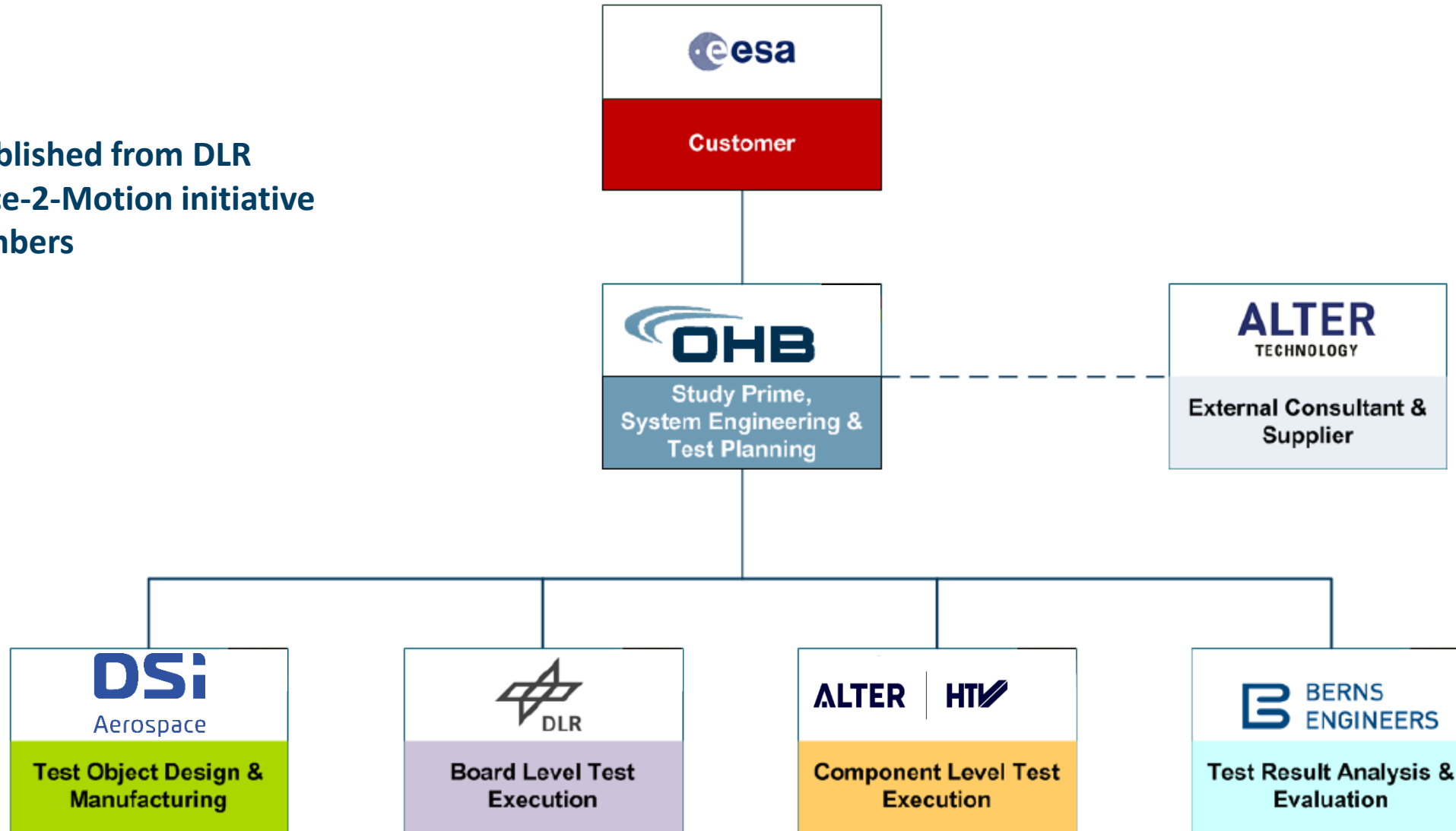
HASS – Highly Accelerated Stress Screening

## Notes:

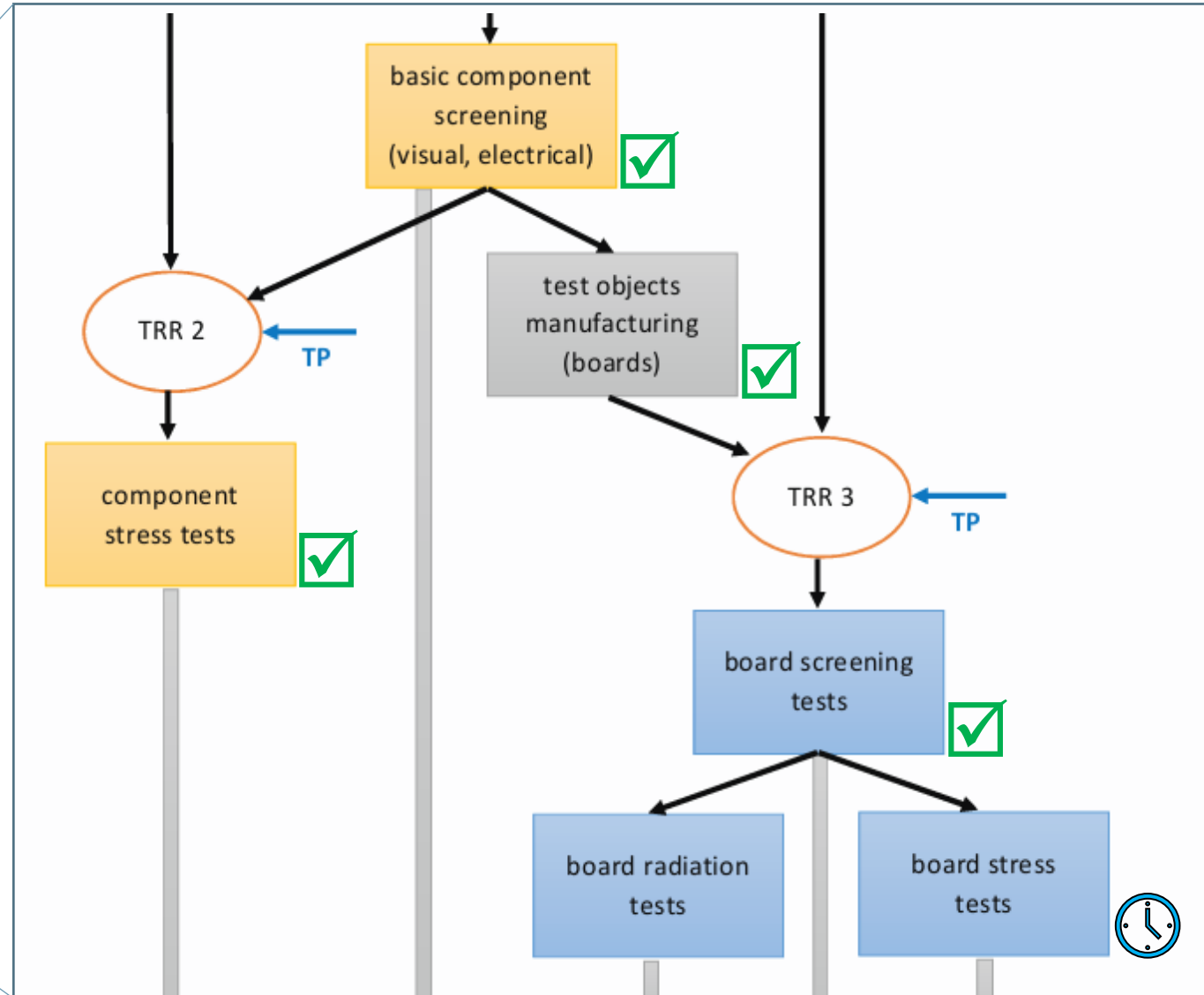
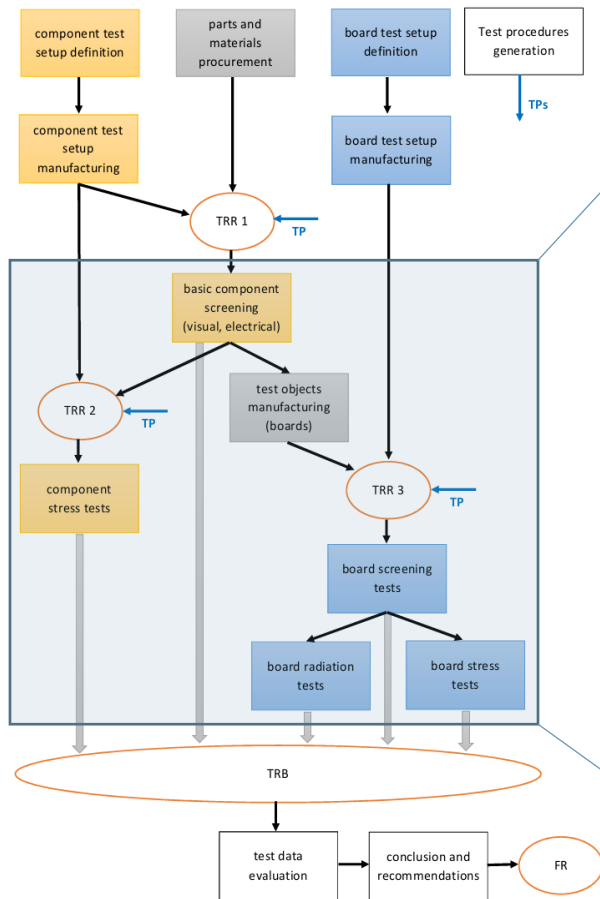
- Study considers qualification testing aspects (flight representative hardware) and screening testing aspects (flight hardware)
- Study is based on existing hardware (board from DSI)

# Consortium

Established from DLR  
Space-2-Motion initiative  
members

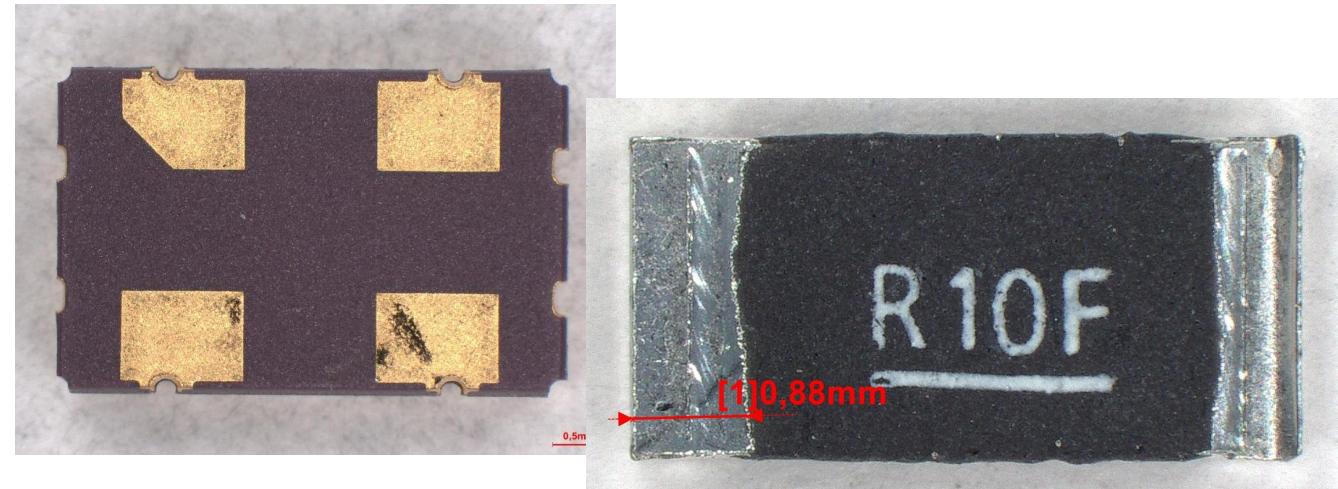


# Test Plans



# Component Level Screening

- **30 component types tested, 1116 components total**  
7 ICs, 1 hybrid, 3 oscillators, 7 discretes, 1 inductor, 6 capacitors, 4 resistors, 1 connector
- **Results of visual inspection:**
  - 1 shipment completely rejected → inadequate packaging (by distributor -> ESD+damage)
  - 17 component types 100% pass, 13 component types with some fails
  - 63 of 1116 components failed → but still being used for board manufacturing
    - Foreign particles and contamination
    - Scratches
    - Corrosion on test points or pins
    - Exposed base material of pins
    - Package discolorations
    - Deviation from specifications
    - Bent pins



# Component Level Screening

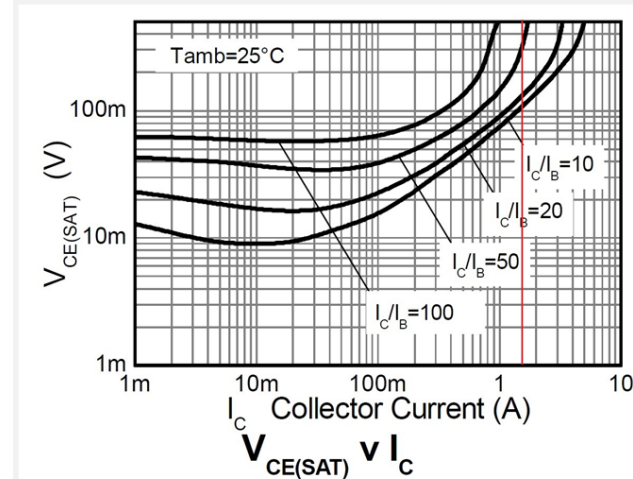
- **Results of electrical testing:**
  - No failures found
  - Found error in one transistor data sheet:  
VCE(sat)(max) listed as 200 mV in one place, 300 mV in another

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Emitter Saturation Voltage (Note 9)	V <sub>CE(sat)</sub>	-	15	20	mV	I <sub>C</sub> = 0.1A, I <sub>B</sub> = 10mA
		-	45	60		I <sub>C</sub> = 0.5A, I <sub>B</sub> = 50mA
		-	145	185		I <sub>C</sub> = 1A, I <sub>B</sub> = 20mA
		-	160	200		I <sub>C</sub> = 1.5A, I <sub>B</sub> = 20mA

All parts are fail at the last VCE(sat) parameter, for which a maximum of 200 mV, measured with I<sub>C</sub> = 1.5 A, I<sub>B</sub> = 20 mA, I<sub>C</sub>/I<sub>B</sub>=75, is given in the "Electrical Characteristics" table in the data sheet.

However, according to the "Typical Electrical Characteristic Diagram" in the data sheet, a typical value much higher than 200 mV is given. (See below, test condition I<sub>C</sub> = 1.5 A is marked in red). The typical value for I<sub>C</sub>/I<sub>B</sub>=75 should be higher than 300 mV.

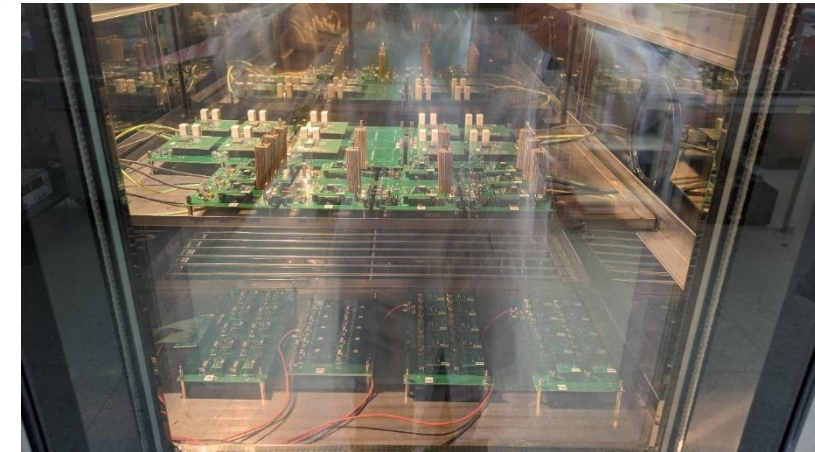


Measured values of VCE(sat) at these conditions vary between 0.692 and 1.373 V, which is a typical, inconspicuous range of values.

We suspect the limit of 200 mV is erroneous.

# Component Level Stress Tests

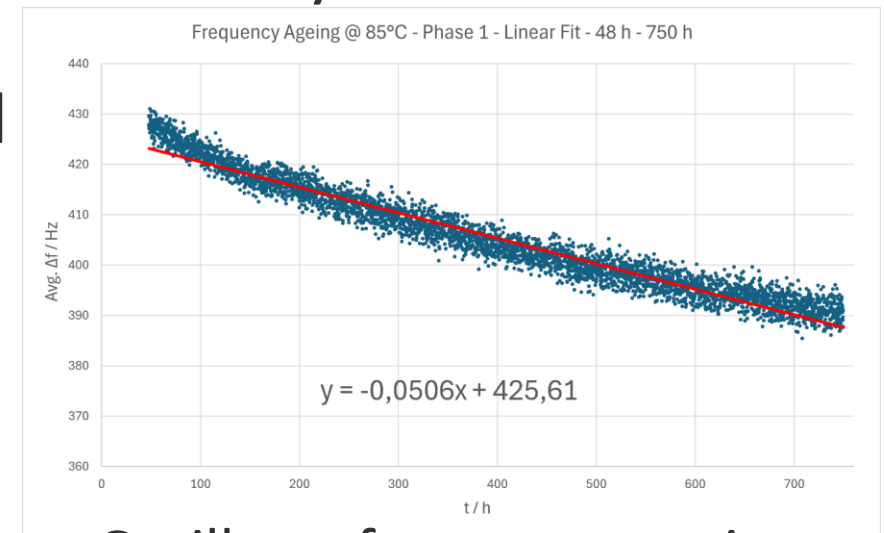
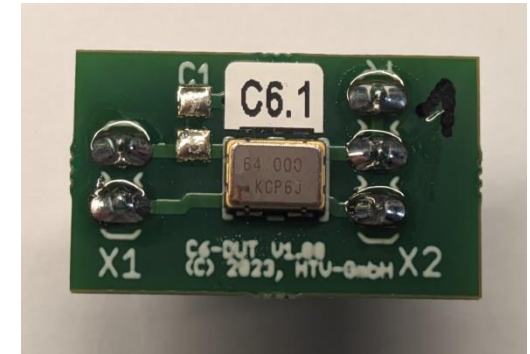
- **15 component types tested, 150 components total**  
3 ICs, 1 module, 1 oscillator, 5 discretes, 1 inductor, 2 capacitors, 1 resistors, 1 connector
- **Stress test = life test + type specific tests + DPA**
- **Life test usually @ 125°C**  
**2 groups 1000h @ 125°C, 1500h @ 85°C**
  - Some components have max. operating temperature 85°C
  - Some are self-heating



# Component Level Stress Tests

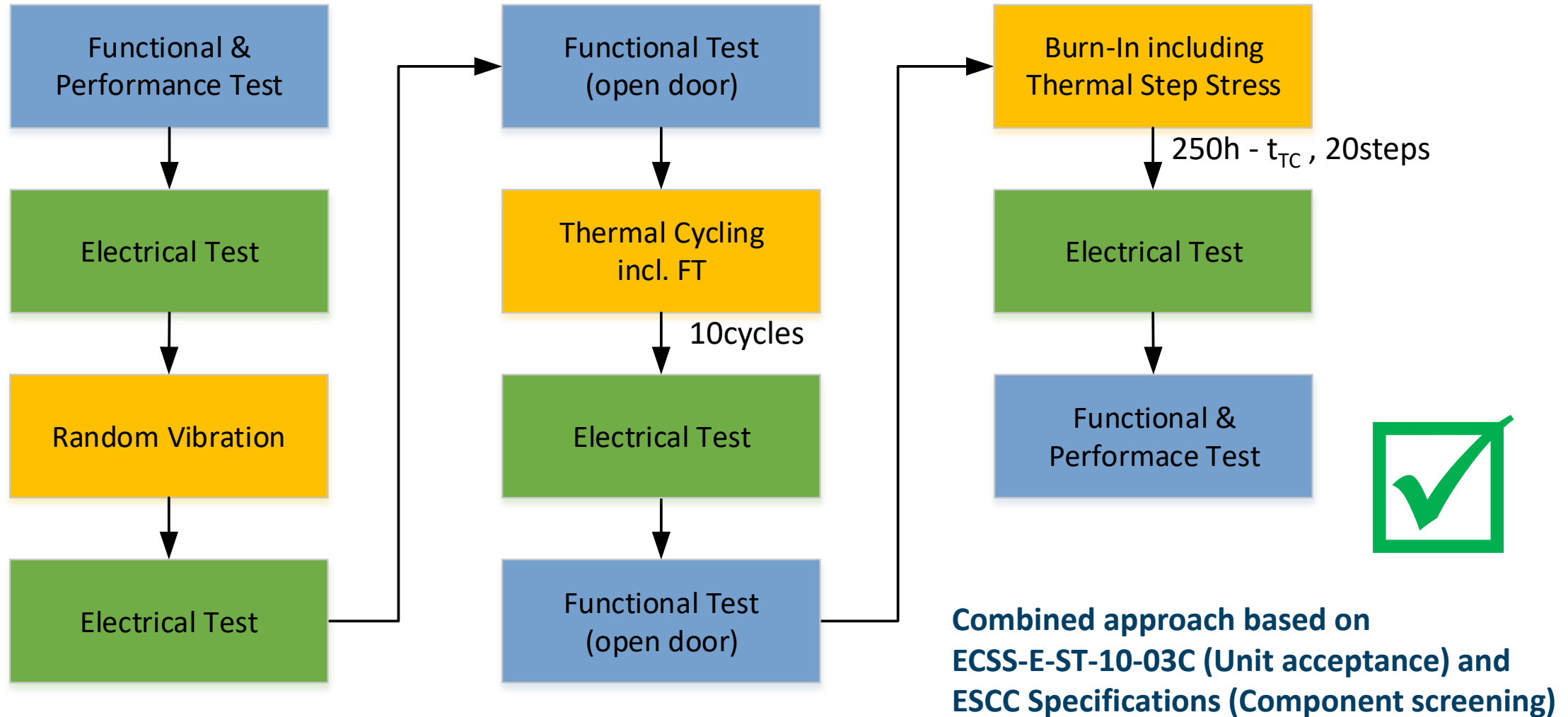
- **Life test results:**

- No catastrophic failures
- Sometimes, large tolerance windows listed in data sheets – component performance generally well within range
- Parametric failure of inductor – inductance increased by ~ 12% during test, exceeds max limit
- Line regulation of power module not as good as expected from data sheet “typical value”
- Oscillator (64 MHz, specified as +/- 50 ppm) performed very well
  - <1 ppm change during 1500 h @ 85°C
  - <2 ppm change during shock and vibration



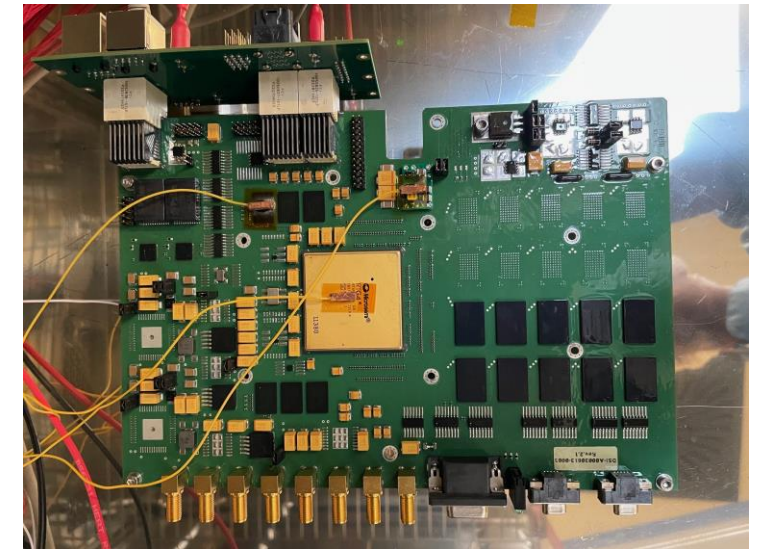
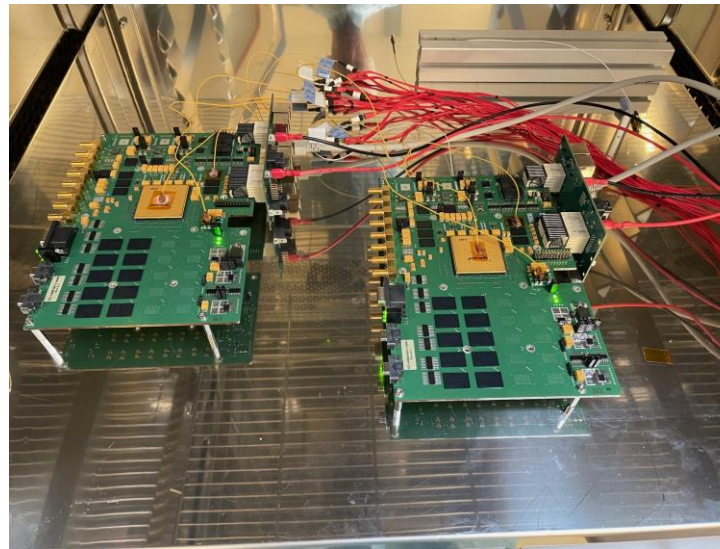
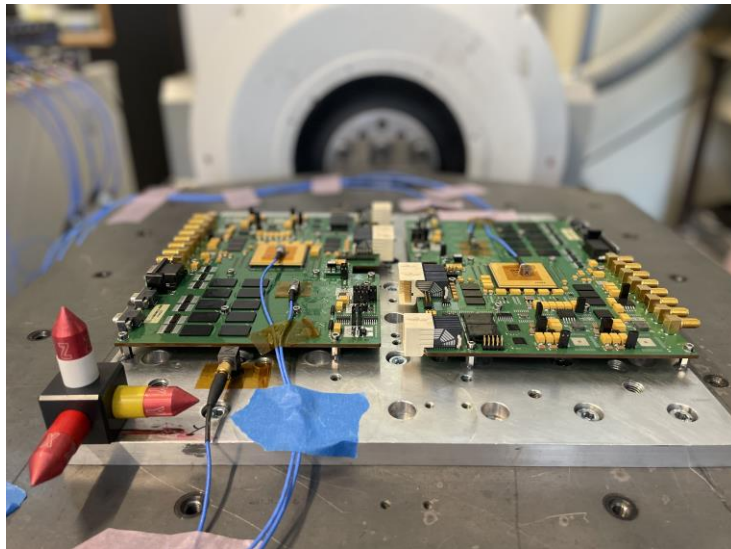
Oscillator frequency ageing

# Board Screening Tests

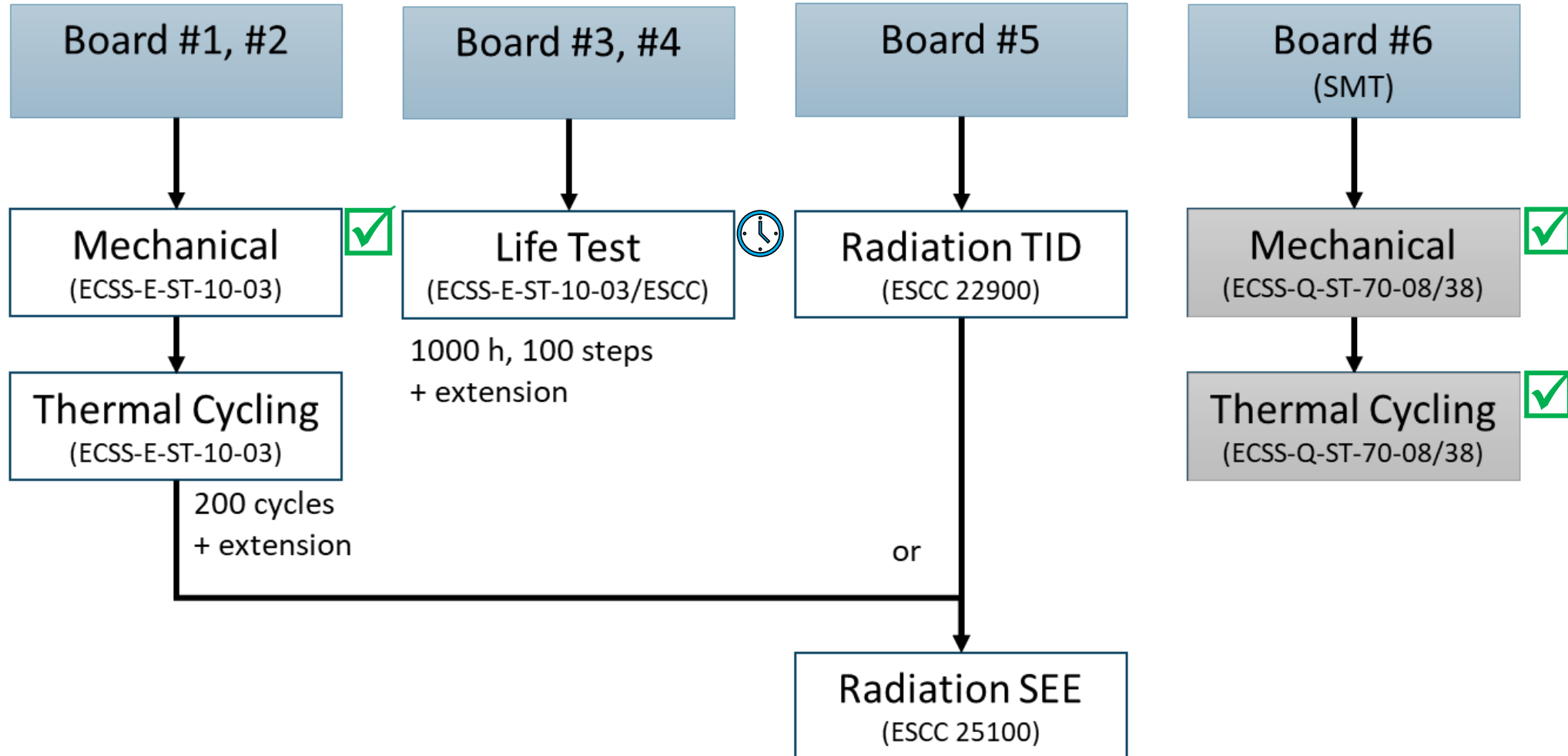


# Board Level Screening Tests

- Screening tests performed on 5 Boards
- Results Visual Inspection: **passed**
- Results Functional Testing: **passed**
- Results Electrical Testing: **passed**

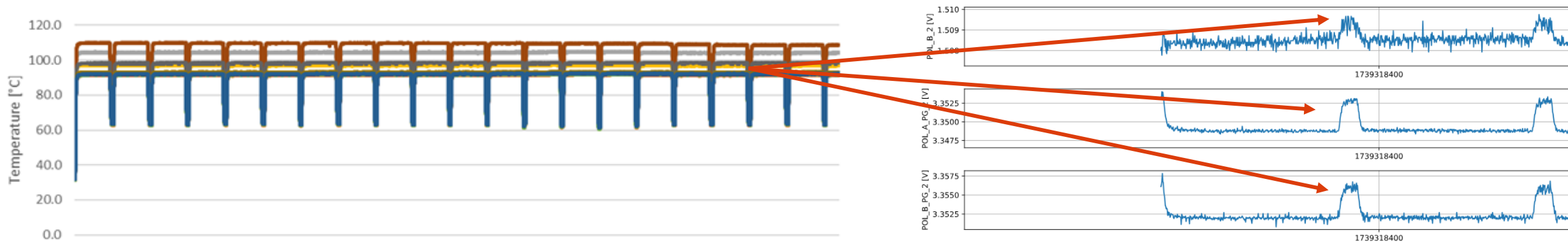


# Test Plans – Board Stress Tests



# Board Level Stress Tests - ongoing

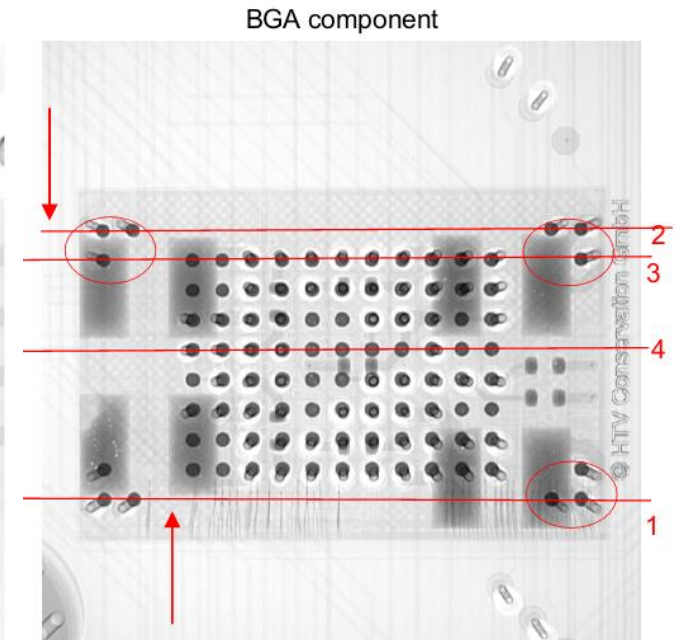
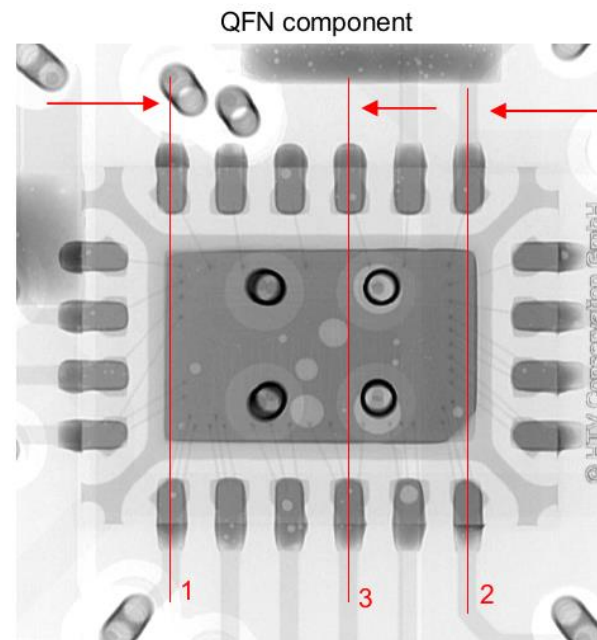
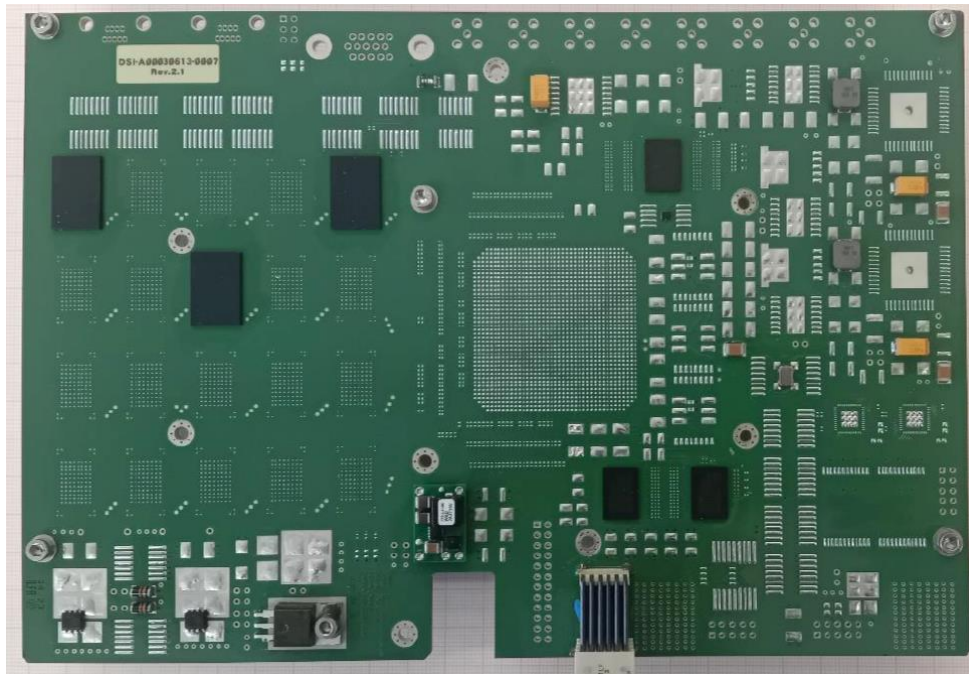
- Mechanical tests performed on Board 1 and Board 2 (**passed**)
- Life test almost completed on Board 3 and Board 4 (~800h)
  - All functions still regular
  - No significant drift in monitored electrical parameters



In-Situ parameter measurements

# Board Level Stress Tests - ongoing

- **Mounting Verification on passive board (16 component types)**
  - Environmental Testing completed → no obvious damages
  - Microsectioning ongoing



# Conclusion

- **No severe issues during component level testing**
- **Screening without failure on all 5 boards**
- **Board stress tests ongoing**
  - Mechanical Tests successful
  - Life Test at 800h out of 1000h (+extension) – so far fully functional
- **Mounting verification testing completed, microsectioning ongoing**
- **Comparison between component level results and board level results ongoing**

**Commercial components selected so far appear to be robust and industrial mounting appears to be reliable, pending**

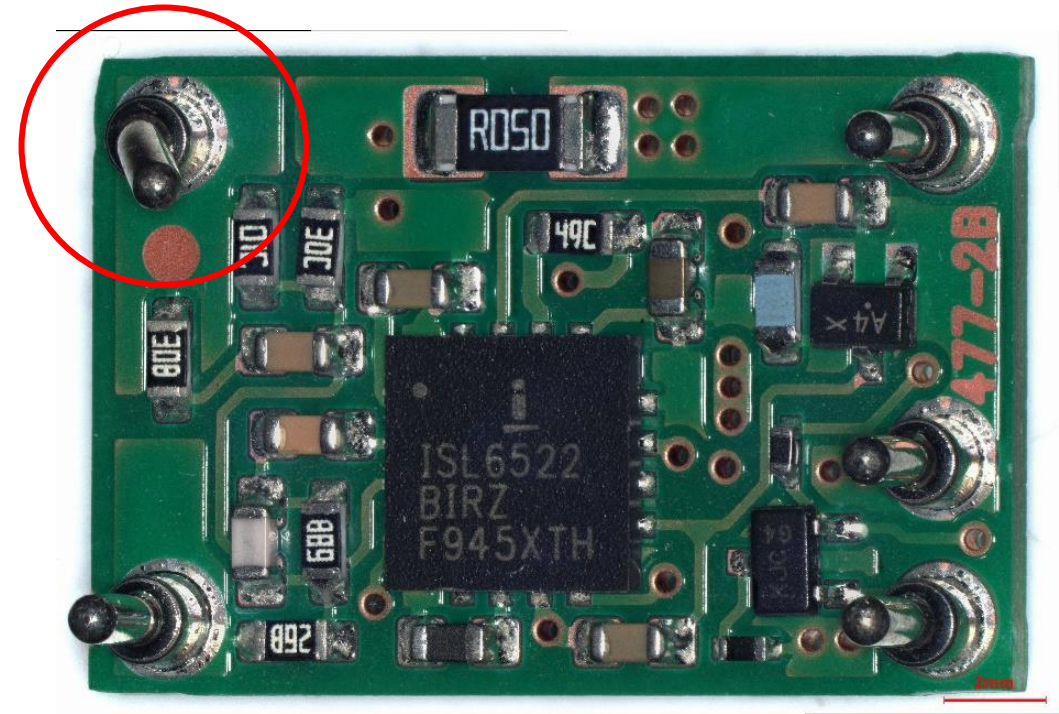
- **confirmation from microsectioning**
- **board level thermal cycle testing**
- **radiation testing**



**Thank you**

# Backup Slides

# Component Level Screening

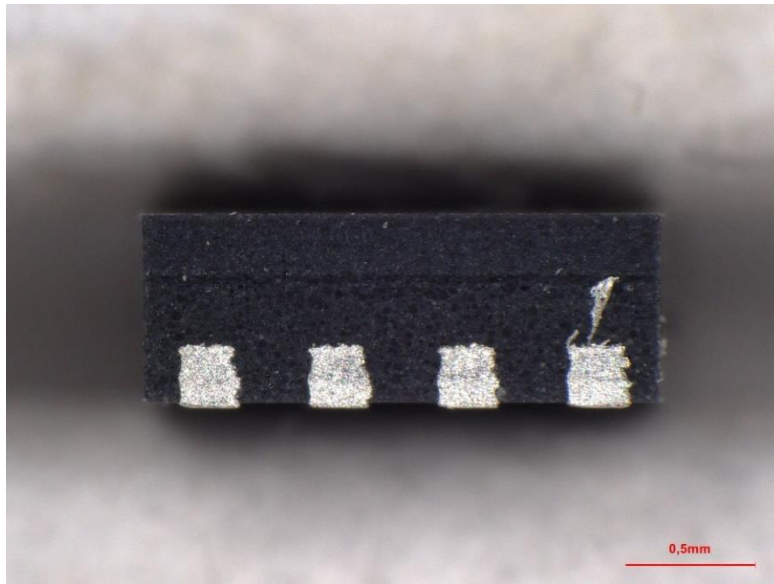


Styrofoam packaging is not ESD safe

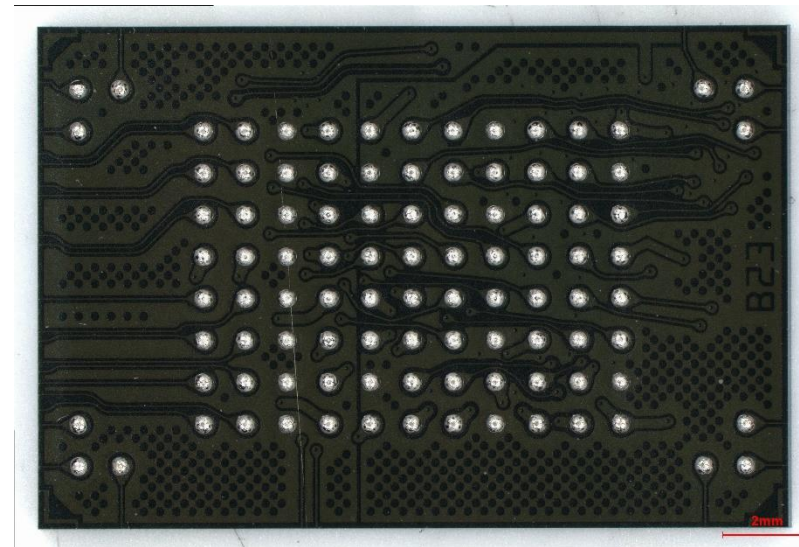
-

and leads to bent pins

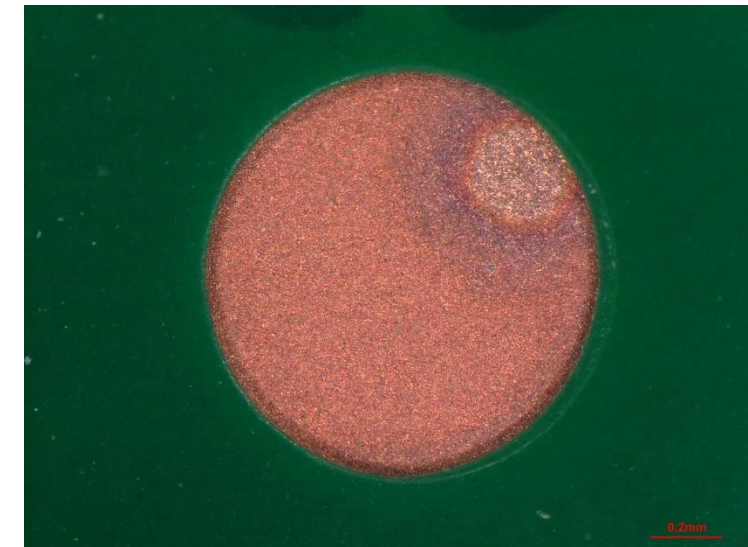
# Component Level Screening



Metallisation particle

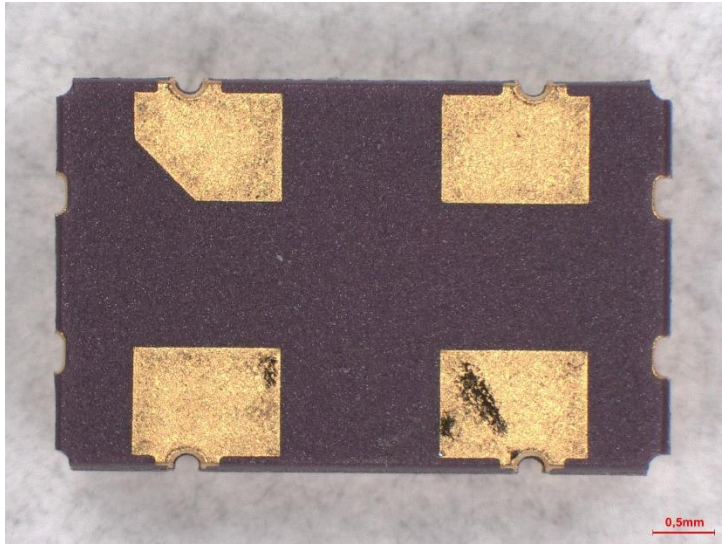


scratch

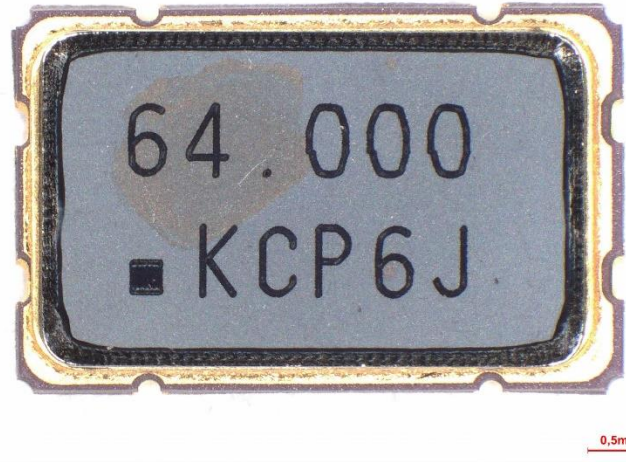


corrosion

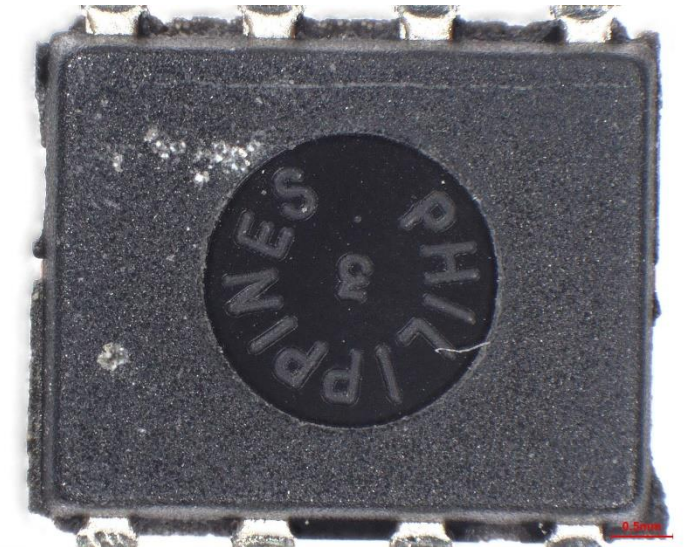
# Component Level Screening



contamination

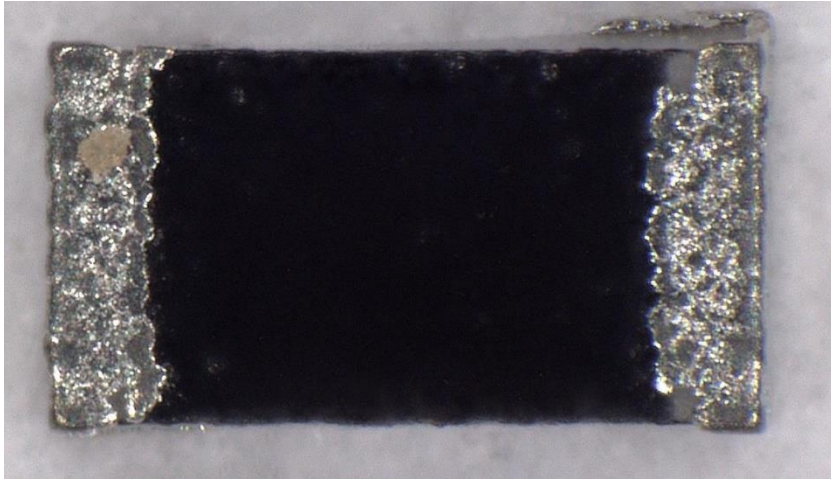


discoloration



contamination

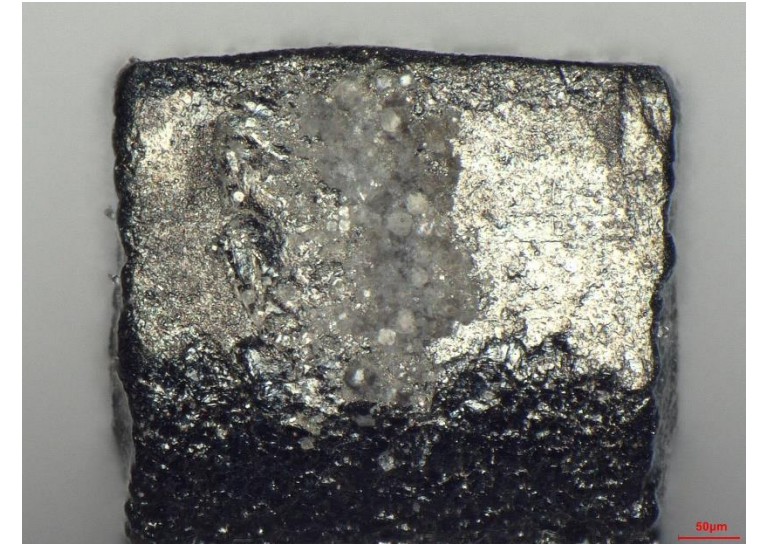
# Component Level Screening



contamination

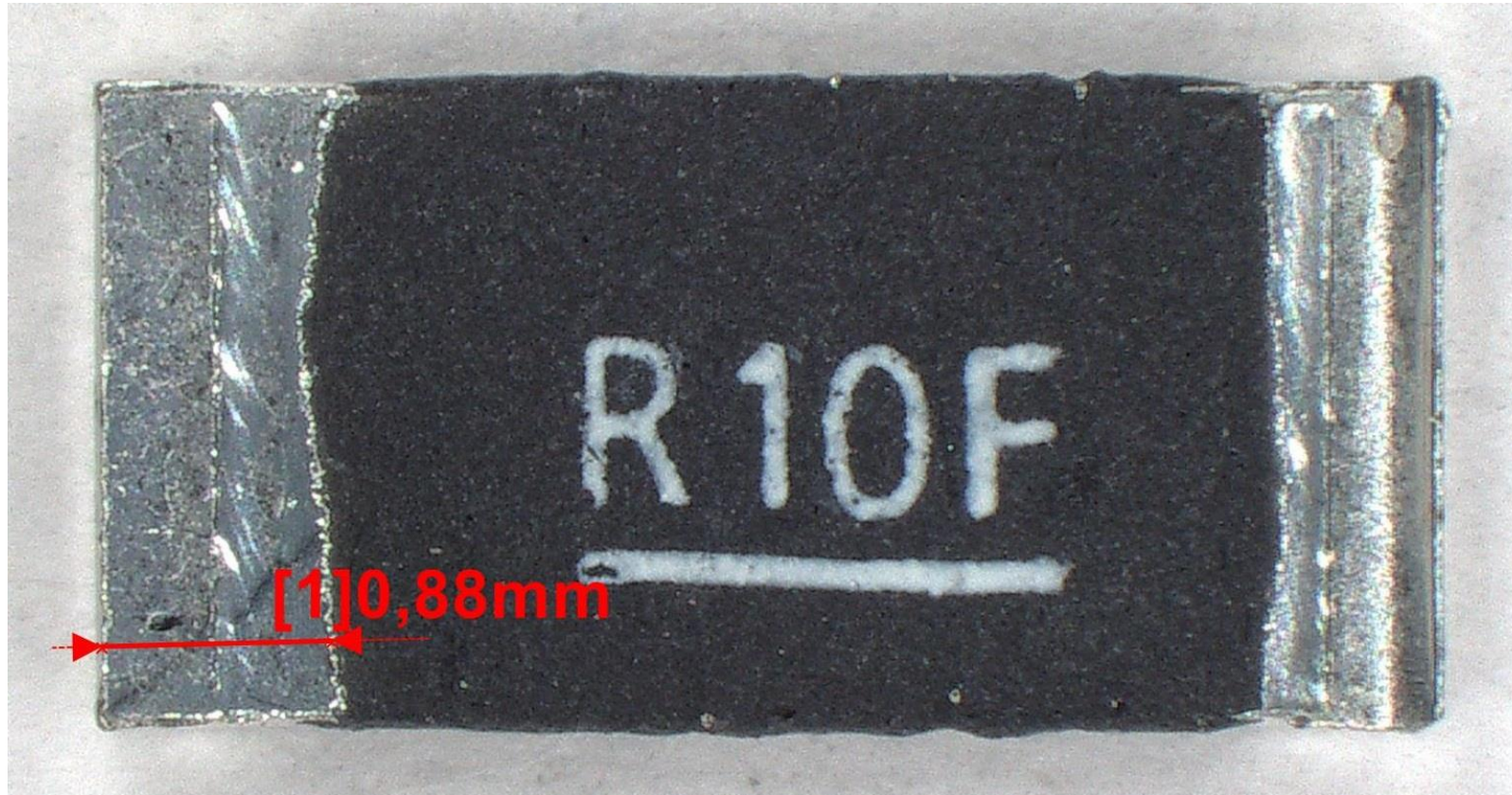


Bent pin



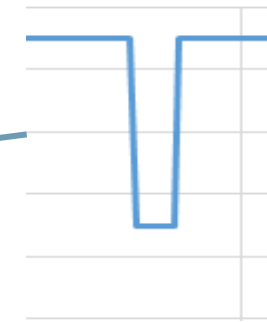
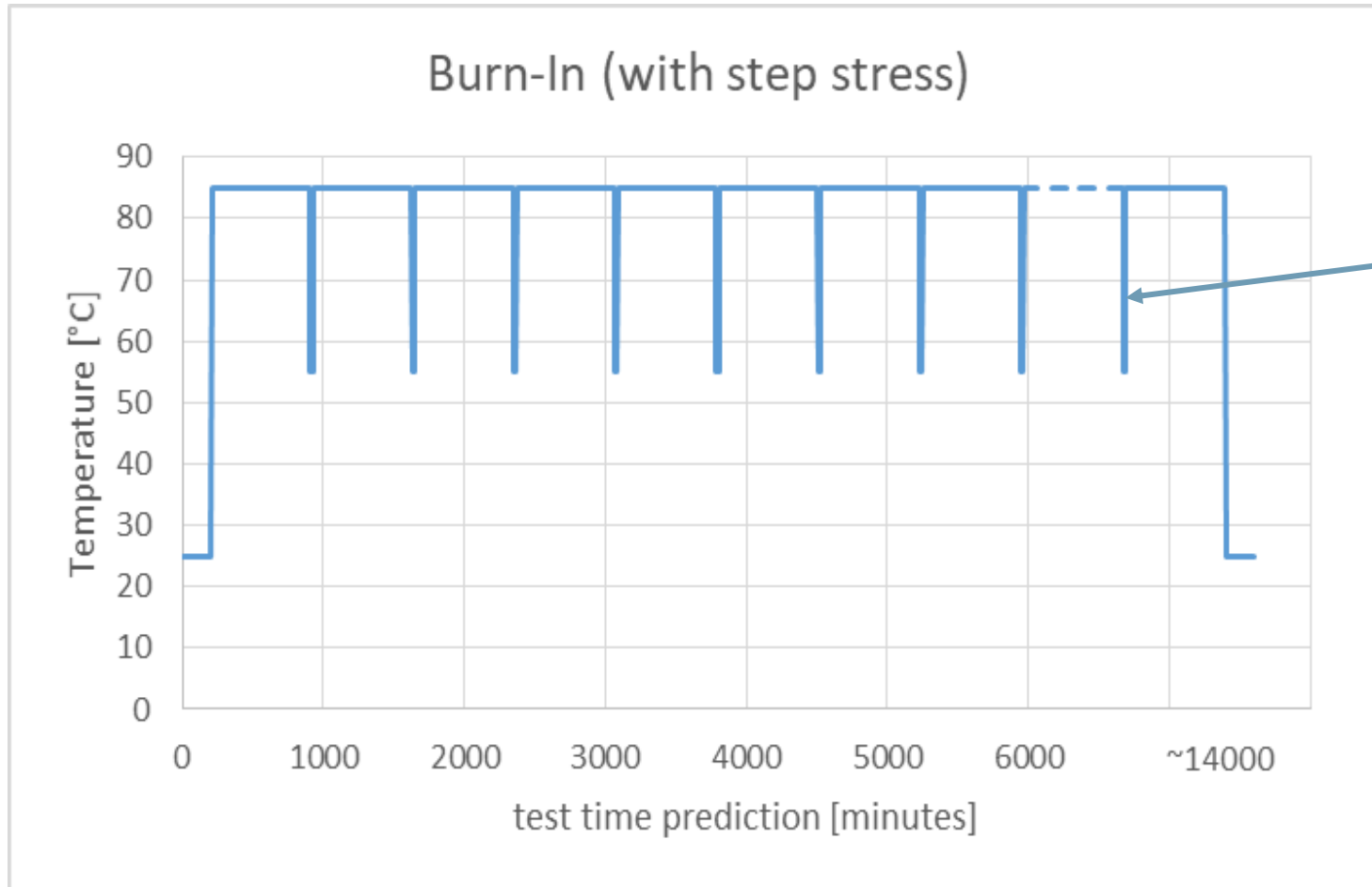
Corrosion on pin

# Component Level Screening

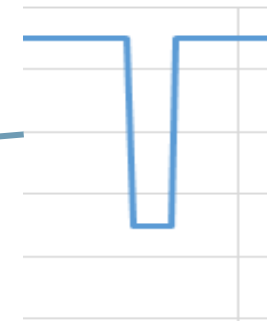
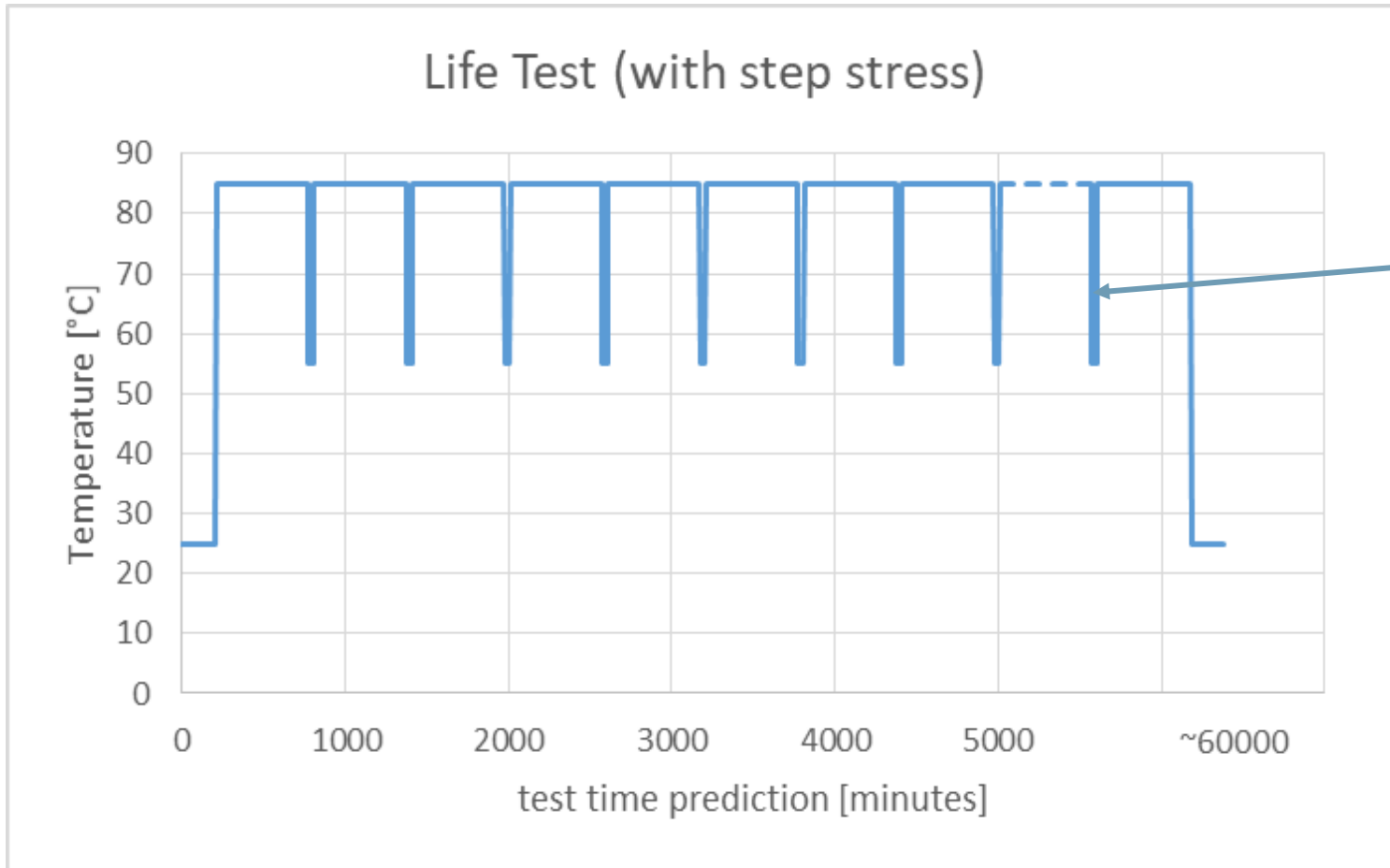


Cap metallization exceeds data sheet limit -  $T_{max}=0.762$  mm

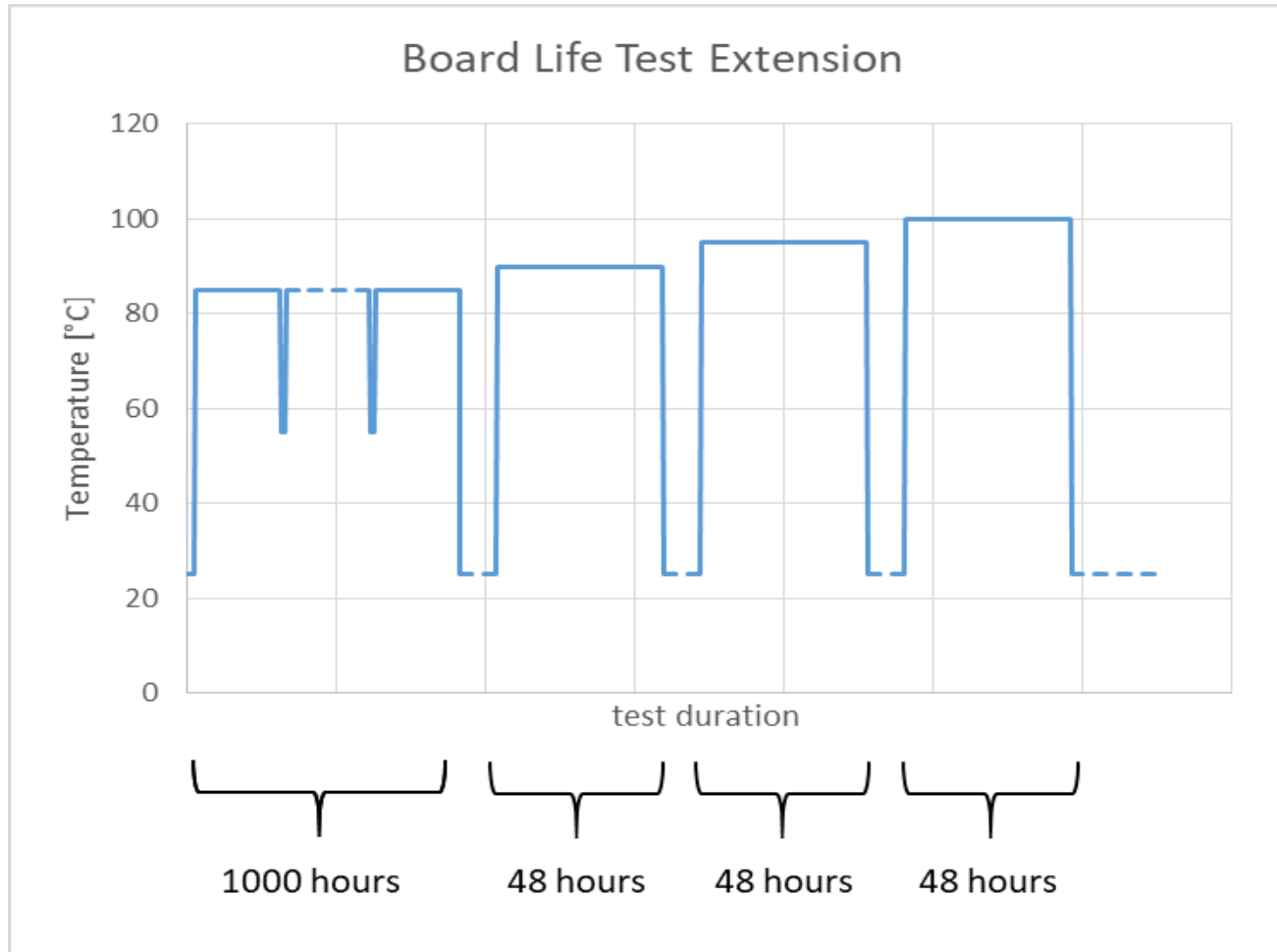
# Test Plans – HASS aspect – burn-in with thermal step stress



# Test Plans – HALT aspects – Life Test with thermal step stress



# Test Plans – HALT aspects – Life Test with temperature increase



# Test Plans – HALT aspects – Thermal Cycle Test with temperature increase

