ALTER

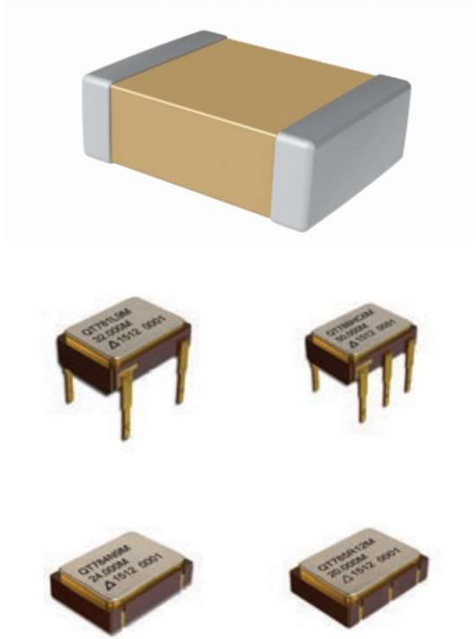
ACCEDE / ESCCON 2025 DAY 0

COTS selection, risks, mitigation techniques and tools.

Manuel Sanchez & Jose Largaespada | Parts Engineering | 24/03/2025

Introduction

- **What do we understand by COTS?**



COTS = Commercial Off The Shelf

- Parts designed and manufactured for commercial/industrial use
- Not supported for Military nor Space applications
- Technically, parts described as COTS have some kind of traceability and production controls, depending on manufacturer
- Nevertheless, it is usual to call COTS to any commercial part colloquially

Introduction

- **Why Use COTS? Key Advantages**

- **Proven Technology:**
  - Breakthrough technologies come earlier to the COTS market than to the “traditional” Space market.
  - In terms of performance, they usually provide further limits than Space/Military parts. They always allow a wider portfolio of references for type required.
  - Higher availability in general

- **Cost and Time Savings?**
  - lower lead times and wider availability.
  - Lower upfront costs due to mass production, compared to traditional Space/Military quality parts.
  - However…

Introduction

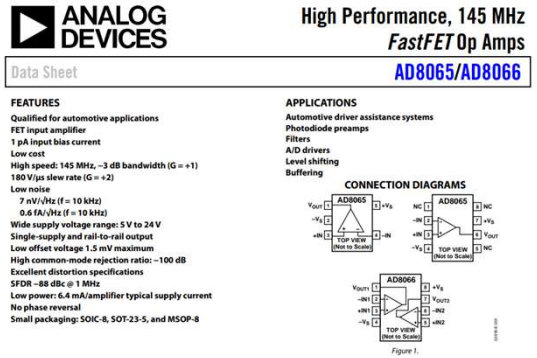
- **Why Use COTS? Key Advantages**

AD8065ARZ for a Class 1 mission (old ECSS-Q-ST-60-13C approach):

Unit price: 1.77 USD/Unit. Lead time: 7w

Total NRE: approx. 140 kEUR (2020)

Total Testing Lead Time: 52 weeks



ANALOG DEVICES

High Performance, 145 MHz *FastFET* Op Amps

Data Sheet AD8065/AD8066

FEATURES

Qualified for automotive applications
FET input amplifier
1 pA input bias current
Low cost
High speed: 145 MHz, −3 dB bandwidth (G = +1)
180 V/µs slew rate (G = +2)
Low noise
7 nV/√Hz (f = 10 kHz)
0.6 fA/√Hz (f = 10 kHz)
Wide supply voltage range: 5 V to 24 V
Single-supply and rail-to-rail output
Low offset voltage 1.5 mV maximum
High common-mode rejection ratio: −100 dB
Excellent distortion specifications
SFDR −88 dBc @ 1 MHz
Low power: 6.4 mA/amplifier typical supply current
No phase reversal
Small packaging: SOIC-8, SOT-23-5, and MSOP-8

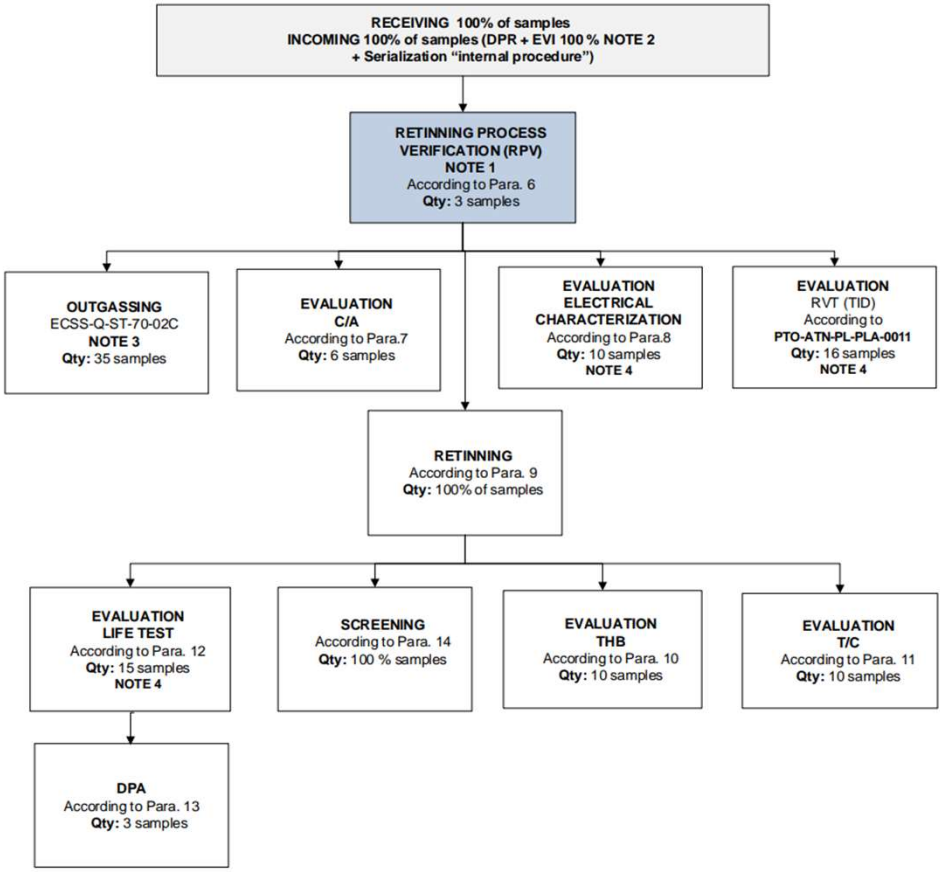
APPLICATIONS

Automotive driver assistance systems
Photodiode preamps
Filters
A/D drivers
Level shifting
Buffering

CONNECTION DIAGRAMS

AD8065 TOP VIEW (Not to Scale)
AD8065 TOP VIEW (Not to Scale)
AD8066 TOP VIEW (Not to Scale)

Figure 1.



Introduction

- **Challenges of Using COTS**

- **Reliability risks:**
  - They involve higher risks in terms of reliability regarding cosmic and solar radiation, not providing data against them.
  - Problems with materials used including pure tin (tin whiskers), outgassing and some restricted materials.
  - Lack of testing, limited heritage, high level of uncertainties in terms of adecuacy for Space applications

- **Vendor Dependency:**
  - Lack of Traceability and lack of production control or testing
  - Reliance on the supplier for updates and support. Manufacturer does not need to inform of changes in the manufacturing process, supply change…
  - Risk of obsolescence if the vendor discontinues the product.
  - High non-recurrent expenses and lead time for testing

Introduction

- **COTS constraints and risks for Space Use**

- **Materials:**
  - **COTS can contain materials such as Cd or BeO, limited or forbidden for Space Applications**
  - **COTS lead finish is usually pure Sn, leading to risks of Tin Whiskers: mitigation measurements are required**
  - **COTS packages tend to be plastic, leading to risk of Outgassing depending on materials.**
- **Temperature:**
  - **COTS performance is usually guaranteed on a more stringent temperature range than the military one, for example: (-40ºC to +85ºC) or even (0ºC to 70ºC).**
  - **This introduces a risk when qualifying the COTS for the project**
- **Risk of Counterfeits**

Introduction

- **COTS constraints and risks for Space Use**

- **Mechanical Constraints:**
  - **COTS are not designed nor tested to withstand vibration and shock conditions for Space applications and can fail to these tests.**

- **Obsolescence:**
  - **A manufacturer can obsolete a COTS part with no notice. Also, unnotified changes can be done on datasheet**

- **Radiation:**
  - **COTS PARTS ARE NOT DESIGN NOR TESTED TO RADIATION AND THIS IS KEY FOR SPACE APPLICATIONS.**

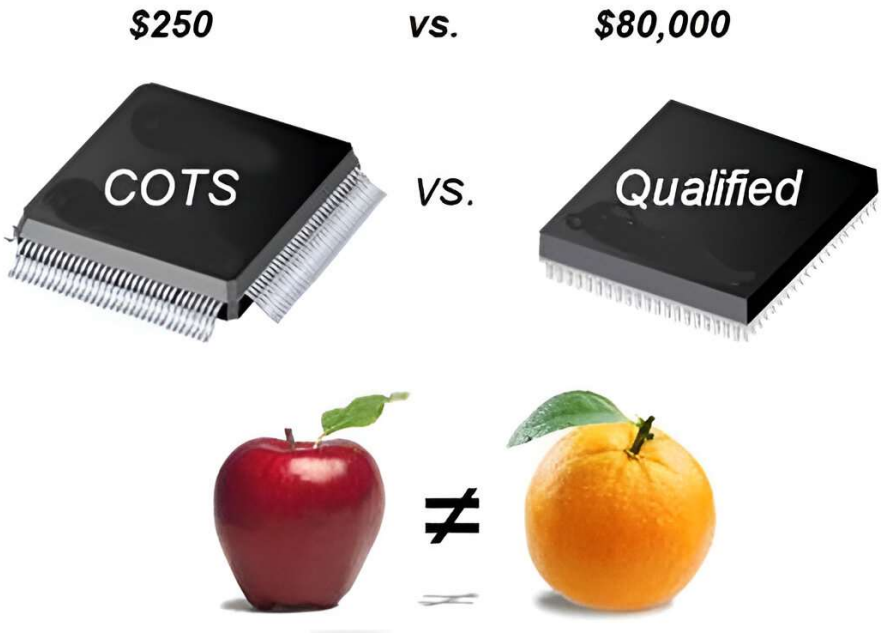
  - **This introduces high uncertainty and along with the possible unnotified design changes, important uncertainties.**

  - **Search for Heritage is usually a must**

Introduction

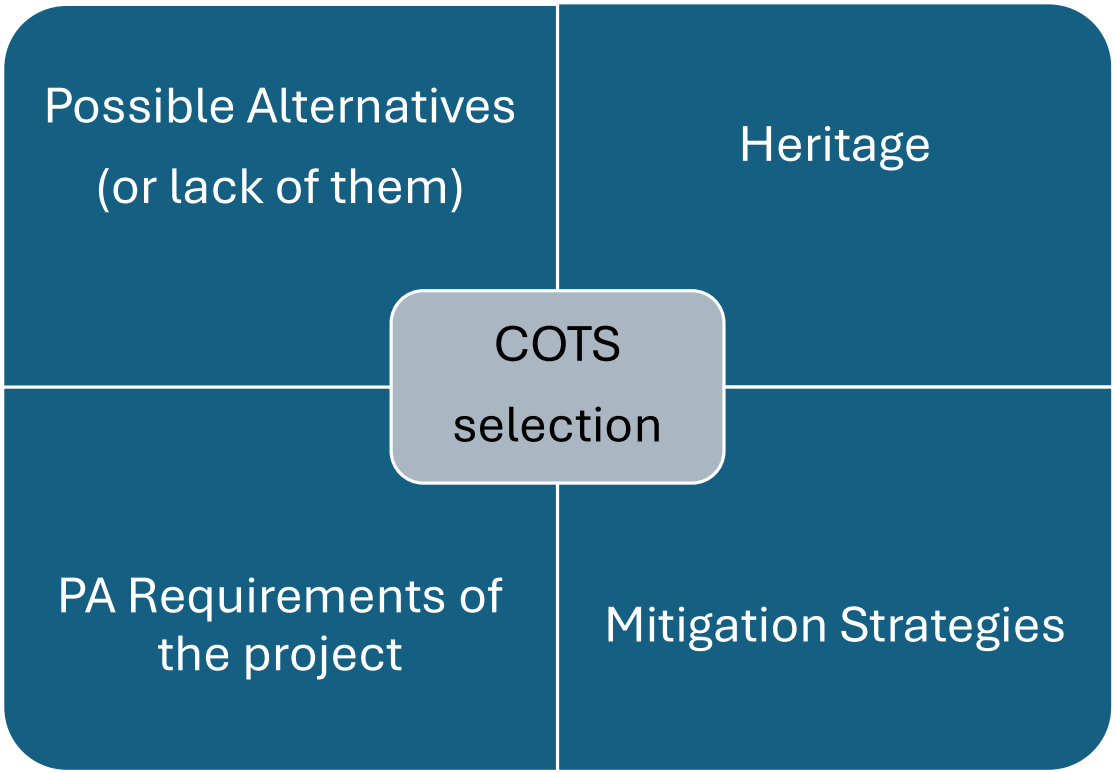
- **Then…Why are COTS used in space projects?**

- Regarding the mentioned characteristics, COTS tend to be more interesting than space qualified products in terms of cost, lead time and technical features.
- However, the lack of sufficient reliability data makes them unable to be used in some Space applications without testing.
- But it is not always required a very high reliability level and stringent Product Assurance requirements.



COTS Selection, Mitigation Strategies

- **COTS Selection Considerations**



COTS Selection, Mitigation Strategies

- **Possible Alternatives: Real Case**

Renesas ISL7457 Vs EL7457

ISL7457SRH ● Active Samples Available

Radiation Hardened, SEE Hardened, Non-Inverting, Quad CMOS Driver

EL7457 ● Active Samples Available

40MHz Non-Inverting Quad CMOS Driver

ISL7457 is a qualified product, while EL7457 is a COTS. At a first sight, the choice would be ISL7457, but…

ISL7457

Features

- Electrically screened to SMD 5962-08230
- QML qualified per MIL-PRF-38535 requirements
- Full mil-temp range operation: T_A = -55°C to +125°C
- Radiation hardness
  - TID [50-300 rad(Si)/s]: 10krad(Si) minimum
- **SEE hardness**
  - LET (SEL and SEB Immunity): 40MeV/mg/cm^2 minimum
  - LET [SET = ΔV_{OUT} < 15V, Δt < 500ns]: 40MeV/mg/cm^2
- 4 channels
- Clocking speeds up to 40MHz
- 11ns/12ns typical t_R/t_F with 1nF Load (15V bias)
- 1ns typical rise and fall time match (15V bias)
- 1.5ns typical prop delay match (15V bias)
- Low quiescent current - < 1mA Typical
- Fast output enable function - 12ns typical (15V bias)
- Wide output voltage range
  - 0V ≤ V_L ≤ 8V
  - 2.5V ≤ V_H ≤ 16.5V
- 2A typical peak drive current (15V Bias)
- 3.5Ω typical ON-resistance (15V bias)
- Input level shifters
- 3.3V/5V CMOS compatible inputs

EL7457

Features

- Clocking speeds up to 40MHz
- 4 channels
- 12ns t_R/t_F at 1000pF C_{LOAD}
- 1ns rise and fall time match
- 1.5ns prop delay match
- Low quiescent current - <1mA
- Fast output enable function - 12ns
- Wide output voltage range
- 8V ≥ V_L ≥ -5V
- -2V ≤ V_H ≤ 16.5V
- 2A peak drive
- 3Ω on resistance
- Input level shifters
- TTL/CMOS input-compatible
- Pb-free (RoHS compliant)

COTS Selection, Mitigation Strategies

- **Heritage: Real Case**

Renesas EL7457

- This part had been used on Euclid and Kepler:
  - SEL information available with Safe Operating Area
  - Unstable behavior on TID
  - Constructional Analysis
  - Upscreening (percentage of failures 0.367%.)
  - Qualification
  - DPA
  - HAST

Kepler Mission Development Challenges and Early Results

James Fanson (818-354-7014; james.l.fanson@jpl.nasa.gov)
Margaret Frerking (818-354-4902; margaret.a.frerking@jpl.nasa.gov)
Riley Duren (818-354-5753; riley.m.duren@jpl.nasa.gov)
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Dr.
Pasadena CA 91109

  - This information provided highly valuable inputs for the selection and design-in

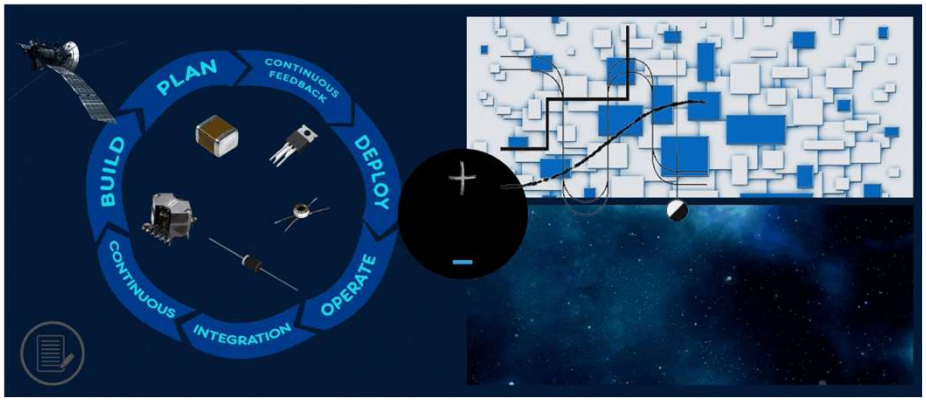
COTS Selection, Mitigation Strategies

- **PA Requirements**

- A Product Assurance (PA) Plan is a comprehensive framework designed to ensure that the space system (satellite, spacecraft, or any related equipment) meets the required quality, safety, and reliability standards throughout its lifecycle.

- The PA Plan will define the reliability requirements for all components, including COTS.

- A PA Plan for a Class 1 mission will be totally different to the one of a Cubesat mission

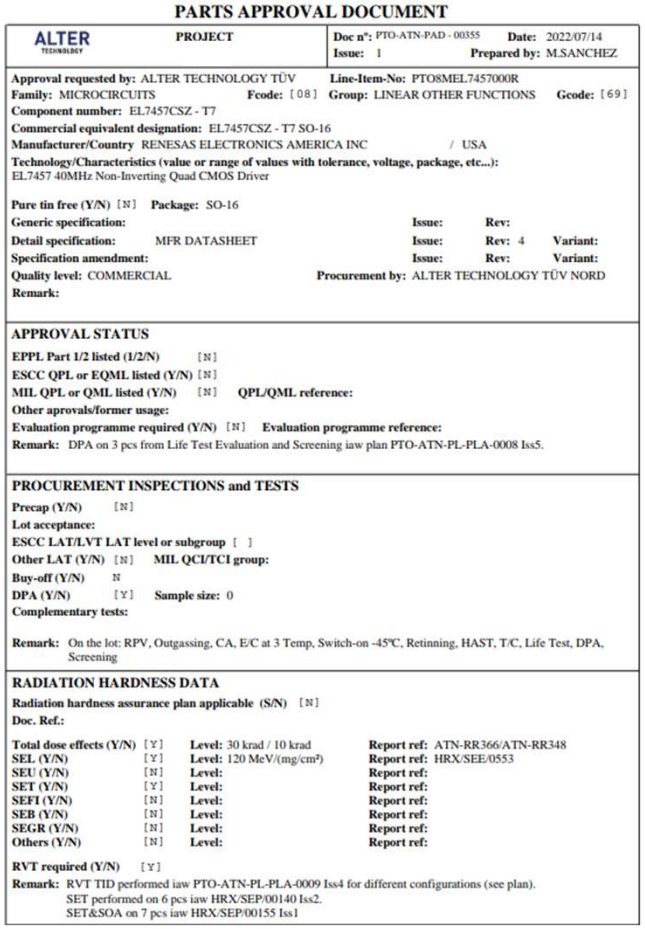


COTS Selection, Mitigation Strategies

- **PA Requirements**

Renesas EL7457

- These are related to the type of mission and also additional particularities
- Heritage helps to tailor the actual testing need



PARTS APPROVAL DOCUMENT

ALTER TECHNOLOGY — **PROJECT**

Doc n°: PTO-ATN-PAD - 00355 **Date:** 2022/07/14
Issue: 1 **Prepared by:** M.SANCHEZ

Approval requested by: ALTER TECHNOLOGY TÜV **Line-Item-No:** PTO8MEL7457000R
Family: MICROCIRCUITS **Fcode:** [08] **Group:** LINEAR OTHER FUNCTIONS **Gcode:** [69]
Component number: EL7457CSZ - T7
Commercial equivalent designation: EL7457CSZ - T7 SO-16
Manufacturer/Country RENESAS ELECTRONICS AMERICA INC / USA
Technology/Characteristics (value or range of values with tolerance, voltage, package, etc...):
EL7457 40MHz Non-Inverting Quad CMOS Driver

Pure tin free (Y/N) [N] **Package:** SO-16
Generic specification: **Issue:** **Rev:**
Detail specification: MFR DATASHEET **Issue:** **Rev:** 4 **Variant:**
Specification amendment: **Issue:** **Rev:** **Variant:**
Quality level: COMMERCIAL **Procurement by:** ALTER TECHNOLOGY TÜV NORD
Remark:

APPROVAL STATUS

EPPL Part 1/2 listed (1/2/N) [N]
ESCC QPL or EQML listed (Y/N) [N]
MIL QPL or QML listed (Y/N) [N] **QPL/QML reference:**
Other aprovals/former usage:
Evaluation programme required (Y/N) [N] **Evaluation programme reference:**
Remark: DPA on 3 pcs from Life Test Evaluation and Screening iaw plan PTO-ATN-PL-PLA-0008 Iss5.

PROCUREMENT INSPECTIONS and TESTS

Precap (Y/N) [N]
Lot acceptance:
ESCC LAT/LVT LAT level or subgroup [ ]
Other LAT (Y/N) [N] **MIL QCI/TCI group:**
Buy-off (Y/N) N
DPA (Y/N) [Y] **Sample size:** 0
Complementary tests:

Remark: On the lot: RPV, Outgassing, CA, E/C at 3 Temp, Switch-on -45°C, Retinning, HAST, T/C, Life Test, DPA, Screening

RADIATION HARDNESS DATA

Radiation hardness assurance plan applicable (S/N) [N]
Doc. Ref.:

Total dose effects (Y/N) [Y]	**Level:** 30 krad / 10 krad	**Report ref:** ATN-RR366/ATN-RR348
SEL (Y/N) [Y]	**Level:** 120 MeV/(mg/cm²)	**Report ref:** HRX/SEE/0553
SEU (Y/N) [N]	**Level:**	**Report ref:**
SET (Y/N) [Y]	**Level:**	**Report ref:**
SEFI (Y/N) [N]	**Level:**	**Report ref:**
SEB (Y/N) [N]	**Level:**	**Report ref:**
SEGR (Y/N) [N]	**Level:**	**Report ref:**
Others (Y/N) [N]	**Level:**	**Report ref:**

RVT required (Y/N) [Y]
Remark: RVT TID performed iaw PTO-ATN-PL-PLA-0009 Iss4 for different configurations (see plan).
SET performed on 6 pcs iaw HRX/SEP/00140 Iss2.
SET&SOA on 7 pcs iaw HRX/SEP/00155 Iss1

COTS Selection, Mitigation Strategies

- **Mitigation Strategies**

- The key risk-reducing factors are the following:

1. Material Finish

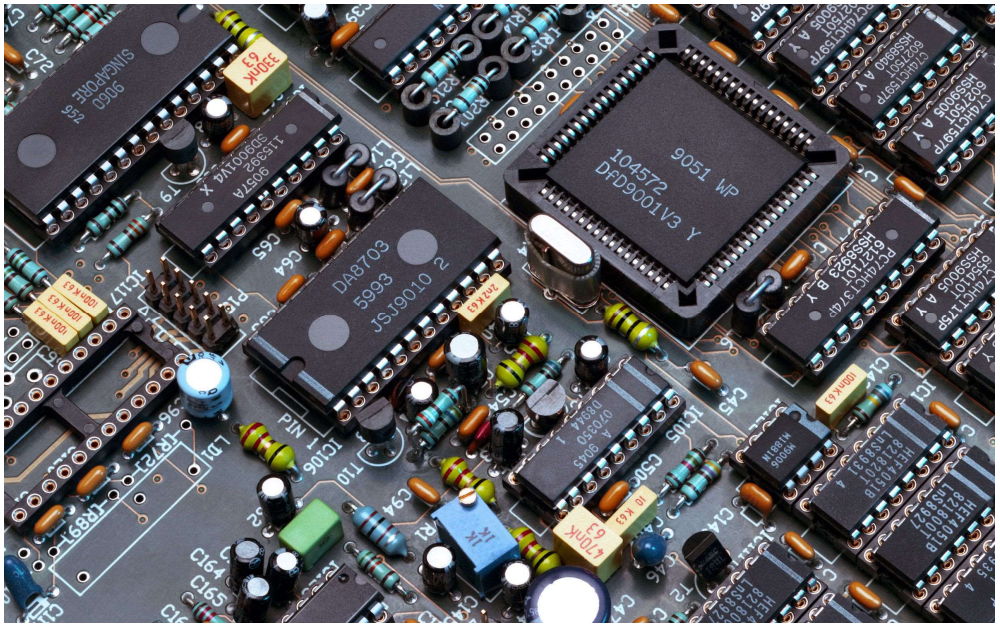
- Avoid pure tin to reduce tin whisker risks.
- Prefer alternatives like SnPb or nickel-gold finishes.

2. Reliability Data

- Look for comprehensive vendor-provided reliability reports.
- Emphasis on operating life and stress-testing results.

3. Technology Type

- Favor bipolar technology for radiation tolerance.
- CMOS for high-performance but evaluate susceptibility.



COTS Selection, Mitigation Strategies

- **Mitigation Strategies**

- Regarding soldering and packaging considerations:

1. Moisture Sensitivity Level (MSL)

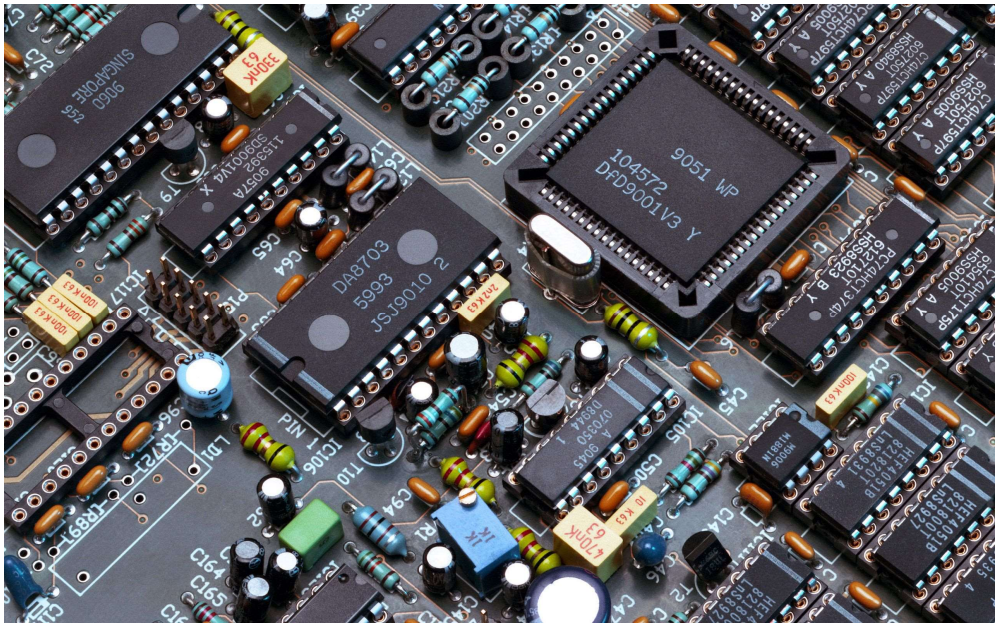
- Prefer components rated MSL-1 for better durability.
- Lower sensitivity to humidity during storage and assembly.

2. Package Compatibility

- Ensure the package type is compatible with your soldering process.
- Verify the thermal characteristics of the package.

3. Soldering Finish

- Validate lead finishes for ease of soldering and compatibility.



COTS Selection, Mitigation Strategies

- **Mitigation Strategies**

- For this, we need to consider the ESA Technical Note: “Guidelines for the Utilization of COTS components and Modules in ESA”

- This note intends to classify COTS components according to applications criticality categories and identify provisions for these criticality categories

- This note shall be used as guideline and not as a standard, and is limited to ESA missions only and it covers EEE parts and modules in equipment, subsystems and systems

- Not related to mission class but to parts and modules

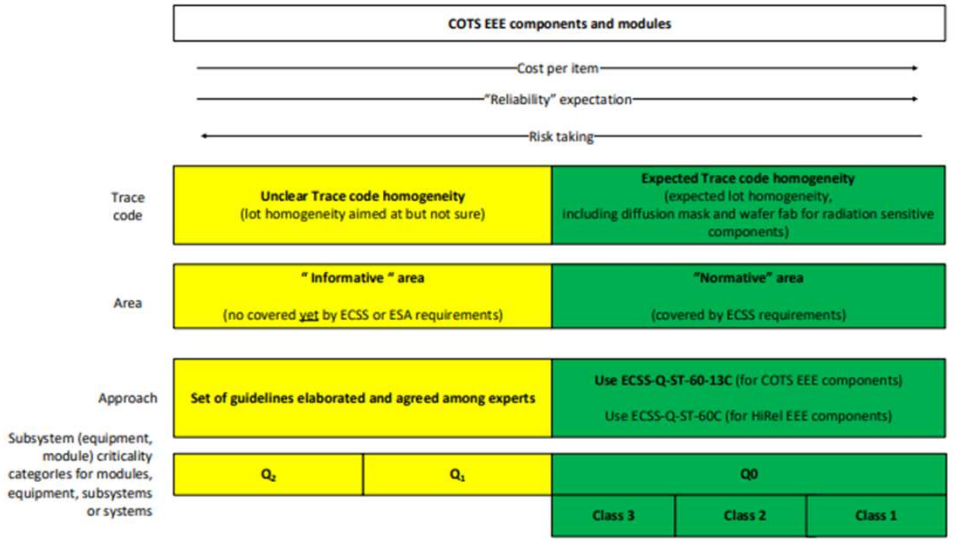


Figure 1, COTS, overall approach, versus Criticality Categories

COTS Selection, Mitigation Strategies

- **Mitigation Strategies**

- Q0: Normative area, all standard ECSS requirements apply (see ECSS-Q-ST-60-13C Rev.1)

- Q1 and Q2: Informative area, lower requirements and higher risks can be accepted:
  - Q2: most risky and economic class
  - Q1: less risky and more expensive than Q2

Q_2 application perimeter is defined by the following recommendations:

- The mission radiation exposure TIDL at component level should be limited to <5 krad(Si)
- The mission operational duration should be limited to few months, typically less than one year.

Q_1 application perimeter is defined by the following recommendations:

- The mission radiation environment (TIDL) limit is indicatively 10-15 krad(Si)
- The mission operational duration should be limited to few years, typically less than five years.

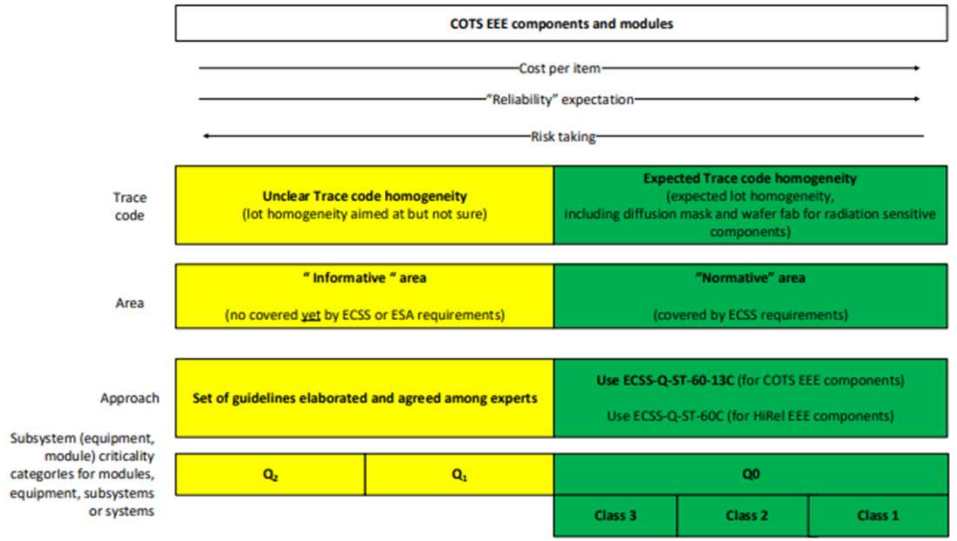


Figure 1, COTS, overall approach, versus Criticality Categories

COTS Selection, Mitigation Strategies

- **Mitigation Strategies**
  - Grey Area:

One difference between “Informative” and “Normative” area is linked to the traceability information (or trace code, according to the definition 3.2.1 of ECSS-Q-ST-60-13). If the same trace code can be guaranteed between the EEE COTS components subject to evaluation/lot acceptance test, and the ones that will actually be used for flight, requirements of the normative area can be fully applied, and we can be sure of consistent functionality and performance in flight with respect to the test performed on ground.

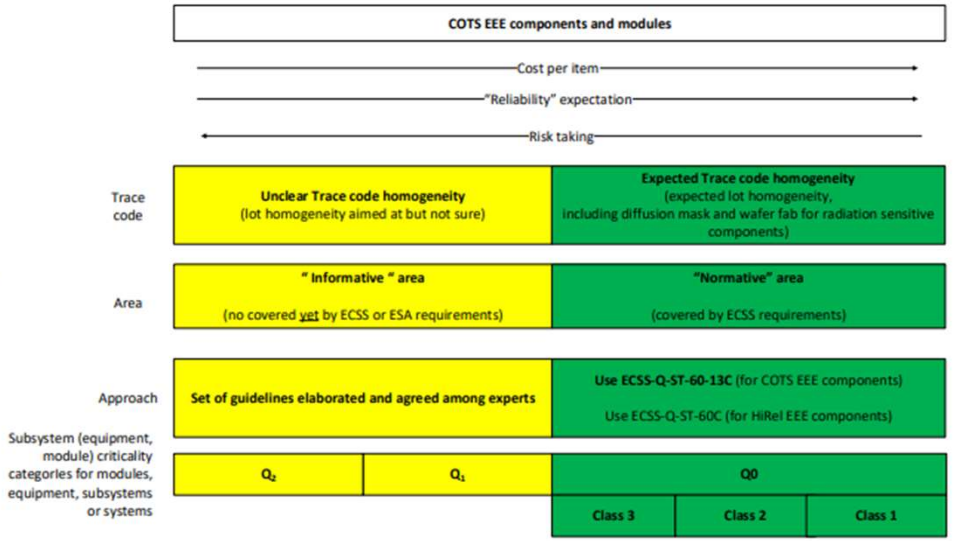


Figure 1, COTS, overall approach, versus Criticality Categories

COTS Selection, Mitigation Strategies

- **Mitigation Strategies**

- Traceability of the parts is not often available from manufacturer. For this same reason, it is preferred to procure all the required quantity at the same time from high volume productions.
- Once the flight lot is procured, traceability at user premises shall be developed including identification of batch number, disposition of CoC and any additional record from manufacturer, record of datasheet applicable at time of procurement, mask pictures, electrical measurements…
- It is recommended the procurement of parts from trusted manufacturers with reliability test programs for generating reliability data for processes/products and an effective policy ensuring continuous process improvement. The procurement directly from manufacturers, CPPA or franchised distributors is preferred.
- Outgassing should be evaluated if camera or other sensitive equipment are closed, according to ECSS-Q-ST-70-02C. If outgassing is a concern, the list of materials included in the COTS part should be review and the performance of outgassing test considered if necessary.
- AEC-Q components are preferred versus pure commercial devices. Recent enhanced plastic versions and dedicated LEO versions for high runners parts are available.

COTS Selection, Mitigation Strategies

- **Mitigation Strategies**

- COTS components should preferably be used within their operating temperature range.
- Handling:
  - Procedure shall be implemented to comply with mechanical and ESD precautions
  - ESD sensitive parts shall be identified and handled only by trained personnel using anti-static packaging, tools and other means.
  - Any handling of stored parts shall be reduced to the minimum. The removed components shall be repacked in a package identical or equivalent to the original manufacturer package.
  - Any component transfer from package to package shall be performed using dedicated pick and place tools, as applicable.
  - Special attention shall be given to multileaded SMT packaged components in order to avoid mechanical damage/missalignment.
  - For space applications it is recommended to consider packages MSL-1 (moisture sensitive level-1). At least, it is recommended to assess the MSL level for each COTS and establish appropriate measurements in order to avoid issues. Moisture sensitivity levels are specified in technical standard IPC/JEDEC Moisture/reflow Sensitivity Classification for Non-hermetic Surface-Mount Devices. This standard indicates indicate how long components can be outside of dry storage before they have to be baked to remove any absorbed moisture. For example, 1y for MSL-2 and 168h for MSL-3 levels.

COTS Selection, Mitigation Strategies

- **Mitigation Strategies**

- Storage:
  - COTS are usually manufactured on plastic non-hermetic packages being sensitive to moisture.
  - COTS encapsulated in plastic package shall be stored in a +22°C±5°C temperature range, max. 55%±10%relative humidity, controlled and clean area and in one of the following conditions:
    - Nitrogen or Dry and ionized air (RH shall be kept in the range 15% to 20%)
    - Dry packs (see J-STD-033 for dry pack inspection an control).

  - Commercial parts shall be stored and shipped in moisture barrier bags meeting requirements of MIL-PRF-81705, Type I, with desiccant, indicators and nitrogen backfills

COTS Selection, Mitigation Strategies

- **Design Considerations: Redundancy**

- When using COTS, the uncertainties on reliability are higher.
- Therefore, it is logical to think about adding redundancy to circuits in order to mitigate risk
- However, this can cause increase in cost, in mechanical/thermal stress on boards, weight, board dimensions…

- The ESA technical note focuses the redundancy considerations on radiation mitigation:
  - For Class Q1 & Q2:
    - For SRAM-based and Flash-based FPGAs spatial redundancy techniques may be utilized for mitigation against radiation induced SEE
    - Critical functions should be provided with redundancy and voting.

COTS Selection, Mitigation Strategies

- **Design Considerations: Redundancy**
  - For Class Q0:

- *Spatial redundancy, temporal redundancy* or a combination of both.
  In *spatial* redundancy, the logic resources are replicated in order to process the same task in parallel. The results from each replicated path are majority voted to detect and correct possible errors.
  In *temporal* redundancy signals are sampled (or full functions are executed) in varying time instances, and then majority voted to filter out SET and SEU.
- *Mitigation techniques specifically addressing Finite State Machines (FSM)*
  Specific FSM state coding and deadlock-recovery logic can be used to protect FSMs.
- *Error mitigation methods applied for memory arrays*
  Information redundancy methods are employed, using error detection and correction (EDAC) codes to protect data in memory arrays. Spatial redundancy can also be used, where the memory blocks are replicated and majority voted.

The following main digital electronic component category types will be considered:

- FPGAs
- Memories
- Microcontrollers
- Microprocessors
- Programmable Systems-on-a-Chip

COTS Selection, Mitigation Strategies

- **Design Considerations: Derating**

- For Q2, Derating Rules:

  - For EEE components, the same or higher derating margins should be applied as defined in the ECSS-Q-ST-30-11and ECSS-Q-ST-60-13.
  - If complete modules are procured, the relevant application ratings (temperature, power, voltage, current) should be respected with margins to be agreed with the customer
  - PSA document (Parts Stress Analysis) may not be delivered.

COTS Selection, Mitigation Strategies

- **Design Considerations: Derating**

- For Q1, Derating Rules:

  - For EEE components, the same or higher derating margins should be applied as defined in the ECSS-Q-ST-30-11and ECSS-Q-ST-60-13.
  - If complete modules are procured, the relevant application ratings (temperature, power, voltage, current) should be respected with margins to be agreed with the customer
  - PSA (Parts Stress Analysis) is a deliverable document.

COTS Selection, Mitigation Strategies

- **Design Considerations: Derating**

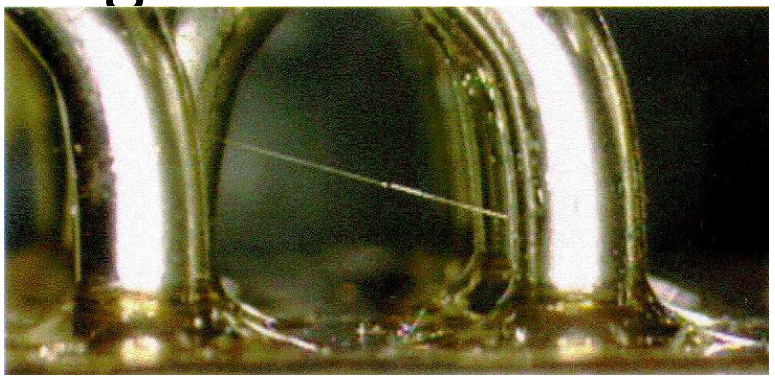
- For Q0, Derating Rules:

  - For EEE components, the same or higher derating margins should be applied as defined in the ECSS-Q-ST-30-11and ECSS-Q-ST-60-13.
  - PSA (Parts Stress Analysis) is a deliverable document.

- For NASA Case: EEE-INST-002 has tables with derating guidelines for each component type

COTS Selection, Mitigation Strategies

- **Design Considerations: Circuit Design**



- When testing is performed only at Board Level, usually for missions requiring lower reliability, functional points for measuring and identification of failures shall be included.

- Use higher rated parts where single point failures exist.

- Heat treating (reflow, annealing, hot dip, etc)
- Use of conformal coating: lower cost and can be used on built-up hardware
- Geometry on circuitry
- Control circuitry

- See JEDEC JP002

COTS Selection, Mitigation Strategies

- **Design Considerations: Tin Whiskers “To be lead or not to be”**

- Tin whiskers are a general concern when working with COTS on Space missions

- While for Space applications, the ECSS-Q-ST-60C limits the use of pure tin to avoid the apparition of tin whiskers, this finish is widely used on COTS parts, for manufacturers to comply with RoHS directive

COTS Selection, Mitigation Strategies

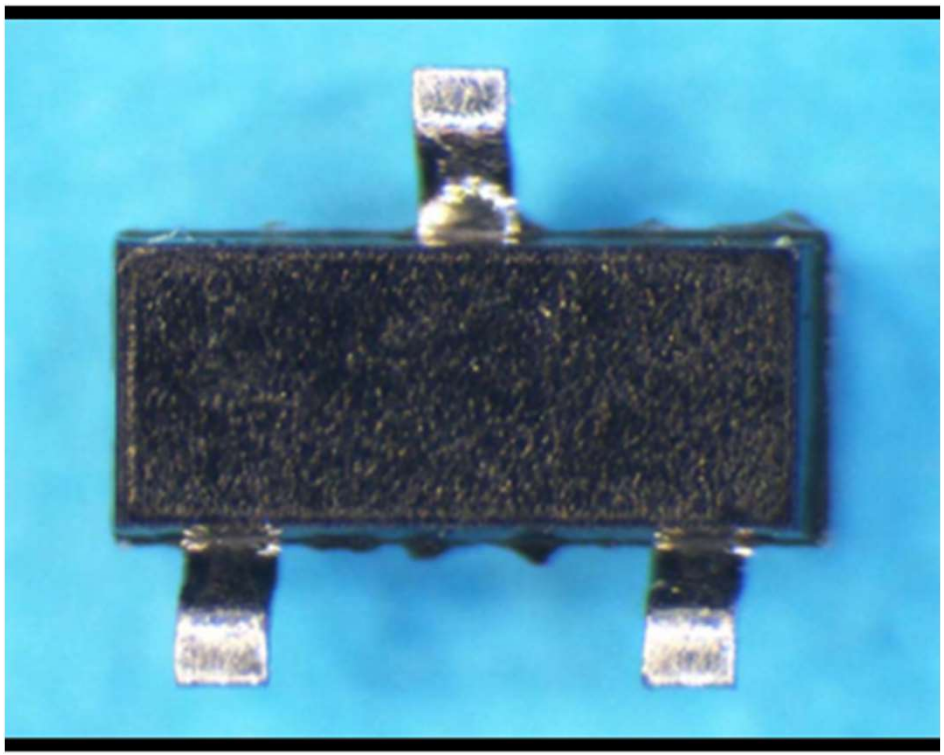
- **Design Considerations: Tin Whiskers "To be lead or not to be"**

- Therefore, when pure tin finish on the leads is used techniques to mitigate tin whiskers growth are required:
  - Design rules
  - PCB treatment (potting, use of conformal coating, etc)
  - Ask manufacturer to supply the parts finish in SnPb
  - Retin the parts without stand-off
  - …
- Considering Tin Whiskers mitigation, retinning has been one of the most used strategies in the past, but of course it entail several risks

COTS Selection, Mitigation Strategies

- **Design Considerations: Tin Whiskers "To be lead or not to be"**

- However, retinning can be difficult in some packages as SOIC or SMD and can introduce in the part:
  - Thermal degradation
  - Loss of hermeticity
  - Thermal shock induced damage
  - Poor wettability
  - Contamination
- In summary, damage due to difference in thermal coefficient of the materials



COTS Selection, Mitigation Strategies

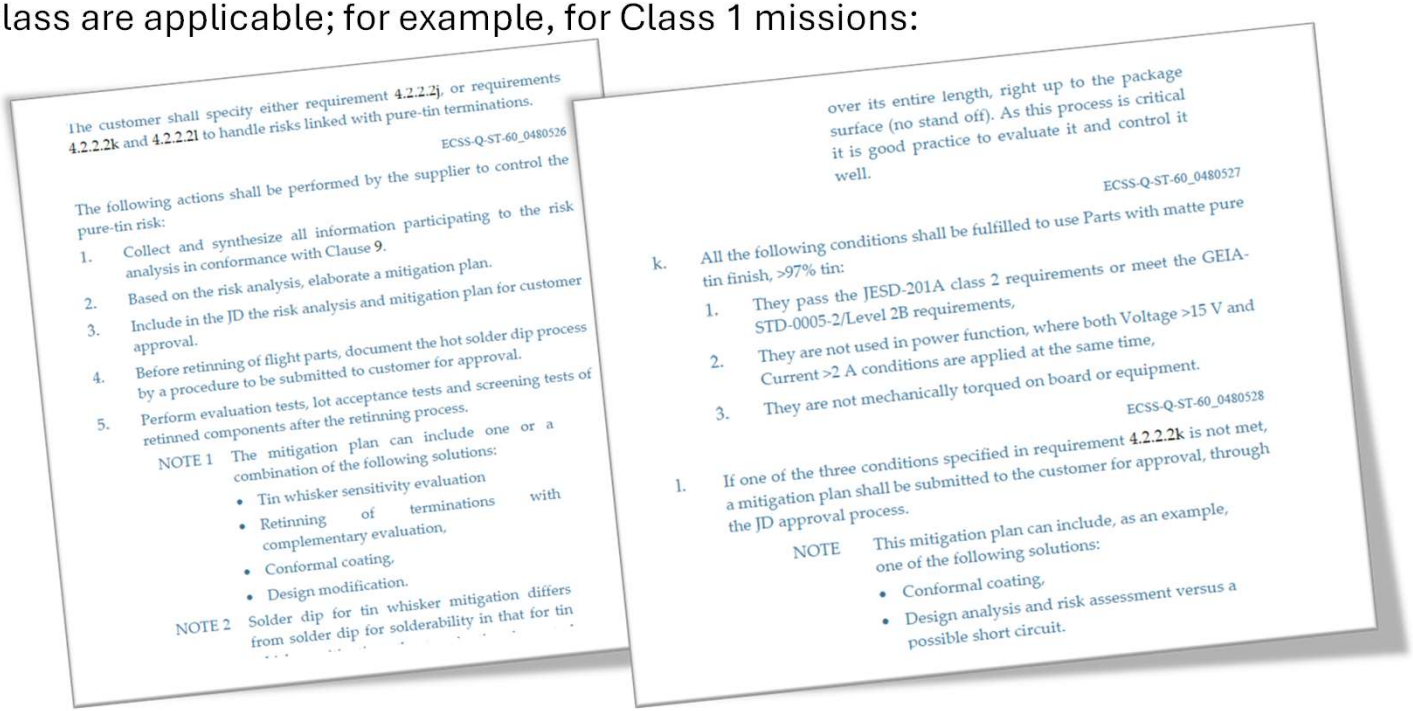
- **Design Considerations: Tin Whiskers "To be lead or not to be"**

- Considering all of this, the new revision of ECSS-Q-ST-60-13C has opted for a more flexible approach:
  - It is Required from the User a "Procedure for hot solder dip process for retinning operation"
  - A pure tin finish risk analysis is also Required, as per the provisions of new ECSS-Q-ST-60C Rev3

COTS Selection, Mitigation Strategies

- **Design Considerations: Tin Whiskers "To be lead or not to be"**

- Also, the provisions of ECSS-Q-ST-60C Rev3 in terms of Parts and material restriction for each mission Class are applicable; for example, for Class 1 missions:



The customer shall specify either requirement 4.2.2.2j, or requirements 4.2.2.2k and 4.2.2.2l to handle risks linked with pure-tin terminations.

ECSS-Q-ST-60_0480526

The following actions shall be performed by the supplier to control the pure-tin risk:

1. Collect and synthesize all information participating to the risk analysis in conformance with Clause 9.
2. Based on the risk analysis, elaborate a mitigation plan.
3. Include in the JD the risk analysis and mitigation plan for customer approval.
4. Before retinning of flight parts, document the hot solder dip process by a procedure to be submitted to customer for approval.
5. Perform evaluation tests, lot acceptance tests and screening tests of retinned components after the retinning process.

NOTE 1 The mitigation plan can include one or a combination of the following solutions:

- Tin whisker sensitivity evaluation
- Retinning of terminations with complementary evaluation,
- Conformal coating,
- Design modification.

NOTE 2 Solder dip for tin whisker mitigation differs from solder dip for solderability in that for tin

over its entire length, right up to the package surface (no stand off). As this process is critical it is good practice to evaluate it and control it well.

ECSS-Q-ST-60_0480527

k. All the following conditions shall be fulfilled to use Parts with matte pure tin finish, >97% tin:

1. They pass the JESD-201A class 2 requirements or meet the GEIA-STD-0005-2/Level 2B requirements,
2. They are not used in power function, where both Voltage >15 V and Current >2 A conditions are applied at the same time,
3. They are not mechanically torqued on board or equipment.

ECSS-Q-ST-60_0480528

1. If one of the three conditions specified in requirement 4.2.2.2k is not met, a mitigation plan shall be submitted to the customer for approval, through the JD approval process.

NOTE This mitigation plan can include, as an example, one of the following solutions:

- Conformal coating,
- Design analysis and risk assessment versus a possible short circuit.

COTS Selection, Mitigation Strategies

- **Design Considerations: Tin Whiskers "To be lead or not to be"**

- These provisions strongly highlight the need of checking the retinning, in case it is performed, due to the associated risks mentioned before.
- In the case of paragraph 4.2.2.2.k, it is remarkable that if the listed conditions are met, no retinning is Required

COTS Selection, Mitigation Strategies

- **Design Considerations: Tin Whiskers "To be lead or not to be"**

- Example: Ceramic Capacitor 1812, 100nF NO RETINNING

Ordering Information

C	1206	C	104	J	3	G	A	C	AUTO
Ceramic	Case Size (L" x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance[1]	Rated Voltage (VDC)	Dielectric	Failure Rate/ Design	Termination Finish[2]	Packaging/Grade (C-Spec)
	0402 0603 0805 1206 1210 1812 2220	C = Standard	Two significant digits and number of zeros Use 9 for 1.0 – 9.9 pF Use 8 for 0.5 – .99 pF ex. 2.2 pF = 229 ex. 0.5 pF = 508	B = ±0.10 pF C = ±0.25 pF D = ±0.5 pF F = ±1% G = ±2% J = ±5% K = ±10% M = ±20%	8 = 10 4 = 16 3 = 25 5 = 50 1 = 100 2 = 200 A = 250	G = C0G	A = N/A	C = 100% Matte Sn	See "Packaging C-Spec Ordering Options Table"

Maximum Whisker Density Range

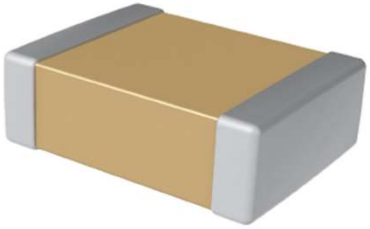
Low: < 10 whiskers per (mm^2)
Medium: 10 - 45 whiskers per (mm^2)
High: > 45 whiskers per (mm^2)

Whisker Definition

Spontaneous columnar or cylindrical filament emanating from the surface
Length ≥ 10µm.
Aspect ratio (l/w) > 2.

Preconditioning Exposure

A: No preconditioning
C: SnPb reflow conditions, 220°C peak
D: Pb-free reflow conditions, 260°C peak



		Configuration	Rectangular / Square 5 Side Termination		
		Applicable Products	Ceramic Chips		
		Example			
		Termination Code	C		
		Termination Finish	100% Matte Tin		
		Finish Thickness	100 - 400 µ-inch		
		Barrier Plating	Nickel		
		Barrier Thickness	50 µ-inch min.		
		Terminals Inspected	18		
		Inspection Area per Terminal	3.4 mm^2		
		Inspection Equipment / Mag	SEM / 3000X		
		Preconditioning	A	C	D
Exposure	Temperature / Humidity Storage 30°C, 60% RH, 4000 hours	Whisker Count	0	0	0
		Longest Whisker	n/a	n/a	n/a
		Meets Class Level	2	2	2
		Whisker Density Range	Low	Low	Low
	High Temp / Humidity Storage 55°C and 85% RH, 4000 hours	Whisker Count	0	3	4
		Longest Whisker	n/a	26µm	20µm
		Meets Class Level	2	2	2
		Whisker Density Range	Low	Low	Low
	Temperature Cycling -55°C to +85°C, 1500 cycles	Whisker Count	0	>45	0
		Longest Whisker	n/a	43µm	n/a
		Meets Class Level	2	2	2
		Whisker Density Range	Low	High	Low

THANK YOU!

Jose Largaespada
josef.largaespada@altertechnology.com
+34 664 70 30 07

www.altertechnology-group.com
info@altertechnology.com
+34 95 446 70 50